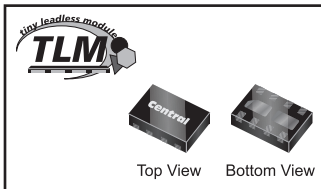
CTLDM303N-M832DS

SURFACE MOUNT
DUAL N-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET



Top View Bottom View

TLM832DS CASE

Central Semiconductor Corp.

www.centralsemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM303N-M832DS is a dual enhancement-mode N-Channel silicon MOSFET designed for high speed pulsed amplifier and driver applications. This energy efficient MOSFET offers beneficially low $r_{DS(ON)}$, low gate charge, and low threshold voltage.

MARKING CODE: C330

APPLICATIONS:

- DC-DC converters
- Drive circuits
- Power management

FEATURES:

- Low $r_{DS(ON)}$ (0.078Ω MAX @ V_{GS}=2.5V)
- High current (I_D=3.6A)
- Low gate charge

MAXIMUM RATINGS: (T_A=25°C)	**SYMBOL**		**UNITS**
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	12	V
Continuous Drain Current (Steady State)	I_D	3.6	A
Maximum Pulsed Drain Current, tp=10μs	I_{DM}	14.4	A
Power Dissipation	P_D	1.65	W
Operating and Storage Junction Temperature	T_J, T_{stg}	-55 to +150	°C
Thermal Resistance (Note 1)	Θ_{JA}	76	°C/W

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: (T_A=25°C unless otherwise noted)

SYMBOL	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{GSSF}, I_{GSSR}	V_{GS}=12V, V_{DS}=0			10	μA
I_{DSS}	V_{DS}=20V, V_{GS}=0			1.0	μA
BV_{DSS}	V_{GS}=0, I_D=250μA	30			V
$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	0.6		1.2	V
$r_{DS(ON)}$	V_{GS}=4.5V, I_D=1.8A		0.033	0.04	Ω
$r_{DS(ON)}$	V_{GS}=2.5V, I_D=1.8A		0.042	0.078	Ω
$Q_{g(tot)}$	V_{DD}=10V, V_{GS}=4.5V, I_D=3.6A		5.0	13	nC
Q_{gs}	V_{DD}=10V, V_{GS}=4.5V, I_D=3.6A		0.9	1.4	nC
Q_{gd}	V_{DD}=10V, V_{GS}=4.5V, I_D=3.6A		1.0	2.7	nC
g_{FS}	V_{DS}=5.0V, I_D=3.6A		11.8		S
C_{rss}	V_{DS}=10V, V_{GS}=0, f=1.0MHz		55		pF
C_{iss}	V_{DS}=10V, V_{GS}=0, f=1.0MHz		590		pF
C_{oss}	V_{DS}=10V, V_{GS}=0, f=1.0MHz		50		pF
t_{on}	V_{DD}=10V, V_{GS}=4.0V, I_D=3.6A, R_G=10Ω		15		ns
t_{off}	V_{DD}=10V, V_{GS}=4.0V, I_D=3.6A, R_G=10Ω		29		ns

Notes: (1) FR-4 Epoxy PCB with copper mounting pad area of 54mm^2

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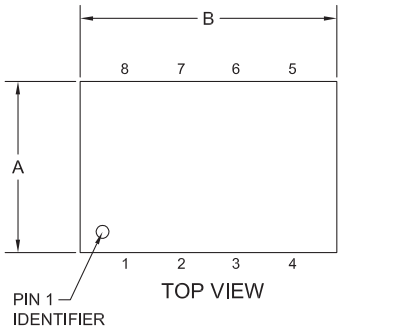
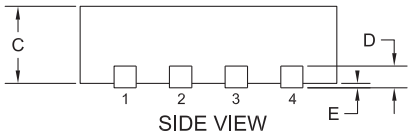
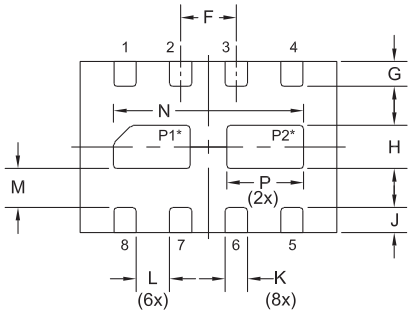
TLM832DS CASE - MECHANICAL OUTLINE





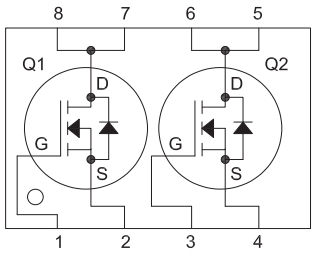


* Exposed pad P1 common to pins 7 and 8
Exposed pad P2 common to pins 5 and 6

DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.077	0.081	1.95	2.05
B	0.116	0.120	2.95	3.05
C	0.031	0.039	0.80	1.00
D	0.006	0.010	0.16	0.25
E	0.000	0.002	0.00	0.05
F	0.026		0.65	
G	0.008	0.016	0.19	0.40
H	0.014	0.024	0.35	0.61
J	0.008	0.016	0.19	0.40
K	0.008	0.012	0.21	0.31
L	0.013	0.017	0.34	0.44
M	0.006	–	0.15	–
N	0.087		2.22	
P	0.029	0.039	0.74	1.00

TLM832DS (REV:R1)

PIN CONFIGURATION



LEAD CODE:

1) Gate Q1
2) Source Q1
3) Gate Q2
4) Source Q2
5) Drain Q2
6) Drain Q2
7) Drain Q1
8) Drain Q1

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R2 (8-October 2012)