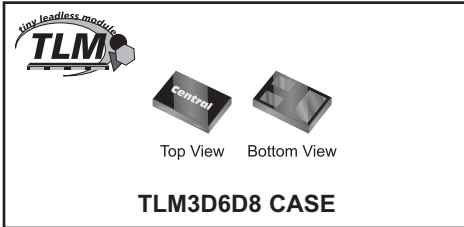


CTLDM7590

**SURFACE MOUNT
P-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET**



www.centrasemi.com



DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM7590 is an enhancement-mode P-channel MOSFET designed for applications including high speed pulsed amplifiers and drivers. This MOSFET has beneficially low $r_{DS(ON)}$, low threshold voltage, and very low gate charge characteristics.

MARKING CODE: 2

FEATURES:

- ESD protection up to 2kV
- Power dissipation: 125mW
- Low $r_{DS(ON)}$
- Low threshold voltage
- Ultra small, ultra low profile 0.6mm x 0.8mm x 0.4mm TLM™ leadless surface mount package

APPLICATIONS:

- Load/Power Switches
- Boost/Buck Converters
- Battery Charging/Power Management

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

| |
|--|
| Drain-Source Voltage |
| Gate-Source Voltage |
| Continuous Drain Current (Steady State) |
| Pulsed Drain Current, $t_p=10\mu\text{s}$ |
| Power Dissipation |
| Operating and Storage Junction Temperature |
| Thermal Resistance |

SYMBOL

| | | |
|----------------|-------------|--------------------|
| V_{DS} | 20 | V |
| V_{GS} | 8.0 | V |
| I_D | 140 | mA |
| I_D | 600 | mA |
| P_D | 125 | mW |
| T_J, T_{stg} | -65 to +150 | $^\circ\text{C}$ |
| θ_{JA} | 1000 | $^\circ\text{C/W}$ |

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)

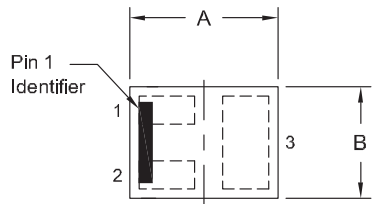
| SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------|---|-----|------|-----|----------|
| I_{GSSF}, I_{GSSR} | $V_{GS}=5.0\text{V}, V_{DS}=0$ | | | 100 | nA |
| I_{DSS} | $V_{DS}=5.0\text{V}, V_{GS}=0$ | | | 50 | nA |
| I_{DSS} | $V_{DS}=16\text{V}, V_{GS}=0$ | | | 100 | nA |
| BV_{DSS} | $V_{GS}=0, I_D=250\mu\text{A}$ | 20 | | | V |
| $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=250\mu\text{A}$ | 0.4 | | 1.0 | V |
| $r_{DS(ON)}$ | $V_{GS}=4.5\text{V}, I_D=100\text{mA}$ | | 4.0 | 5.0 | Ω |
| $r_{DS(ON)}$ | $V_{GS}=2.5\text{V}, I_D=50\text{mA}$ | | 5.5 | 7.0 | Ω |
| $r_{DS(ON)}$ | $V_{GS}=1.8\text{V}, I_D=20\text{mA}$ | | 8.0 | 10 | Ω |
| $r_{DS(ON)}$ | $V_{GS}=1.5\text{V}, I_D=10\text{mA}$ | | 11 | 17 | Ω |
| $r_{DS(ON)}$ | $V_{GS}=1.2\text{V}, I_D=1.0\text{mA}$ | | 20 | | Ω |
| $Q_g(\text{tot})$ | $V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=100\text{mA}$ | | 0.50 | | nC |
| Q_{gs} | $V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=100\text{mA}$ | | 0.17 | | nC |
| Q_{gd} | $V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=100\text{mA}$ | | 0.11 | | nC |
| g_{FS} | $V_{DS}=5.0\text{V}, I_D=125\text{mA}$ | | 140 | | mS |
| C_{rss} | $V_{DS}=15\text{V}, V_{GS}=0, f=1.0\text{MHz}$ | | 4.0 | | pF |
| C_{iss} | $V_{DS}=15\text{V}, V_{GS}=0, f=1.0\text{MHz}$ | | 10 | | pF |
| C_{oss} | $V_{DS}=15\text{V}, V_{GS}=0, f=1.0\text{MHz}$ | | 3.7 | | pF |
| t_{on} | $V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=200\text{mA}$ | | 35 | | ns |
| t_{off} | $V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=200\text{mA}$ | | 100 | | ns |

R3 (21-September 2012)

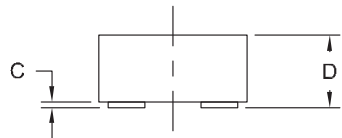
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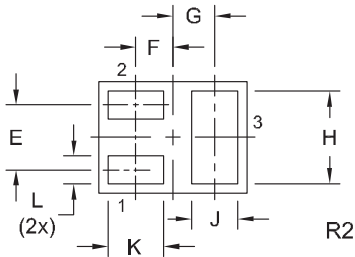
TLM3D6D8 CASE - MECHANICAL OUTLINE



TOP VIEW



SIDE VIEW

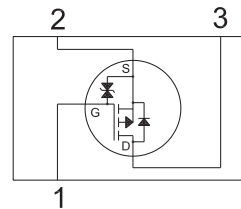


BOTTOM VIEW

| SYMBOL | INCHES | | MILLIMETERS | |
|--------|--------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.029 | 0.034 | 0.75 | 0.85 |
| B | 0.021 | 0.026 | 0.55 | 0.65 |
| C | 0.000 | 0.002 | 0.00 | 0.05 |
| D | 0.012 | 0.016 | 0.31 | 0.40 |
| E | 0.014 | | 0.35 | |
| F | 0.008 | | 0.20 | |
| G | 0.009 | | 0.225 | |
| H | 0.017 | 0.022 | 0.45 | 0.55 |
| J | 0.008 | 0.012 | 0.20 | 0.30 |
| K | 0.010 | 0.014 | 0.25 | 0.35 |
| L | 0.004 | 0.008 | 0.10 | 0.20 |

TLM3D6D8 (REV: R2)

PIN CONFIGURATION
(Bottom View)



LEAD CODE:

- 1) Gate
- 2) Source
- 3) Drain

MARKING CODE: 2

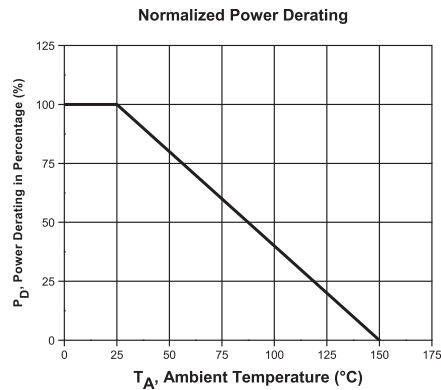
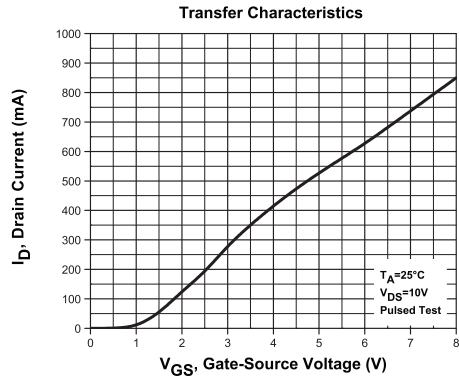
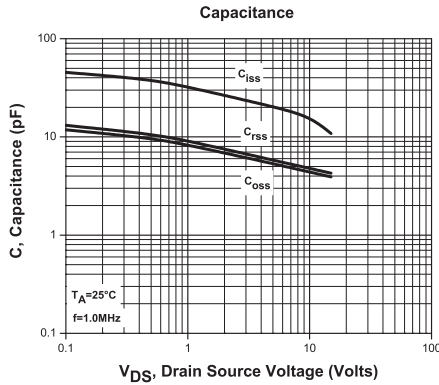
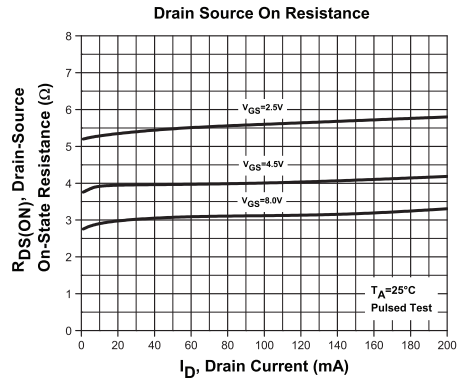
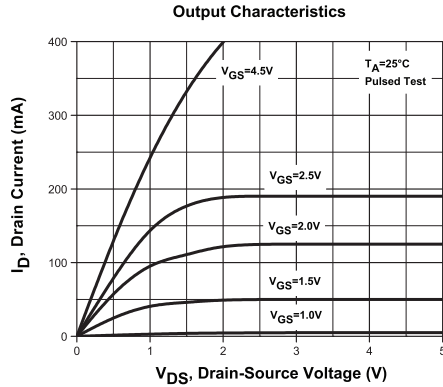
R3 (21-September 2012)

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TYPICAL ELECTRICAL CHARACTERISTICS



R3 (21-September 2012)