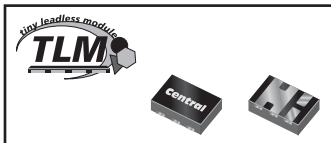
CTLDM8002A-M621

SURFACE MOUNT SILICON P-CHANNEL ENHANCEMENT-MODE MOSFET



Top View Bottom View

TLM621 CASE

www.centralsemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM8002A-M621 is a silicon P-Channel enhancement-mode MOSFET in a small, thermally efficient, TLM™ 2x1mm package.

MARKING CODE: CN

APPLICATIONS:

- Load/Power Switches
- Power Supply Converter Circuits
- Battery Powered Portable Equipment

FEATURES:

- Low $r_{DS(on)}$
- Low $V_{DS(on)}$
- Low Threshold Voltage
- Fast Switching
- Logic Level Compatible
- Small TLM™ 2x1mm Package

MAXIMUM RATINGS: (T_A=25°C)	**SYMBOL**		**UNITS**
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage	V_{DG}	50	V
Gate-Source Voltage	V_{GS}	20	V
Continuous Drain Current	I_D	280	mA
Continuous Source Current (Body Diode)	I_S	280	mA
Maximum Pulsed Drain Current	I_{DM}	1.5	A
Maximum Pulsed Source Current	I_{SM}	1.5	A
Power Dissipation (Note 1)	P_D	0.9	W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C
Thermal Resistance (Note 1)	Θ_{JA}	139	°C/W

ELECTRICAL CHARACTERISTICS: (T_A=25°C unless otherwise noted)

SYMBOL	**TEST CONDITIONS**	**MIN**	**MAX**	**UNITS**
I_{GSSF}, I_{GSSR}	V_{GS}=20V, V_{DS}=0		100	nA
I_{DSS}	V_{DS}=50V, V_{GS}=0		1.0	μA
I_{DSS}	V_{DS}=50V, V_{GS}=0, T_J=125°C		500	μA
$I_{D(ON)}$	V_{GS}=10V, V_{DS}=10V	500		mA
BV_{DSS}	V_{GS}=0, I_D=10μA	50		V
$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.0	2.5	V
$V_{DS(ON)}$	V_{GS}=10V, I_D=500mA		1.5	V
$V_{DS(ON)}$	V_{GS}=5.0V, I_D=50mA		0.15	V
V_{SD}	V_{GS}=0, I_S=115mA		1.3	V
$r_{DS(ON)}$	V_{GS}=10V, I_D=500mA		2.5	Ω
$r_{DS(ON)}$	V_{GS}=10V, I_D=500mA, T_J=125°C		4.0	Ω
$r_{DS(ON)}$	V_{GS}=5.0V, I_D=50mA		3.0	Ω
$r_{DS(ON)}$	V_{GS}=5.0V, I_D=50mA, T_J=125°C		5.0	Ω
g_{FS}	V_{DS}=10V, I_D=200mA	200		mS
C_{rss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz		7.0	pF
C_{iss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz		70	pF
C_{oss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz		15	pF

Note: (1) FR-4 Epoxy PCB with copper mounting pad area of 33mm^2.

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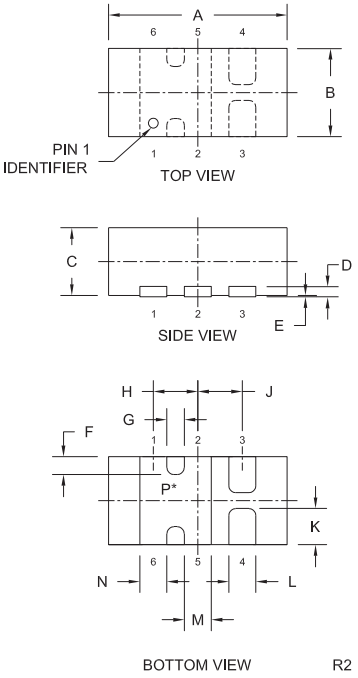
ELECTRICAL CHARACTERISTICS - Continued: (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	TYP	MAX	UNITS
$Q_{g(tot)}$	V_{DS}=25V, V_{GS}=4.5V, I_D=100mA	0.72		nC
Q_{gs}	V_{DS}=25V, V_{GS}=4.5V, I_D=100mA	0.25		nC
Q_{gd}	V_{DS}=25V, V_{GS}=4.5V, I_D=100mA	0.16		nC
t_{on}, t_{off}	V_{DD}=30V, V_{GS}=10V, I_D=200mA, R_G=25Ω, R_L=150Ω		20	ns

TLM621 CASE - MECHANICAL OUTLINE



*Exposed pad P connects pins 1, 2, 5, and 6

DIMENSIONS				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.073	0.085	1.850	2.150
B	0.033	0.045	0.850	1.150
C	0.028	0.031	0.700	0.800
D	0.006		0.150	
E	0.000	0.002	0.000	0.050
F	0.008		0.200	
G	0.010		0.250	
H	0.020		0.500	
J	0.020		0.500	
K	0.012	0.020	0.300	0.500
L	0.007	0.012	0.180	0.300
M	0.007	0.012	0.180	0.300
N	0.007	0.012	0.180	0.300

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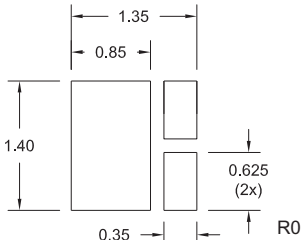
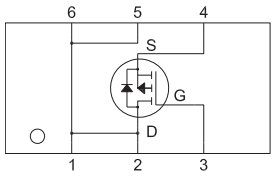
SUGGESTED MOUNTING PADS

(Dimensions in mm)



PIN CONFIGURATION



LEAD CODE:

1) Drain
2) Drain
3) Gate
4) Source
5) Drain
6) Drain

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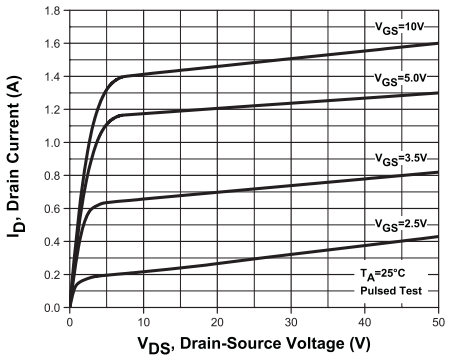
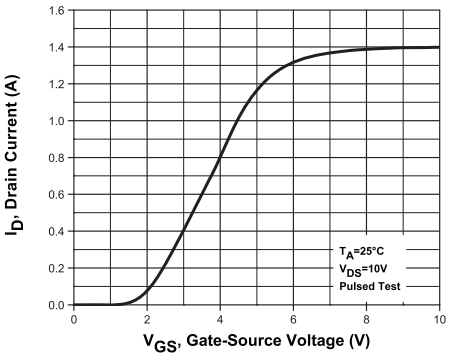
TYPICAL ELECTRICAL CHARACTERISTICS

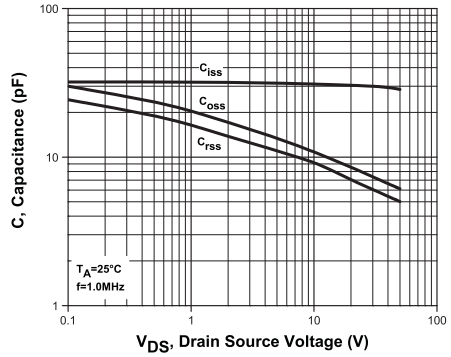
Output Characteristics



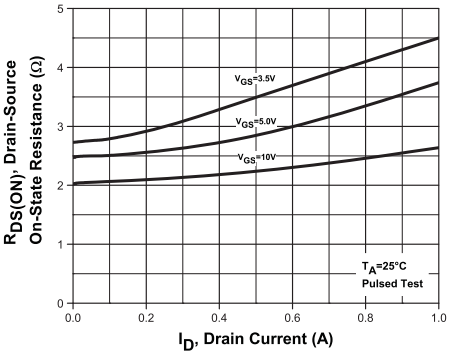
Transfer Characteristics



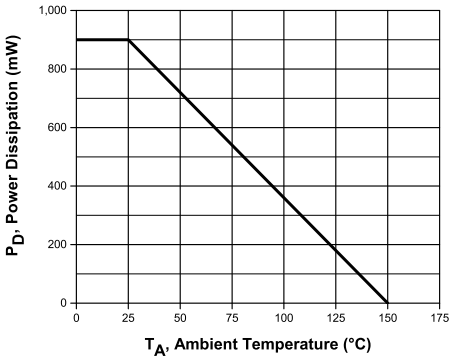
Capacitance



Drain Source On Resistance



Power Derating



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SURFACE MOUNT SILICON P-CHANNEL ENHANCEMENT-MODE MOSFET

SERVICES

- Bonded Inventory
- Custom Electrical Screening
- Custom Electrical Characteristic Curves
- SPICE Models
- Custom Packaging
- Package Base Options
- Custom Device Development / Multi Discrete Modules (MDM™)
- Bare Die Available for Hybrid Applications

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