



CTLM1074-M832D

MULTI DISCRETE MODULE™

SURFACE MOUNT

**LOW V_{CE} (SAT) SILICON PNP TRANSISTOR
AND
LOW V_F SILICON SCHOTTKY RECTIFIER**



Top View



Bottom View

TLM832D CASE

MARKING CODE: CFD

APPLICATIONS

- Switching Circuits
- DC / DC Converters
- LCD Backlighting
- Battery powered / Portable Equipment applications including Cell Phones, Digital Cameras, Pagers, PDAs, Notebook PCs, etc.

MAXIMUM RATINGS (TLM832D Package): (T_A=25°C) SYMBOL

	SYMBOL		UNITS
Power Dissipation*	P _D	1.65	W
Operating and Storage Junction Temperature	T _J , T _{stg}	-65 to +150	°C
Thermal Resistance	θ _{JA}	76	°C/W

MAXIMUM RATINGS Q1: (T_A=25°C)

Collector-Base Voltage	V _{CB0}	40	V
Collector-Emitter Voltage	V _{CEO}	25	V
Emitter-Base Voltage	V _{EBO}	6.0	V
Collector Current	I _C	1.0	A

MAXIMUM RATINGS D1: (T_A=25°C)

Peak Repetitive Reverse Voltage	V _{RRM}	40	V
Continuous Forward Current	I _F	1.0	A
Peak Repetitive Forward Current, t _p ≤ 1ms	I _{FRM}	3.5	A
Forward Surge Current, t _p = 8ms	I _{FSM}	10	A

ELECTRICAL CHARACTERISTICS Q1: (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I _{CBO}	V _{CB} =40V			100	nA
I _{EBO}	V _{EB} =6.0V			100	nA
BV _{CB0}	I _C =100µA	40			V
BV _{CEO}	I _C =10mA	25			V
BV _{EBO}	I _E =100µA	6.0			V
V _{CE(SAT)}	I _C =50mA, I _B =5.0mA		25	50	mV
V _{CE(SAT)}	I _C =100mA, I _B =10mA		40	75	mV

*FR-4 Epoxy PCB with copper mounting pad area of 54mm²

Central™
Semiconductor Corp.

DESCRIPTION: The Central Semiconductor Corp. CTLM1074-M832D consists of a Low V_{CE} (SAT) PNP Transistor and a Low V_F Schottky Rectifier. Packaged in a small, thermally efficient, leadless 3x2mm surface mount case, it is designed for applications where small size, operational efficiency, and low energy consumption are the prime requirements. Due to its leadless package design this device is capable of dissipating up to 4 times the power of similar devices in comparable sized surface mount packages.

FEATURES

- Dual Chip Device
- High Current (1.0A) Transistor and Schottky Rectifier
- Low V_{CE(SAT)} PNP Transistor (450mV @ I_C = 1.0A Max)
- Low V_F Schottky Rectifier (550mV @ 1.0A Max)
- High Power to Footprint Ratio of 275mW per sq mm (Package Power Dissipation / Package Surface Area)
- Small TLM 3x2mm Leadless Surface Mount Package
- Complementary Device **CTLM1034-M832D**

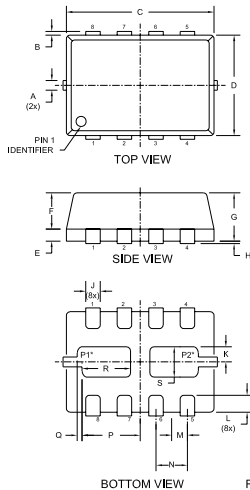
ELECTRICAL CHARACTERISTICS Q1 (Continued):

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CE(SAT)}$	$I_C=200mA, I_B=20mA$		80	150	mV
$V_{CE(SAT)}$	$I_C=500mA, I_B=50mA$		150	250	mV
$V_{CE(SAT)}$	$I_C=800mA, I_B=80mA$		220	400	mV
$V_{CE(SAT)}$	$I_C=1.0A, I_B=100mA$		275	450	mV
$V_{BE(SAT)}$	$I_C=800mA, I_B=80mA$			1.1	V
$V_{BE(ON)}$	$V_{CE}=1.0V, I_C=10mA$			0.9	V
h_{FE}	$V_{CE}=1.0V, I_C=10mA$	100			
h_{FE}	$V_{CE}=1.0V, I_C=100mA$	100		300	
h_{FE}	$V_{CE}=1.0V, I_C=500mA$	100			
h_{FE}	$V_{CE}=1.0V, I_C=1.0A$	50			
f_T	$V_{CE}=10V, I_C=50mA, f=100MHz$	100			MHz
C_{ob}	$V_{CB}=10V, I_E=0, f=1.0MHz$			15	pF

ELECTRICAL CHARACTERISTICS D1: ($T_A=25^\circ C$)

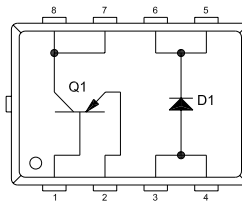
SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_R	$V_R=5V$			10	μA
I_R	$V_R=8V$			20	μA
I_R	$V_R=15V$			50	μA
BV_R	$I_R=100\mu A$	40			V
V_F	$I_F=10mA$			0.29	V
V_F	$I_F=100mA$			0.36	V
V_F	$I_F=500mA$			0.45	V
V_F	$I_F=1.0A$			0.55	V
C_J	$V_R=4.0V, f=1.0MHz$		50		pF

TLM832D - MECHANICAL OUTLINE

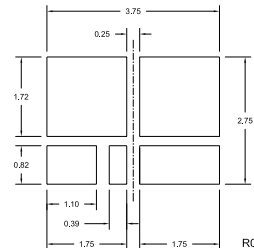


LEAD CODE:

- 1) BASE Q1
- 2) EMITTER Q1
- 3) ANODE D1
- 4) ANODE D1
- 5) CATHODE D1
- 6) CATHODE D1
- 7) COLLECTOR Q1
- 8) COLLECTOR Q1



Suggested mounting pad layout for maximum power dissipation (Dimensions in mm)



For standard mounting refer to TLM832D Package Details

MARKING CODE: CFD

SYMBOL	DIMENSIONS		DIMENSIONS	
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.007	0.012	0.170	0.300
B	-	0.005	-	0.125
C	0.114	0.122	2.900	3.100
D	0.075	0.083	1.900	2.100
E	0.006	0.010	0.150	0.250
F	0.026	0.030	0.650	0.750
G	0.031	0.039	0.800	1.000
H	0.000	0.002	0.000	0.050
J	0.009	0.013	0.240	0.340
K	0.006	0.014	0.160	0.360
L	0.008	0.018	0.200	0.450
M	0.013	-	0.325	-
N	0.026	-	0.650	-
P	0.040	0.048	1.010	1.210
Q	0.004	-	0.100	-
R	0.032	0.040	0.820	1.020
S	0.017	0.025	0.430	0.630

TLM832D (REV: R2)

* Note:

- Exposed pad P1 common to pins 7 and 8
- Exposed pad P2 common to pins 5 and 6

R1 (22-July 2008)