CTLSMS05-M622
CTLSMS12-M622
CTLSMS15-M622
CTLSMS24-M622

SURFACE MOUNT TLM™
SILICON QUAD TVS/ZENER ARRAY
5.0 THRU 24 VOLTS


Top View


Bottom View

TLM622 CASE

Central™
Semiconductor Corp.

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLSMS05 Series is a 4 line TVS/Zener Array packaged in a space saving TLM™ (Tiny Leadless Module™) TLM622 case. These devices are designed to protect sensitive equipment against ESD and to prevent latch-up events in CMOS circuitry operating at 5V, 12V, 15V and 24V.

MARKING CODES:
CTLSMS05-M622: CBC
CTLSMS12-M622: CBD
CTLSMS15-M622: CBF
CTLSMS24-M622: CBH

FEATURES:
- Very low clamping voltage
- Low leakage current
- 350W power dissipation
- IEC61000-4-2 ESD 20kV air, 15kV contact compliance
- New Tiny Leadless Module (TLM) package with a footprint compatible with the SOT-363 footprint.

APPLICATIONS:
- PDA's
- Memory Card Ports
- Mobile Phones
- Instrumentation

MAXIMUM RATINGS: (T_A=25°C)

	SYMBOL		UNITS
Peak Pulse Power (8x20µsec waveform)	P_{pp}	350	W
ESD Voltage (HBM)	V_{ESD}	>25	kV
Operating Temperature Range	T_J	-50 to +125	°C
Storage Temperature Range	T_{stg}	-50 to +150	°C

ELECTRICAL CHARACTERISTICS PER DIODE: (T_A=25°C unless otherwise noted)

Type No.	Reverse Stand-Off Voltage	Reverse Breakdown Voltage		Reverse Leakage Current		Clamping Voltage 8x20µsec		Clamping Voltage 8x20µsec		Off State Junction Capacitance V_R=0V f=1.0MHz	Marking Code
	V_{WRM} MAX (V)	V_{BR} MIN (V)	I_{BR} (mA)	I_R MAX (µA)	V_R (V)	Vcl MAX (V)	Ipp (A)	Vcl MAX (V)	Ipp (A)	Cj MAX (pF)	
CTLSMS05-M622	5	6	1.0	5.0	5.0	9.5	5.0	13	24	200	CBC
CTLSMS12-M622	12	13.3	1.0	5.0	12	17	5.0	21	15	90	CBD
CTLSMS15-M622	15	16.7	1.0	5.0	15	22	5.0	27	12	70	CBF
CTLSMS24-M622	24	26.7	1.0	5.0	24	35	5.0	40	8	50	CBH

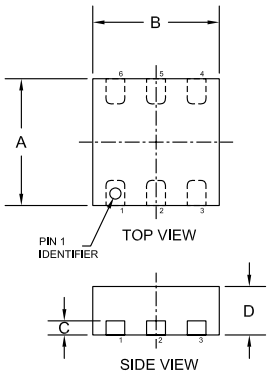
R1 (10-April 2006)

Central™
Semiconductor Corp.

CTLSMS05-M622
CTLSMS12-M622
CTLSMS15-M622
CTLSMS24-M622

SURFACE MOUNT TLM™
SILICON QUAD TVS/ZENER ARRAY
5.0 THRU 24 VOLTS

TLM622 CASE - MECHANICAL OUTLINE



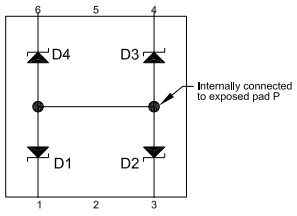
DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.077	0.081	1.95	2.05
B	0.077	0.081	1.95	2.05
C	0.007	0.009	0.18	0.23
D	0.029	0.031	0.73	0.78
E	0.012	0.016	0.30	0.40
F	0.053	0.057	1.35	1.45
G	0.061		1.55	
H	0.030	0.033	0.75	0.85
J	0.008	0.012	0.20	0.30
K	0.026		0.65	

TLM622 (REV:R1)

* See lead code for internal connections to exposed pad P

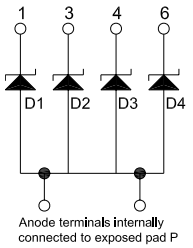
Marking Codes:
CTLSMS05-M622: CBC
CTLSMS12-M622: CBD
CTLSMS15-M622: CBF
CTLSMS24-M622: CBH

Pinout

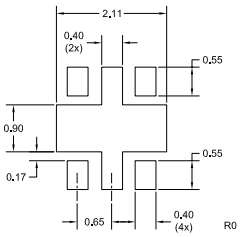


Lead Code:
1) Cathode D1
2) No Connection
3) Cathode D2
4) Cathode D3
5) No Connection
6) Cathode D4
P) Anode D1, D2, D3, D4

Schematic



Suggested mounting pad layout
for maximum power dissipation
(Dimensions in mm)



For standard mounting refer to TLM622 Package Details

R1 (10-April 2006)