

CTLT3410-M621 (NPN)
CTLT7410-M621 (PNP)

**SURFACE MOUNT
COMPLEMENTARY
LOW $V_{CE(SAT)}$
SILICON TRANSISTORS**



Top View Bottom View

TLM621 CASE



www.centralemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLT3410-M621 and CTLT7410-M621 are Low $V_{CE(SAT)}$ transistors in a very small leadless 1x2mm surface mount package, designed for applications where small size, operational efficiency, and low energy consumption are prime requirements. Due to the leadless package design, these devices are capable of dissipating up to 3 times the power of similar devices in comparable sized surface mount packages.

**MARKING CODES: CTLT3410-M621: CB
CTLT7410-M621: CD**

FEATURES:

- High Operational Efficiency
- High Power to Footprint Ratio
- $V_{CE(SAT)}$ @ 1.0A = 250mV TYP
- High Collector Current
- Small TLM621 1x2mm Package

APPLICATIONS:

- DC/DC Converters
- Switching Circuits
- LCD Backlighting
- Battery Powered Portable Equipment

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

Collector-Base Voltage
Collector-Emitter Voltage
Emitter-Base Voltage
Continuous Collector Current
Peak Collector Current
Power Dissipation (Note 1)
Operating and Storage Junction Temperature
Thermal Resistance (Note 1)

SYMBOL

V_{CBO} 40
 V_{CEO} 25
 V_{EBO} 6.0
 I_C 1.0
 I_{CM} 1.5
 P_D 0.9
 T_J, T_{stg} -65 to +150
 θ_{JA} 139

UNITS

V
V
V
A
A
W
 $^\circ\text{C}$
 $^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP		MAX	UNITS
			PNP	NPN		
I_{CBO}	$V_{CB}=40\text{V}$				100	nA
I_{EBO}	$V_{EB}=6.0\text{V}$				100	nA
BV_{CBO}	$I_C=100\mu\text{A}$	40				V
BV_{CEO}	$I_C=10\text{mA}$	25				V
BV_{EBO}	$I_E=100\mu\text{A}$	6.0				V
$V_{CE(SAT)}$	$I_C=50\text{mA}, I_B=5.0\text{mA}$		20	25	50	mV
$V_{CE(SAT)}$	$I_C=100\text{mA}, I_B=10\text{mA}$		35	40	75	mV
$V_{CE(SAT)}$	$I_C=200\text{mA}, I_B=20\text{mA}$		75	80	150	mV
$V_{CE(SAT)}$	$I_C=500\text{mA}, I_B=50\text{mA}$		130	150	250	mV
$V_{CE(SAT)}$	$I_C=800\text{mA}, I_B=80\text{mA}$		200	220	400	mV
$V_{CE(SAT)}$	$I_C=1.0\text{A}, I_B=100\text{mA}$		250	275	450	mV

Notes (1) FR-4 Epoxy PCB with copper mounting pad area of 33mm²

R2 (2-December 2010)

CTLT3410-M621 (NPN)
CTLT7410-M621 (PNP)

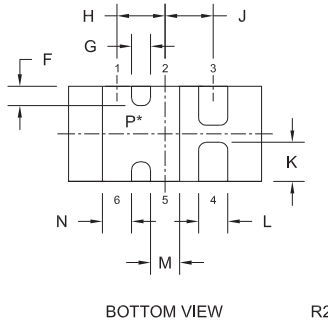
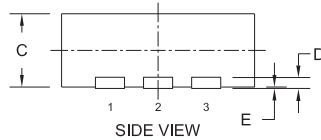
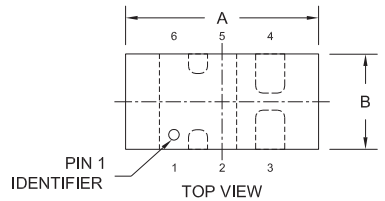
SURFACE MOUNT
COMPLEMENTARY
LOW $V_{CE(SAT)}$
SILICON TRANSISTORS



ELECTRICAL CHARACTERISTICS - Continued: ($T_A=25^\circ\text{C}$)

SYMBOL	TEST CONDITIONS	MIN	NPN	TYP	PNP	MAX	UNITS
$V_{BE(SAT)}$	$I_C=800\text{mA}$, $I_B=80\text{mA}$					1.1	V
$V_{BE(ON)}$	$V_{CE}=1.0\text{V}$, $I_C=10\text{mA}$					0.9	V
h_{FE}	$V_{CE}=1.0\text{V}$, $I_C=10\text{mA}$	100					
h_{FE}	$V_{CE}=1.0\text{V}$, $I_C=100\text{mA}$	100				300	
h_{FE}	$V_{CE}=1.0\text{V}$, $I_C=500\text{mA}$	100					
h_{FE}	$V_{CE}=1.0\text{V}$, $I_C=1.0\text{A}$	50					
f_T	$V_{CE}=10\text{V}$, $I_C=50\text{mA}$, $f=100\text{MHz}$	100					MHz
C_{ob}	$V_{CB}=10\text{V}$, $I_E=0$, $f=1.0\text{MHz}$		10		15		pF

TLM621 CASE - MECHANICAL OUTLINE

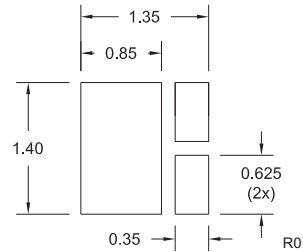


* Exposed pad P connects pins 1, 2, 5, and 6.

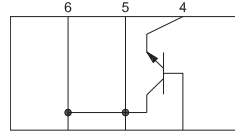
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.073	0.085	1.850	2.150
B	0.033	0.045	0.850	1.150
C	0.028	0.031	0.700	0.800
D	0.006		0.150	
E	0.000	0.002	0.000	0.050
F	0.008		0.200	
G	0.010		0.250	
H	0.020		0.500	
J	0.020		0.500	
K	0.012	0.020	0.300	0.500
L	0.007	0.012	0.180	0.300
M	0.007	0.012	0.180	0.300
N	0.007	0.012	0.180	0.300

TLM621 (REV: R2)

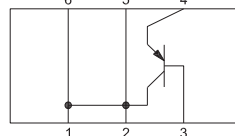
SUGGESTED MOUNTING PADS
(Dimensions in mm)



PIN CONFIGURATIONS



CTLT3410-M621



CTLT7410-M621

LEAD CODES:

- 1) Collector
- 2) Collector
- 3) Base
- 4) Emitter
- 5) Collector
- 6) Collector

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