CTN2304 N-Channel Enhancement Mode MOSFET

Features

- 30V/2.5A,$R_{DS(ON)}$=117 mΩ @V_{GS}=10V
- 20V/2.4A,$R_{DS(ON)}$=190 mΩ @V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

Applications

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

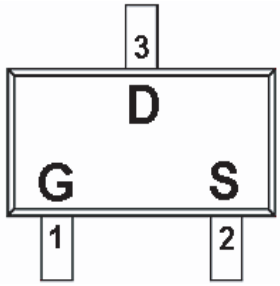
Description

The CTN2304 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

Pin Configuration (SOT-23-3L)

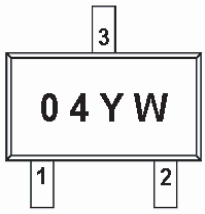


1 Gain
2 Source
3 Drain

Ordering Information

Part Number	Package	Part Marking
CTN2304S23RP	SOT-23-3L	04YW

Note: Suffix "P" means Pb - Free products.



Year Code :
4: 2004
5: 2005

Week Code :
A ~ Z(1 ~ 26)
a ~ z (27~52)

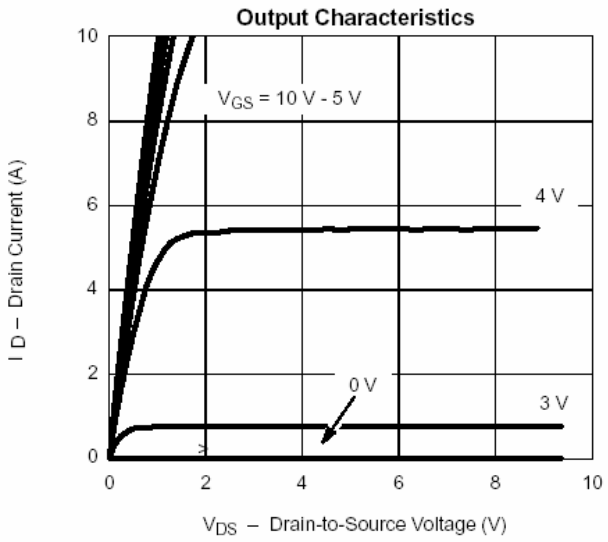
Absolute Maximum Ratings (T_A=25°C Unless otherwise noted)

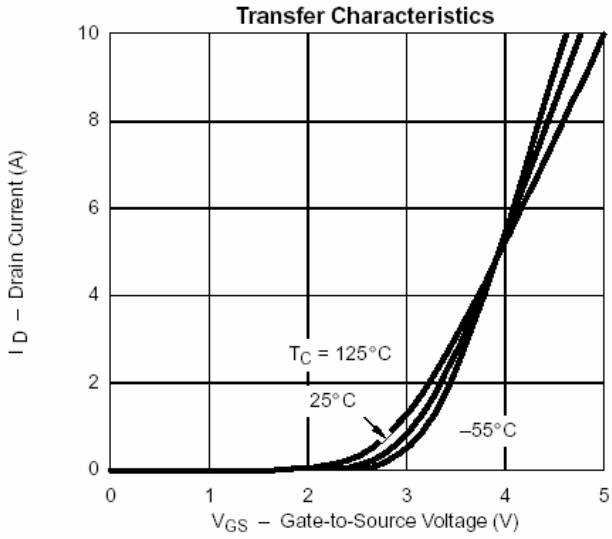
Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate–Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150°C)	T_A=25°C	I_D	2.5	A
	T_A=70°C		2.0	
Pulsed Drain Current		I_{DM}	10	A
Continuous Source Current(Diode Conduction)		I_S	1.25	A
Power Dissipation	T_A=25°C	P_D	1.25	W
	T_A=70°C		0.8	
Operating Junction Temperature		T_J	150	°C
Storage Temperature Range		T_{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R_{thJA}	100	°C/W

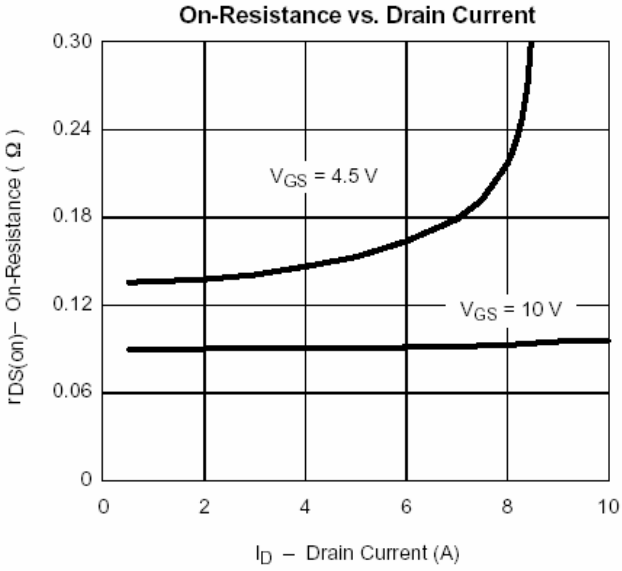
Electrical Chracteristics (T_A=25°C Unless otherwise noted)

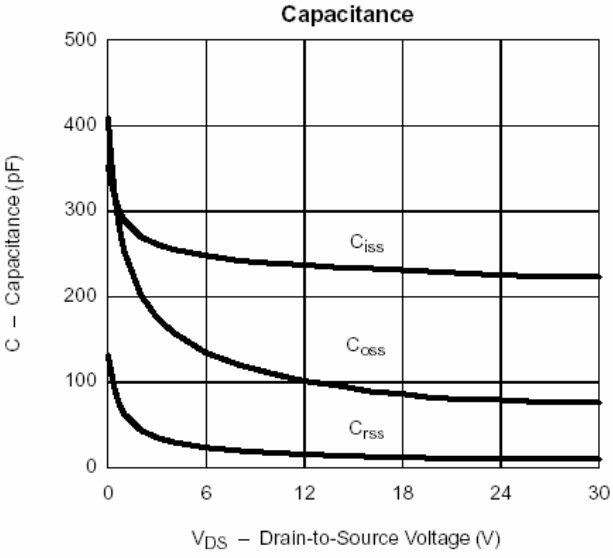
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	V_{GS}=0 V, I_D=250uA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	1.0		3.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0 V, V_{GS}=± 20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V			1	uA
		V_{DS}=30V, V_{GS}=0V T_J=55°C			10	
On-State Drain Current	$I_{D(on)}$	V_{DS}>= 4.5V, V_{GS}=10V	6			A
		V_{DS}>= 4.5V, V_{GS}=4.5V	4			
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=2.5A		0.092	0.117	Ohm
		V_{GS}=4.5V, I_D=2.0A		0.142	0.190	
Forward Transconductance	gfs	V_{DS}=4.5V, I_D=2.5A		4.6		S
Diode Forward Voltage	V_{SD}	I_S=1.25A, V_{GS}=0V		0.77	1.2	V
Total Gate Charge	Q_g	V_{DS}=15V, V_{GS}=10V I_D≅2.5A		4.5	10	nC
Gate-Source Charge	Q_{gs}			0.8		
Gate-Drain Charge	Q_{gd}			1.0		
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V f=1MHz		240		pF
Output Capacitance	C_{oss}			110		
Reverse Transfer Capacitance	C_{rss}			17		
Turn-On Time	$t_{d(on)}$	V_{DD}=15V, R_L=15Ohm I_D≅1.0A, V_{GEN}=10V R_G=6Ohm		8	20	ns
	t_r			12	30	
Turn-Off Time	$t_{d(off)}$			17	35	
	t_f			82	0	

Typical Characteristics Curves









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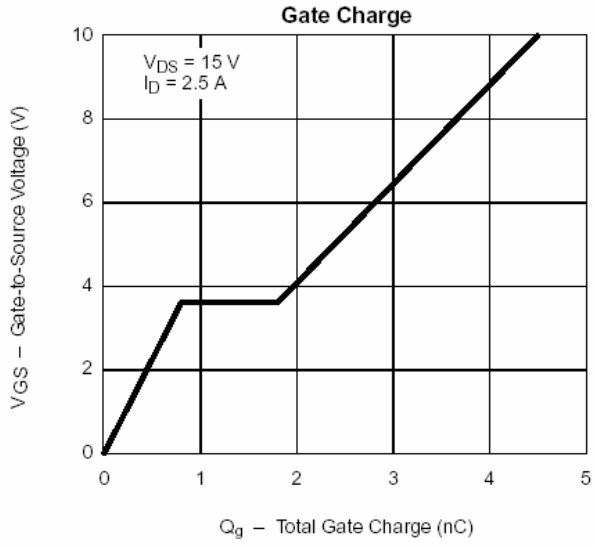

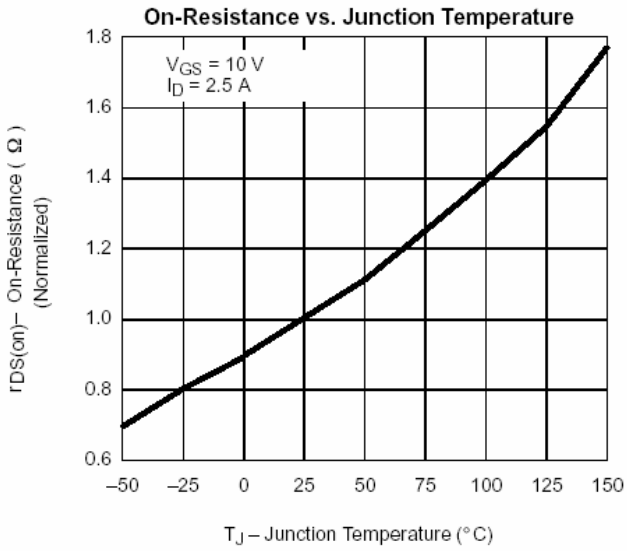

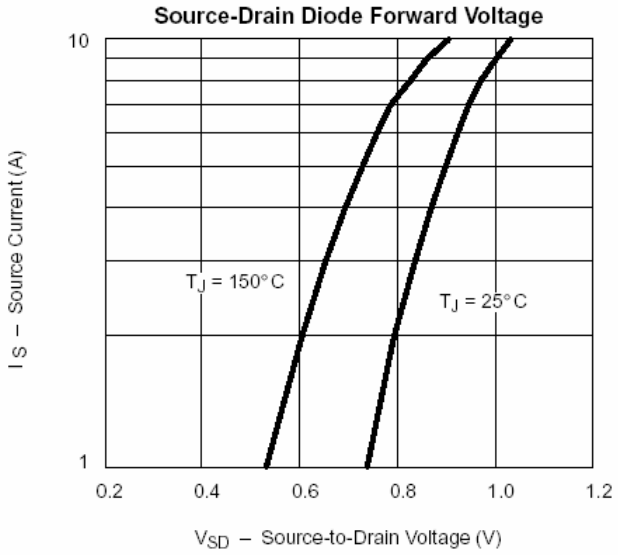

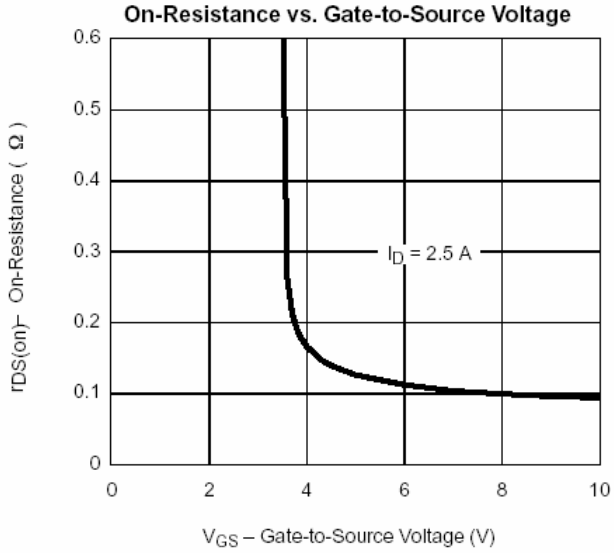

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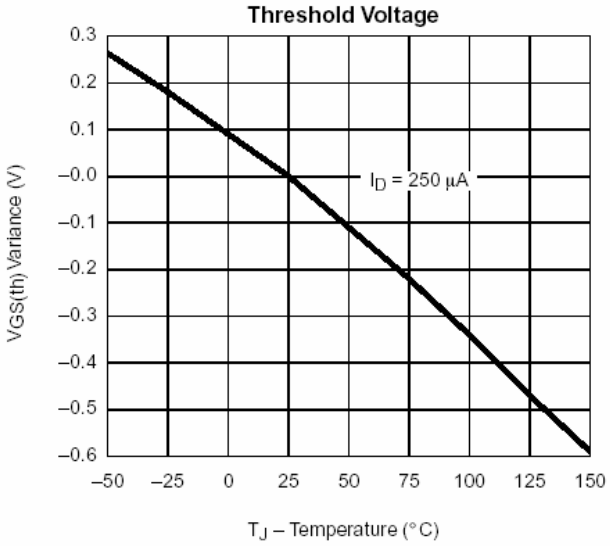
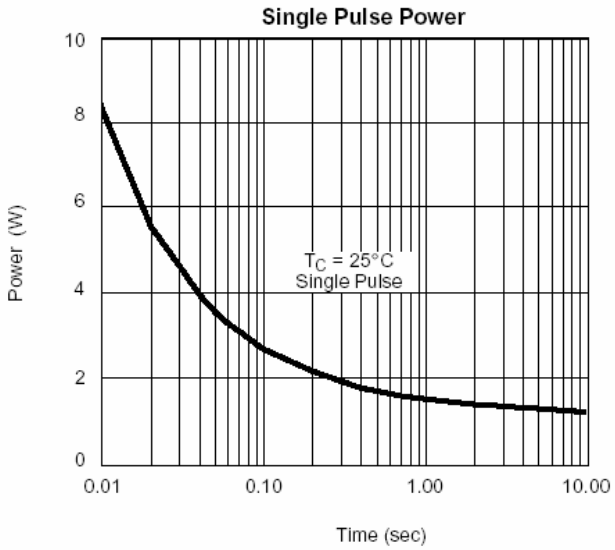
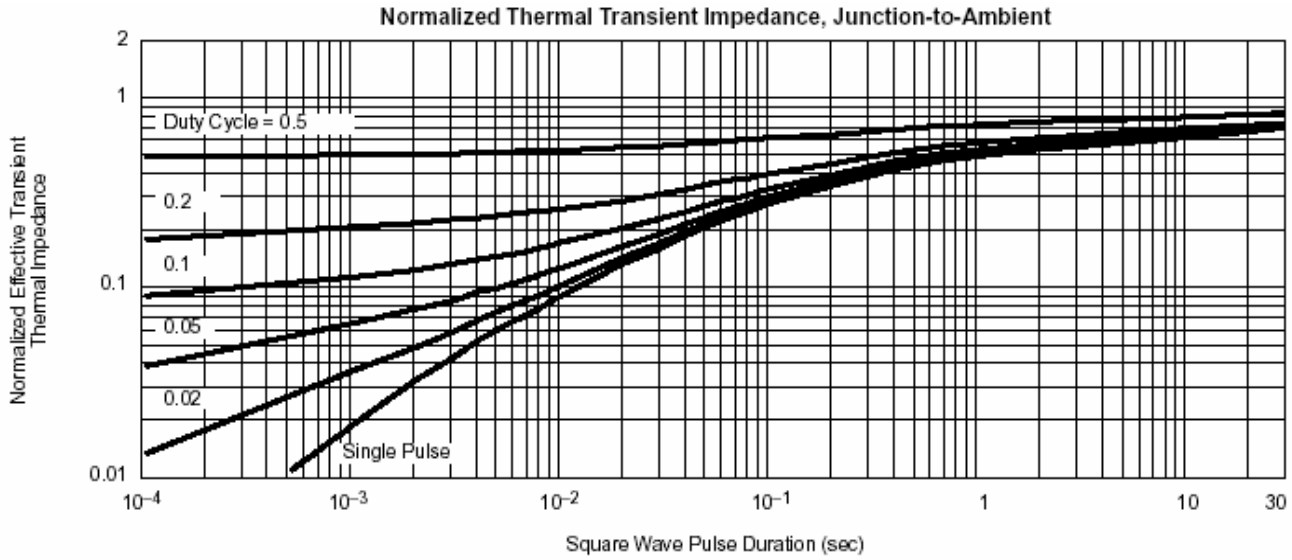
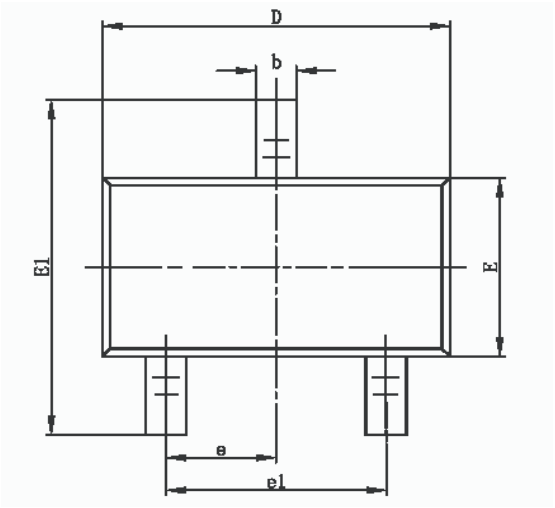
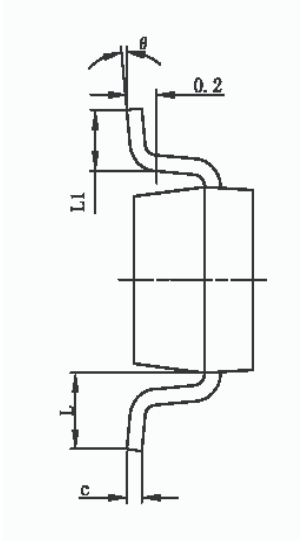


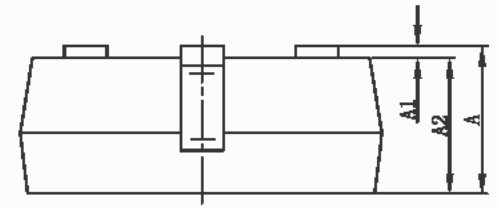




Package Outline







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
B	0.300	0.400	0.012	0.016
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.1 11	0.1 19
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.700 REF		0.028 REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°