PRODUCT SPECIFICATION

MODEL: CTW70R1140B01

< ◆ > PRELIMINARY SPECIFICAION

< ◇ > APPROVAL SPECIFICATION

CUSTOMER
APPROVED BY
DATE:

DESIGNED	CHECKED	APPROVED

REVISION STATUS

Version	Revise Date	Page	Content	Modified by
V1.0	2019.05.14	-	First Issued.	Jason

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1. GENERAL DESCRIPTION

1.1 DESCRIPTION

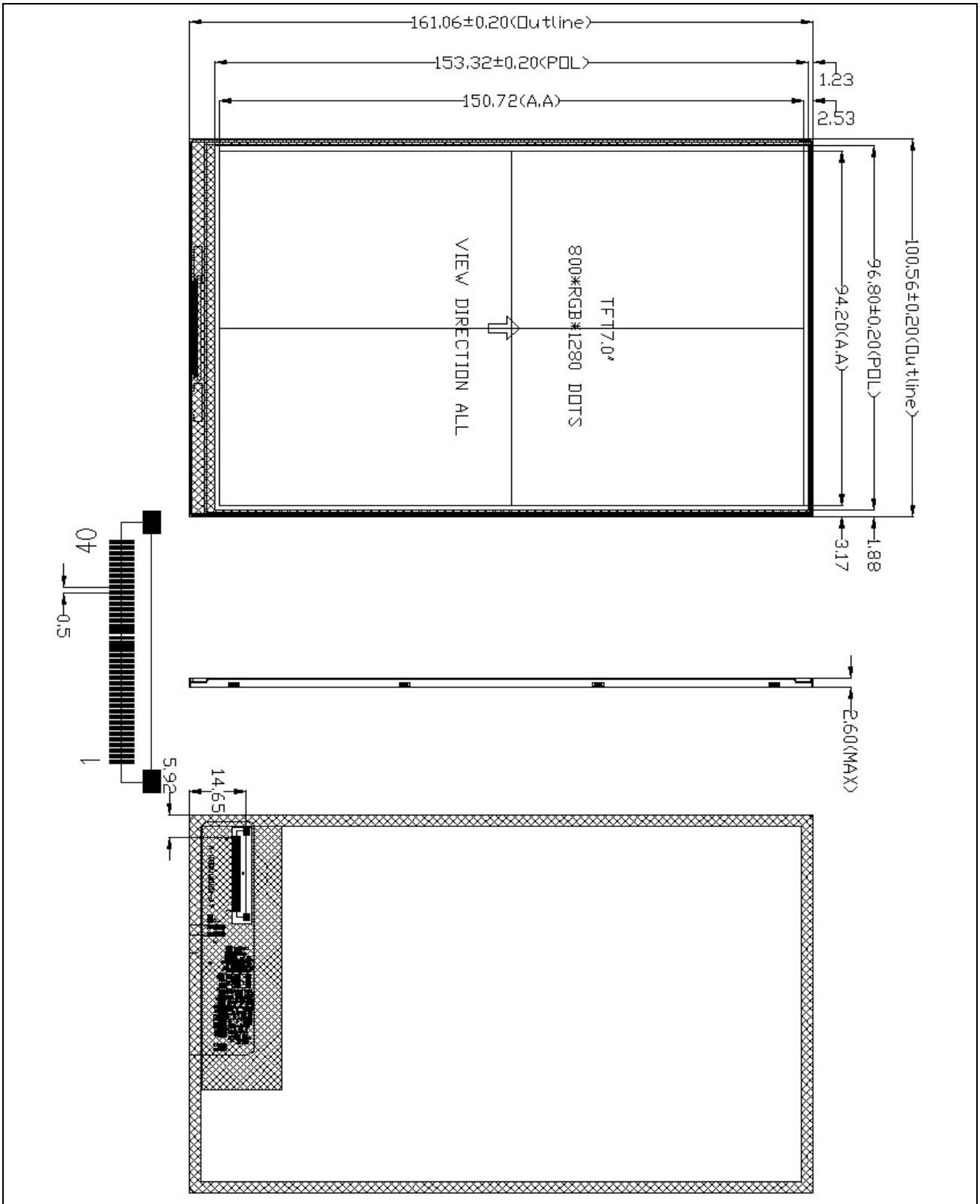
CoTiWei Display model CTW070R1140B01 is a transmissive type color active matrix liquid crystal display (LCD) which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT LCD panel, driver ICs and a backlight unit. The following table describes the features of this LCM.

1.2 FEATURES

No.	Item	Specification	Unit
1	Panel Size	7	inch
2	Number of Pixels	800 × 3(RGB) ×1280	pixels
3	Active Area	94.20(H) ×150.72(V)	mm
4	Pixel Pitch	0.11775(H) ×0.11775(V)	mm
5	Outline Dimension	100.56 (H) × 161.06(V) × 2.60(D)	mm
6	Pixel arrangement	RGB Vertical stripe	-
7	Display Mode	IPS with Normally Black	-
8	Viewing Direction	ALL Viewing Direction	-
9	Display Color	16.7M	-
10	Surface Treatment	Anti-Glare and Hard-coating 3H	-
11	Interface	MIPI	-
12	Backlight	White LED	-
13	Drive IC	-	-
14	Operation Temperature	0~50	ºC
15	Storage Temperature	-20~60	ºC
16	Weight	TBD(Typ.)	g

2. MECHANICAL SPECIFICATION

Unit:mm



Connector:pitch=0.5mm,40Pin

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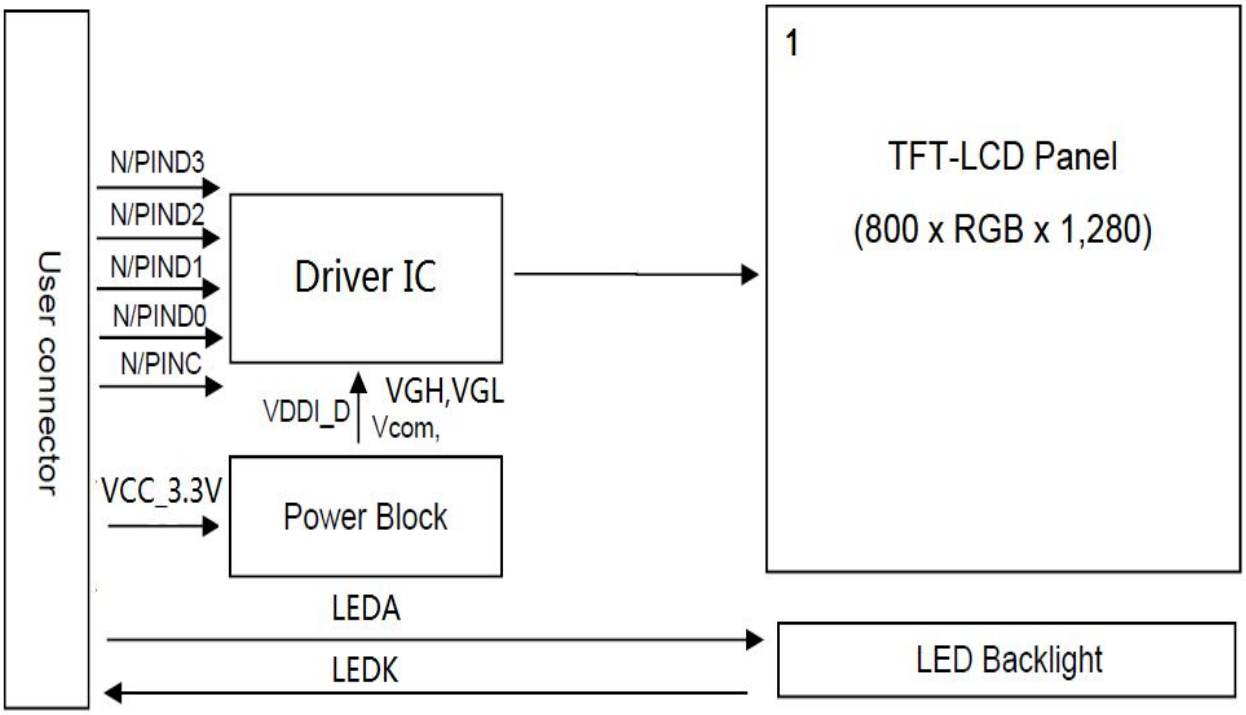
3. PIN DESCRIPTION

3.1 CN1 of FPC

Pin No.	Symbol	I/O	Function	Remark
1	NC	-	No connection	
2	VDD	P	Power supply VDDIN=3.3V	
3	VDD	P	Power supply VDDIN=3.3V	
4	GND	P	Ground	
5	RESET	I	Global reset signal(3.3V)	
6	NC	-	No connection	
7	GND	P	Ground	
8	D0N	I	0-MIPI differential data	
9	R0P	I	0+MIPI differential data	
10	GND	P	Ground	
11	D1N	I	1-MIPI differential data	
12	D1P	I	1+MIPI differential data	
13	GND	P	Ground	
14	CLKN	I	- MIPI differential clock input	
15	CLKP	I	+MIPI differential clock input	
16	GND	P	Ground	
17	D2N	I	2-MIPI differential data	
18	D2P	I	2+MIPI differential data	
19	GND	P	Ground	
20	D3N	I	3-MIPI differential data	
21	D3P	I	3+MIPI differential data	
22	GND	P	Ground	
23	NC	-	No connection	
24	NC	-	No connection	
25	GND	P	Ground	
26	NC	-	No connection	
27	NC	-	No connection	
28	NC	-	No connection	
29	NC	-	No connection	
30	GND	P	Ground	
31	LED-	P	LED Cathode	
32	LED-	P	LED Cathode	
33	NC	-	No connection	
34	NC	-	No connection	
35	NC	-	No connection	
36	NC	-	No connection	
37	NC	-	No connection	
38	NC	-	No connection	
39	LED+	P	LED Anode	
40	LED+	P	LED Anode	

Note1: I/O definition:I: input, O: output, P: Power, -:No connection

4. BLOCK DIAGRAM



5. ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS

AGND= GND=0V, Ta = 25 ℃

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Power voltage	VDD-VSS	-0.5	5.0	V	

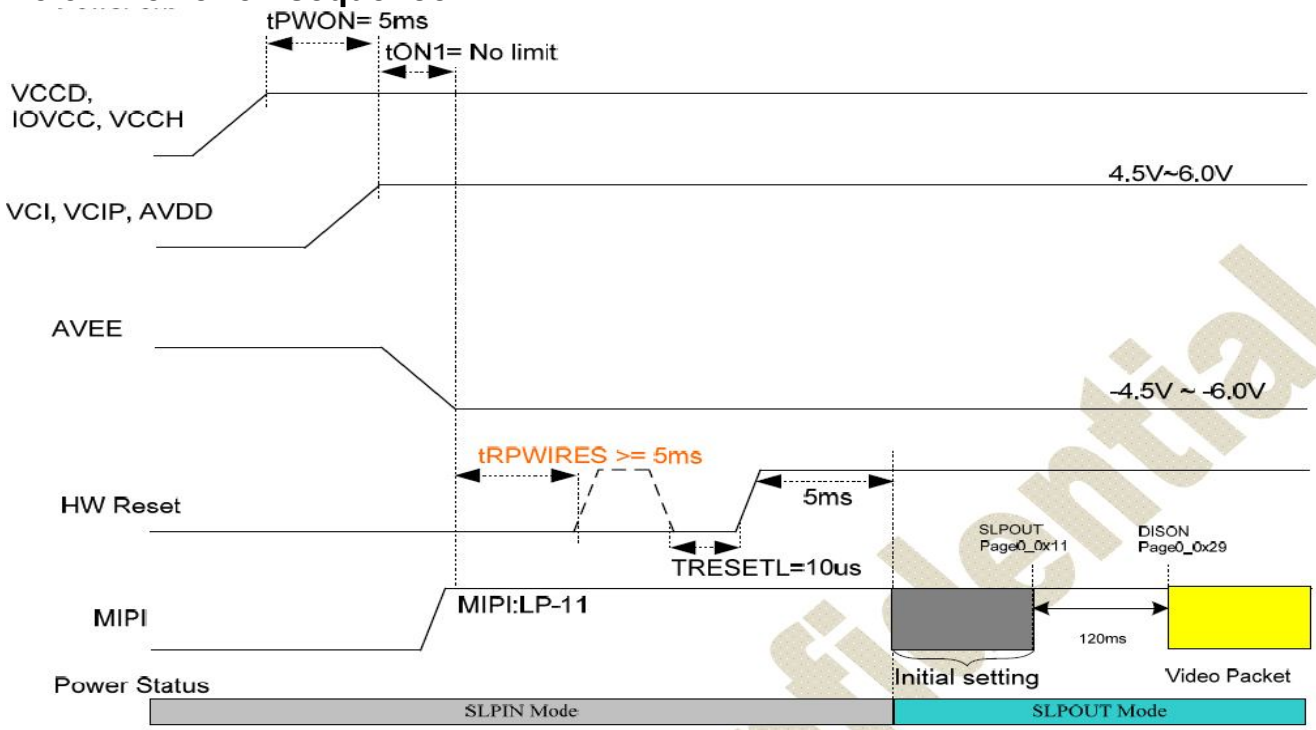
5.2 RECOMMENDED OPERATING CONDITION

AGND=GND=0V, Ta = 25℃

Item		Symbol	Values			Unit	Remark
			Min.	Typ.	Max.		
Digital Supply Voltage		VDD	3.0	3.3	3.6	V	-
Power IC provides voltage		AVEE	-6	-5	-4.5	V	-
		AVDD	4.5	5.5	6.0	V	-
Driver IC provides voltage internally		VGH	9	-	20	V	-
		VGL	-20	-	-9	V	-
Input Signal Voltage	Low Level	VIL	0	-	0.3*VDD	V	-
	High Level	VIH	0.7*VDD	-	VDD	V	

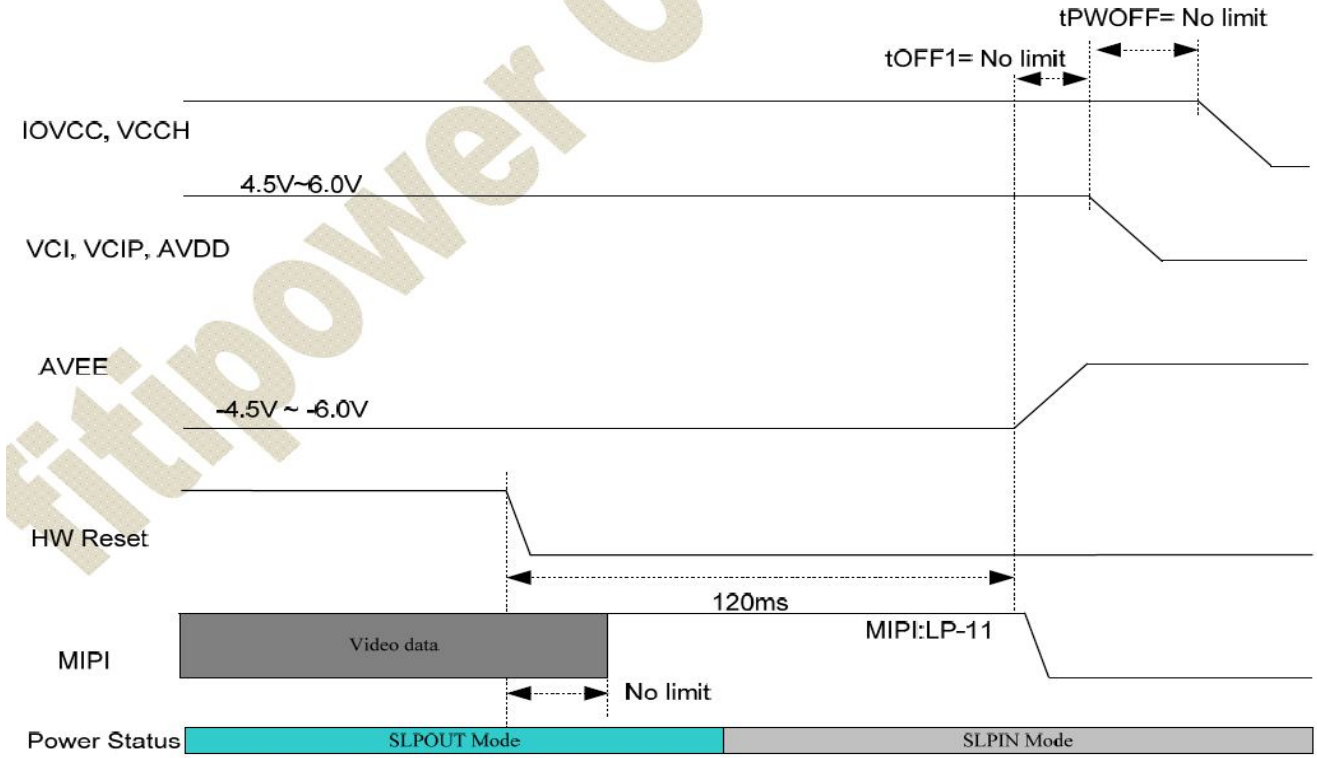
5.3 POWER SEQUENCE

5.3.1 Power on sequence



Note: tON1: The space time between VCI/VCIP/AVDD Power On and AVEE Power On.

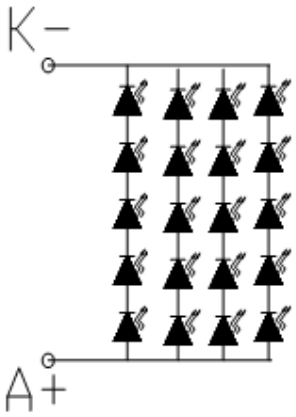
5.3.2 Power off sequence



5.5 BACKLIGHT UNIT

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Forward voltage	VF	14	15	16.5	V	IF=20mA/1-chip
Forward current	If	-	80	-	mA	

5.5.1 Internal Circuit Diagram

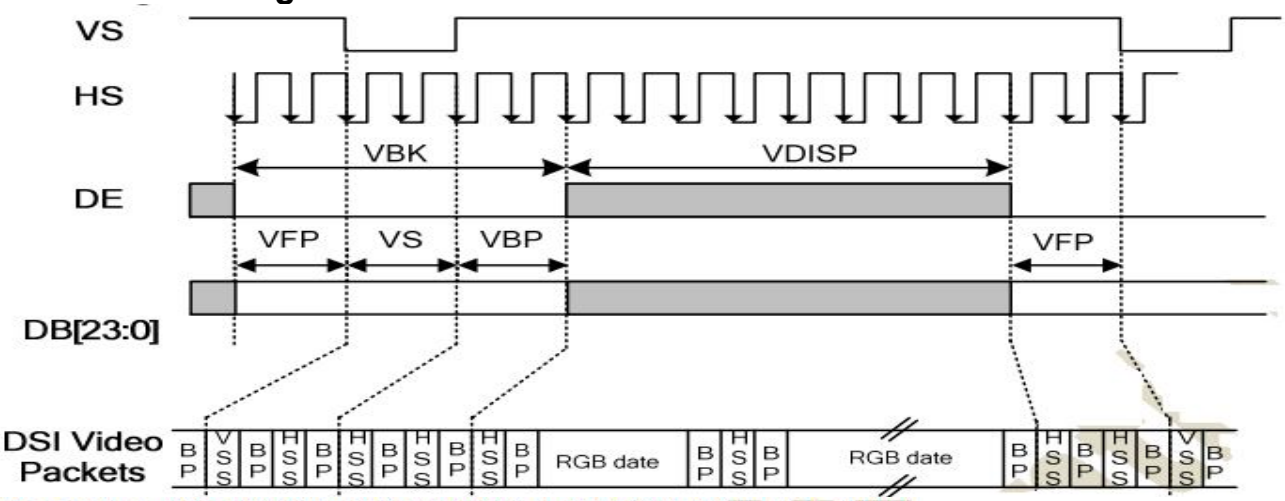


CURRENT IF=80mA
20mA*4=80mA

6. INPUT SIGNAL CHARACTERISTICS

6.1 Timings for DSI Video mode

Vertical Timings

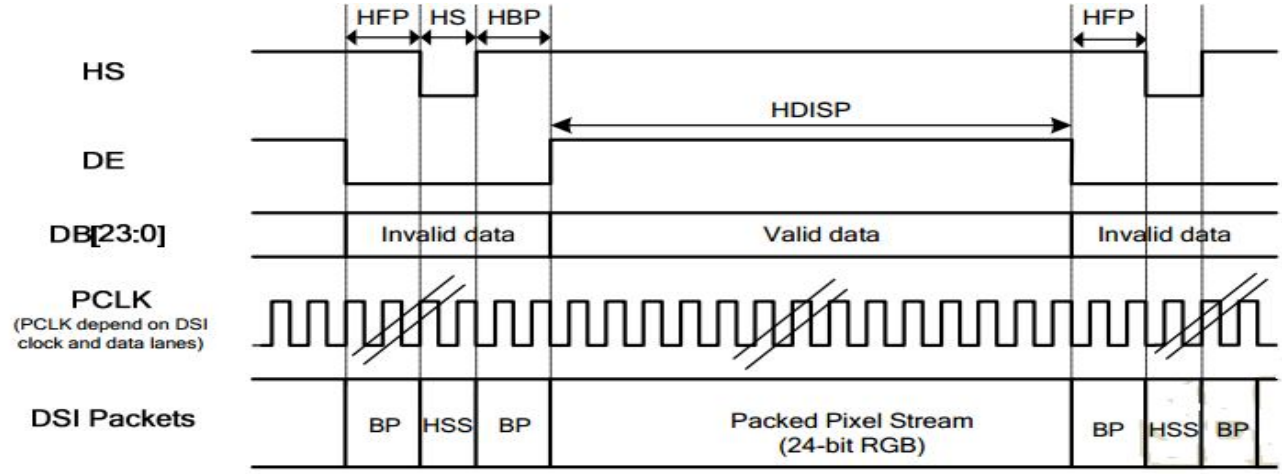


Resolution=800x1280(T_A=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

Horizontal Timings



Resolution=800x1280 (T_A=25°C, IOVCC=1.8V, VCIP=VCI=VCCH=2.8V)

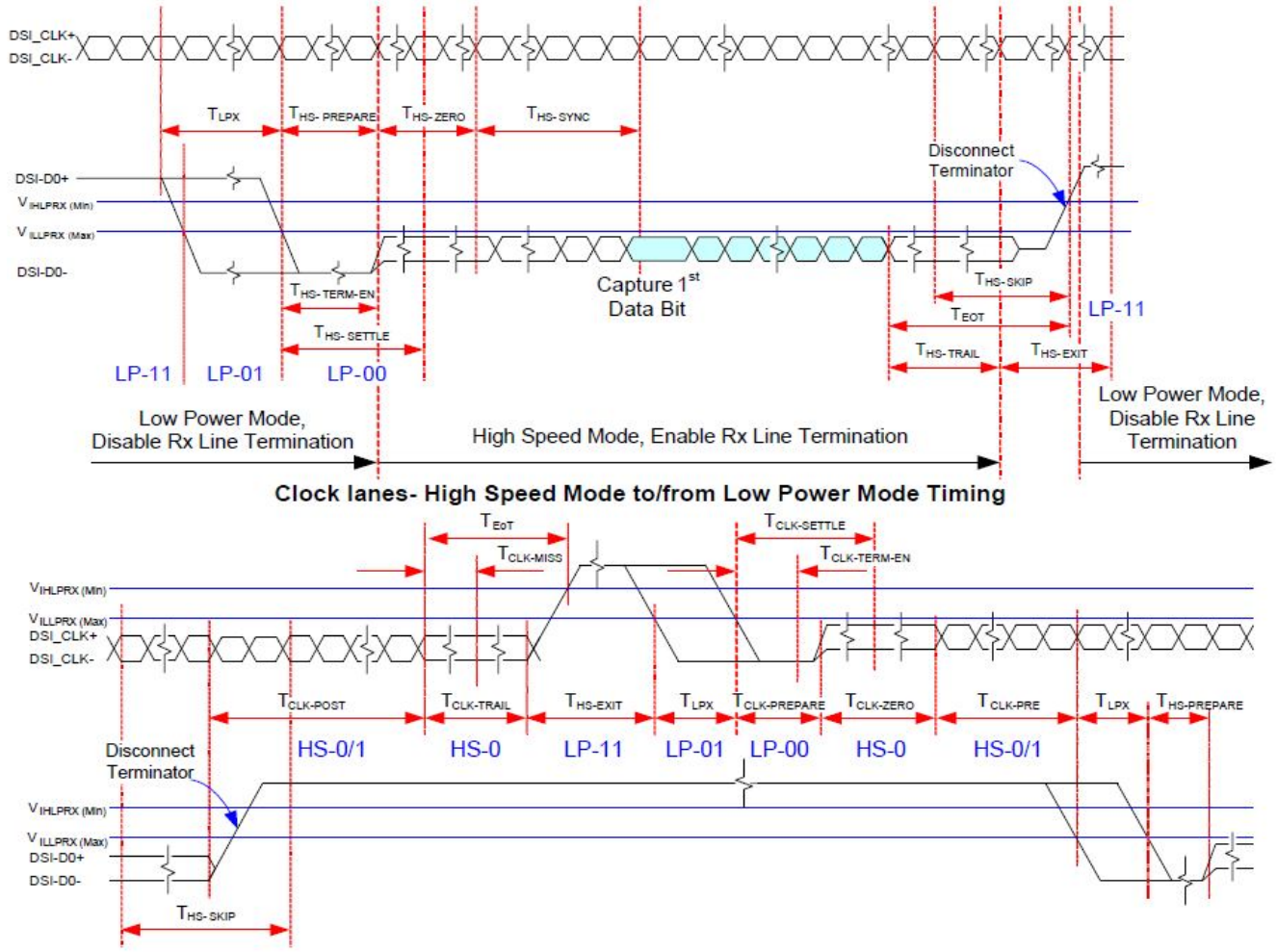
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	6	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	16	-	88	DCK
Horizontal active area	HDISP	-	-	800	-	DCK

6.2 Burst Mode Data Transmission

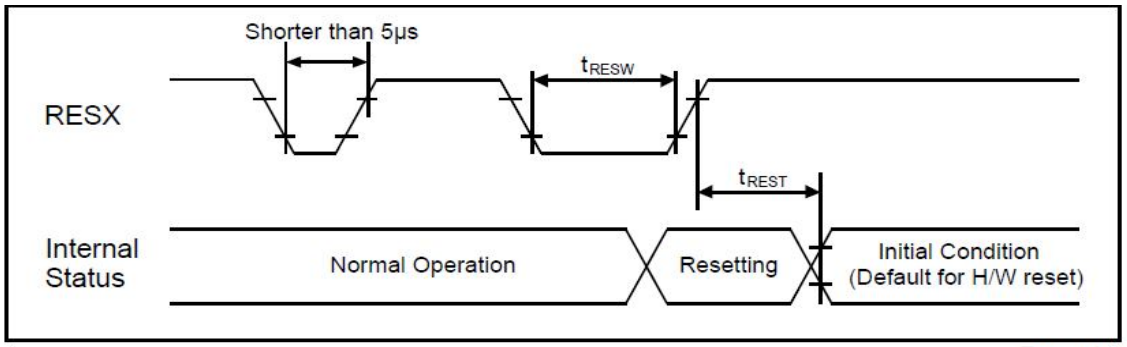
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	TCLK-TR	Time to drive HS	60	-	-	ns	Input
	AIL	differential state after last payload clock bit of a HS transmission burst					
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE+ TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn=D0, D1, D2, D3.

Note 2) Two HS transmission can be sent with a break as short as THS-EXIT from each other in continuous clock mode.In discontinuous mode,the break is longer which account TCLK-POS,TCLK-TRAIL and THS-EXIT,before activity in clock and data lanes again.



6.3 Reset Input Timing



Reset input timing
(VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tRESW	Reset "L" pulse width (Note 1)	10	-	-	μs	
	tREST	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

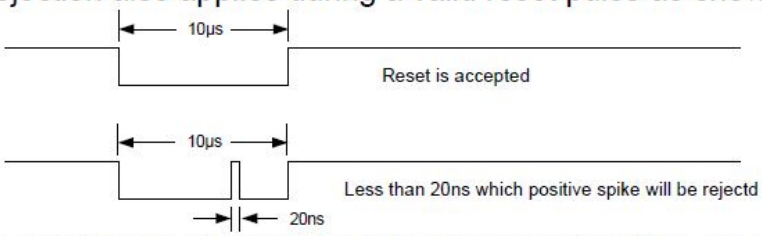
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset Start

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

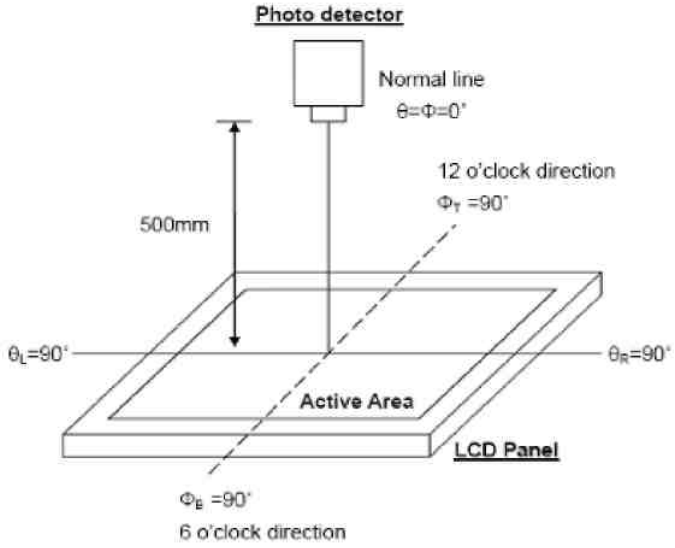
7. OPTICAL CHARACTERISTICS

Light source :c-light(with normal polarizer)

Item		Symbol	Condition	Values			Unit	Remark
				Min.	Typ.	Max.		
Viewing angle		Θ_u	CR≧10	80	85	-	degree	Note2
		Θ_D		80	85	-		
		Θ_L		80	85	-		
		Θ_R		80	85	-		
Response time		$T_{ON}+T_{OFF}$	θ=Φ =0° Normal viewing angle	-	25	50	ms	Note1 Note3
Contrast ratio		CR		600	800	-	-	Note1 Note4
Luminance		L		280	300	-	cd/m²	
Luminance uniformity		YU		75	-	-	%	
Color chromaticity (CIE1931)	White	W_X		0.276	0.296	0.316		Note1 Note5
		W_Y		0.302	0.322	0.342		
	Red	R_X		-	-	-		
		R_Y		-	-	-		
	Green	G_X		-	-	-		
		G_Y		-	-	-		
	Blue	B_X		-	-	-		
		B_Y		-	-	-		
NTSC					60%			

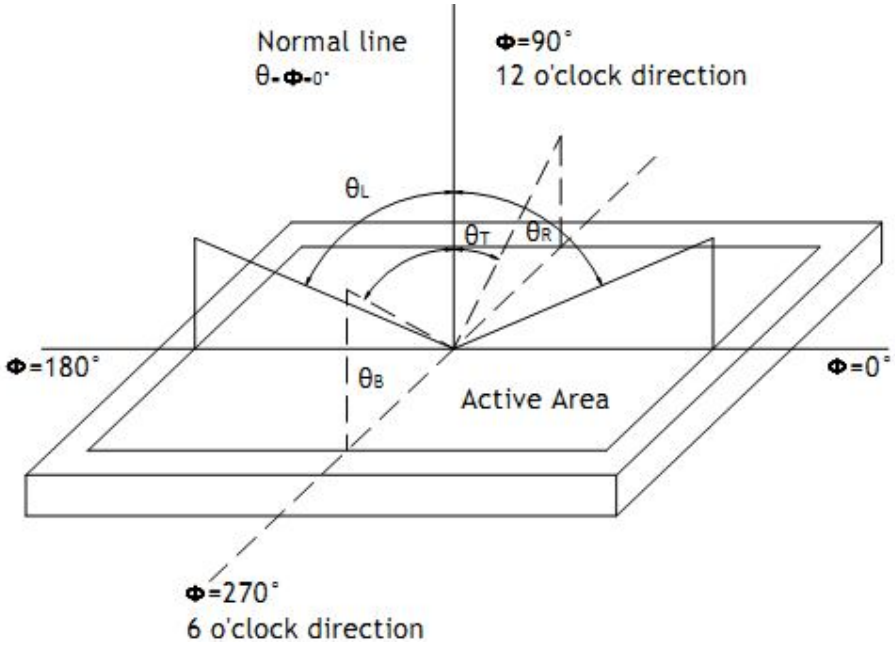
Test Conditions:
1.Measuring surrounding:dark room
2.The ambient temperature is 25±2°C.
3.The test systems refer to Note1 and Note2.

Note1: Definition of optical measurement system



Note2: Definition of viewing angle range and measurement system

Viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80).



Note3: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.

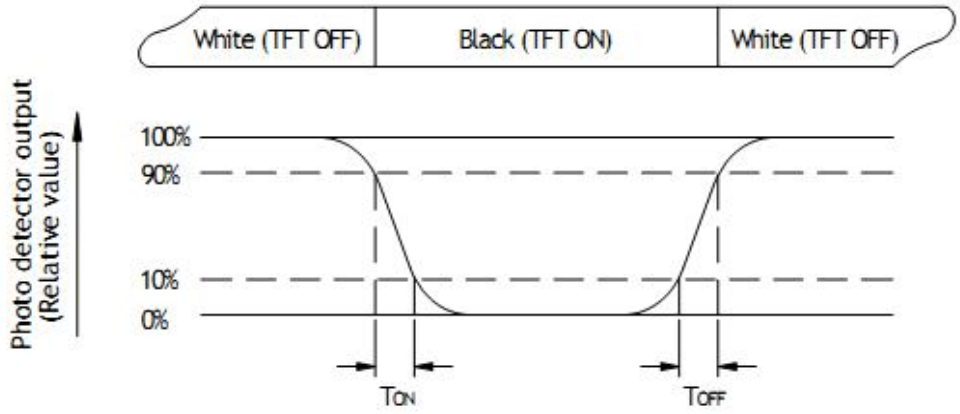


Fig. 6-3 Definition of response time

Note4: Definition of contrast ratio

$$\text{Contrast ratio(CR)} = \frac{\text{Luminance measured when LCD on the Whitestate}}{\text{Luminance measured when LCD on the Blackstate}}$$

"White state ": The state is that the LCD should drive by Vwhite.

"Black state": The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note6: All input terminals LCD panel must be ground while measuring the center area of the panel.

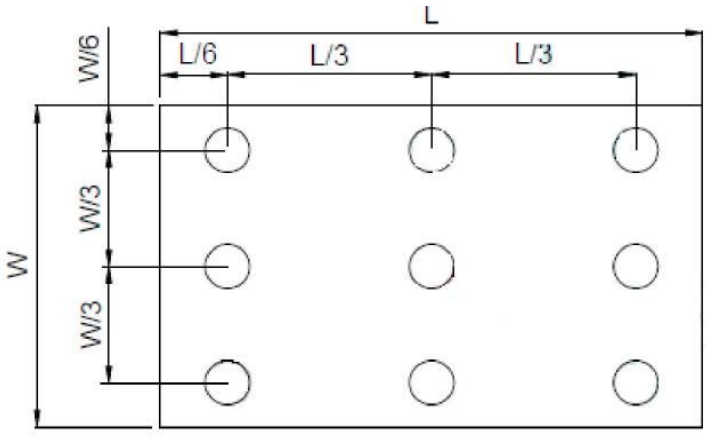
The LED driving condition is IL=20mA of which each LED module is 3 LED serial.

Note7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas.Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L----Active area length, W---- Active area width



Bmax: The measured maximum luminance of all measurement position.

Bmin: The measured minimum luminance of all measurement position.

Note8: Definition of Luminance

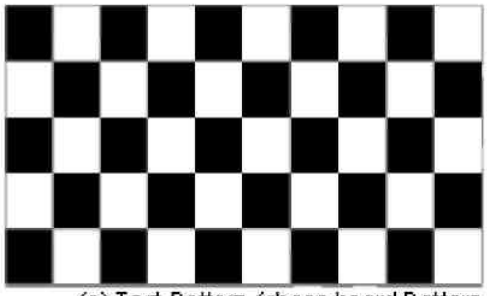
Measure the luminance of white state at center point.

8. QUALITY ASSURANCE SYSTEM

8.1 TEMPERATURE AND HUMIDITY

Test Item	Test Condition
High Temperature Storage	Ta=60℃; 240hrs
Low Temperature Storage	Ta=-20℃; 240hrs
High Temperature Operation	Ta=50℃；240hrs
Low Temperature Operation	Ta=0℃; 240hrs
High Temperature High Humidity Operation	Ta=50℃； 90%RH； 240hrs(no condensation)
Thermal Shock	-20℃(0.5hrs) ~ 60℃(0.5hrs) / 100 cycles
Image Sticking	25℃ ；2hrs Note1

Note1:Condition of image sticking test :25°C±2°C
Operation with test pattern sustained for 4hrs,then change to gray pattern immediately.after5 mins,the mura must be disappeared completely


(a) Test Pattern (chess board Pattern)


(b) Gray Pattern

8.2 VIBRATION & SHOCK

Test item	Conditions
Packing Shock (non-operation)	Shock level:980m/s^2 Waveform:1/2 Sine wave,6msec ±X, ±Y ±Z,each axis 1 times
Packing Vibration (non-operation)	Frequency range:8 HZ~33.3HZ Stroke:1.0mm,sweep:10 HZ ~50 HZ x,y,z 2 hours for each direction

8.3 ESD

Test item	Conditions
Electro Static Discharge Test (non-operation)	150pF,330Ω， Contact±4KV,Air :±8KV Note 1
	200pF,0Ω， ±200V Contact test.Note 2

Note1:LCD glass and metal bezel
Note2:IF connector pins

9. GENERAL PRECAUTION

9.1 SAFETY

(1) Do not swallow any liquid crystal, even if there is no proof that liquid crystal is poisonous.
(2) If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.
(3) If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

9.2 STORAGE CONDITIONS

(1) Store the panel or module in a dark place where the temperature is 23±5°C and the humidity is below 50±20%RH.
(2) Store in anti-static electricity container.
(3) Store in clean environment, free from dust, active gas, and solvent.
(4) Do not place the module near organics solvents or corrosive gases.
(5) Do not crush, shake, or jolt the module.

9.3 HANDLING PRECAUTIONS

(1) Avoid static electricity which can damage the CMOS LSI.
(2) The polarizing plate of the display is very fragile. So, please handle it very carefully.
(3) Do not give external shock.
(4) Do not apply excessive force on the surface.
(5) Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the Surface of plate.
(6) Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.
(7) Do not operate it above the absolute maximum rating.
(8) Do not remove the panel or frame from the module.
(9) When the module is assembled, it should be attached to the system firmly, Be careful not to twist and bend the module.
(10)Wipe off water droplets or oil immediately. If you leave the droplets for a long time, staining and discoloration may occur.
(11) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

9.4 WARRANTY

(1)The period is within twelve months since the date of shipping out under normal using and storage conditions.
(2) Do not repaired or modified the LCM . It may cause function to lose efficacy , Starry does not warrant the LCM.
(3) All process and material comply RoHS.

10. PACKAGE DRAWING

TBD