

**AMI5HG 0.5 micron CMOS Gate Array**

**Description**

CVDD is the resistive tie-up to the core  $V_{DD}$  bus for all cell inputs.

**Equivalent Gates** ..... 1.0

**HDL Syntax**

Verilog ..... `CVDD inst_name (Q);`

VHDL..... `inst_name: CVDD port map (Q);`

