

## AMI5HG 0.5 micron CMOS Gate Array

### Description

CVSS is the resistive tie-down to the core  $V_{SS}$  bus for all cell inputs.

Equivalent Gates ..... 1.0

### HDL Syntax

Verilog ..... CVSS *inst\_name* (Q);

VHDL ..... *inst\_name*: CVSS port map (Q);

Core  
Logic

