Four-Channel, Low Phase Noise, Low Power, Continuous Wave Transmitter

Features

- Low phase noise
- 100V open drain N-channel
- High speed D flip-flop
- High speed MOSFET gate driver
- Up to 200MHz clock input
- V_{DD} and V_{LL} undervoltage lockout

Applications

- Diagnostic medical ultrasound
- Fluid flow measurement

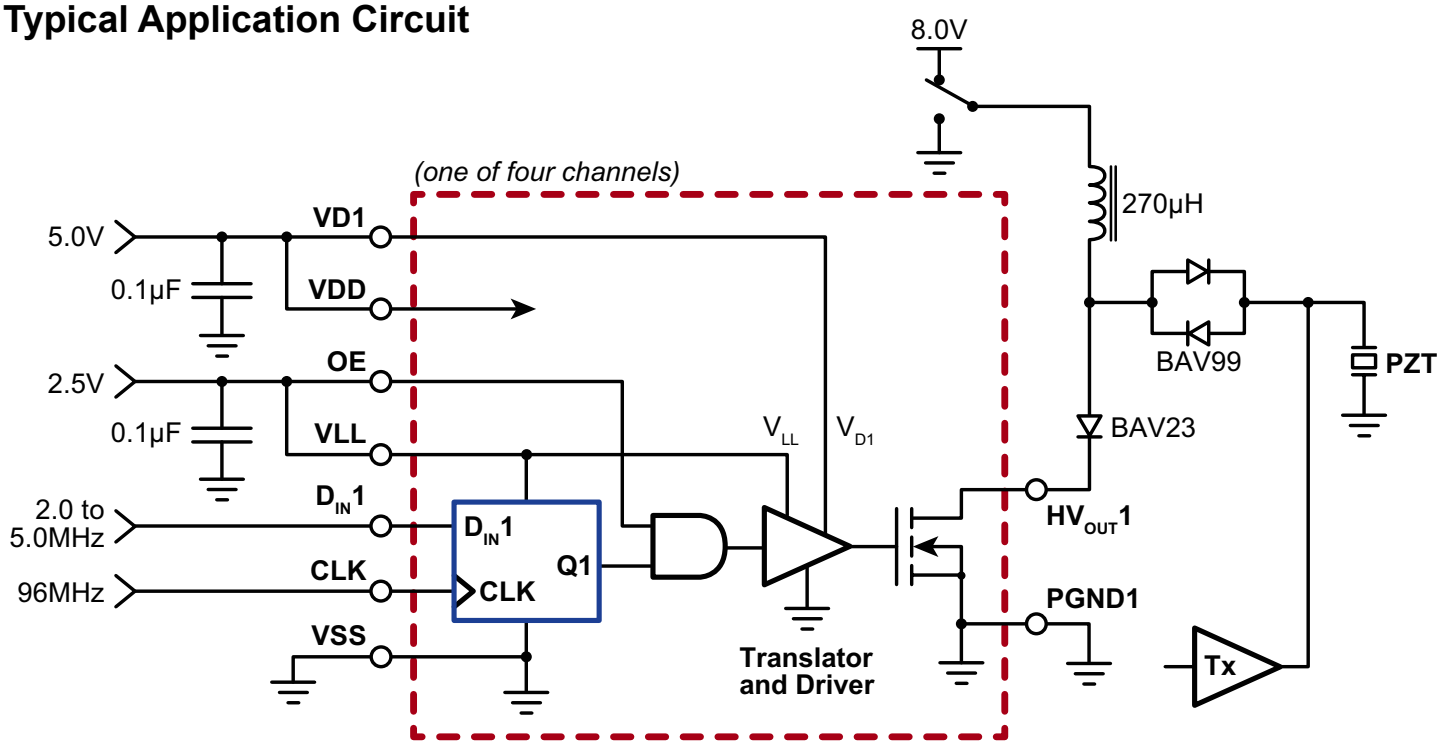
General Description

The Supertex CW01 is a four-channel, low phase noise, continuous wave transmit IC. A high speed D flip-flop is provided to allow the D_{IN} frequency to be aligned to a high frequency clock. The output N-channel is turned on when a logic high is clocked into the D flip-flop. Data are clocked in during the low to high transition.

VD1, VD2, VD3 and VD4 are four individual input supply voltages for the N-channel output MOSFET gate drivers. High peak currents are drawn from these gate drives when the output MOSFETs are switching. To minimize jitter caused by voltage ripples, each channel has its own gate drive voltage pin; VD1, VD2, VD3 and VD4. A series ferrite bead and a decoupling capacitor are recommended on each VDX pin to minimize output jitter and channel to channel crosstalk.

Both V_{DD} and V_{LL} have undervoltage lockout to prevent spurious turn-on.

Typical Application Circuit



Ordering Information

Device	Package Option
	24-Lead QFN *4.00x5.00mm body* *1.00mm height (max) 0.50mm pitch*
CW01	CW01K6-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

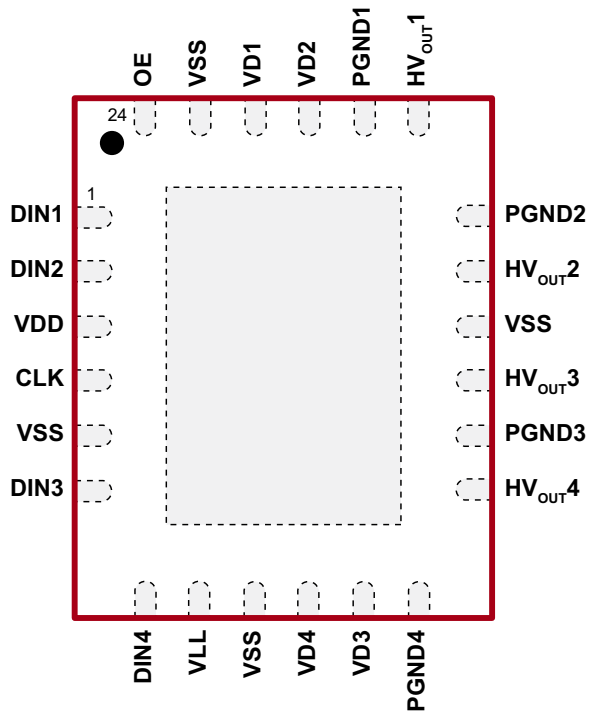
Parameter	Value
V_{LL}, logic supply	-0.3 to +6.0V
V_{DD}, level translator voltage	-0.5 to +6.0V
V_{DX}, gate drive voltage	-0.5 to +6.0V
HV_{OUT}, high voltage output drain voltage	-0.5 to 120V
Maximum junction temperature	+125°C
Storage temperature range	-65°C to +150°C
Power dissipation, T_A = 25°C	3.0W[1]
θ_{ja}	26.9°C/W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Note:

1. *Device mounted on a 4 layer 3" by 4" board.*

Pin Configuration



24-Lead QFN (K6)
(top view)

Product Marking

Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
———— = "Green" Packaging

Package may or may not include the following marks: Si or ⚡

24-Lead QFN (K6)

DC Electrical Characteristics

(V_{DD} = V_{DX} =5.0V, V_{LL} = 2.5V, T_J = 25ºC unless otherwise specified)

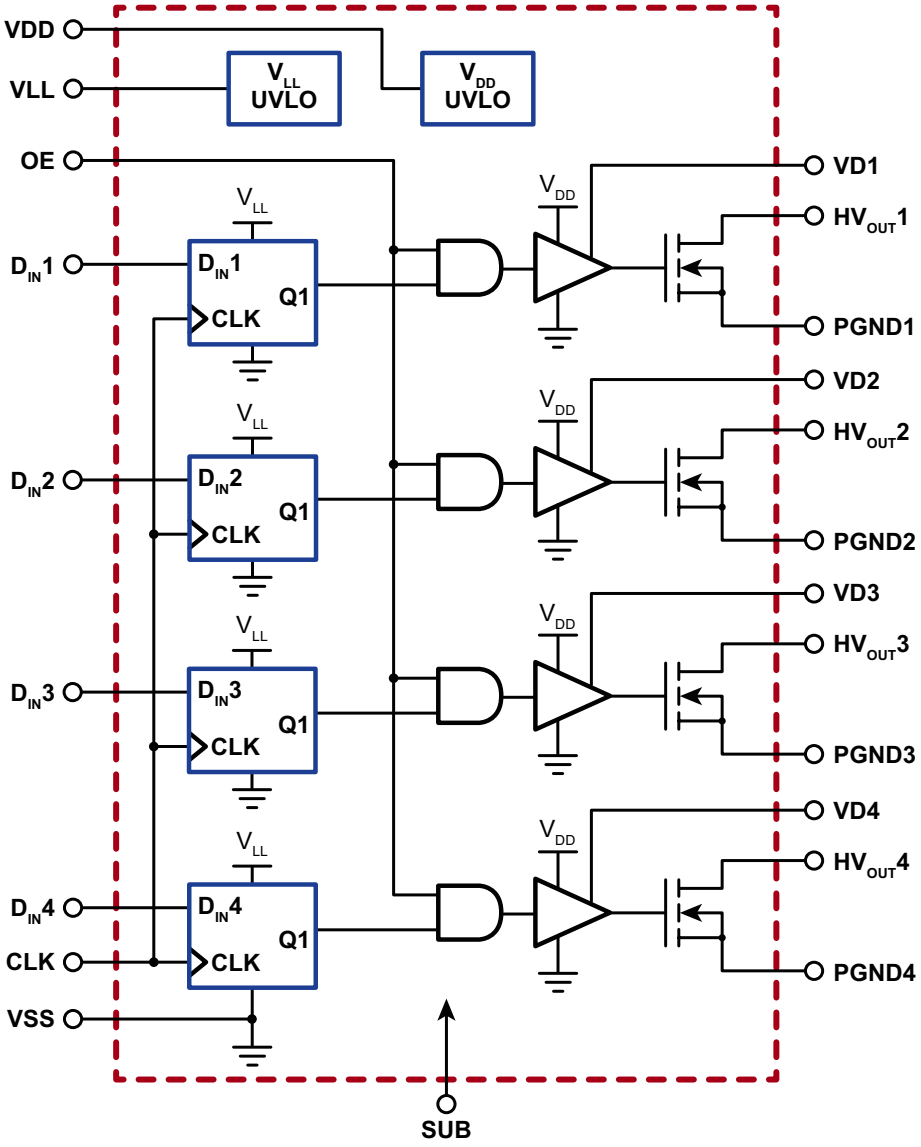
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
HV_{OUT}	High voltage output	0	-	100	V	---
V_{DD}	V_{DD} voltage range	4.5	5.0	5.5	V	---
t_{VDD-ON}	V_{DD} rise time	50	-	-	µs	---
V_{LL}	V_{LL} voltage range	1.65	2.5	5.5	V	---
t_{VLL-ON}	V_{LL} rise time	50	-	-	µs	---
V_{DIN}	Logic input voltage range	0	-	V_{LL}	V	---
V_{DX}	Gate drive voltage	4.5	5.0	5.5	V	---
t_{VDX-ON}	V_{DX} rise time	50	-	-	µs	---
I_{DDQ}	V_{DD} quiescent current	-	63	100	µA	---
I_{DD}	V_{DD} average current	-	23.5	30	mA	f_{CLK} = 200MHz, f_{OUT} = 5.0MHz, all 4-ch active
I_{LLQ}	V_{LL} quiescent current	-	8.1	20	µA	---
I_{LL}	V_{LL} average current	-	380	600	µA	f_{CLK} = 200MHz, f_{OUT} = 5.0MHz, all 4-ch active
I_{DXQ}	V_{DX} quiescent current	-	0	1.0	µA	---
I_{DX}	V_{DX} average current	-	11.3	30	mA	f_{CLK} = 200MHz, f_{OUT} = 5.0MHz, all 4-ch active
V_{IH}	Input logic high voltage	$0.8V_{LL}$	-	V_{LL}	V	---
V_{IL}	Input logic low voltage	0	-	$0.2V_{LL}$	V	---
I_{IH}	Input logic high current	-	-	1.0	µA	---
I_{IL}	Input logic high current	-1.0	-	-	µA	---
R_{ON}	Output on resistance	-	4.7	7.0	Ω	I_{IN} = 100mA
I_{SAT}	Output saturation current	-	0.8	-	A	V_{DD} = HV_{OUT} = 5.0V
I_{HVleak}	High voltage output leakage	-	-	10	µA	HV_{OUT} = 100V
UVLO_V_{LL}	UVLO trip point for V_{LL}	-	1.5	-	V	---
UVLO_V_{DD}	UVLO trip point for V_{DD}	-	4.0	-	V	---
T_J	Operating junction temperature	-40	-	+125	°C	---

AC Electrical Characteristics

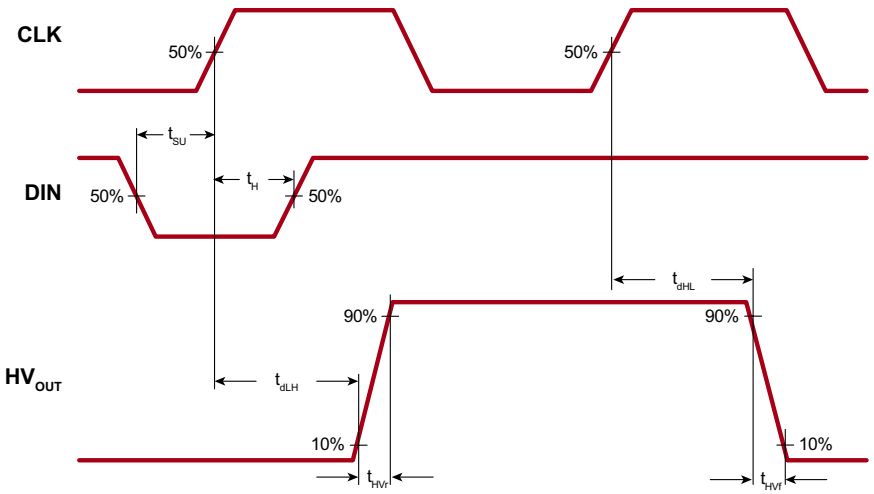
(V_{DD} = V_{DX} =5.0V, V_{LL} = 2.5V, T_J = 25ºC unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{CLK}	Clock frequency	0	-	200	MHz	-
t_r, t_f	Clock rise and fall times	-	0.5	5.0	ns	-
t_{SU}	Set-up time, DIN to CLK	2.0	-	-	ns	-
t_H	Hold time, DIN from CLK	1.0	-	-	ns	-
t_{HVf}	HV_{OUT} fall time	-	0.8	-	ns	Load = 50Ω to 8.0V. See timing diagram
t_{HVr}	HV_{OUT} rise time	-	3.3	-	ns	Load = 50Ω to 8.0V. See timing diagram
t_{dLH}	Delay time from CLK to HV_{OUT} from low to high	-	5.1	-	ns	Load = 50Ω to 8.0V. See timing diagram
t_{dHL}	Delay time from CLK to HV_{OUT} from high to low	-	2.6	-	ns	Load = 50Ω to 8.0V. See timing diagram
$\Delta t_{dLHdelay}$	Delay time matching for t_{dLH}	-	0.5	1.0	ns	-
$\Delta t_{dHLdelay}$	Delay time matching for t_{dHL}	-	0.5	1.0	ns	-
$t_{OE(ON)}$	Output enable turn-on time	-	-	10	µs	
$t_{OE(OFF)}$	Output enable turn-off time	-	-	0.1	µs	-
C_{OUT}	Output capacitance	-	8.0	-	pF	At 8.0V
		-	4.0	-	pF	At 100V
Phase noise	Phase noise	-	-171	-160	dBC	dB below carrier CLK = 80MHz, D_{IN} = 2.0MHz freq offset = 1.0kHz noise bandwidth = 140Hz See test circuit.

Block Diagram

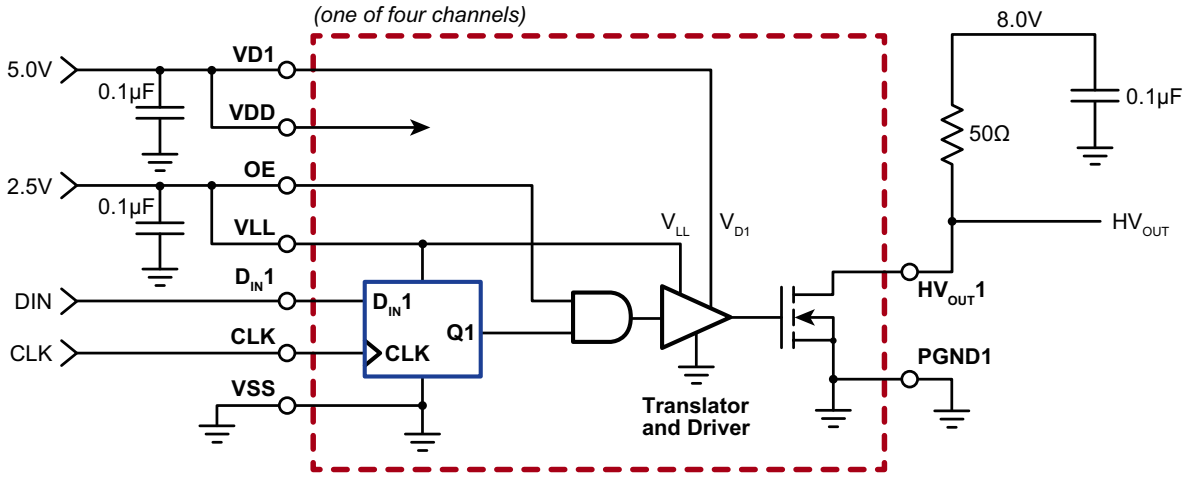


Timing Diagram

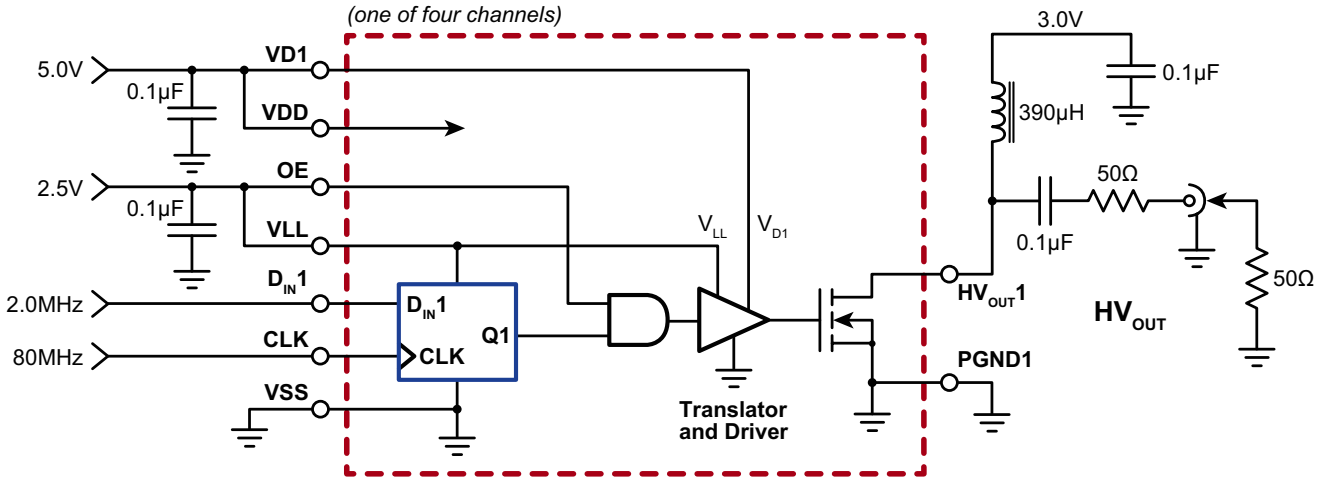


Test Circuits

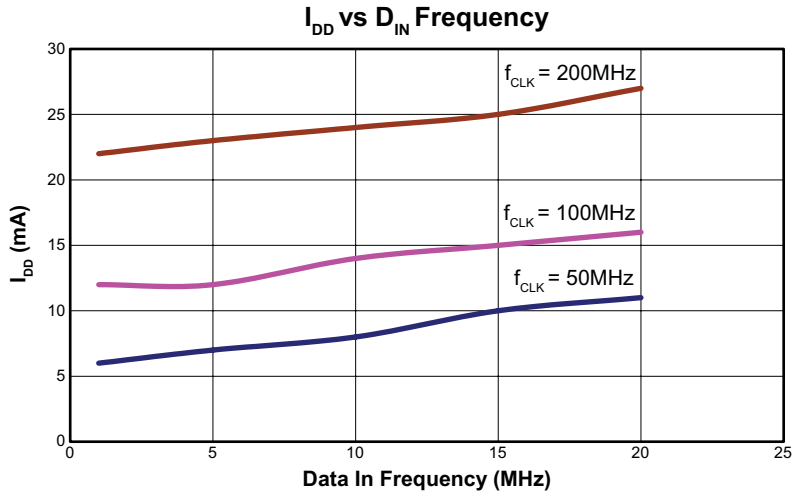
AC Timing



Phase Noise



Typical Performance Curve *(Test conditions: V_{LL} = 2.5V, V_{DD} = 5.0V, V_{D1} = V_{D2} = V_{D3} = V_{D4} = 5.0V, no load)*

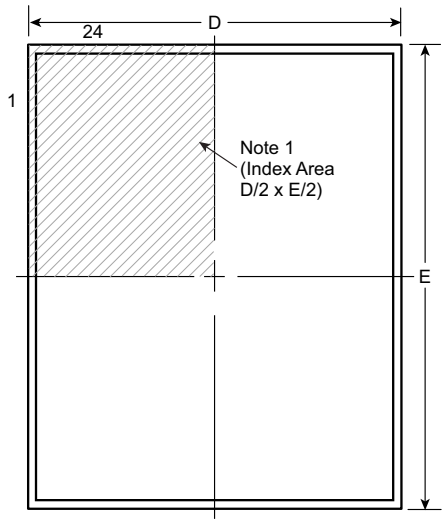


Pin Configuration and Description

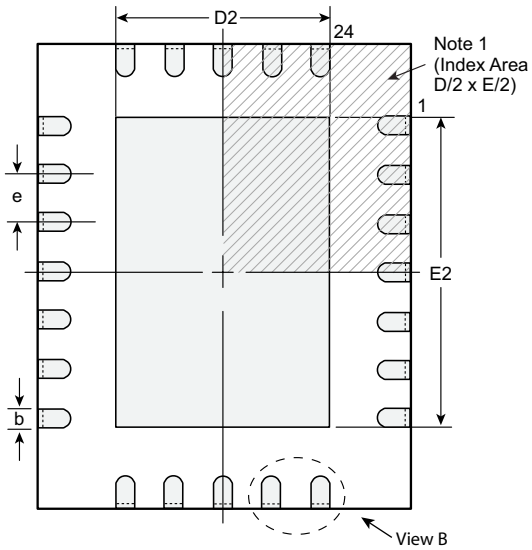
Pin #	Function	Description
1	$D_{IN}1$	D flip-flop logic input for $HV_{OUT}1$. Logic high will turn on output N-channel.
2	$D_{IN}2$	D flip-flop logic input for $HV_{OUT}2$. Logic high will turn on output N-channel.
3	VDD	Level translator supply. Should be at the same potential as V_{DX}.
4	CLK	Logic clock input.
5	VSS	Ground. Should be externally shorted to all PGND and VSS pins.
6	$D_{IN}3$	D flip-flop logic input for $HV_{OUT}3$. Logic high will turn on output N-channel.
7	$D_{IN}4$	D flip-flop logic input for $HV_{OUT}4$. Logic high will turn on output N-channel.
8	VLL	Logic input supply voltage.
9	VSS	Ground. Should be externally shorted to all PGND and VSS pins.
10	VD4	Gate drive supply voltage for $HV_{OUT}4$. Should be at the same potential as V_{DD}.
11	VD3	Gate drive supply voltage for $HV_{OUT}3$. Should be at the same potential as V_{DD}.
12	PGND4	Power ground for $HV_{OUT}4$. Should be externally shorted to all PGND and VSS pins.
13	$HV_{OUT}4$	Drain output for $HV_{OUT}4$.
14	PGND3	Power ground for $HV_{OUT}3$. Should be externally shorted to all PGND and VSS pins.
15	$HV_{OUT}3$	Drain output for $HV_{OUT}3$.
16	VSS	Ground. Should be externally shorted to all PGND and VSS pins.
17	$HV_{OUT}2$	Drain output for $HV_{OUT}2$.
18	PGND2	Power ground for $HV_{OUT}2$. Should be externally shorted to all PGND and VSS pins.
19	$HV_{OUT}1$	Drain output for $HV_{OUT}1$.
20	PGND1	Power ground for $HV_{OUT}1$. Should be externally shorted to all PGND and VSS pins.
21	VD2	Gate drive supply voltage for $HV_{OUT}2$. Should be at the same potential as V_{DD}.
22	VD1	Gate drive supply voltage for $HV_{OUT}1$. Should be at the same potential as V_{DD}.
23	VSS	Ground. Should be externally shorted to all PGND and VSS pins.
24	OE	Output enable logic input. Logic low will turn all HV_{OUT} off.
Center Pad	---	Should be externally shorted to all PGND and VSS pins.

24-Lead QFN Package Outline (K6)

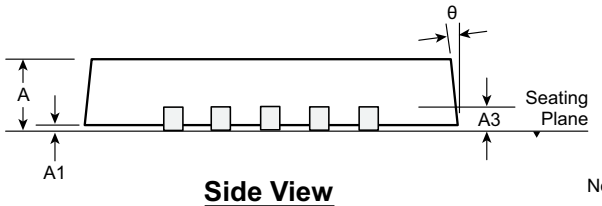
4.00x5.00mm body, 1.00mm height (max), 0.50mm pitch



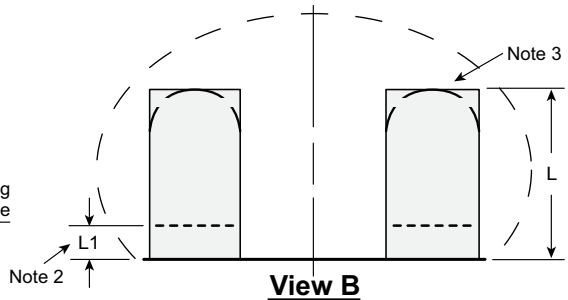
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	3.85*	2.50	4.85*	3.50	0.50 BSC	†0.30	0.00	0°
	NOM	0.90	0.02		0.25	4.00	2.65	5.00	3.65		0.40	-	-
	MAX	1.00	0.05		0.30	4.15*	2.80	5.15*	3.80		†0.50	0.15	14°

JEDEC Registration MO-220, Variation VGHD-1, Issue K, June 2006
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc.#: *DSPD-24QFNK64X5P050, Version A101111.*

(The package drawings in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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