



CW1073

6~7 battery protection IC

Features

• Overcharge detection
 function • Threshold range 3.750V, 4.175V~4.450V, 25mV step, ± 25mV accuracy
 • Overdischarge detection function • Threshold range 2.100V~3.000V, 100mV step, ± 80mV accuracy
 • Overcurrent detection function 1
 Threshold range 0.050V~0.100V, 50mV step, ± 5mV accuracy
 • Overcurrent detection 2
 Threshold range 0.100V~0.200 V, 100mV step, ± 5mV accuracy
 • Short circuit protection threshold range 0.200V~0.500V, 100mV step, ± 10mV accuracy
 • Temperature protection function • Charging high and low temperature protection, temperature can be set externally
 • Discharging high temperature protection, discharging low temperature protection optional
 • Balance function • Achieve 6 through SEL terminal 1-cell, 7-cell battery switch • Disconnection detection function • Load detection function
 PWM control drive • Low operating current
 • Working state 15mA (25°C) • Sleep state 5mA (25°C)
 • Package : SSOP24

Basic Description

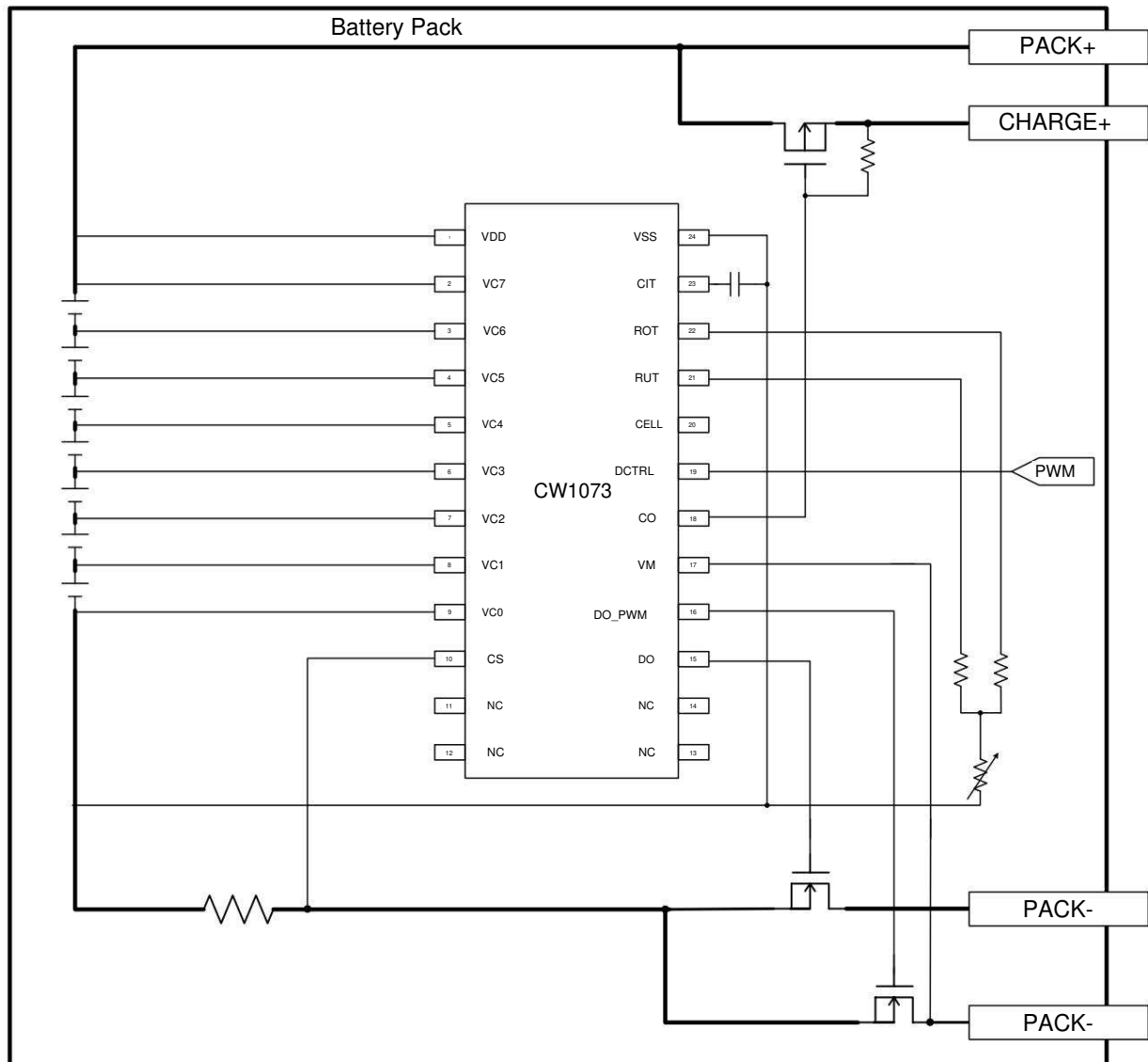
The CW1073 series is a lithium battery protection chip with built-in high-precision detection circuit and delay circuit, suitable for 6-7 series lithium-ion batteries or lithium polymer battery packs. It provides overcharge detection, over-discharge detection, over-current detection, balancing, disconnection detection, and high and low temperature protection for lithium battery packs.

CW1073 has built-in MOSFET driving function and supports external PWM signal to control DO_PWM terminal output through DCTRL terminal to realize motor speed regulation and soft start function.

Application Areas

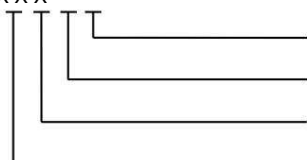
• Power tools
 • Electric bicycles
 • Vacuum cleaners
 • Lithium - ion and lithium -polymer battery packs

Typical application block diagram



Product Selection Guide

CW1073 X X X X



Package type: S: SSOP24

Parameter type: from A to Z

Battery type: A: Lithium-ion battery B: Lithium iron phosphate battery

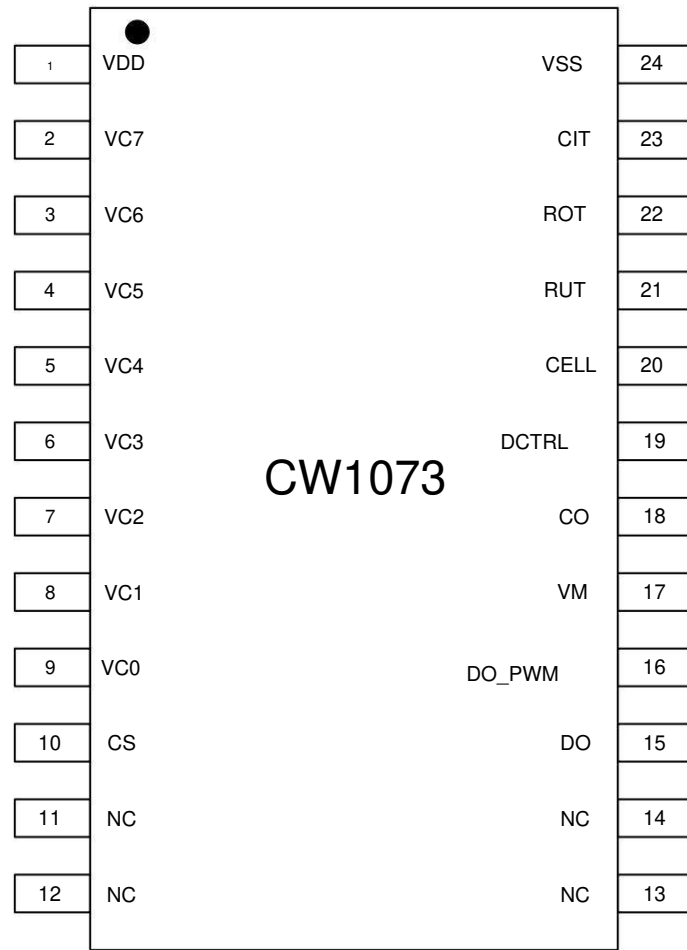
Features and Version Information: From A to Z

Product Catalog

Product Model	Overcharge threshold [VOC]	Overcharge delay [TOC]	Overcharge release [VOCR]	Over discharge threshold [VOD]	Over discharge delay [TOD]	Over discharge release [VODR]
CW1073AAAS	4.250V	1s	4.150V	2.700V	1s	3.000V
CW1073AABS	4.200V	1s	4.100V	2.700V	1s	3.000V
CW1073AACS	4.250V	1s	4.150V	2.500V	1s	3.000V
CW1073AADS	4.200V	1s	4.100V	2.500V	1s	3.000V
CW1073AAES	4.175V	1s	4.075V	2.700V	1s	3.000V
CW1073ABCS	3.750V	1s	3.650V	2.100V	1s	2.400V
CW1073AAFS	4.225V	1s	4.125V	2.700V	1s	3.000V
CW1073AAGS	4.175V	1s	4.075V	2.700V	1s	3.000V
CW1073AAJS	4.200V	1s	4.050V	2.700V	1s	3.000V
CW1073AAKS	4.150V	1s	4.000V	2.700V	1s	3.000V
CW1073AALS	4.200V	1s	4.050V	2.700V	0.3s	3.000V
CW1073AAIS	4.200V	1s	4.100V	2.800V	1s	3.000V

Product Model	Balance start threshold [VBAL]	Overcurrent 1 threshold [VEC1]	Overcurrent 2 threshold [VEC2]	Short circuit threshold [VSHR]	Discharge low Thermal protection	Discharge over temperature recovery Complex load detection
CW1073AAAS	4.125V	0.100V	0.200V	0.500V	N	AND
CW1073AABS	4.075V	0.100V	0.200V	0.500V	N	AND
CW1073AACS	4.125V	0.100V	0.200V	0.500V	N	AND
CW1073AADS	-	0.100V	0.200V	0.400V	N	N
CW1073AAES	4.050V	0.100V	0.200V	0.500V	N	AND
CW1073ABCS	3.625V	0.100V	0.200V	0.500V	N	AND
CW1073AAFS	-	0.100V	0.200V	0.400V	N	N
CW1073AAGS	-	0.100V	0.200V	0.400V	N	N
CW1073AAJS	4.025V	0.100V	0.200V	0.500V	N	AND
CW1073AAKS	-	0.050V	0.100V	0.200V	N	AND
CW1073AALS	4.025V	0.050V	0.100V	0.200V	AND	AND
CW1073AAIS	4.075V	0.100V	0.200V	0.500V	AND	N

Pin Assignment Diagram



Pin Definition

serial number	name	Functional Description
1	VDD	Chip power supply, connected to the highest potential of the battery pack, if there are 7 batteries, then it is the positive terminal of battery 7
2	VC7	Battery 7 positive terminal
3	VC6	Battery 6 positive terminal
4	VC5	Battery 5 positive terminal
5	VC4	Battery 4 positive terminal
6	VC3	Battery 3 positive terminal
7	VC2	Battery 2 positive terminal
8	VC1	Battery 1 positive terminal
9	VC0	Battery 1 Negative terminal
10	CS	Overcurrent detection terminal
11	NC	No connection
12	NC	No connection
13	NC	No connection
14	NC	No connection
15	DO	Discharge protection output terminal, push-pull output, driving NMOS

16	DO_PWM discharge protection	output terminal, push-pull output, driving NMOS
17	VM	P-terminal voltage detection terminal
18	CO	Charging protection output terminal, open drain output, driving PMOS
19	DCTRL	DO_PWN control terminal, PWM signal input
20	CELL	6-cell and 7-cell battery selection terminals
21	RUT	Low temperature detection terminal
22	ROT	Over temperature detection terminal
23	CIT	Overcurrent delay setting terminal
24	VSS	Chip ground terminal, connected to the negative terminal of battery 1

Absolute Maximum Ratings

		scope		unit
		Minimum	Maximum	
Terminal input voltage	VDD _{VM} CO _{SEL} CS _{DCTRL} VSS-0.3		VSS+40	V
Terminal input voltage	ROOT _{CIT}	VSS-0.3	6	V
Terminal input voltage	VCX _{DO_PWM}	VSS-0.3	VDD+0.3	V
Operating temperature	T1	-30	85	°C
Storage temperature	T2	-40	125	°C

Note: Absolute maximum ratings are the ratings that cannot be exceeded under any conditions. If these ratings are exceeded, product damage may occur. hurt.

ESD Level

			Parameter Value	unit
V(ESD) level electrostatic discharge	HBM Mode		±4000	V
	CDM Mode		±1000	V

Rated operating voltage

describe	project	Min	Typ	Max	Unit
VDD Input Voltage	VDD	4		31.5	V
VCX input voltage	VCX	0		4.5	V
Terminal input voltage	VCIT _{WANTED}	0		5	V

Electrical characteristics

Unless otherwise specified, T=25°C

describe	project	Test conditions	Min	Typ	Max	Unit
power supply						
Normal operating current	IOPR	VC1=VC2=VC3=VC4=VC5=VC6=VC7=3.7V		15	20	µA
Sleep current	ISLEEP	VC1=VC2=VC3=VC4=VC5=VC6=VC7=2.0V		5		µA
Channel input current	ICELL	VC1=VC2=VC3=VC4=VC5=VC6=VC7=3.7V		0.5		µA
Voltage, temperature detection and protection thresholds						
Overcharge detection voltage	VOC* 1	VC1=VC2=VC3=VC4=VC5=VC6=3.7V VC7=3.7V±4.5V	VOC - 0.025	VOC	VOC + 0.025	V
Overcharge release voltage	VOCR	VC1=VC2=VC3=VC4=VC5=VC6=3.7V VC7=4.5V±3.7V	VOCR - 0.030	VOCR	VOCR + 0.030	V
Over discharge detection voltage	VOD	VC1=VC2=VC3=VC4=VC5=VC6=3.7V VC7=3.7V±2.0V	VOD- 0.080	VOD	VOD+ 0.080	V
Over discharge release voltage	V.O.D.R.	VC1=VC2=VC3=VC4=VC5=VC6=3.7V VC7=2.0±3.7V	V.O.D.R.- 0.100	V.O.D.R.	VODR + 0.100	V
Balanced starting voltage	VBAL	VC1=VC2=VC3=VC4=VC5=VC6=3.7V VC7=3.7V±4.4V	VBAL- 0.025	VBAL	VBAL+ 0.025	V
Overcurrent 1 detection voltage	VEC1	VC1=VC2=VC3=VC4=VC5=VC6=VC7=3.7V CS=0±0.15V	VEC1- 0.005	VEC1	VEC1+ 0.005	V
Overcurrent 2 detection voltage	VEC2	VC1=VC2=VC3=VC4=VC5=VC6=VC7=3.7V CS=0±0.3V	VEC2- 0.005	VEC2	VEC2+ 0.005	V
Short circuit detection voltage	disabled with mask	VC1=VC2=VC3=VC4=VC5=VC6=VC7=3.7V CS=0±0.6V	VSHR- 0.010	disabled with mask	VSHR + 0.010	V
Charging over-temperature detection temperature	TCOT* 2	VDD=25.9V,NTC=103AT B=3435	TCOT-3	TCOT	TCOT+3	°C
Charging over-temperature protection release delay <small>Hysteresis Temperature</small>	TCOTR			5		°C
Discharge over-temperature detection temperature	TDOT* 2	VDD=25.9V,NTC=103AT B=3435	TDOT-3	TDOT	TDOT+3	°C
Discharge over-temperature protection release delay <small>Hysteresis Temperature</small>	TDOTR			5		°C
Charging low temperature detection temperature	TCUT	VDD=25.9V,NTC=103AT B=3435	TCUT-3	TCUT	TCUT+3	°C
Charging low temperature protection release delay <small>Hysteresis Temperature</small>	TCUTR			5		°C
Discharge low temperature detection temperature	TDUT	VDD=25.9V,NTC=103AT B=3435	TDUT-3	TDUT	TDUT+3	°C
Discharge low temperature protection release delay <small>Hysteresis Temperature</small>	TDUTR			5		°C
DCTRL terminal high level input Input voltage	VCTRLH		2.5			V
DCTRL terminal low level input Input voltage	VCTRLLL					V
Discharge state judgment voltage	VDCH		2	3.5	5	mV
Wire break judgment voltage	VOW		20	50	100	mV

describe	project	Test conditions	Min	Typ	Max	Unit	
Load detection voltage	VLD					2	V
Delay time							
Overcharge protection delay	TOC	VC1=VC2=VC3=VC4=VC5=VC6=3.7V VC7=3.7V \ddot{y} 4.5V	0.8*			TOC	1.2* TOC s
Overcharge protection reset delay TRESET			1	2.5	4		ms
Overcharge protection release delay	TOCR	VC1=VC2=VC3=VC4=VC5=VC6=3.7V VC7=4.5V \ddot{y} 3.7V	150	200	250		ms
Over discharge protection delay	TOD	VC1=VC2=VC3=VC4=VC5=VC6=3.7V VC7=3.7V \ddot{y} 2.0V	0.7*			TOD	1.3* TOD s
Over discharge protection release delay	TODR	VC1=VC2=VC3=VC4=VC5=VC6=3.7V VC7=2.0V \ddot{y} 3.7V	150	200	360		ms
Balanced start delay	TBAL	VC1=VC2=VC3=VC4=VC5=VC6=3.7V VC7=3.7V \ddot{y} 4.5V			64		ms
Balanced off delay					64		ms
Overcurrent 1 protection delay	TEC1	CIT connects to a 0.1 \ddot{y} F capacitor	0.7	1	1.3		s
Overcurrent 2 protection delay	TEC2	CIT connects to a 0.1 \ddot{y} F capacitor	60	100	140		ms
Short circuit protection	TSHORT		180	240	300		\ddot{y} s
delay Overcurrent release delay	TECR* 3		90	120	150		ms
Load lock state release delay TLLR		VC1=VC2=VC3=VC4=VC5=VC6=VC7=3.7V VM \ddot{y} VLD	5	10	16		ms
Sleep delay	TSLP		25	30	40		s
charging over temperature protection delay	TCOT		0.8	1.5	2		s
Charging over-temperature protection release delay	TCOTR		0.8	1.5	2		s
hour							
Discharge over-temperature protection delay	TDOT		0.8	1.5	2		s
Discharge over-temperature protection release delay	TDOTR		0.8	1.5	2		s
hour							
Charging low temperature protection delay	TCUT		0.8	1.5	2		s
Charging low temperature protection release delay	TCUTR		0.8	1.5	2		s
hour							
Discharge low temperature protection delay	TDUT		0.8	1.5	2		s
Discharge low temperature protection release delay	TDUTR		0.8	1.5	2		s
hour							
Disconnection detection delay	TOW input capacitance = 0.1 \ddot{y} F			1			s
Disconnection recovery delay	TOWR			6			s
Discharge state detection delay TDCH			3	5	10		ms
0V charging function							
0V charging start voltage	V0V		1.5				V
VM terminal							
Resistance between VM and VSS RVM/VSS			30	50	80		k \ddot{y}

describe	project	Test conditions	Min	Typ	Max	Unit	
Pin output voltage							
CO logic low output Voltage	CO*4					VSS	V
DO logic high output Voltage	DO	VDD>=11V				10.6	V
DO logic high output Voltage		VDD<11V				VDD - 0.7	V
DO logic low output Voltage						VSS	V
DO_PWM logic high Flat output voltage	DO_ PWM	VDD>=11V				10.6	V
DO_PWM logic high Flat output voltage		VDD<11V				VDD - 0.7	V
DO_PWM logic low Flat output voltage						VSS	V
Drive current* 5							
CO terminal output current	CO	CO terminal logic high level				-	ȳA
		CO terminal logic low level				10	ȳA
DO terminal output current	DO	DO terminal logic high level				70	ȳA
		DO terminal logic low level				-680	ȳA
DO_PWM terminal							
DO_PWM Pull-up resistor DO_	PWM	DO_PWM terminal logic high level				3.7	kȳ
DO_PWM pull-down resistor *1		DO_PWM terminal logic low level				700	Oh

For detailed protection threshold selection, please refer to the selection guide table

*2 The charging over-temperature protection temperature depends on the setting of different resistors. The discharge over-temperature protection temperature defaults to the charging over-temperature protection temperature + 20°C, that is, the charging over-temperature protection temperature

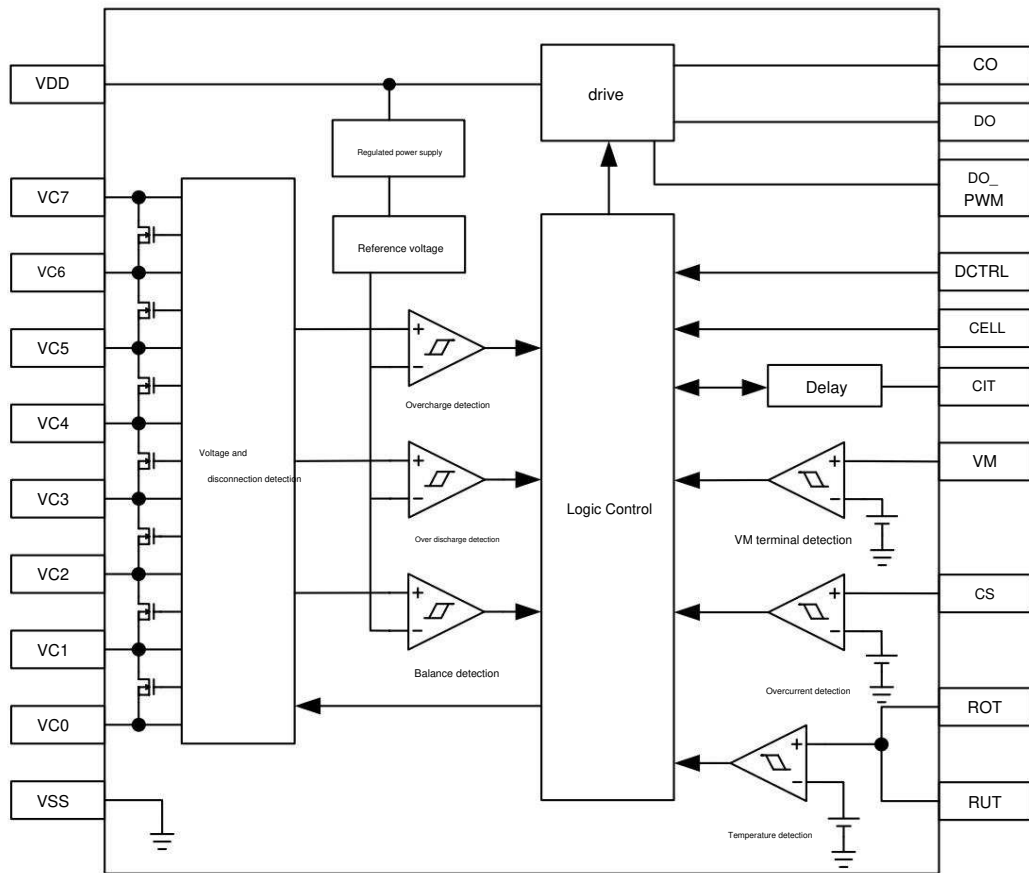
If the over-temperature protection temperature is 50ȳ, the over-temperature protection temperature for discharge is 70ȳ; the low-temperature protection temperature setting for charge and discharge is consistent with the high-temperature setting for charge and discharge;

*3 All over-current protection (including over-current 1, over-current 2 and short-circuit protection) release delay time is 120ms

*4 The output high level of the CO terminal is high impedance state.

*5 The external voltage source for the CO and DO terminal output current test is 0.5V

Block Diagram



Functional Description

Normal state

All battery voltages are between the overcharge detection voltage (VOC) and the overdischarge detection voltage (VOD), the battery temperature is within the operating range, and CS

When the terminal voltage is lower than the overcurrent detection voltage (VEC1), CW1073 is in normal working state. Overcharge state

Under normal conditions, if the voltage of any battery cell is higher than the overcharge detection voltage (VOC) and exceeds the overcharge protection delay time (TOC), CO

The terminal outputs a high impedance state to turn off the charging MOSFET and stop charging.

During the overcharge protection delay time (TOC), if the detected battery voltage is lower than the overcharge detection voltage (VOC) for a period longer than the overcharge reset delay time (TRESET), the accumulated overcharge delay time (TOC) is reset. Otherwise, the drop in battery voltage is considered as irrelevant interference and is shielded.

Overcharge protection release condition:

All battery voltages are lower than the overcharge release voltage (VOCR) and exceed the overcharge release delay time (TOCR).

Over discharge state

Under normal conditions, if the voltage of any battery is lower than the over-discharge protection voltage (VOD) and exceeds the over-discharge protection delay time (TOD), the DO terminal

The DO_PWM terminal outputs a low level to turn off the discharge MOSFET and stop discharging. Over-discharge protection

release conditions: VM terminal voltage is

lower than 2V (load release), all battery voltages are higher than the over-discharge release voltage (VODR) and maintain for more than the over-discharge release delay time.

Time (TODR).

Overcurrent status

CW1073 has three levels of built-in overcurrent detection, overcurrent 1, overcurrent 2 and short circuit protection.

Protection mechanism: The voltage of the current sampling resistor on the main circuit is detected through the CS terminal to determine whether CW1073 enters the corresponding overcurrent protection state.

Taking

overcurrent 1 protection as an example, the discharge current changes with the external load. If the CS terminal detects that the voltage on the current sampling resistor is higher than the overcurrent 1 protection threshold (VEC1) and maintains more than the overcurrent 1 protection delay time (TEC1), the DO terminal and DO_PWM terminal output low level to turn off the discharge MOSFET and stop discharging. Overcurrent

protection release condition: The VM terminal

voltage is lower than 2V (load release) and

exceeds the overcurrent release delay time (TECR), and the overcurrent protection is released.

Temperature protection function

CW1073 uses an NTC resistor to achieve charge and discharge over-temperature protection and charge and discharge low-temperature protection functions. The ROT and RUT terminals detect the NTC resistor voltage. If the detection voltage reaches the internal comparison threshold and maintains the charge and discharge temperature protection delay time, the temperature protection function is triggered.

After the charging temperature protection, the charging MOSFET is turned off and charging stops; After

the discharging temperature protection, the discharging MOSFET is turned off and discharging stops;

Charging temperature protection release

condition: The temperature returns to within the charging release temperature, and the time exceeds the charging temperature release delay, the charging temperature

protection is released. Discharging temperature

protection release condition: 1. The chip has a temperature protection recovery load lock function: The VM terminal voltage is lower than 2V (load release), the temperature returns to within the discharge release

temperature, and the time exceeds the discharge temperature release delay, the discharge temperature protection is

released. 2. The chip does not have a temperature protection recovery load lock function: The temperature returns to within the discharge release temperature, and the time exceeds the discharge temperature release delay.

When the discharge temperature protection is

released. Over-temperature threshold

setting steps 1. Select the NTC resistor. The recommended NTC resistor model for CW1073 is: 103AT, B=3435;

2. Determine the charge over-temperature protection threshold, such as 50°C; 3. According to the temperature curve of the NTC resistor, find the resistance value corresponding to 50°C, such as 3.5k Ω ; 4. Use a normal resistor with 10 times the resistance to connect to the ROT terminal, that is, 35k Ω ; 5. After determining the charge over-temperature protection threshold, the discharge over-temperature protection threshold defaults to 50°C+20°C = 70°C; 6. The charge low-temperature protection setting uses the same method, but the resistor needs to be connected to the RUT terminal; 7. Please refer to the application circuit for detailed circuits, and set the appropriate protection temperature by selecting resistors;

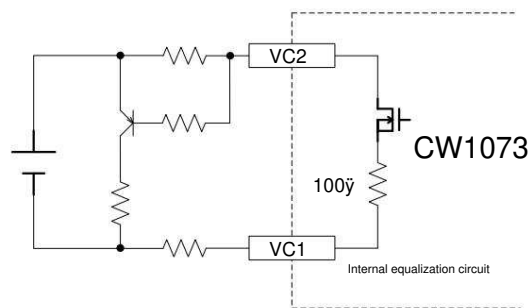
CW1073 has an optional discharge low temperature protection function. The default discharge low temperature protection temperature setting is the charge low temperature protection temperature of -20 \circ C.

Low power state

CW1073 enters the over-discharge protection state and exceeds the sleep delay time (TSLP), then CW1073 enters the low power state. DO terminal Keep low level to keep the discharge MOSFET off; keep CO terminal low level to keep the charge MOSFET on. Sleep state release condition: the battery voltage is higher than the over-discharge release voltage (VODR) and lasts longer than the over-discharge release delay time (TODR).

Equalization function

CW1073 has built-in balancing function, internal balancing resistor is 100 μ Ω , and balancing current is adjusted by external voltage sampling resistor. The sample resistance is 200 Ω -1k Ω . If large current balancing is required, an external balancing circuit can be added to expand the current. The balancing current is determined by the external balancing resistor.

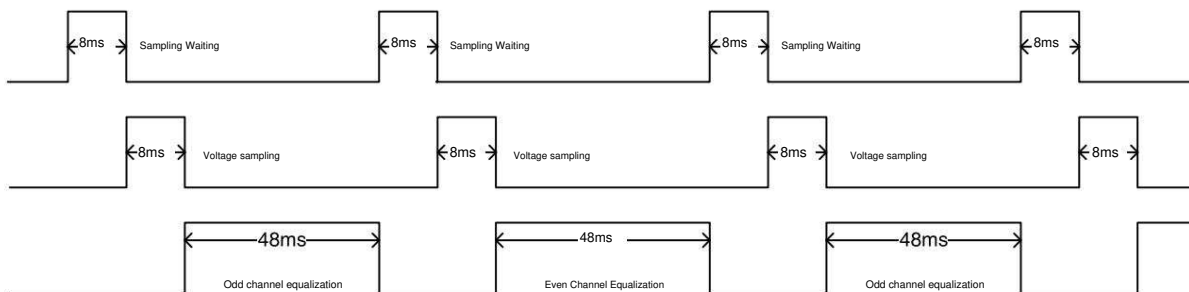


Equalization function diagram

Under normal conditions, if the voltage of any cell is higher than the balancing detection voltage (VBAL) and the voltage of the other cells is lower than the balancing detection voltage (VBAL), and the balancing start delay time (TBAL) is exceeded, CW1073 starts balancing. Balancing stop conditions: 1.

1. All cell voltages are lower than the balancing detection voltage (VBAL).
2. All cell voltages are higher than the balancing detection voltage (VBAL).
3. CW1073 enters the disconnection protection state, discharge temperature protection state, and low power consumption state.

CW1073 uses odd-even channel time-sharing balancing. The balancing function does not affect the normal battery voltage sampling. When multiple balancing channels are turned on at the same time, the odd channels will enter the balancing state first, and the even channels will enter the balancing state in the next cycle. The specific battery voltage sampling and balancing start timing diagram is as follows:



Voltage sampling and balancing start timing diagram

Line break protection function

CW1073 includes disconnection detection and protection functions.

Under normal conditions, when the detection line of any battery in the battery pack is disconnected and maintained for more than the disconnection detection delay (TOW), the DO terminal and DO_PWM terminal output low level to turn off the discharge MOSFET; CO output high impedance to turn off the charging MOSFET; CW1073 enters the disconnection protection state. Conditions for releasing the

disconnection protection state: VM terminal

voltage is lower than 2V (load release), the detection line is reconnected, and maintained for more than the disconnection release delay (TOWR), the disconnection protection state is released.

0V charging (allowed)

CW1073 supports the battery 0V charging function, that is, when the battery voltage is lower than the normal operating voltage of the chip, the battery pack can be charged normally.

The VDD voltage of CW1073 is higher than the 0V charging start voltage (VOV), a charger is connected and the charger output voltage is higher than the charging MOSFET

The battery pack starts charging after the threshold

is turned on. Delay time setting

The delay time refers to the time from when CW1073 detects that the voltage reaches the set protection threshold to when CW1073 drives the CO or DO terminal to output high or low.

Level time.

The overcurrent 1 and overcurrent 2 protections of CW1073 can be set with external capacitors to set the delay time.

String number selection

The SEL terminal is the battery series number selection terminal, which can be used to select the number of batteries connected in series.

If the SEL terminal is connected to the ground with a resistor in series, the number of battery strings protected by CW1073 is 6. When 6 battery strings are used, the VC7 terminal and the VC6 terminal are shorted.

catch;

If the SEL terminal is left unconnected, the number of battery strings protected by CW1073 is 7;

Discharge status detection function

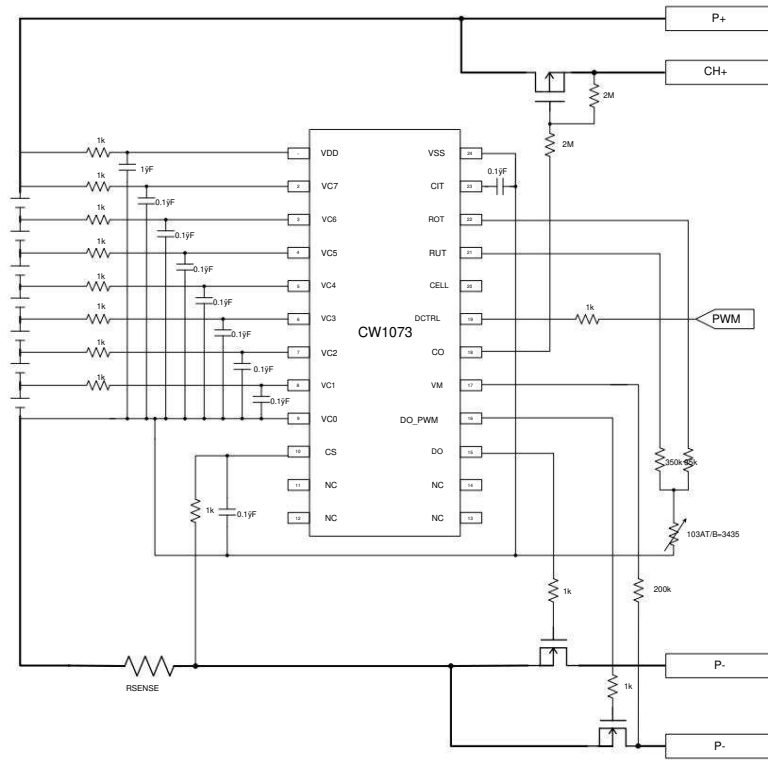
In the application of charging and discharging at the same port, the battery pack is in the overcharge and charging temperature protection state. If the CS terminal detection voltage is higher than 3.5mV and the discharge state detection delay (TDCH) continues, the battery pack is considered to be in the discharge state, and the CO terminal outputs a low level to turn on the charging MOSFET.

PWM control drive

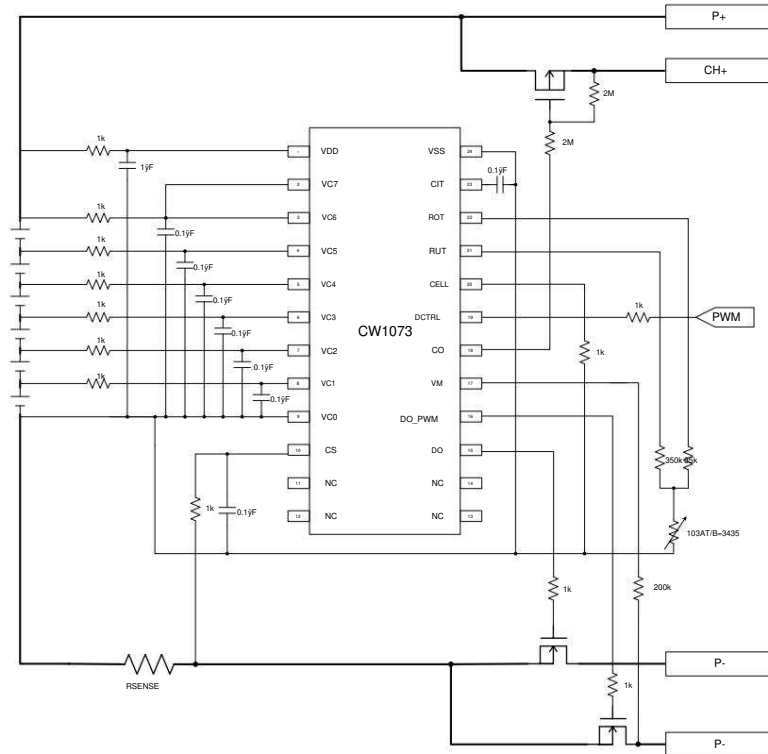
CW1073 has built-in MOS drive function, supports external PWM signal to control DO_PWM terminal output through DCTRL terminal, DCTRL terminal input voltage is higher than 2.5V, DO_PWM terminal outputs low level; DCTRL terminal input voltage is lower than 1V, DO_PWM terminal outputs high level. When external signal is not needed to control DO_PWM terminal, DCTRL terminal series resistor is grounded;

When the internal protection state of the CW1073 chip occurs, such as over-discharge, over-current, discharge over-temperature and disconnection protection, the chip protection action will be executed first.

Reference Application Circuit



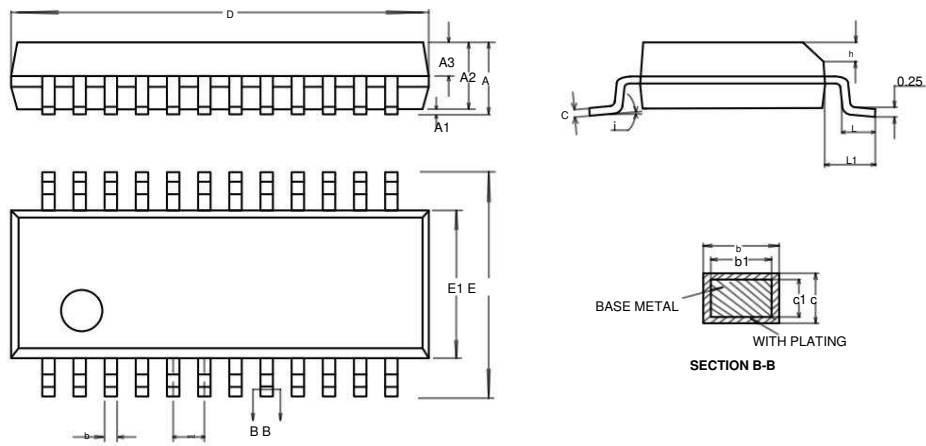
7-string application circuit without equalization function



6-string application circuit without equalization function

Package Drawing and Package Dimensions

SSOP24 package



SYMBOL	MILLIMETER		
	MIN.	NAME.	MAX.
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
Δ	5.80	6.00	6.20
E1	3.80	3.90	4.00
Δ	0.635BSC		
h	0.30	—	0.50
L	0.50	—	0.80
L1	1.05REF		
γ	0	—	8°

Version History

Date	Version	Modify Project	Modify	approve
2017-08-25	1.0	New version of the manual released	Zeng	Zhou Jun
2018-01-25	1.1	Added CW1073AACS model	Kang	Zhou Jun
2018-06-29	1.2	Added CW1073AADS model	Zeng Kang Zeng Kang	Zhou Jun
2018-08-14	1.3	1. Added CW1073AAES model 2. Modify CW1073AADS parameters 3. Modify the discharge over-temperature recovery condition and the description of the balancing function 4. Added ESD level description	Zeng Kang	Zhou Jun
2018-11-26	1.4	1. Modify the reference application circuit 2. Increase the upper and lower limits of parameters 3. Add PWM control instructions	Zeng Kang	Zhou Jun
2019-01-14	1.5	Added CW1073AAFS, CW1073AAGS models	Zeng Kang	Zhou Jun
2019-06-18	1.6	1. Added CW1073AAJS, AAKS, AAIS product models 2. Adjust the over-discharge delay accuracy	Zeng Kang	Zhou Jun

statement

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The details are as follows:

1. Life support devices or systems are devices or systems that

System: (a) intended for surgical implantation in the human body, or (b) sustain or maintain life, and even if used according to the instructions Follow the instructions to perform the correct operation, but if the operation fails, Will cause serious harm to the user.

2. Critical components refer to those components in life support equipment or systems.

Failure of this device can lead to the failure of the entire life support device or system failure, or affect its safety and use Effect.