SONY

CX20185

Read/Write Amplifier for Floppy Disk Drive

Functions:
CX20185 is an integrated circuit designed for Read/Write of Floppy Disk Drive (FDD)
This IC offers the following features.

1. Including Head Sw Matrix for selecting Read/Write.
2. The voltage gain of Pre-Amplifier can be selected to 100 or 200 by connecting the external capacitor.
3. Peak Shift is less than 1% over Pre-Amplifier input range of 0.25 $mV_{p\text{-}p}$ to 10 $mV_{p\text{-}p}$ without adjustment.
4. Time Domain Filter contains retriggerable monostable multivibrator which has internal timing capacitor allowing to be used only external resistor.
5. Common, Write, and Erase drivers have large current capacities to satisfy versatile FDD's conditions.
6. Write current can be determined by external resistors and is virtually independent against a change of temperature and power supply voltage.
7. Write current may be selected to two different values by Digital input signal, if Write current compensation is required on inner tracks of the disk.
8. WRITE GATE and ERASE GATE input timings can be set independently.
9. Power Monitor circuit with Schmitt-Trigger function inhibits illegal writing against power supply voltage fluctuation including power ON/OFF transients.
10. The number of external components is greatly reduced by this one-chip Read/Write IC.

Absolute Maximum Ratings (Ta = 25°C)

• Power Supply Voltage V_{CC2}	17V
• Power Supply Voltage V_{CC1}	7V
• Digital Signal Inputs (NOTE 1) Input Voltage	−0.5 ~ +5.5V
• POWER ON OUTPUT Voltage Applied	15V
• ERASE OUTPUT Voltage Applied	20V
• COMMON ϕ, COMMON 1, SOURCE Currents	150mA
• POWER ON OUTPUT SINK Current	20mA
• ERASE OUTPUT SINK Current	150mA
• HEAD ϕA and ϕB, HEAD 1A and 1B, Voltage Applied	23V
• Operating Ambient Temperature	T_{opr} −20 ~ +75°C
• Operating Junction Temperature	T_j +150°C
• Storage Temperature	Tst_g −65 ~ +150°C

NOTE 1: These inputs are WRITE CURRENT, WRITE DATA, WRITE GATE, ERASE GATE, SIDE 1, and MMVA CONTROL

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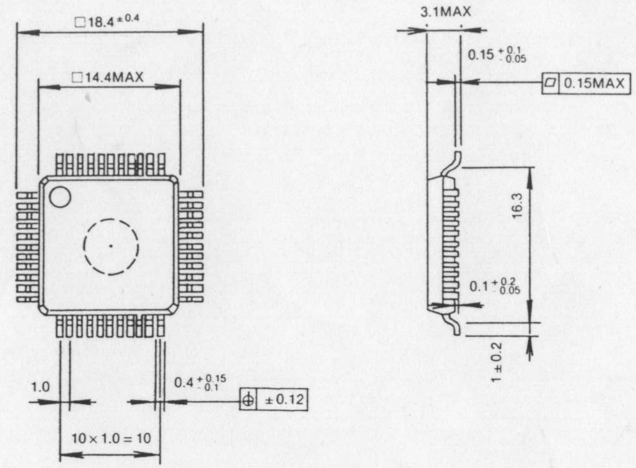
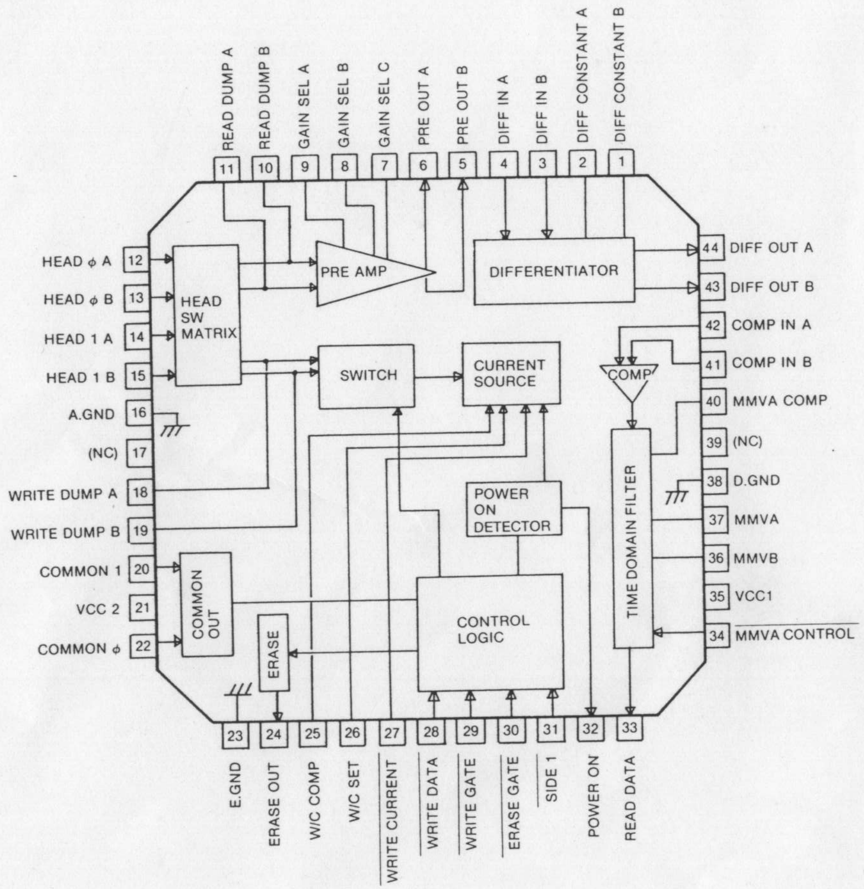


Package Outline (unit: mm)

Block Diagram



Terminal Description

Terminal	Function
HEADϕ A HEADϕ B	Input and output terminals for Read/Write head on Side ϕ
COMMONϕ	Connect the center tap of Read/Write head on Side ϕ
HEAD1 A HEAD1 B	Input and output terminals for Read/Write head on Side 1
COMMON1	Connect the center tap of Read/Write head on Side 1
READ DUMP A READ DUMP B	Connect the head dumping resistor for Read.
GAIN SEL A.B.C	The voltage gain of Pre-Amplifier can be set to 100 or 200 by connecting a capacitor between these pins.
PRE OUT A PRE OUT B	Pre-Amplifier output
DIFF IN A DIFF IN B	Differentiator input
DIFF CONSTANT A DIFF CONSTANT B	Connect external components to set the differential constant.
DIFF OUT A DIFF OUT B	Differentiator output
COMP IN A COMP IN B	Comparator input
MMVA COMP	Connect a resistor for the pulse width compensation of Time Domain Filter's mono-multi.
D. GND	Digital circuit Ground
MMVA	Connect a resistor to determine the pulse width of Time Domain Filter's mono-multi.
MMVB	Connect a resistor to determine the pulse width of Read Data output.
VCC1	5V Power supply terminal
MMVA CONT	Digital input pin. When MMVA CONT is set to "L", the pulse width of Time Domain Filter's mono-multi is decreased.
READ DATA	Read Data output (Totem-Pole output)
POWER ON	Open Collector output. When Power Monitor circuit detects the power supply voltage drop, POWER ON output is ON.
SIDE 1	Digital input pin. When SIDE 1 is set to "L", Read/Write head on Side 1 becomes Active.
ERASE GATE	Digital input pin. When ERASE GATE is set to "L", Erase circuit becomes Active, causing Erase current to be ON.
WRITE GATE	Digital input pin. When WRITE GATE is set to "L", Write circuit block becomes Active, causing Write current to be ON.
WRITE DATA	Digital input pin with Schmitt-Trigged function. When WRITE DATA is set from "H" to "L", Write current is switched.
WRITE CURRENT	Digital input pin. When WRITE CURRENT is set to "L", Write current is increased.
W/C SET	Connect a resistor to determine Write current.
W/C COMP	Connect a resistor for Write current compensation.
ERASE OUT	Open Collector Erase current output.
E. GND	Erase circuit Ground
WRITE DUMP A WRITE DUMP B	Connect the head dumping resistor for Write.
VCC2	12V Power supply terminal
A. GND	Analog circuit Ground

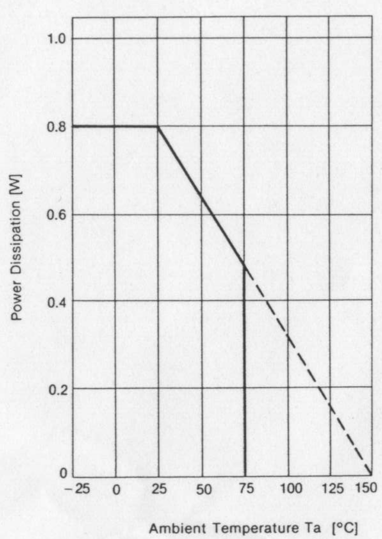
Electrical Characteristics

(V_{CC1} = 5V, V_{CC2} = 12V, T_a = 25°C unless specified)

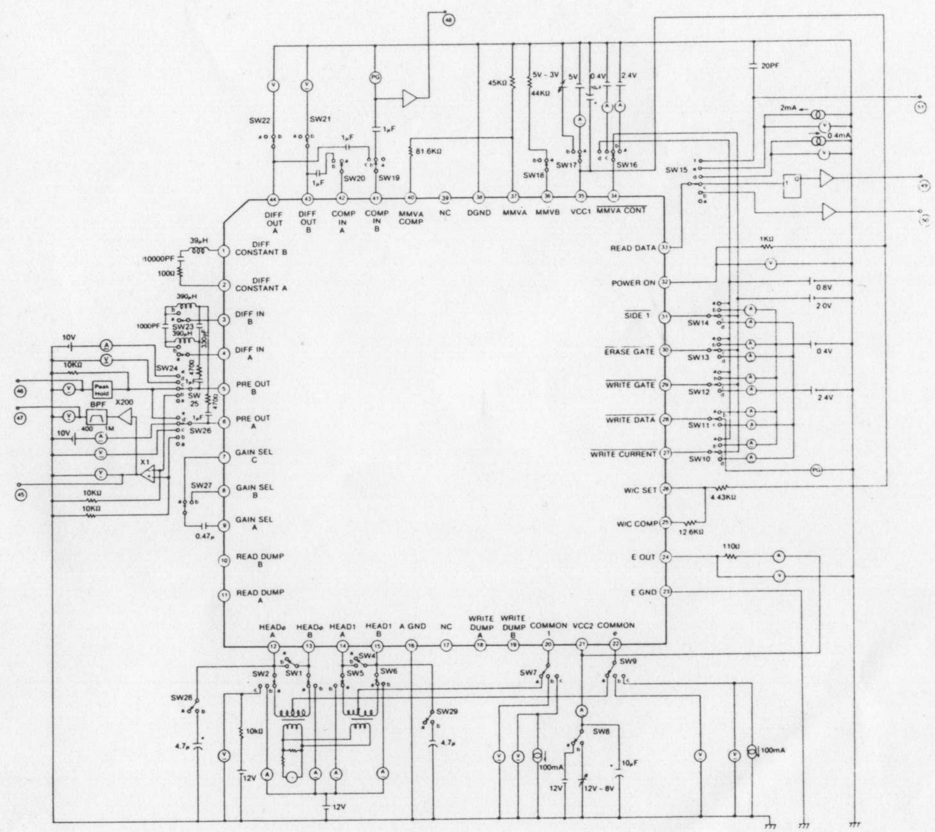
Characteristic	Symbol	Min	Typ	Max	Unit
Head Input Terminal Leakage Current (Write)	I LKM	—	—	10.0	μA
Head Selector/Pre-Amplifier Voltage Gain Accuracy	EGV	– 15.0	—	+ 15.0	%
Head Selector/Pre-Amplifier High Frequency Gain Attenuation (f = 5MHz)	BW	—	—	3.0	dB
Pre-Amplifier Differential Output Offset Voltage	V OFS	—	—	0.5	V
Pre-Amplifier Output Voltage Swing	V OUT	3.7	4.2	—	V P-P
Pre-Amplifier Differential Output Current Swing	I OUT	3.0	4.0	—	mA P-P
Pre-Amplifier Input Equivalent Noise Voltage (Pre-Amp Gain. ×200, f = 400Hz to 1MHz)	EN	—	4.5	5.5	μV
Differentiator Differential Output Offset Voltage	V OFD	—	—	10.0	mV
Pulse Width Accuracy of Time Domain Filter's Mono-Multi	ETM1	– 10.0	—	+ 10.0	%
Pulse Width Accuracy of Read Data Output	ETM2	– 15.0	—	+ 15.0	%
Pulse Width Compensation Accuracy of Time Domain Filter's Mono-Multi	ETM1C	– 15.0	—	+ 15.0	%
Peak Shift (Vin = 0.25 ~ 10 $mV_{p\text{-}p}$)	PS	—	—	1.0	%
Write Current Accuracy	EW	– 7.0	—	+ 7.0	%
Write Current Imbalance	DW	—	—	1.0	%
Write Current Compensation Accuracy	EWC	– 10.0	—	+ 10.0	%
Head Input Terminal Saturation Voltage (Write)	V SAT	—	—	3.6	V
Common Voltage "L" (Write)	V WLCM	—	—	0.1	V
Common Voltage "H" (Write)	V WHCM	10.5	—	—	V
Common Voltage "H" (Read)	V RHCM	4.8	—	5.4	V
Erase Current Output Saturation Voltage	VIR	—	—	0.5	V
Erase Current Output Leakage Current	I LKIR	—	—	15.0	μA
Low-Level Input Voltage	V LIN	—	—	0.8	V
High-Level Input Voltage	V HIN	2.0	—	—	V
Low-Level Input Voltage (Terminal 28) (Schmitt Trigger Input)	V LINS	—	—	0.8	V
High-Level Input Voltage (Terminal 28) (Schmitt Trigger Input)	V'HINS	2.0	—	—	V
Low-level Input Current	I LIN	—	—	250.0	μA

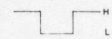
Characteristic	Symbol	Min	Typ	Max	Unit
High-Level Input Current (Terminals 28, 29, 30, and 31)	I HIN1	—	—	10.0	μA
High-Level Input Current (Terminal 27)	I HIN2	—	—	130.0	μA
High-Level Input Current (Terminal 34)	I HIN3	—	—	60.0	μA
Power ON/OFF Detector V_{CC1} Threshold Voltage	V TH5	3.6	4.0	4.4	V
Power ON/OFF Detector V_{CC2} Threshold Voltage	V TH12	8.2	9.2	10.0	V
Read Data Output Low-Level Output Voltage (I_{OL} = 2 mA)	V LOUT	—	—	0.5	V
Read Data Output High-Level Output Voltage (I_{OH} = – 0.4 mA)	V HOUT	2.8	—	—	V
Read Data Output Rise Time	TR	—	—	100.0	nS
Read Data Output Fall Time	TF	—	—	100.0	nS
V_{CC1} Supply Current (Read)	I CC1R	16.0	22.0	28.0	mA
V_{CC1} Supply Current (Write)	I CC1W	7.0	12.5	16.5	mA
V_{CC2} Supply Current (Read)	I CC2R	7.0	10.0	14.0	mA
V_{CC2} Supply Current (Write)	I CC2W	9.0	12.5	16.0	mA

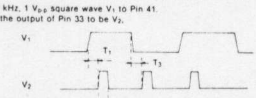
Derating Curve



Electrical Characteristic Measuring Circuit



Measurement No.	Measurement Item	Symbol	SW Condition																													Measuring Point	Description of Measurement	Limit			
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29			Min.	Typ.	Max.	Unit
1	Head Input Terminal Leakage Current (Write)	I_{LKM}	a	b	b	a	a	a	a	a	a	c	b	c ↓ a	c	c	a	b	a	a	a	a	a	a	a	a	a	a	a	a	a		Assuming the current to Pin 12 to be I_1, and the current to Pin 12 after applying the following pulse once to Pin 28 to be I_1'. Smaller of I_1 and I_1' is designated I_{LKM1}. Similarly, I_{LKM2} through I_{LKM4} are obtained for Pins 13 through 15.	—	—	10	μA
1-1	Head Input Terminal Leakage Current (12 pin)	I_{LKM1}																														12					
1-2	Head Input Terminal Leakage Current (13 pin)	I_{LKM2}		↓	↓		↓	↓						↓		↓																13					〃
1-3	Head Input Terminal Leakage Current (14 pin)	I_{LKM3}		a	a		b	b						c ↓ a		a																14	Applied Pulse 				
1-4	Head Input Terminal Leakage Current (15 pin)	I_{LKM4}					↓	↓					↓	↓		↓											↓	↓	↓			15					
2	Head Selector/Pre-Amplifier Voltage Gain Accuracy	EGV					a	a					c	c		c											b	b	b				Input a 100 kHz, 10 mV_{rms} sine wave between Pins 12 and 13 and between Pins 14 and 15. Assuming the AC voltage between Pins 5 and 6 to be V_0 [V_{rms}], gains will be $G = \frac{V_0}{0.01}$ EGV1, EGV2: $(1 - \frac{G}{100}) \times 100$ EGV3, EGV4: $(1 - \frac{G}{200}) \times 100$	-15	—	15	%
2-1	Head Selector/Pre-Amplifier Voltage Gain Accuracy (X100 HEAD 0)	EGV_1														↓																45					
2-2	Head Selector/Pre-Amplifier Voltage Gain Accuracy (X100 HEAD 1)	EGV_2														a													↓			45					
2-3	Head Selector/Pre-Amplifier Voltage Gain Accuracy (X200 HEAD 0)	EGV_3														c													a			45					
2-4	Head Selector/Pre-Amplifier Voltage Gain Accuracy (X200 HEAD 1)	EGV_4														a																45					
3	Head Selector/Pre-Amplifier High Frequency Gain Attenuation (f = 5MHz)	BW														c																	Input a 250 kHz, 10 mV_{rms} sine wave between Pins 12 and 13 and between Pins 14 and 15, and assume the AC voltage at Pin 5 to V_{01} [V_{rms}]. Assuming the measured voltage value when the frequency was adjusted to 5 MHz to be V_{02} [V_{rms}]. $BW = \lvert 20 \log \frac{V_{02}}{V_{01}} \rvert$	—	—	3	dB
3-1	Head Selector/Pre-Amplifier High Frequency Gain Attenuation (HEAD 0)	BW_1														↓																45					
3-2	Head Selector/Pre-Amplifier High Frequency Gain Attenuation (HEAD 1)	BW_2														a																45					
			↓			↓										↓											↓	↓									
4	Pre-Amplifier Differential Output Offset Voltage	V_{OFS}	b			b										c											d	c					Assuming the voltage at Pin 5 to be V_1 and the voltage at Pin 6 to be V_2. $V_{OFS} = \lvert V_1 - V_2 \rvert$	—	—	0.5	V
4-1	Pre-Amplifier Differential Output Offset Voltage (HEAD 0)																															5					
4-2	Pre-Amplifier Differential Output Offset Voltage (HEAD 0)	V_{OFS1}														↓																6					
4-3	Pre-Amplifier Differential Output Offset Voltage (HEAD 1)															a																5					
4-4	Pre-Amplifier Differential Output Offset Voltage (HEAD 1)	V_{OFS2}	↓			↓										↓											↓	↓				6					
5	Pre-Amplifier Output Voltage Swing	V_{OUT}	a			a										c											c	a					Input a 100 kHz, 16 [mV_{rms}] sine wave between Pins 12 and 13 and check that the output waveforms of Pins 5 and 6 are clipped. Peak-to-peak values of Pins 5 and 6 are designated as V_{OUT1} and V_{OUT2}.	3.7	4.2	—	V_{P-P}
5-1	Pre-Amplifier Output Voltage Swing (5 pin)	V_{OUT1}																									↓	↓				46					
5-2	Pre-Amplifier Output Voltage Swing (6 pin)	V_{OUT2}																									a	e				46					
6-1	Pre-Amplifier Differential Output Current Swing (5 pin)	I_{OUT}																									e	d				5	Connect 10 V power supply to Pins 5 and 6, add values of the currents flowing from these pins, and designate the new value as I_{OUT}.	3.0	4.0	—	mA_{P-P}
6-2	Pre-Amplifier Differential Output Current Swing (6 pin)		↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	6					

Measurement No.	Measurement Item	Symbol	SW Condition																													Measuring Point	Description of Measurement	Limit			
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29			Min.	Typ.	Max.	Unit
7	Pre-Amplifier Input Equivalent Noise Voltage (f = 400Hz ~ 1MHz) Pre-Amp Gain, X200	EN	b	a	a	b	a	a	a	a	a	c	c	c	c	c	a	b	a	a	a	a	a	a	a	a	b	b	a	b	a		Set the voltage gain of Pre-Amplifier to 200 Amplify, the Pre-Amplifier differential output voltage 200 times and feed it to a BPF of 400Hz to 1MHz to obtain a voltage value V_0 [V_{rms}]. Assuming the Pre-Amplifier differential gain to be G. $EN = \frac{V_0}{200G}$	—	4.5	5.5	μV
7-1	Pre-Amplifier Input Equivalent Noise Voltage (HEAD 0)	EN1														↓														↓	↓	47					
7-2	Pre-Amplifier Input Equivalent Noise Voltage (HEAD 1)	EN2	↓			↓										a							↓	↓			↓	↓		a	b	47					
8-1	Differentiator Differential Output Offset Voltage (43 pin)	V_{OFD}	a			a										c							b	b			a	a			a	43	Assuming voltages at Pins 43 and 44 to be V_B and V_A. $V_{OFD} = \lvert V_B - V_A \rvert$	—	—	10	mV
8-2	Differentiator Differential Output Offset Voltage (44 pin)																↓				↓		↓	↓								44					
9	Pulse Width Accuracy of Time Domain Filter's Mono-Multi	ETM1															b				b		a	a									Apply a 10 kHz, 1 V_{p-p} square wave V_1 to Pin 41. Assuming the output of Pin 33 to be V_2.	-10	—	+10	%
																																					
																																48 (V1) 50 (V2)	Trigger Level 1.3 [V] $T_1 \sim T_3$ [μsec]				
																																	Measuring T_1 and T_3. $ETM1 = (1 - \frac{T_1}{3}) \times 100$ or $(1 - \frac{T_3}{3}) \times 100$				
10	Pulse Width Accuracy of Read Data Output	ETM2																															Measure T_2 in the measuring conditions of Test 9.	-15	—	+15	%
																	↓															48 (V1) 50 (V2)	$ETM2 = (1 - T_2) \times 100$				
11	Pulse Width Compensation Accuracy of Time Domain Filter's Mono-Multi	ETM1C																d															Assuming that T_1 is changed to T_1' and T_3, to T_3' when the level of Pin 34 is set to "L" in the measuring conditions of Test 9.	-15	—	+15	%
																																48 (V1) 50 (V2)	$ETM1C = \lvert 1 - (T_1 - T_1') \rvert \times 100$ or $\lvert 1 - (T_3 - T_3') \rvert \times 100$				
																	↓	↓			↓	↓			↓	↓											
12	Peak Shift	PS															c	b			c	b			b	b							Input a 62.5 kHz, 0.25 mV_{p-p} sine wave between Pins 12 and 13. Output pulse widths, T_1 and T_2 at measurement point 49 are defined as shown below T_1 and T_2 are the mean values of 100 times measuring.	—	—	1	%
12-1	Peak Shift (VIN = 0.25 mV_{p-p})	PS1																															Waveform at Measurement Point 49				
12-2	Peak Shift (VIN = 10mV_{p-p})	PS2																																			
																																49	$PS = \frac{1}{2} \lvert \frac{T_1 - T_2}{T_1 + T_2} \rvert \times 100$				
																																	Measure in the same method changing input voltage from 0.25 mV_{p-p} to 10 mV_{p-p}.				
			↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓						

Measurement No.	Measurement Item	Symbol	SW 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	Measuring Point	Description of Measurement	Limit Min.	Typ.	Max.	Unit
13	Write Current Accuracy	EW	a	b	b	a	a	a	a	a	a	c	b	c↓a	c	c	a	b	a	a	a	a	a	a	a	a	a	a	a	a	a		Assume that the current to Pin 12 to be I_1, and the current Pin 12 after applying the following pulse once to Pin 28 to be I_1'. The larger of I_1 and I_1', is assumed to be I_{EW1}. $EW1 = (1 - \frac{I_{EW1}}{3}) \times 100$ Similarly, EW2 through EW4 are obtained for Pins 13 through 15. Applied pulse (H, L)	−7	—	+7	%
13-1	Write Current Accuracy (12 pin)	EW1																														12					
13-2	Write Current Accuracy (13 pin)	EW2		↓	↓		↓	↓						↓		↓																13					
13-3	Write Current Accuracy (14 pin)	EW3		a	a		b	b						c↓a		a																14					
13-4	Write Current Accuracy (15 pin)	EW4																														15					
14	Write Current Imbalance	DW																															Based on measured values of Test 13: $DW1 = \frac{2 \mid I_{EW1} - I_{EW2} \mid}{I_{EW1} + I_{EW2}} \times 100$ $DW2 = \frac{2 \mid I_{EW3} - I_{EW4} \mid}{I_{EW3} + I_{EW4}} \times 100$	—	—	1	%
14-1	Write Current Imbalance (HEAD 0)	DW1																																			
14-2	Write Current Imbalance (HEAD 1)	DW2		↓	↓		↓	↓				↓		↓		↓																					
15	Write Current Compensation Accuracy	EWC		b	b		a	a				a		c↓a		c																12	Assuming the current flowing to Pin 12 to be I_{EWC1} when the level of Pin 27 is changed to "L" in measuring conditions of Test 13-1, $EWC = \mid 1 - (I_{EWC1} - I_{EW1}) \mid \times 100$	−10	—	+10	%
			↓	↓	↓				↓		↓	↓																									
16	Head Input Terminal Saturation Voltage (Write)	V_{SAT}	b	c	a				b		b	c																				12	Assume the voltage at Pin 12 to be V_1. Further assume the voltage of Pin 12 after applying the following pulse once to Pin 28 to be V_1'. The higher of V_1 and V_1' is designated V_{SAT}. Applied Pulse (H, L)	—	—	3.6	V
			↓	↓									↓																								
17	Common Voltage "L" (Write)	V_{WLCM}	a	a									c																					—	—	0.1	V
17-1	Common Voltage "L" (20 pin)	V_{WLCM1}												↓		↓																20					
17-2	Common Voltage "L" (22 pin)	V_{WLCM2}									↓			c↓a		a																22					
18	Common Voltage "H" (Write)	V_{WHCM}									c			c↓a		c																		10.5	—	—	V
18-1	Common Voltage "H" (22 pin)	V_{WHCM1}							↓		↓			↓		↓																22					
18-2	Common Voltage "H" (20 pin)	V_{WHCM2}							c		b			c↓a		a																20					
19	Common Voltage "H" (Read)	V_{RHCM}							b					c		c																		4.8	—	5.4	V
19-1	Common Voltage "H" (22 pin)	V_{RHCM1}														↓																22					
19-2	Common Voltage "H" (20 pin)	V_{RHCM2}	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	a	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	20					

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Measurement No.	Measurement Item	Symbol	SW 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	Measuring Point	Description of Measurement	Limit Min.	Typ.	Max.	Unit
20	Erase Current Output Saturation Voltage	V_{IR}	a	a	a	a	a	a	a	a	a	c	c	c	a	c	a	b	a	a	a	a	a	a	a	a	a	a	a	a	a	24		—	—	0.5	V
															↓																						
21	Erase Current Output Leakage Current	I_{LKIR}													c																	24		—	—	15	μA
			↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓						
22	Low-Level Input Voltage	V_{LIN}																																—	—	0.8	V
22-1	Low-Level Input Voltage (27 pin)	V_{LIN1}										a																					Confirm in test 15.				
22-2	Low-Level Input Voltage (29 pin)	V_{LIN2}												a																			Confirm in test 13.				
22-3	Low-Level Input Voltage (30 pin)	V_{LIN3}													a																		Confirm in test 20.				
22-4	Low-Level Input Voltage (31 pin)	V_{LIN4}														a																	Confirm in test 13.				
22-5	Low-Level Input Voltage (34 pin)	V_{LIN5}																d															Confirm in test 11.				
23	High-Level Input Voltage	V_{HIN}																																2.0	—	—	V
23-1	High-Level Input Voltage (27 pin)	V_{HIN1}										c																					Confirm in test 13.				
23-2	High-Level Input Voltage (29 pin)	V_{HIN2}												c																			Confirm in test 2.				
23-3	High-Level Input Voltage (30 pin)	V_{HIN3}													c																		Confirm in test 21.				
23-4	High-Level Input Voltage (31 pin)	V_{HIN4}														c																	Confirm in test 13.				
23-5	High-Level Input Voltage (34 pin)	V_{HIN5}																b															Confirm in test 9.				
24	Low-Level Input Voltage (Schmitt Trigger Input) (28 pin)	V_{LINS}	a	b	b	a	a	a	a	a	a	c	b	a	c	c	a	b	a	a	a	a	a	a	a	a	a	a	a	a	a	12	Apply the following pulse to Pin 28 and check that the current value of Pin 12 changes. (2.0V / 0.8V)	—	—	0.8	V
25	High-Level Input Voltage (Schmitt Trigger Input) (28 pin)	V_{HINS}																														12	Same as above	2.0	—	—	V
			↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓						

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Measurement No.	Measurement Item	Symbol	SW Condition 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	Measuring Point	Description of Measurement	Limit Min.	Typ.	Max.	Unit
26	Low-Level Input Current	I_{LIN}	a	a	a	a	a	a	a	a	a	b	c	c	c	c	a	b	a	a	a	a	a	a	a	a	a	a	a	a	a		Apply 0.4 V to each digital signal input pin and measure the current that flows out.	—	—	250	μA
26-1	Low-Level Input Current (27 pin)	I_{LIN1}										↓	↓																			27					
26-2	Low-Level Input Current (28 pin)	I_{LIN2}										c	a	↓																		28					
26-3	Low-Level Input Current (29 pin)	I_{LIN3}											c	b	↓																	29					
26-4	Low-Level Input Current (30 pin)	I_{LIN4}												c	b	↓																30					
26-5	Low-Level Input Current (31 pin)	I_{LIN5}													c	b		↓														31					
26-6	Low-Level Input Current (34 pin)	I_{LIN6}														c		c														34					
27	High-Level Input Current	I_{HIN1}																b															Apply 2.4 V to each digital signal input pin and measure the current that flows out.	—	—	10	μA
27-1	High-Level Input Current (28 pin)	I_{HIN11}												↓																		28					
27-2	High-Level Input Current (29 pin)	I_{HIN12}												d	↓																	29					
27-3	High-Level Input Current (30 pin)	I_{HIN13}												c	d	↓																30					
27-4	High-Level Input Current (31 pin)	I_{HIN14}										↓			c	d																31					
28	High-Level Input Current (27 pin)	I_{HIN2}										d				c																27	Apply 2.4 V to Pin 27 and measure the current that flows out.	—	—	130	μA
												↓						↓																			
29	High-Level Input Current (34 pin)	I_{HIN3}										c						a														34	Apply 2.4 V to Pin 34 and measure the current that flows out.	—	—	60	μA
														↓				↓	↓																		
30	Power ON/OFF Detector V_{CC1} Threshold Voltage	V_{TH5}												a				b	b													32	V_{TH5} OFF is the voltage of V_{CC1} when the voltage of Pin 32 becomes 0.5 V or less when V_{CC1} is decreased from 5 V. V_{TH5} ON is the voltage of V_{CC1} when the voltage of Pin 32 becomes 4.5 V or greater when V_{CC1} is increased from 3 V.	3.6	4.0	4.4	V
										↓									↓																		
31	Power ON/OFF Detector V_{CC2} Threshold voltage	V_{TH12}								b									a													32	V_{TH12} OFF is the voltage of V_{CC2} when the voltage of Pin 32 becomes 0.5 V or less when V_{CC2} is decreased from 12 V. V_{TH12} ON is the voltage of V_{CC2} when the voltage of Pin 32 becomes 4.5 V or greater when V_{CC2} is increased from 8 V.	8.2	9.2	10.0	V
			↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓						

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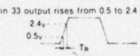
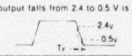
Measurement No.	Measurement Item	Symbol	SW Condition 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	Measuring Point	Description of Measurement	Limit Min.	Typ.	Max.	Unit
32	Read Data Output Low-Level Output Voltage (I_{OL} = 2mA)	V_{LOUT}	a	a	a	a	a	a	a	a	a	c	c	c	c	c	e	b	a	a	a	a	a	a	a	a	a	a	a	a	a	33	Pin 33 voltage when 2 mA is applied to Pin 33 is designated V_{LOUT}.	—	—	0.5	V
																	↓			↓	↓																
33	Read Data Output High-Level Output Voltage (I_{OH} = 0.4mA)	V_{HOUT}															d			b	b											33	Input a 10 kHz, 1 V_{p-p} square wave to Pin 41. Pin 33 voltage when 0.4 mA flows from Pin 33 is designated V_{HOUT}.	2.8	—	—	V
																	↓			↓																	
34	Read Data Output Rise Time	TR															f			a												51	Input a 10 kHz, 1 V_{p-p} square wave to Pin 41. The time Pin 33 output rises from 0.5 to 2.4 V is designated T_R.  	—	—	100	nS
35	Read Data Output Fall Time	TF																														51	Input a 10 kHz, 1 V_{p-p} square wave to Pin 41. The time Pin 33 output falls from 2.4 to 0.5 V is designated T_F.  	—	—	100	nS
																	↓				↓																
36	V_{CC1} Supply Current (Read)	I_{CC1R}															a				a											35		16.0	22.0	28.0	mA
													↓																								
37	V_{CC1} Supply Current (Write)	I_{CC1W}												a																		35		7.0	12.5	16.5	mA
													↓																								
38	V_{CC2} Supply Current (Read)	I_{CC2R}												c																		21		7.0	10.0	14.0	mA
													↓																								
39	V_{CC2} Supply Current (Write)	I_{CC2W}												a																		21		9.0	12.5	16.0	mA
			↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓						

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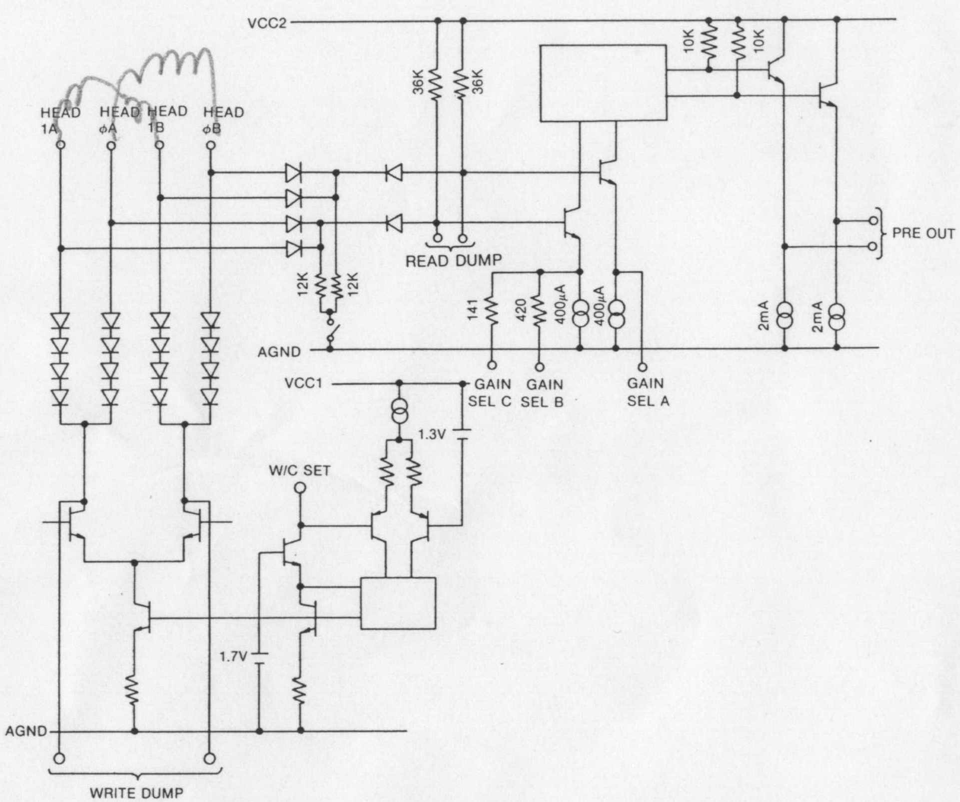
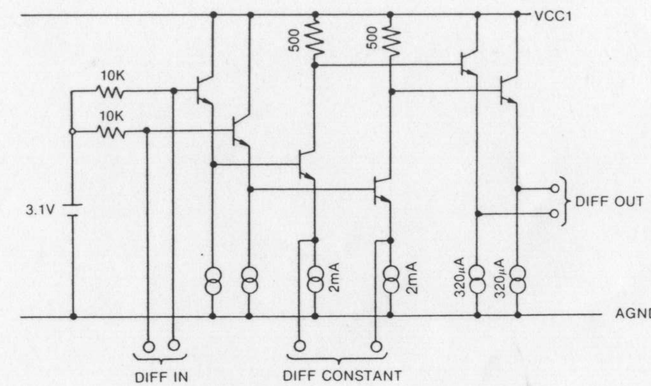
CX-20185 INPUT/OUTPUT CIRCUIT

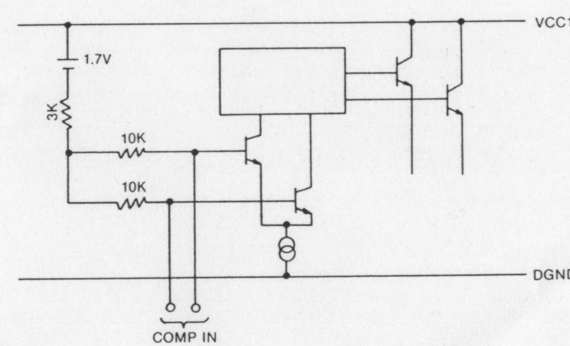
(1) PRE AMP



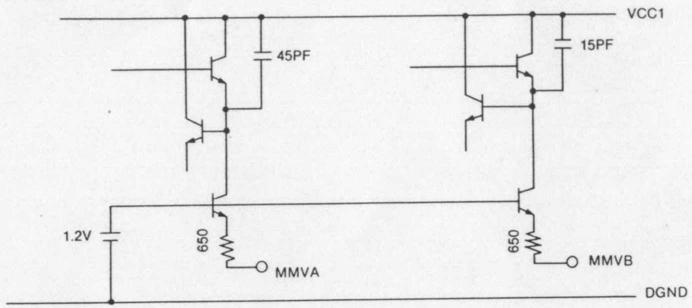
(2) DIFFERENTIATOR



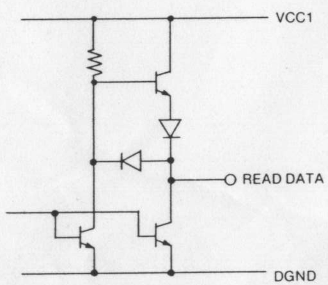
(3) COMPARATOR



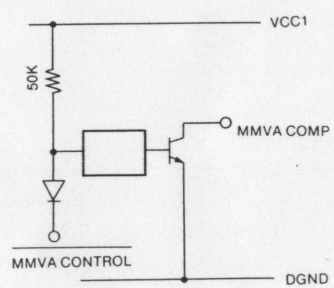
(4) TIME DOMAIN FILTER



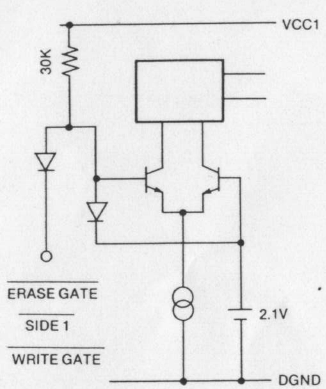
(5) READ OUTPUT



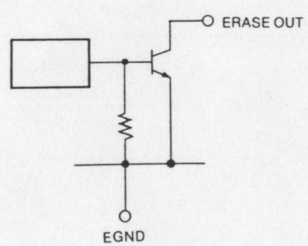
(6) MMVA CONTROL



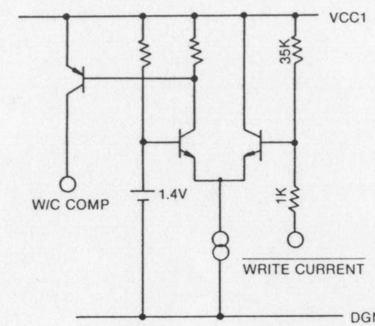
(7) INPUT GATE



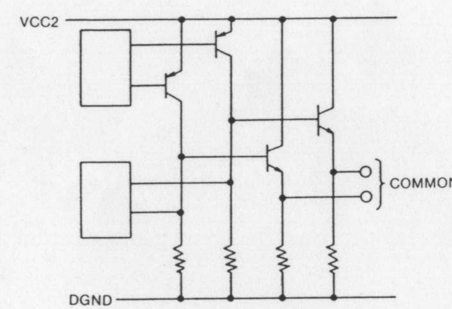
(8) ERASE OUTPUT



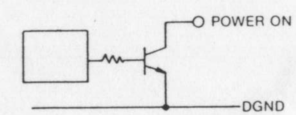
(9) W/C CONT



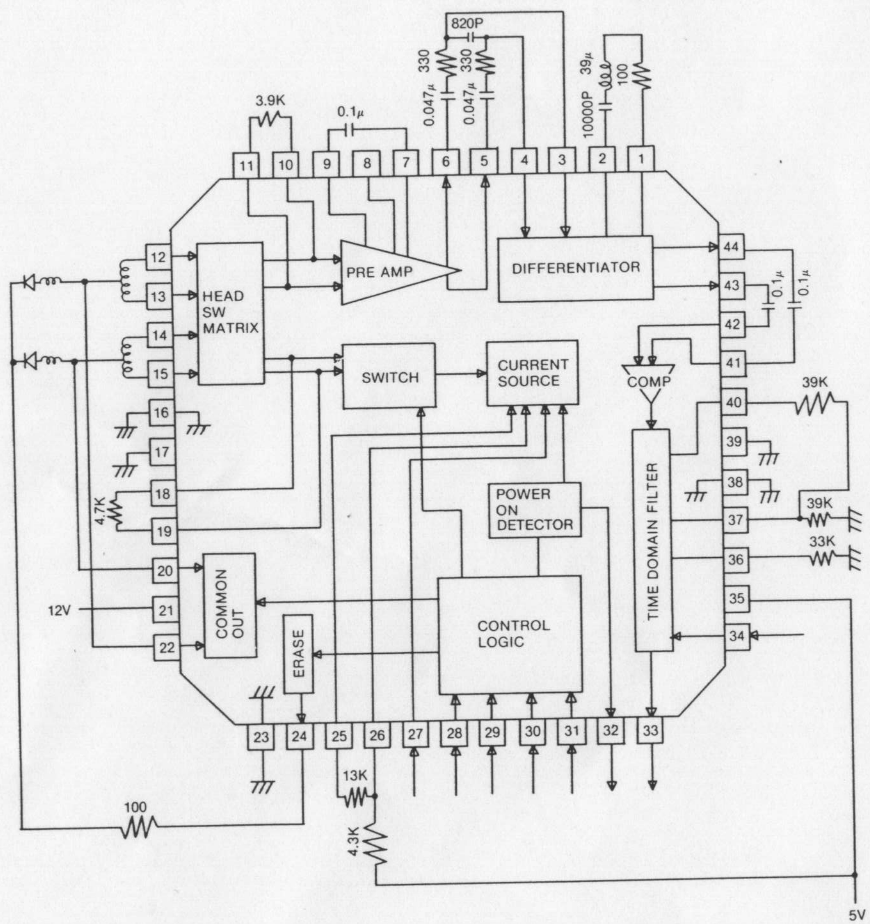
(10) COMMON



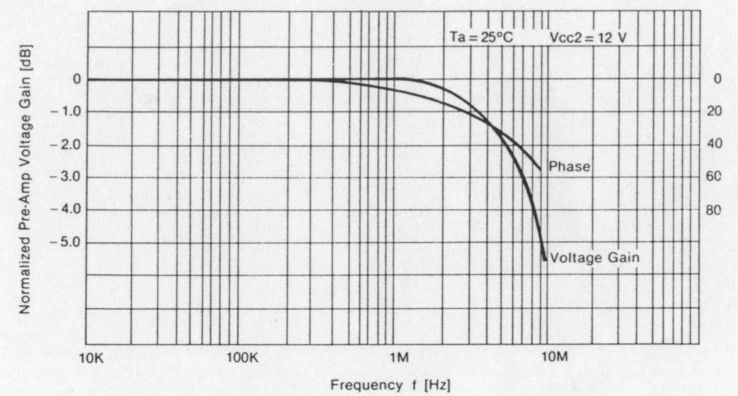
(11) POWER ON



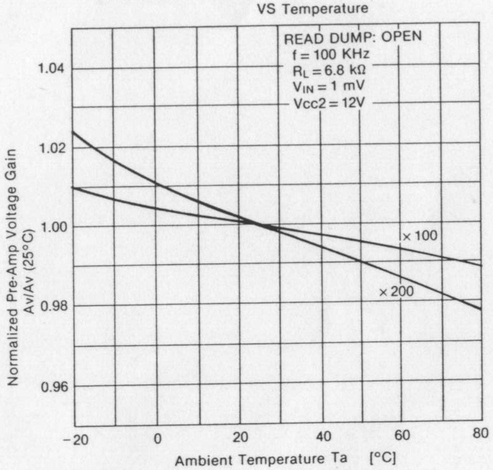
Example of Applied Circuit (For 300rpm)



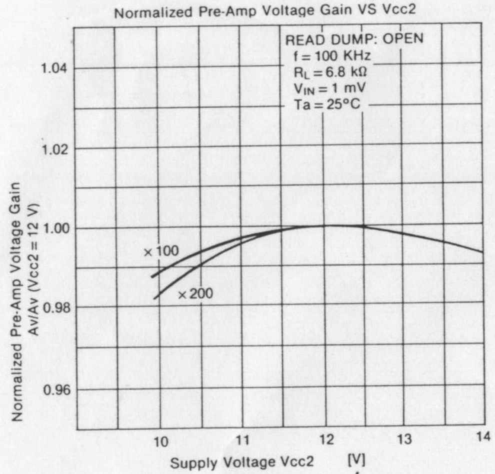
Phase and Normalized Voltage Gain
VS Frequency



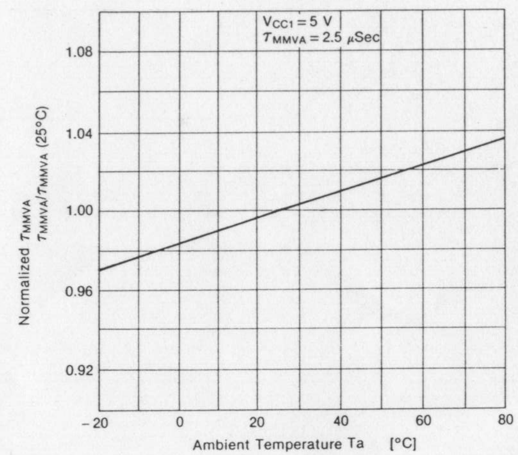
Normalized Pre-Amp Voltage Gain VS Temperature



Normalized Pre-Amp Voltage Gain VS Vcc2

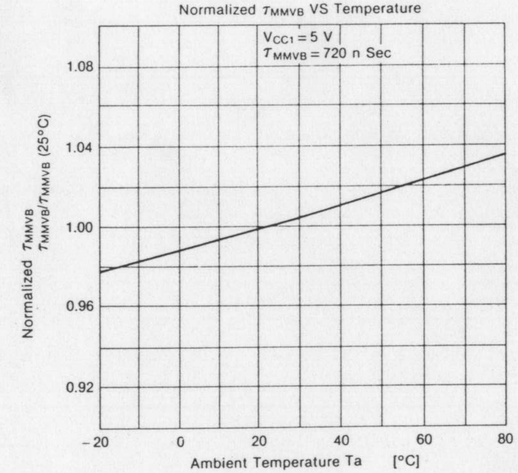


Normalized τ_{MMVA} VS Temperature

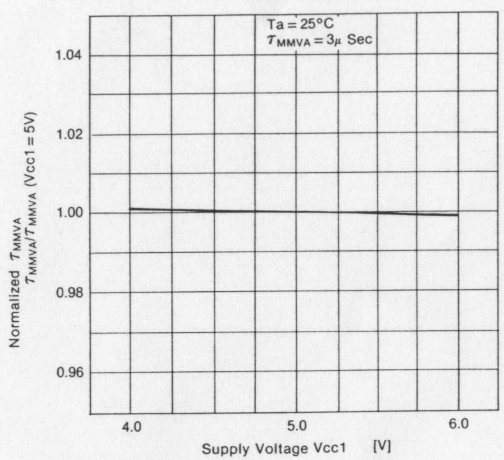


τ_{MMVA}: Pulse Width of Time Domain Filter's Mono-Multi
τ_{MMVB}: Pulse Width of Read Data Output

Normalized τ_{MMVB} VS Temperature

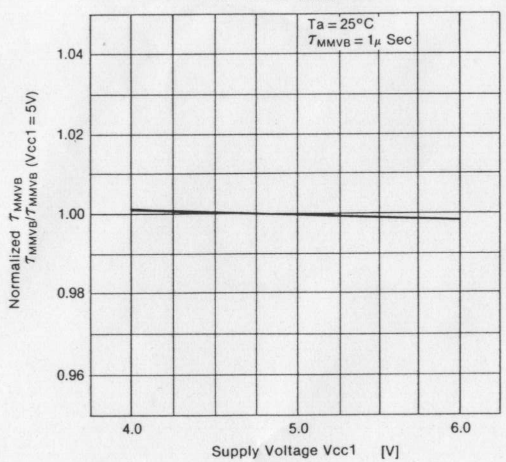


Normalized τ_{MMVA} VS Vcc1

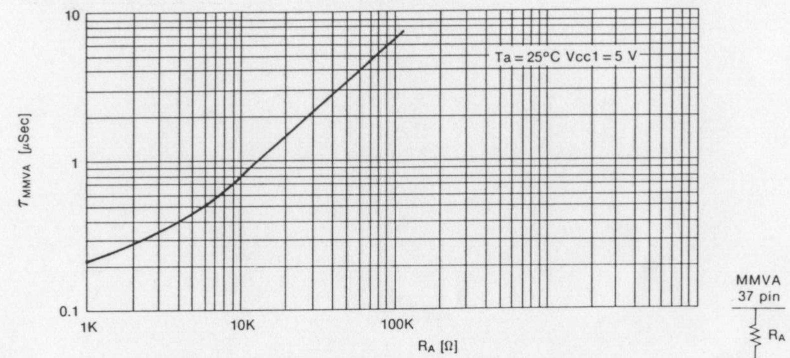


τ_{MMVA}: Pulse Width of Time Domain Filter's Mono-Multi
τ_{MMVB}: Pulse Width of Read Data Output

Normalized τ_{MMVB} VS Vcc1

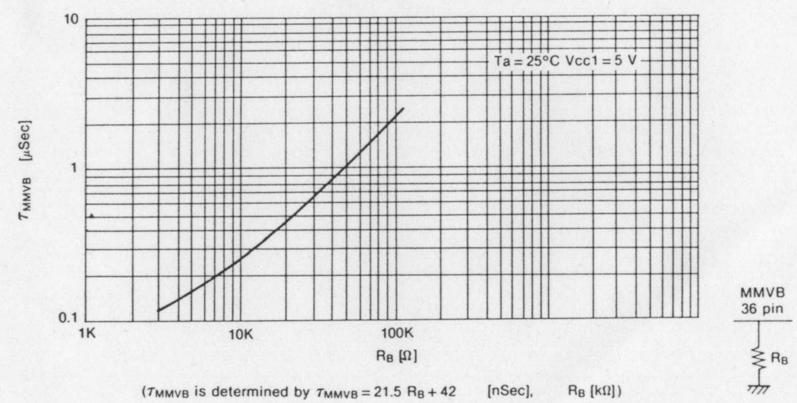


τ_{MMVA} VS R_A

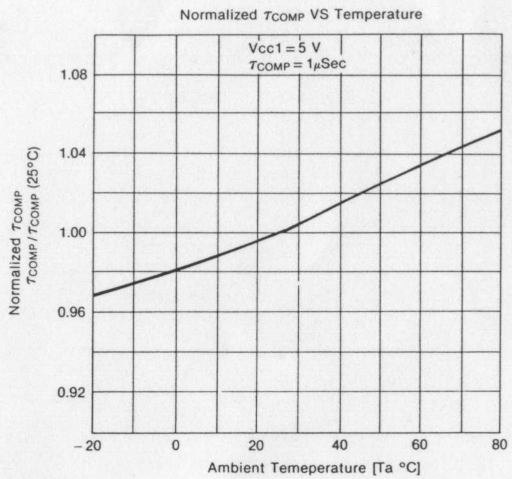


(τ_{MMVA} is determined by $\tau_{MMVA} = 62.5\ R_A + 155$ [nSec], R_A [kΩ])

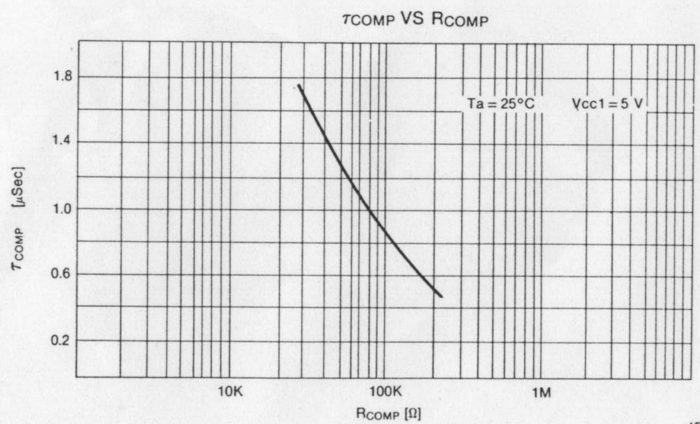
τ_{MMVB} VS R_B

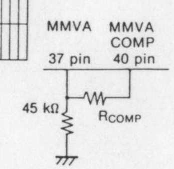


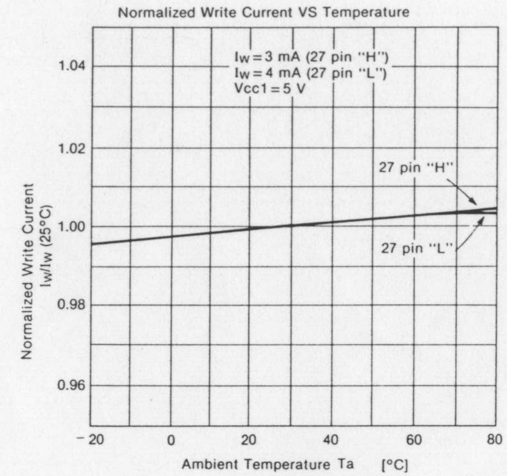
(τ_{MMVB} is determined by $\tau_{MMVB} = 21.5\ R_B + 42$ [nSec], R_B [kΩ])

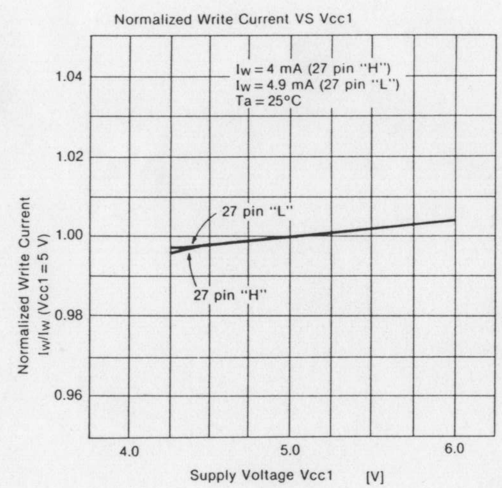


τCOMP: Pulse Width Compensation of Time Domain Filter's Mono-Multi
τCOMP = τMMVA (34 pin "H") — τMMVA(34 pin "L")

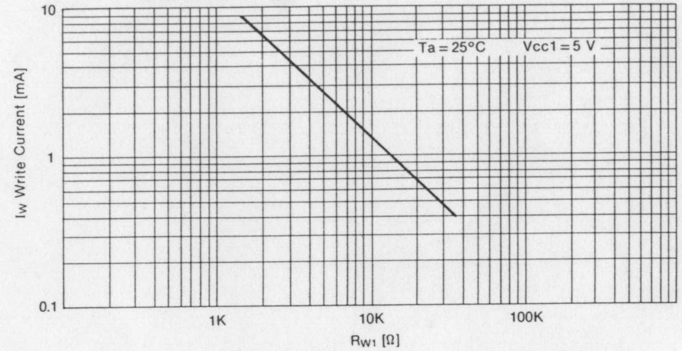


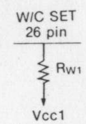






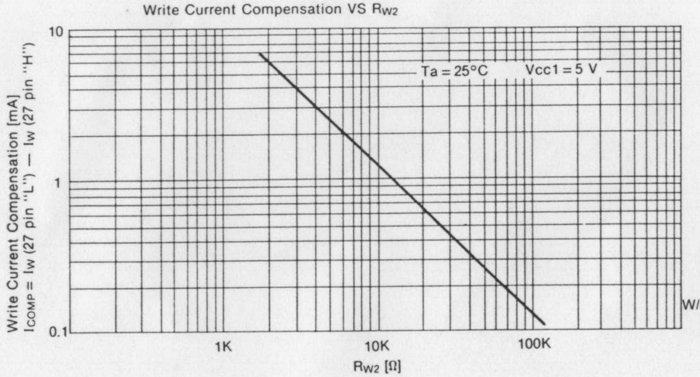
Write Current VS R_{W1}

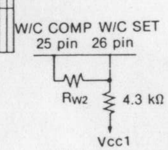




(I_W is determined by $I_W = 13.4/R_{W1}$ [mA], R_{W1} [kΩ])

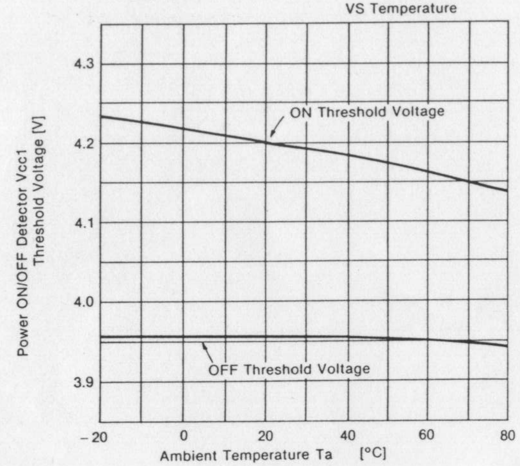
Write Current Compensation VS R_{W2}





(I_{COMP} is determined by $I_{COMP} = 12.65/R_{W2}$ [mA], R_{W2} [kΩ])

Power ON/OFF Detector Vcc1 Threshold Voltage VS Temperature



Power ON/OFF Detector Vcc2 Threshold Voltage VS Temperature