CX20709

USB/I^{2}S Audio CODEC, Audio/ Voice DSP, Stereo Class-D, Headphone Driver

Data Sheet

DSH-202806A
October 2011

CONEXANT

Revision History

Revision	Date	Description
A	October 18, 2011	Initial release

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1 CX20709 Introduction

1.1 Summary

The CX20709 is one of Conexant's Audio/Voice DSP CODEC family solutions with highly integrated hardware DSP, CODEC, Class-D amplifier, USB, I^2S, S/PDIF, and I^2C interfaces. The solution features a suite of turnkey audio and voice enhancement algorithms designed for convergence audio entertainment and voice communication applications, such as PC Docking System/Sound-Bar, Portable Multimedia/Navigation Devices, Smart Home Intercom System, Media IP Phone, and Unified Communication Peripherals.

The CX20709 offers multiple digital data and control I/O for flexible peripheral or MCU/MPU connectivity. The device features one 4-wire and one 5-wire digital audio interface which can be mixed or multiplexed to support bi-directional I^2S, PCM, and S/PDIF. The device can be controlled and configured by both read and write capability through I^2C and SPI. The device features a USB 2.0 Compliant Audio Class interface (full-speed for data and control) and a UART interface for the external MCU/MPU interface.

The device integrates three high-performance 102 dB SNR, 24-bit DACs for 2.1CH speaker output, capless headphone output, and single-ended/differential line-output. The analog input paths feature four high performance 24-bit ADC supporting up to four microphones or three stereo Line-Inputs. Different audio sampling rates ranging from 8 kHz to 96 kHz are generated directly from the master clock without the need for external PLL. The power-efficient integrated Class-D stereo amplifier operates at 5 V or 3.3 V with an optional maximum power of 2.8 W at a 4 Ω load. For intercom application, the mono line-out supports 600 Ω drivers, which can drive the isolation transformer directly without an external operational amplifier.

The on-chip DSP is designed to run a suite of Voice Processing Algorithms and Audio Post Processing Effects offered by Conexant. The device features Conexant's soundbar algorithm for USB 5.1 channel sound-bar enhancement. The audio designer has the ability to adjust and optimize performance on the target system by using the SPoC Configuration Toolbox.

The CX20709 operates at supply voltages down to 3.3 V for analog and 1.8 V for the digital core. An advanced power management scheme can be configured to achieve <7.55 mW in sleep mode

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1.2 Features

1.2.1 Codec Features

- 4-wire and 5-wire digital audio I/O (I^2S/PCM/SPDIF), supporting full duplex independent sampling rates, master clock for optional PCM/I^2S slave codec (SPDIF-in available in CX20709-21Z)
- One 2-wire I^2C and one 4-wire SPI slave interface for external MCU
- USB 2.0 Compliant full speed UAC Interface
- Supporting dual USB playback end points (available in CX20709-21Z)
- Stereo Digital Microphone, up to 12 MHz clock rate (available in CX20709-21Z)
- Eight GPIO pins
- 2.8 W x 2 BTL filter-less stereo Class-D Speaker Amplifier
  - Low EMI Class-D amplifier output with Spread Spectrum and common mode scrambler
- Integrated 50 mW headphone driver with jack sense
- Single-ended or differential line output
- Separate mixed mono line-output for sub-woofer or intercom usage
- Three single-ended stereo or one differential stereo analog audio input
- Up to 4 microphone interfaces with on-chip bias supply (available in CX20709-21Z)
- 24-bit DAC/ADC, SNR 102 dB, THD - 92 dB at 48 kHz 3.3 V
  - In DSP mode, the processing will be limited the input and output to 16-bit effective resolution
- Audio sample rate: 8,16, 22.05, 24, 32, 44.1, 48, 88.2, 96 kHz
- 90 dB Dynamic Range with 0.1% THD+N at 4 Ω load
- 12-bit ADC multiplexed to support analog volume potentiometer and DC level detection
- Flexible Power Management
- Variable master clock rates
- Configurable On-Chip proprietary Voice/Audio Processing
  - Subband Acoustic Echo Cancellation
  - Dual Microphone Beam Forming
  - Noise Reduction
  - Dynamic Loudness Adaptor
  - Microphone Automatic Gain Control
  - Subband Line Echo Cancellation (2-way intercom applications)
  - Digital Equalizer (10 bands/channel)
  - Dynamic Range Compression
  - 4th Order Digital Crossover for Subwoofer Line-out
  - Conexant sound-bar algorithm for USB 5.1 channel sound-bar enhancement (available in CX20709-21Z)
- SPoC Configuration Toolbox
  - Fast configuration via USB-to-I^2C from PC
  - Data path, I/O setup, and DSP parameter adjustment
  - Output log for convenient MCU programming

1.2.2 Ordering Options

Table 1 list the ordering options for each device.

Table 1. Ordering Options

Order Number	Part Number	Package	Description
DSAC-L709-21CH	CX20709-21Z	76QFN	
DSAC-L709-12CH	CX20709-12Z	76QFN	Not recommended for new design
CX20709-EVK2	CX20709-EVK2		CX20709-21Z Evaluation Kit
CX20709-EVK2-IN	CX20709-EVK2-IN		CX20709-21Z Intercom Daughter Board
All devices are lead-free (Pb Free) and RoHS compliant			

1.2.3 CX20709 Device Differences

Device	20709-12Z	20709-21Z
DAC/ADC	3/4	3/4
I^2S/PCM (5 wires interface)	1	1
SPDIF OUT (uses TX, 5^{th} wire from I^2S)	1	1
I^2S/PCM(4 wires interface)	1	1
USB Client	1	1
I^2C (2 or 3 wires) /SPI (Slave)	1	1
Digital Mic (Retaskable to 1 SPDIF IN)	—	2
UART	1	1
GPIO	8	8
EEPROM Interface (I^2C Master)	1	1
Stereo Line In Single Ended (convertible to Differential)	3	3
Microphone In	2	4
Mic Bias	2	2
600ohm Mono Out (Diff/Single Ended)	1	1
Jack Sense Jacks (4 jacks via 1 pin)	4	4
Stereo Headphone	1 capless	1 capless
Stereo Class D Amplified Output	1	1
Stereo Line Out (Diff/Single Ended)	1	1

1.2.4 Applications

- PC Speakers System
- LCD Display/SoundBar
- Home Automation/Intercom
- PND/PMP
- Multi Media IP Phone
- Telepresence/Unified Communication Device
- Embedded Applications

1.2.5 CX20709 Interface Diagram

Figure 1 provides a diagram of the CX20709-21Z interface. Figure 2 provides a diagram of the CX20709-12Z interface.

Figure 1. CX20709-21Z Interface Diagram

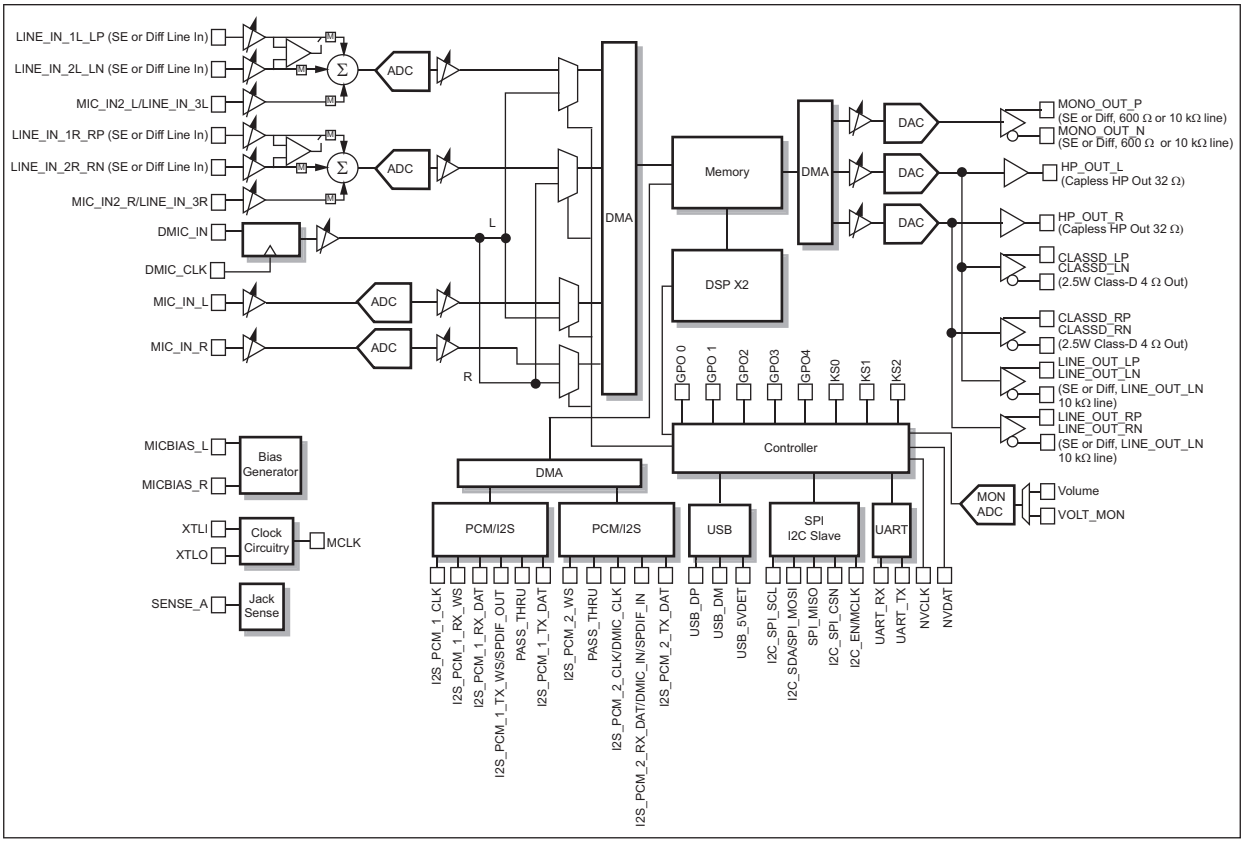
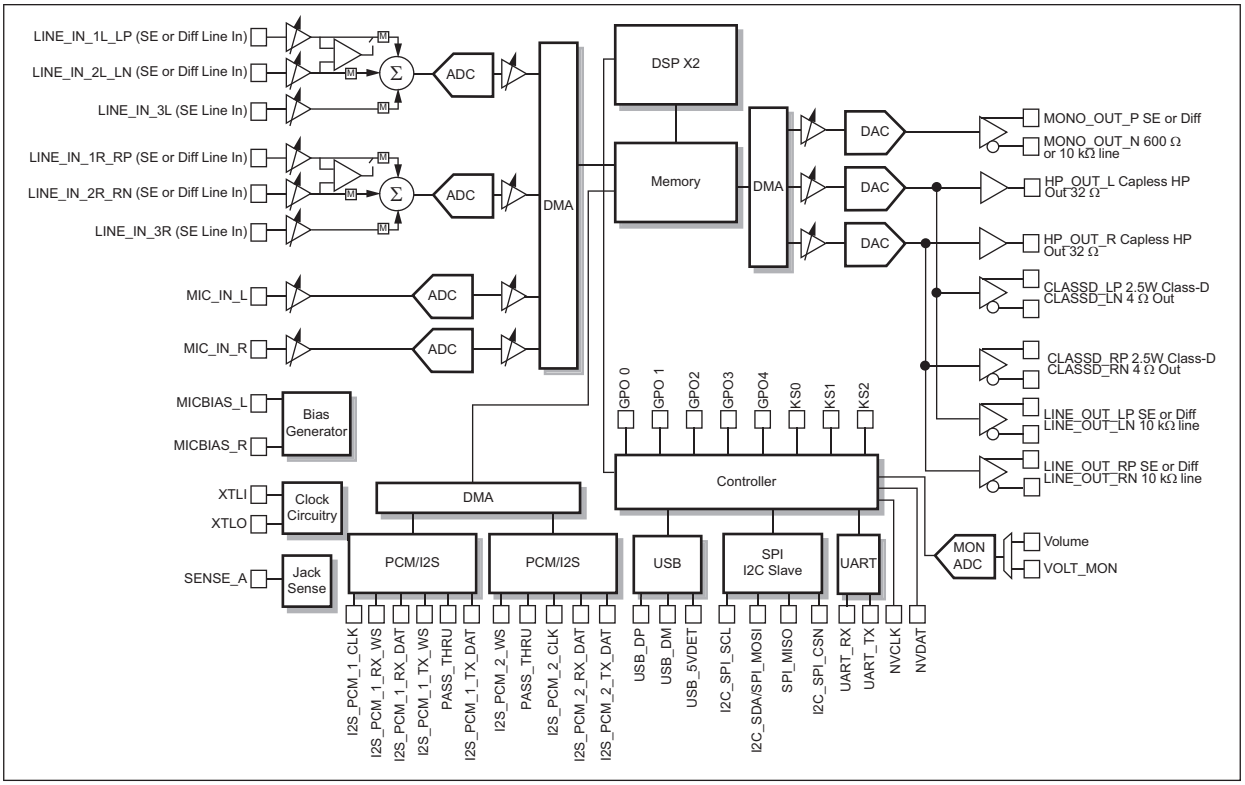


Figure 2. CX20709-12Z Interface Diagram



2 CX20709-21Z Hardware Interface

2.1 CX20709-21Z Pin Assignments

Table 2 provides the pin assignments.

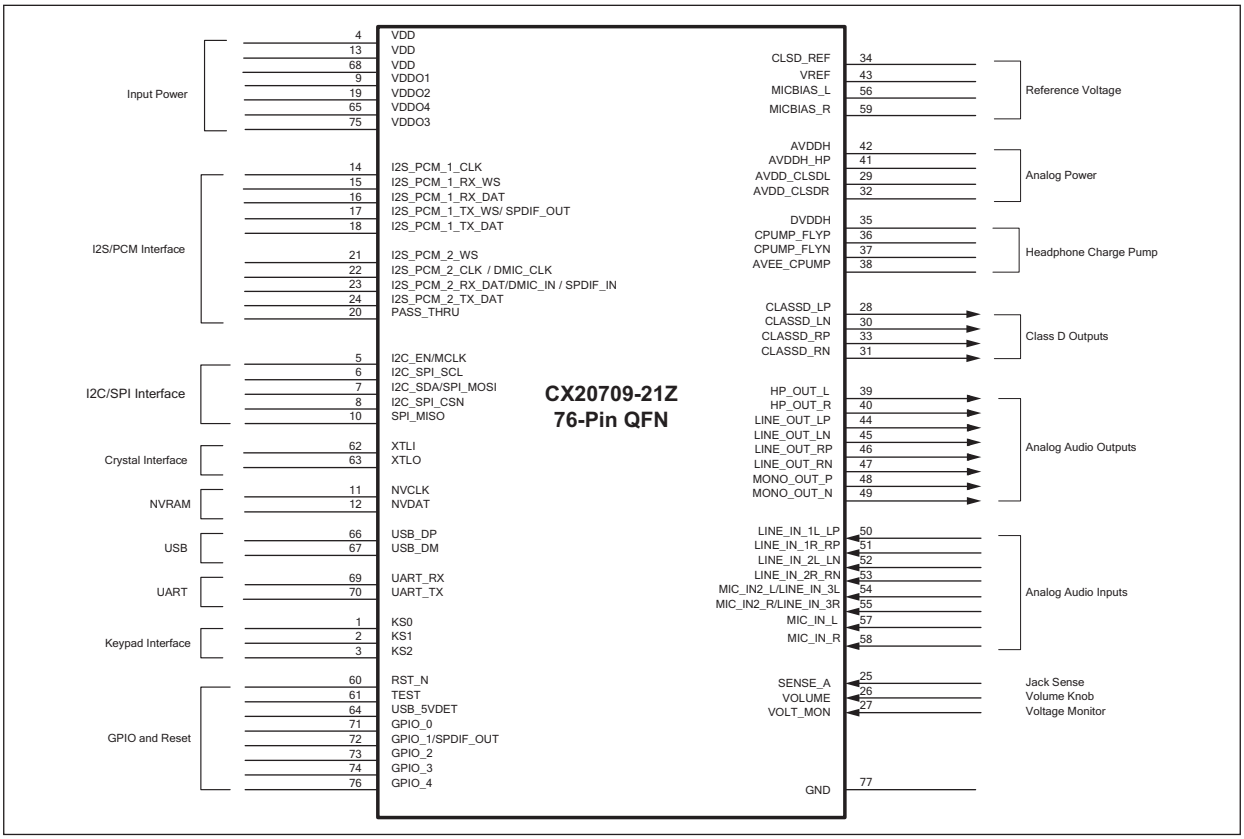
Table 2. CX20709-21Z Pin Assignments and Signal Definitions

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	KS0	20	PASS_THRU	39	HP_OUT_L	58	MIC_IN_R
2	KS1	21	I2S_PCM_2_WS	40	HP_OUT_R	59	MIC_BIAS_R
3	KS2	22	I2S_PCM_2_CLK/ DMIC_CLK	41	AVDDH_HP	60	RST_N
4	VDD	23	I2S_PCM_2_RX_DAT/ DMIC_IN / SPDIF_IN	42	AVDDH	61	TEST
5	I2C_EN/MCLK	24	I2S_PCM_2_TX_DAT	43	VREF	62	XTLI
6	I2C_SPI_SCL	25	SENSE_A	44	LINE_OUT_LP	63	XTLO
7	I2C_SDA/SPI_MOSI	26	VOLUME	45	LINE_OUT_LN	64	USB_5VDET
8	I2C_SPI_CSN	27	VOLT_MON	46	LINE_OUT_RP	65	VDDO4
9	VDDO1	28	CLASSD_LP	47	LINE_OUT_RN	66	USB_DP
10	SPI_MISO	29	AVDD_CLSDL	48	MONO_OUT_P	67	USB_DM
11	NVCLK	30	CLASSD_LN	49	MONO_OUT_N	68	VDD
12	NVDAT	31	CLASSD_RN	50	LINE_IN_1L_LP	69	UART_RX
13	VDD	32	AVDD_CLSDR	51	LINE_IN_1R_RP	70	UART_TX
14	I2S_PCM_1_CLK	33	CLASSD_RP	52	LINE_IN_2L_LN	71	GPIO_0
15	I2S_PCM_1_RX_WS	34	CLSD_REF	53	LINE_IN_2R_RN	72	GPIO_1/SPDIF_OUT
16	I2S_PCM_1_RX_DAT	35	DVDDH	54	MIC_IN2_L/ LINE_IN_3L	73	GPIO_2
17	I2S_PCM_1_TX_WS/ SPDIF_OUT	36	CPUMP_FLYP	55	MIC_IN2_R/ LINE_IN_3R	74	GPIO_3
18	I2S_PCM_1_TX_DAT	37	CPUMP_FLYN	56	MICBIAS_L	75	VDDO3
19	VDDO2	38	AVEE_CPUMP	57	MIC_IN_L	76	GPIO_4
GENERAL NOTES: The device also has a ground paddle referred to as pin 77 in this document.							

2.2 CX20709-21Z Hardware Interface Signals

Figure 3 shows the signals for the hardware interface. Table 2 provides a list of the CX20709-21Z hardware signal definitions.

Figure 3. CX20709-21Z Hardware Interface Signals



2.3 Signal Definitions

Table 3. CX20709-21Z Hardware Signal Definitions *(1 of 4)*

Label	Pin	I/O Type	Signal Name/Description
Crystal Signals			
XTLI	62	Digital In	**Crystal In**. Connect XTALI to a 48.0 MHz crystal circuit.
XTLO	63	Digital Out	**Crystal Out.** Connect XTALO to the crystal circuit return.
I^2S/PCM Interface			
I2S_PCM_1_CLK	14	Digital I/O	**Digital Port 1.** I^2S/PCM Bit Clock.
I2S_PCM_1_RX_WS	15	Digital I/O	**Digital Port 1.** I^2S/PCM Receive Word Select.
I2S_PCM_1_RX_DAT	16	Digital In	**Digital Port 1.** I^2S/PCM Receive Word Data.
I2S_PCM_1_TX_WS/ SPDIF_OUT	17	Digital I/O	**Digital Port 1.** I^2S/PCM Transmit Word Select. This pin can optionally be defined as the SPDIF output.
I2S_PCM_1_TX_DAT	18	Digital Out	**Digital Port 1.** I^2S/PCM Transmit Word Data.
PASS_THRU	20	Digital In	**I^2S Pass Through.** This allows the interface to be shared with another I^2S device. In pass through mode, the transmit data pin is driven by the pass through pin instead of the internal interface engine.
I2S_PCM_2_WS	21	Digital I/O	**Digital Port 2.** I^2S/PCM Word Select.
I2S_PCM_2_CLK/ DMIC_CLK	22	Digital I/O	**Digital Port 2.** I^2S/PCM Bit Clock. DMIC_CLK: Can be optionally programmed as the digital microphone clock.
I2S_PCM_2_RX_DAT/ DMIC_IN / SPDIF_IN	23	Digital In	**Digital Port 2.** I^2S/PCM Receive Word Data. DMIC_IN: Digital Mic input. Can be selected either as Line Input stream or Analog Mic input stream SPDIF_IN: SPDIF input. (Shared pin)
I2S_PCM_2_TX_DAT	24	Digital Out	**Digital Port 2.** I^2S/PCM Transmit Word Data.
I^2C/SPI Interface			
I2C_EN/MCLK	5	Digital I/O	**I^2C Enable.** Selects I^2C or SPI interface. Connect to VDDO1 for I^2C mode, 0V for SPI mode. MCLK: After CX20709-21Z firmware has been successfully loaded, this pin can be configured as an optional I^2S codec master clock output.
I2C_SPI_SCL	6	Digital I/O	**I^2C/SPI Clock.**
I2C_SDA/SPI_MOSI	7	Digital I/O	**I^2C/SPI Data.**
I2C_SPI_CSN	8	Digital In	**I^2C/SPI Chip Select.** I2C_ SPI_CSN=0 enables I2C/SPI. I2C_SPI_CSN=1 disables I2C/SPI access.
SPI_MISO	10	Digital I/O	**SPI Data to Host.** In I^2C mode, this pin is used to select between I^2C slave address of 14H and 54H, respectively.

***Table 3. CX20709-21Z Hardware Signal Definitions** (2 of 4)*

Label	Pin	I/O Type	Signal Name/Description
USB			
USB_DP	66	Digital I/O	**USB Data Positive.**
USB_DM	67	Digital I/O	**USB Data Negative.**
Control Signals			
RST_N	60	Digital In	**Reset.** Active low input asserted to initialize registers, sequencers, and signals to a consistent reset state. RST_N should remain low for 5ms after all power rails have become stable. Then RST_N should go to VDDO4.
TEST	61	Digital In	**TEST.** Connect to ground through a 0 Ω resistor.
USB_5VDET	64	Digital In	**USB 5V Detect.** USB +5V VBUS signal should be connected to a resistor divider to reduce the level to 3.3 V at this pin.
GPIO_0	71	Digital I/O	**GPIO.** If using the UART interface, this pin should be used as the UART CTS signal.
GPIO_1/SPDIF_OUT	72	Digital I/O	**GPIO.** Pin can be configured as the SPDIF output.
GPIO_2	73	Digital I/O	**GPIO.**
GPIO_3	74	Digital I/O	**GPIO.**
GPIO_4	76	Digital I/O	**GPIO.**
SENSE_A	25	Analog In	**Jack Sense.** Connect to external resistor network to sense up to 4 jacks.
VOLUME	26	Analog In	**Analog Volume Control.** Connect to potentiometer. When set to 3.3 V, volume is maximum.
VOLT_MON	27	Analog In	**Voltage Monitor.** This pin can be used to monitor an external battery voltage.
Button Interface			
KS[0:2]	1, 2, 3	Digital I/O	**Keypad Scan I/O.** These pins can be used to form a button matrix or can be used as GPIO.
UART Interface			
UART_RX	69	Digital In	**UART Receive.**
UART_TX	70	Digital Out	**UART Transmit.**
NVRAM Signals			
NVCLK	11	Digital I/O	**NVRAM Clock.** Connect to external NVRAM clock signal.
NVDAT	12	Digital I/O	**NVRAM Data.** Connect to external NVRAM data signal. Connect to VDDO1 via 4.7 kΩ pull-up resistor.

***Table 3. CX20709-21Z Hardware Signal Definitions** (3 of 4)*

Label	Pin	I/O Type	Signal Name/Description
Analog Audio Inputs			
LINE_IN_1L_LP	50	Analog In	**Line Input Left 1/Positive.** In single-ended mode, this pin is the left input for line input 1. In differential mode, this pin is the left positive input and is paired with pin 52.
LINE_IN_1R_RP	51	Analog In	**Line Input Right 1/Positive.** In single-ended mode, this pin is the right input for line input 1. In differential mode, this pin is the right positive input and is paired with pin 53.
LINE_IN_2L_LN	52	Analog In	**Line Input Left** 2/Negative. In single-ended mode, this pin is the left input for line input 2. In differential mode, this pin is the left negative input and is paired with pin 50.
LINE_IN_2R_RN	53	Analog In	**Line Input Right** 2/Negative. In single-ended mode, this pin is the right input for line input 2. In differential mode, this pin is the right negative input and is paired with pin 51.
MIC_IN2_L/R LINE_IN_3L/R	54, 55	Analog In	**Left and Right Microphone 2 Input/Line Input 3.** The 2nd set of microphone inputs. Can be used as stereo line input 3 by attenuating the mic boost amplifier.
MIC_IN_L/R	57, 58	Analog In	**Left and Right Microphone Inputs.** L Mic is used in both DSP mode and Pass-Thru mode. R Mic is used in either: 1. Pass-Thru mode or 2. Beam-Forming in DSP mode. It is not enabled in DSP mode unless it is used in Beam Forming.
Analog Audio Outputs			
CLASSD_LP/N	28, 30	Analog Out	**Class-D Left Differential Output.**
CLASSD_RN/P	31, 33	Analog Out	**Class-D Right Differential Output.**
HP_OUT_L/R	39, 40	Analog Out	Headphone Out. 50 mW Capless headphone output
LINE_OUT_LP/N	44, 45	Analog Out	**Line Out Left.** Can be configured as single-ended or differential. In single-ended mode, the output is on the positive pin.
LINE_OUT_RP/N	46, 47	Analog Out	**Line Out Right.** Can be configured as single-ended or differential. In single-ended mode, the output is on the positive pin.
MONO_OUT_P/N	48, 49	Analog Out	**Mono Out.** Can be configured as single-ended or differential. In single-ended mode, the output is on the positive pin. Can be used as a subwoofer output or to drive a 600 Ω load for intercom applications.
Headphone Charge Pump			
DVDDH	35	Power	**3.3 V Power for HP & Class-D digital circuits.** Requires 3.3 V external power supply.
CPUMP_FLYP	36	Power	**Charge Pump Positive Transfer Charge.** Connect to CPUMP_FLYN through a 1 μF capacitor.
CPUMP_FLYN	37	Power	**Charge Pump Negative Transfer Charge.** Connect to CPUMP_FLYP through a 1 μF capacitor.

***Table 3. CX20709-21Z Hardware Signal Definitions** (4 of 4)*

Label	Pin	I/O Type	Signal Name/Description
AVEE_CPUMP	38	Power	**Charge Pump Negative Power Supply.** Internally generated negative charge pump power. Connect to 10 µF and 0.1 µF external filtering capacitors.
Digital Power			
VDD	4, 13, 68	Power	**VDD.** Requires 1.8 V external power supply.
VDDO1	9	Power	**VDDO1.** Power for I^2C and NVRAM interfaces. Requires 1.8 V or 3.3 V external power supply.
VDDO2	19	Power	**VDDO2.** Power for PCM interfaces. Requires 1.8 V or 3.3 V external power supply.
VDDO3	75	Power	**VDDO3.** Power for GPIO. Requires 1.8 V or 3.3 V external power supply.
VDDO4	65	Power	**VDDO4.** Power for crystal and reset blocks. Requires 3.3 V external power supply.
Analog Power			
AVDDH	42	Power	**AVDDH.** Requires 3.3 V external power supply.
AVDDH_HP	41	Power	**AVDDH_HP.** Headphone power. Connect to 3.3 V.
AVDD_CLSDL	29	Power	**Class-D Left Channel Input Power.** This pin can be powered by 3.3 V or 5.0 V. If 3.3 V, maximum speaker power output is 1.0 W per channel. If 5V, maximum speaker power output is 2.5 W per channel. Must be the same voltage as Pin #32.
AVDD_CLSDR	32	Power	**Class-D Right Channel Input Power.** This pin can be powered by 3.3 V or 5.0 V. If 3.3 V, maximum speaker power output is 1.0 W per channel. If 5 V, maximum speaker power output is 2.5 W per channel. Must be the same voltage as Pin #29.
Reference Voltage			
CLSD_REF	34	Power	**Class-D Reference Voltage.** Internally generated supply that is 1.7 V if Class-D power on Pins: 29, 32 = 5 V. Connect to Class-D supply via a 0.1 µF capacitor. 350 mV if Class-D power on Pins: 29, 32 = 3.3 V, depending on Class-D input power on pins 29 and 32.
VREF	43	Power	**VREF.** Internally generated 1.65 V supply.
MICBIAS_L	56	Power	**Left Microphone Bias.** Can be programmed to be 50% or 80% of 3.3 V.
MICBIAS_R	59	Power	**Right Microphone Bias.** Can be programmed to be 50% or 80% of 3.3 V.
Ground Signal			
GROUND	77	Ground	**Ground.** Connect the device paddle to ground on the PCB.

2.4 Electrical Characteristics

2.4.1 Power Supplies

Table 4. General

Parameter	Minimum	Nominal	Maximum	Unit	Comments
1.8 V supply voltage	1.71	1.8	1.89	V	VDD, VDDO
3.3 V supply voltage	3.15	3.3	3.45	V	AVDDH, AVDDH_HP, DVDDH, VDDO
Speaker driver supply voltage 5 V mode 3.3 V mode	 4.75 3.15	 5.0 3.3	 5.25 3.45	V	AVDD_CLDL, AVDD_CLDR

2.4.2 Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Unit	Comments
1.8 V supply voltage	-0.4		1.98	V	VDD, VDDO
3.3 V supply voltage	-0.4		3.60	V	AVDDH, AVDDH_HP, DVDDH, VDDO
Speaker driver supply voltage 5 V mode 3.3 V mode	 -0.4 -0.4		 5.5 3.6	V	AVDD_CLDL, AVDD_CLDR
Pin Voltage					
Input or Hi-Z Output	-0.4		VDDO+ 0.4	V	
Storage Temperature Range	-40		150	°C	Non operating temperature
Operating Temperature Range	-40		85	°C	
Temperature	-40	27	125	°C	Junction temperature

GENERAL NOTES:

1. Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.These are stress ratings only and functional operation under these conditions or at any other condition beyond those indicated for normal operation is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.4.3 Analog Inputs and Outputs

Table 6. Line Inputs

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Gain	-34.5		12	dB	
Full scale input signal		1		Vrms	AC-coupled, 0 dB gain
Dynamic Range(1)		87		dBFS	A-weighted, 20 to 20 kHz
THD+N at -3 dB FS		-84		dBFS	20 to 20 kHz
Input resistance	5		15	kΩ	15k with 0 dB gain, 5k otherwise

Table 7. Mic Inputs

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Gain	0		42	dB	
Full scale input signal		1		Vrms	AC-coupled, 0 dB gain
Dynamic Range(1)		87		dBFS	A-weighted, 20 to 20 kHz Boost = 18 dB
THD+N at -3 dB FS		-80		dBFS	20 to 20 kHz Boost = 18 dB
Input resistance	5		15	kΩ	15k with 0 dB gain, 5k otherwise

Table 8. Sub Outputs

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Full scale output signal Single-ended mode Differential mode	 1	1	 2	Vrms	AC-coupled, programmable when differential
Output load	500			Ω	
Dynamic Range(1)	95			dBFS	A-weighted, 20 to 20 kHz
THD+N 500 Ω load, at -3 dB FS 10 kΩ load, at -3 dB FS			 -75 -85	dBFS	20 to 20 kHz
Crosstalk			-70	dB	

Table 9. Line Output

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Full scale output signal Single-ended mode Differential mode	 1	1	 2	Vrms	AC-coupled, programmable when differential
Output load	10			kΩ	
Dynamic Range(1)	92			dBFS	A-weighted, 20 to 20 kHz
THD+N at -3 dB FS			-85	dBFS	20 to 20 kHz into 10 kΩ load
Crosstalk			-70	dB	

Table 10. Headphone Output

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Full scale output signal		1.25		Vrms	
Output offset	-3	0	3	mV	
Output load	16	32		Ω	Can drive -3 dBFS into 16 Ω without clipping.
Dynamic Range(1)	95			dBFS	A-weighted, 20 to 20 kHz
THD+N at -3 dB FS			-80	dBFS	20 to 20 kHz into 32 Ω
Crosstalk			-70	dB	

Table 11. Charge Pump

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Input voltage	3	3.3	3.6	V	DVDDH
Output voltage	-2		-2.8	V	AVEE_CPUMP
Clock frequency		500		kHz	

Table 12. Speaker Output

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Full scale output signal 5 V mode 3.3 V mode		 2.8 2.1		Vrms	
Output load		4		Ω	
Dynamic Range(1)	85			dBFS	A-weighted, 20 to 20 kHz
THD+N at -3 dB FS			-60	dBFS	20 to 20 kHz into 4 Ω.

Table 13. Microphone Bias

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Output voltage	1.65		2.65	V	Programmable to be 50% or 80% of supply.

Table 14. Jack Sensing

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Input voltage	0		3.3	V	
Pad sampling interval		10		ms	
SAR clock rate		500		kHz	

Table 15. Monitor ADC

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Input voltage	0		3.3	V	

FOOTNOTES:

(1) Dynamic Range is the ratio of the full scale signal level to the RMS noise floor, in the presence of signal, expressed in dB FS. It should be measured by performing a THD+N measurement with a -60 dBFS signal.

(2) Performance data valid over full operating temperature range, -40 to 85 °C.

2.4.4 Digital Inputs and Outputs

Table 16. CX20709-21Z Digital I/O Pad Cells

3.3 V/V.1.8 V Input Pad Cells	
Signal Name	**Supply Level**
I2C_SPI_CSN	VDDO1=3.3V / 1.8V
I2S_PCM_1_RX_DAT	VDDO2=3.3V / 1.8V
I2S_PCM_2_RX_DAT	VDDO2=3.3V / 1.8V
PASS_THRU	VDDO2=3.3V / 1.8V
UART_RX	VDDO3=3.3V / 1.8V
RST_N	VDDO4=3.3V Schmitt & Pull-Up
TEST	VDDO4=3.3V
USB_5VDET	VDDO4=3.3V

3.3 V/V.1.8 V Output Pad Cells	
Signal Name	**Supply Level**
I2S_PCM_1_TX_DAT	VDDO2=3.3V / 1.8V
I2S_PCM_2_TX_DAT	VDDO2=3.3V / 1.8V
UART_TX	VDDO3=3.3V / 1.8V

I2C I/Os	
Signal Name	**Supply Level**
I2C_SPI_SCL	VDDO1=3.3V / 1.8V
I2C_SDA/SPI_MOSI	VDDO1=3.3V / 1.8V

3.3 V/1.8 V I/Os	
Signal Name	**Supply Level**
I2C_EN/MCLK	VDDO1=3.3V / 1.8V
I2S_PCM_1_CLK	VDDO2=3.3V / 1.8V
I2S_PCM_1_RX_WS	VDDO2=3.3V / 1.8V
I2S_PCM_1_TX_WS/ SPDIF_OUT	VDDO2=3.3V / 1.8V
I2S_PCM_2_WS	VDDO2=3.3V / 1.8V
I2S_PCM_2_CLK/DMIC_CLK	VDDO2=3.3V / 1.8V
GPIO_[4:0]	VDDO3=3.3V / 1.8V
KS[2:0]	VDDO3=3.3V / 1.8V
NVDAT	VDDO1=3.3V / 1.8V
NVCLK	VDDO1=3.3V / 1.8V
SPI_MISO	VDDO1=3.3V / 1.8V

Oscillator	
Signal Name	**Supply Level**
XTLI	VDDO4=3.3V
XTLO	VDDO4=3.3V

USB I/O Pads	
Signal Name	**Supply Level**
USB_DP	VDDO4=3.3V
USB_DM	VDDO4=3.3V

The above table lists all CX20709-21Z digital I/O pad cells. Their electrical characteristics are listed in Section 2.4.4.1.

2.4.4.1 3.3 V/1.8 V I/Os: I2C_EN/MCLK,I2S_PCM_1_CLK, I2S_PCM_1_RX_WS, I2S_PCM_1_TX_WS/ SPDIF_OUT, I2S_PCM_2_WS, I2S_PCM_2_CLK/ DMIC_CLK, GPIO_[4:0], KS[2:0], NVDAT, NVCLK, SPI_MISO

NOTE: 3.3V/1.8V interface levels. These pads are not 5 V-tolerant.

Table 17. 3.3 V I/O Electrical Characteristics

		Minimum	Maximum	Units	Conditions[1]
Output Mode					OEN = 0
Output Low Voltage	VOL		0.4	VDC	IOL = + 9.2 mA
Output High Voltage	VOH	VDDO-0.4		VDC	IOH = –9.2 mA
Output Impedance (2)	Z7	12	45	Ω	
Input Mode					
Input Low Voltage - TTL	VIL		0.8	VDC	
Input High Voltage - TTL	VIH	2.0		VDC	
Input Current	IIL	–1	1	μA	OEN = 1

GENERAL NOTES: VDDO= 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = -40C to +125C.

Table 18. 3.3 V I/O Switching Characteristics

		C_L=7 pF	C_L=20 pF	C_L=50 pF	Units	Conditions[1]
Max Slew Rate (3)	SR7	6.2	3.1	1.8	V/ns	
Max Transition Time (3)	tT7	0.7	1.2	2.4	ns	

GENERAL NOTES:
1. VDDO= 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = -40C to +125C.
2. Slew rates and transition times are for the voltage transition between 25% and 75% of VDDO.

Table 19. 1.8 V I/O Electrical Characteristics

		Minimum	Maximum	Units	Conditions[1]
Output Mode					OEN = 0
Output Low Voltage	VOL7		0.45	VDC	IOL = +5.7mA
Output High Voltage	VOH7	VDDO-0.45		VDC	IOH = –5.7 mA
Output Impedance(2)	Z7	12	95	Ω	
Input Mode					
Input Low Voltage - CMOS	VILC	0	35	%VDDO	
Input High Voltage-CMOS	VIHC	65	100	%VDDO	
Input Current	IIL	-1	1	µA	OEN=1
GENERAL NOTES: VDDO= 1.65 V to 1.95 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.					

Table 20. 1.8 V I/O Switching Characteristics

		C_L=7 pF	C_L=20 pF	C_L=50 pF	Units	Conditions[1]
Max Slew Rate (3)	SR7	2.1	1.2	0.7	V/ns	
Max Transition Time (3)	tT7	0.9	1.5	3	ns	

GENERAL NOTES:
1. OEN is internally driven by CX20709-21Z.
2. Output impedances are for reference only, they are not tested.
3. Switching characteristics are for reference only, they are not tested.
4. VDDO= 1.65 V to 1.95 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.
5. Slew rates and transition times are for the voltage transition between 25% and 75% of VDD.

2.4.4.2 3.3 V/1.8 V Output Pad Cells: I2S_PCM_1_TX_DAT, I2S_PCM_2_TX_DAT, UART_TX, SPI_MISO

NOTE: 3.3 V/1.8 V interface levels. These pads are not 5 V-tolerant.

Table 21. 3.3 V Output Pad Electrical Characteristics

		Minimum	Maximum	Units	Conditions[1]
Output Mode					
Output Low Voltage	VOL		0.4	VDC	IOL = +9.2 mA
Output High Voltage	VOH	VDDO-0.4		VDC	IOH = –9.2 mA
Output Impedance (2)	Z7	12	45	Ω	
GENERAL NOTES: VDDO = 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.					

Table 22. 3.3 V Output Pad Switching Characteristics

		C_L = 7 pF	C_L = 20 pF	C_L = 50 pF	Units	Conditions[1]
Max Slew Rate (3)	SR7	6.2	3.1	1.8	V/ns	
Max Transition Time (3)	tT7	0.7	1.2	2.4	ns	

GENERAL NOTES:
1. VDDO= 3.0V to 3.6V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.
2. Slew rates and transition times are for the voltage transition between 25% and 75% of VDDO.

Table 23. 1.8 V Output Pad Electrical Characteristics

		Minimum	Maximum	Units	Conditions[1]
Output Mode					
Output Low Voltage	VOL7		0.45	VDC	IOL =+ 5.7 mA
Output High Voltage	VOH7	VDDO-0.45		VDC	IOH = -5.7 mA
Output Impedance (2)	Z7	12	95	Ω	
GENERAL NOTES: VDDO= 1.65 V to 1.95 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.					

Table 24. 1.8 V Output Pad Switching Characteristics

		C_L = 7 pF	C_L = 20 pF	C_L = 50 pF	Units	Conditions[1]
Max Slew Rate (3)	SR7	2.1	1.2	0.7	V/ns	
Max Transition Time (3)	tT7	0.9	1.5	3	ns	

GENERAL NOTES:
1. VDDO= 1.65V to 1.95V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.
2. Slew rates and transition times are for the voltage transition between 25% and 75% of VDDO.
3. Output impedances are for reference only, they are not tested.
4. Switching characteristics are for reference only, they are not tested.

2.4.4.3 3.3 V/1.8 V Input Pad Cells: I2C_EN, I2C_SPI_CSN, I2S_PCM_1_RX_DAT, I2S_PCM_2_RX_DAT/ DMIC_IN/SPDIF_IN, PASS_THRU, UART_RX

NOTE: 3.3 V/1.8 V interface levels. These pads are not 5 V-tolerant.

Table 25. 3.3 V Input Pad Cells Electrical Characteristics

		Minimum	Maximum	Units
Input Mode				
Input Low Voltage - TTL	VIL	0	0.8	VDC
Input High Voltage - TTL	VIH	2.0	VDDO	VDC
Input Current	IIL	–1	1	µA

GENERAL NOTES: VDDO = 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.

Table 26. 1.8 V Input Pad Cells Electrical Characteristics

		Minimum	Maximum	Units
Input Mode				
Input Low Voltage - CMOS	VILC	0	35	%VDDO
Input High Voltage- CMOS	VIHC	65	100	%VDDO
Input Current	IIL	–1	1	µA

GENERAL NOTES: VDDO= 1.65 V to 1.95 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C

2.4.4.4 Input Pad Cells: TEST, USB_5VDET (VDDO4=3.3V)

NOTE: 3.3 V interface levels. These pads are not 5 V-tolerant.

Table 27. 3.3 V Input Pad Cells Electrical Characteristics

		Minimum	Maximum	Units
Input Mode				
Input Low Voltage - TTL	VIL	0	0.8	VDC
Input High Voltage - TTL	VIH	2.0	VDDO	VDC
Input Current	IIL	–1	1	μA
GENERAL NOTES: VDDO = 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.				

2.4.4.5 RST_N (3.3 V Input with Schmidt and Pull-Up)

RST_N is a relatively low speed input pad cell with Schmitt trigger (hysteresis) input receiver.

Features:

- 3.3 V interface level. These pads are not 5 V-tolerant.
- Weak pull-up 3.3 V operation.

Table 28. 3.3 V RST_N Electrical Characteristics

		Minimum	Maximum	Units	Conditions (1)
Input Mode					
Input Low Voltage - Hysteresis	VILS	0	30	%VDDO	
Input High Voltage - Hysteresis	VIHS	70	0	%VDDO	
Input Hysteresis	VHYS	0.5		VDC	
Input Current - Pull-Up2	IPU2	–30	–6	μA	VIN=VSS
Pull-Up Resistance2	RPU2	130	315	kΩ	VIN=VSS

GENERAL NOTES:
1. VDDO = 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.
2. Input pad with hysteresis and internal weak pull-up.

2.4.4.6 XTLI/XTLO (XTAL Oscillator)VDDO4 = 3.3V

3.3 V Crystal Oscillator Pad Cell

XTLI

XTLO

Features:

- Input receiver from XTLO to chip core has 150-250 mV hysteresis to help prevent parasitic feedback paths.
- Internal 1MΩ feedback resistor from XTLO to XTLI.

Table 29. XTLI/XTLO Electrical Characteristics

		Minimum	Maximum	Units	Conditions (1)
Output					
XTLO Output Low Voltage	VOL		0.4	VDC	XTLI=VDDO IOL=+1.5 mA
XTLO Output High Voltage	VOH	VDDO-0.4		VDC	XTLII=VSS IOH=-7.3 mA
XTLO Bias Voltage	VBXO	20	7.5	%VDDO	XTLI=HiZ IOL=IOH=0
XTLO Output Impedance (2)	Z0	300	1200	%VDDO	XTLI=VBXI XTLO=VBXO± 50 mV
Input					
XTLI Input Low Voltage	VIL	0	30	%VDDO	
XTLI Input High Voltage	VIH	70	100	%VDDO	
XTLI Low Input Current	IIL	–8	–1	μA	XTLI=VSS (XO=VDDO)
XTLI High Input Current	IIH	1	8	μA	XTLI=VDDO (XO=VSS)
XTLI Bias Voltage	VBXI	45	55	%VDDO	XTLI=HiZ IOL=IOH=0
XTLI Input Capacitance (2)	CIN		2	pF	XTLI=VBXI

GENERAL NOTES:
1. 3.6 V unless otherwise specified. Junction Temperature Tj = no external components.
2. Output impedance and input capacitance are for reference only, they are not tested.
3. The input capacitance is for the die only and does not include the capacitance of the packaging.

2.4.4.7 I²C I/Os: I2C_SPI_SCL, I2C_SDA/SPI_MOSI

Features:

- 3.3 V/1.8 V interface levels. These pads are not 5 V-tolerant
- Supports Standard and Fast Modes; not Hs Mode.
- Select either I²C mode or SPI mode.

Note: VBUS is the voltage to which the external pull-up for the I²C bus is connected. VBUS must be 3.3 V.

I²C	Conditions
0 (SPI Mode)	The output buffer is push-pull and will drive PAD both low and high.
	The output buffer has normal GPIO delay.
	The output buffer has normal GPIO rise and fall times.
	The input receiver has normal GPIO delays.
	The input has reduced input levels and hysteresis so that it meets VIL>30% VDDO and VIH<70% VDDO for both 3.3 V±10% and 1.8 V±10% VDDO ranges.
1 (I²C mode)	The output buffer is open drain and will only drive PAD low.
	The output buffer has a long delay.
	The output buffer has a long fall time as required by the i²c specification.
	The input receiver has a glitch rejection filter to reject pulses less than 50 ns as required by the i²c specification. This makes the input receiver delay very long; at least 50 ns and up to about 150 ns for the 3.3 V operation. Maximum delay for the 1.8 V operation can be as high as 400 ns.
	The input levels are consistent with the i²c specification.

Table 30. 3.3 V I2C_SPI_SCL, I2C_SDA/SPI_MOSI Electrical Characteristics

		Minimum	Maximum	Units	Conditions (1)
Output Mode					OEN=0
Output Low Voltage	VOL0		0.4	VDC	I2C=X IOL=+3.0 mA
Output High Voltage	VOH0	VDDO-0.4		VDC	I2C=0 IOH=-3. 0 mA
Output Impedance (2)	Z0		45	Ω	I2C=0
Maximum SSO (per VDDO/VSSO pin)	SSO		6		I2C=0
Input Mode					OEN=1
Input Low Voltage	VIL	0	30	%VDDO	I2C=0
I^2C Input Low Voltage – 3.3 V Bus	VIL3	0	30	%VDDO	I2C=1 VDDO=VBUS=3.3V ±10%
Input High Voltage	VIH	70	100	%VDDO	I2C=0
I^2C Input High Voltage - 3.3 V Bus	VIH3	70	100	%VDDO	I2C=1 VDDO=VBUS=3.3V ±10%
Input Hysteresis	VHYS	5		%VDDO	
Input Hysteresis - 3.3 V Bus	VHYS3	5		%VDDO	I2C=1 VDDO=VBUS=3.3V ±10%
Input Current	ILL	–1	1	μA	I2C = 1 VIN=VSS
GENERAL NOTES: VDDO= 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C					

Table 31. 1.8 V I2C_SPI_SCL, I2C_SDA/SPI_MOSI Electrical Characteristics

		Minimum	Maximum	Units	Conditions (1)
Output Mode					OEN=0
Output Low Voltage	VOL1		0.2VDDO	VDC	I2C=X IOL=+3.0 mA
Output High Voltage	VOH1	VDDO-VOL1		VDC	I2C=0 IOH=-3. 0mA
Output Impedance (2)	Z0		96	Ω	I2C=0
Maximum SSO (per VDDO/VSSO pin)	SSO		6		I2C=0
Input Mode					OEN=1
Input Low Voltage – Hysteresis	VIL	0	30	%VDDO	I2C=0
I^2C Input Low Voltage - Hysteresis 1.8 V Bus	VIL1PS	0	30	%VDDO	I2C=1 VDDO=VBUS=1.8V ±10%
Input High Voltage - Hysteresis	VIH	70	100	%VDDO	I2C=0
I^2C Input High Voltage - 1.8 V Bus	VIH3	70	100	%VDDO	I2C=1 VDDO=VBUS=1.8V ±10%
Input Hysteresis	VHYS	10		%VDDO	
Input Hysteresis - 1.8 V Bus	VHYSIPS3	10		%VDDO	I2C=1 VDDO=VBUS=3.3V ±10%
Input Current	ILL	–1	1	μA	I2C = 1 VIN=VSS

GENERAL NOTES:

1. OEN & I^2C are internal signals that control the mode of the driver and receiver.
2. Output impedances are for reference only, they are not tested.
3. VDDO= 1.65V to 1.95V unless otherwise specified. Junction Temperature Tj = -40 ^oC to +125 ^oC.
4. OEN: Active Low Output enable for the 3-state buffer driving PAD, controlled by core logic. Not accessible to user.
5. I^2C: Mode control; selects either I^2C mode or GPIO mode.

2.4.4.8 USB I/O Pads: USB_DP, USB_DM

USB_DP, USB_DM is a full-speed USB pad cell.

Features:

- Designed for Rs = 22 Ω (±1% tolerance) external series resistor on DM and DP.
- Internally designed, selectable Pull-up Resistor (Rpu) to VDDO on DP

Table 32. USB I/O Rpu Control

Bus State	Minimum (Ω)	Typical (Ω)	Maximum (Ω)	Conditions (3)
Transmitting		OPEN		
Receiving	1425	2237	3090	
Idle	900	1237	1575	

***Table 33. USB I/O Electrical Characteristics** (1 of 2)*

		Minimum	Maximum	Units	Conditions (1)
Output Mode					TXEN=1
Output Low Voltage	VOL0		0.4	VDC	IOL= +10 mA
USB “DC Drive”	VOLDC		0.3	VDC	R=1.5 kΩ to VDDO
USB “DC Drive” (2)	VOLDC1		0.3	VDC	IOL= +2.32 mA
USB “AC Drive“(2)	VOLAC		27	%VDDO	IOL=VDDO×+6.10 mA
Output High Voltage	VOH	VDDO-0.4		VDC	IOH= –10 mA
USB “DC Drive”	VOLDC	2.8		VDC	R=15 kΩ to VSS
USB “DC Drive” (2)	VOLDC1	2.8		VDC	IOH= -0.20 mA
USB “AC Drive “(2)	VOHAC	73		%VDDO	IOH=VDDO × –6.10 mA
Output Impedance (3)	ZO	14	36	Ω	Rs = 0
Output Impedance (2) (3)	Z22	28	44	Ω	
Single-Ended Inputs					
Input Low Voltage	VIL	0	0.8	VDC	
Input High Voltage	VIH	2.0	VDDO	VDC	
Differential Inputs					
Differential Input Voltage	VDI	0.2		VDC	
Common Mode Voltage	VCM	0.8	2.5	VDC	

Table 33. USB I/O Electrical Characteristics *(2 of 2)*

		Minimum	Maximum	Units	Conditions (1)
Input Low Condition	VCM_min < DP < DP+VDI < DM < VCM_max				
Input High Condition	VCM_min < DM < DM+VDI < DP < VCM_max				
Input Current		–1	1	μA	TXEN = 0
GENERAL NOTES: VDDO= 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C					

NOTES:

1) Rpu and TXEN are internal signals that control the mode of the driver, receiver (s) and pull-up resistor. Not accessible to user.

2) Based on USB Full Speed Mode V/I Characteristics.

3) Output impedance is for reference only and is not tested.

4) TXEN INPUT Output enable for the 3-state buffer driving DM and DP. Active high. Controlled from the chip core. Not accessible to user.

5) Rpu INPUT Pull-up resistor select from the chip core. Not accessible to user.

6) VDDO = 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = -40 °C to +125 °C.

7) Slew rates and transition times are for the voltage transition between 25% and 75% of VDDO.

2.4.5 CX20709-21Z Power Consumption

Table 34. CX20709-21Z Power Consumption *(1 of 2)*

Scenario	AVDDH (3.3 V) (mA)	DVDDH (3.3 V) (mA)	AVDDH_HP (3.3 V) (mA)	AVDD_CLASSD (5 V) (mA)	DVDD (1.8 V) (mA)	DVDDO (3.3 V) (mA)	Power (mW)
USB							
Suspend	1.28	0.00	0.00	0.00	0.20	0.90	7.55
Idle	2.51	0.31	0.21	1.73	51.20	5.56	129.17
Mono Record from Microphone NR on, AGC on	9.69	0.28	0.21	1.73	73.80	6.67	197.10
Stereo Record from Line In NR on	8.26	0.31	0.21	1.73	73.80	6.49	191.85
Full Duplex Mono mic record, playback to HP 5 mW/ch (0.405 mVrms@33 Ω) NR on, AGC on	12.97	15.87	14.95	1.73	89.40	6.56	335.77
Stereo Playback to Headphone Zero Amplitude Disabled AGC, NR, AEC	6.15	8.15	7.26	1.73	68.00	5.59	220.67
Stereo Playback to Headphone 5mW per channel(.40 5mV@33 Ω) Disabled AGC, NR, AEC	6.15	16.05	15.10	1.73	70.80	5.56	277.58
Stereo Playback to Headphone 10mW per channel(.575 mV@33 Ω) Disabled AGC, NR, AEC	6.15	20.64	19.69	1.73	68.70	5.56	304.10
Stereo Playback to Headphone 24 mW per channel (0.89 Vrms@33 Ω) Disabled AGC, NR, AEC	6.05	29.46	28.49	1.73	68.20	5.56	360.99
Stereo Playback to Line Out 1.0 Vrms sine wave per channel Disabled AGC, NR, AEC	5.49	0.31	0.21	1.73	68.10	5.64	169.66
Stereo Playback to Class D Zero Signal Disabled AGC, NR, AEC	14.54	0.95	0.21	14.00	67.90	5.59	262.45
Stereo Playback to Class D 258 mW/channel, 1000 Hz, Sine Wave Disabled AGC, NR, AEC	14.23	0.95	0.21	136.67	67.90	5.62	874.85
Stereo Playback to Class D 1.0 W per channel, 497 Hz, Square Wave Disabled AGC, NR, AEC	14.56	0.92	0.18	384.67	67.40	0.00	2096.35

Table 34. CX20709-21Z Power Consumption *(2 of 2)*

Scenario	AVDDH (3.3 V) (mA)	DVDDH (3.3 V) (mA)	AVDDH_HP (3.3 V) (mA)	AVDD_CLASSD (5 V) (mA)	DVDD (1.8 V) (mA)	DVDDO (3.3 V) (mA)	Power (mW)
I^2S							
Suspend Sleep Enabled (0x117E, Bit 7 = 1)	1.95	0.31	0.21	1.73	0.20	0.59	19.10
Suspend Deep Sleep Enabled (0x117E, Bits 6 and 7 = 1)	1.95	0.31	0.21	1.73	0.20	0.59	19.10
Idle All streams off	2.08	0.31	0.21	1.73	65.90	5.28	153.26
Idle All streams off, CPX optimized 0x117E = 0x24 (CPX = 3 MHz)	2.08	0.31	0.21	1.73	52.00	4.95	127.14
Stereo Record from Microphone Stream 2 --> VP --> Stream 5, Other streams off NR on, AGC on	11.85	0.31	0.21	1.73	84.20	5.33	218.61
Stereo Record from Line In, Single Ended Stream 1 --> VP --> Stream 5, Other streams off	10.79	0.31	0.21	1.73	86.00	5.28	218.21
Full Duplex Microphone to I2S1, I^2S to HP 5mW per channel (0.405 mVrms@33 Ω) AGC on, NR on	12.97	15.85	14.92	1.73	88.70	5.23	329.94
Stereo Playback to Headphone Zero Amplitude Disabled AGC, NR, AEC	6.18	8.15	7.26	1.73	66.40	5.28	216.86
Stereo Playback to Headphone 10mW per channel (0.575mV@33 Ω) Disabled AEC and NR	6.18	20.67	19.69	1.73	67.40	5.23	300.83
Stereo Playback to Headphone 24 mW per channel (0.89 Vrms@33 Ω) Disabled AGC, NR, AEC	6.15	29.46	28.49	1.73	67.40	5.21	358.70
Stereo Playback to Line Out 1.0 Vrms sine wave per channel Disabled AGC, NR, AEC	5.79	0.28	0.21	1.73	67.40	5.31	168.23
Stereo Playback to Class D Zero Signal Disabled AGC, NR, AEC	14.54	0.95	0.21	14.00	66.20	5.26	258.29
Stereo Playback to Class D 254 mW (1.009 Vrms) per channel Disabled AGC, NR, AEC	14.54	0.95	0.21	130.67	67.20	5.26	843.42
Stereo Playback to Class D 2.0 W (2.83 Vrms), per channel Disabled AGC, NR, AEC	14.51	0.92	0.18	1018.00	67.50	5.36	5280.72

GENERAL NOTES:

1. Typical condition: 25 °C, 1.8 V, 3.3 V, and 5.0 V
2. Class-D speaker load: 4 Ω
3. All power figures include the 4 Ω external speaker load and/or the 33 Ω headphone load.

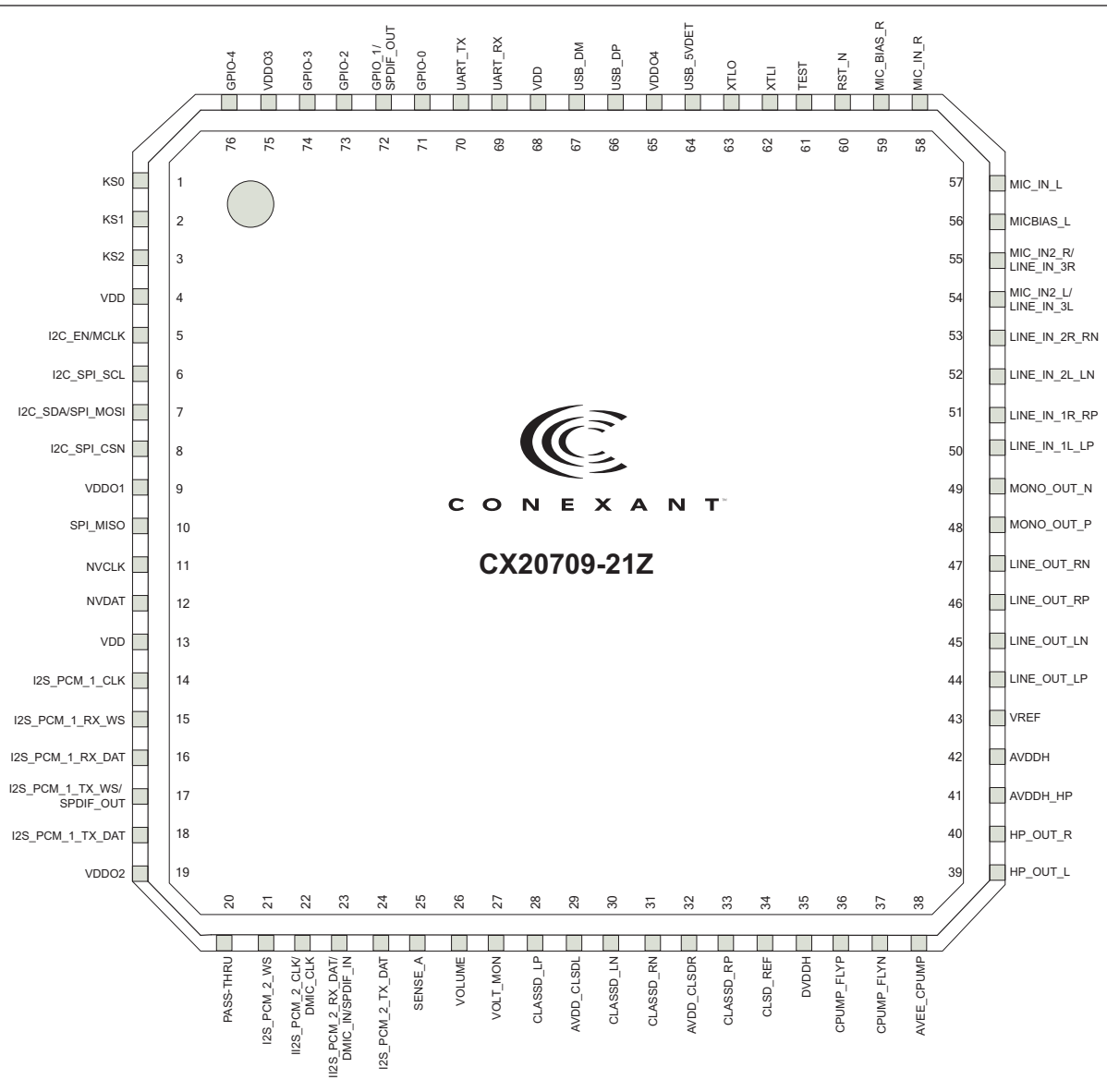
2.4.6 CX20709-21Z Power Sequencing

Please refer to APN-202411-XXX, Application Note 8 - *CX2070x Layout Guide* for CX20709-21Z power sequencing.

2.5 CX20709-21Z Pin Diagram

Figure 4 provides a diagram of the 76-pin QFN.

Figure 4. CX20709-21Z 76-Pin QFN Diagram

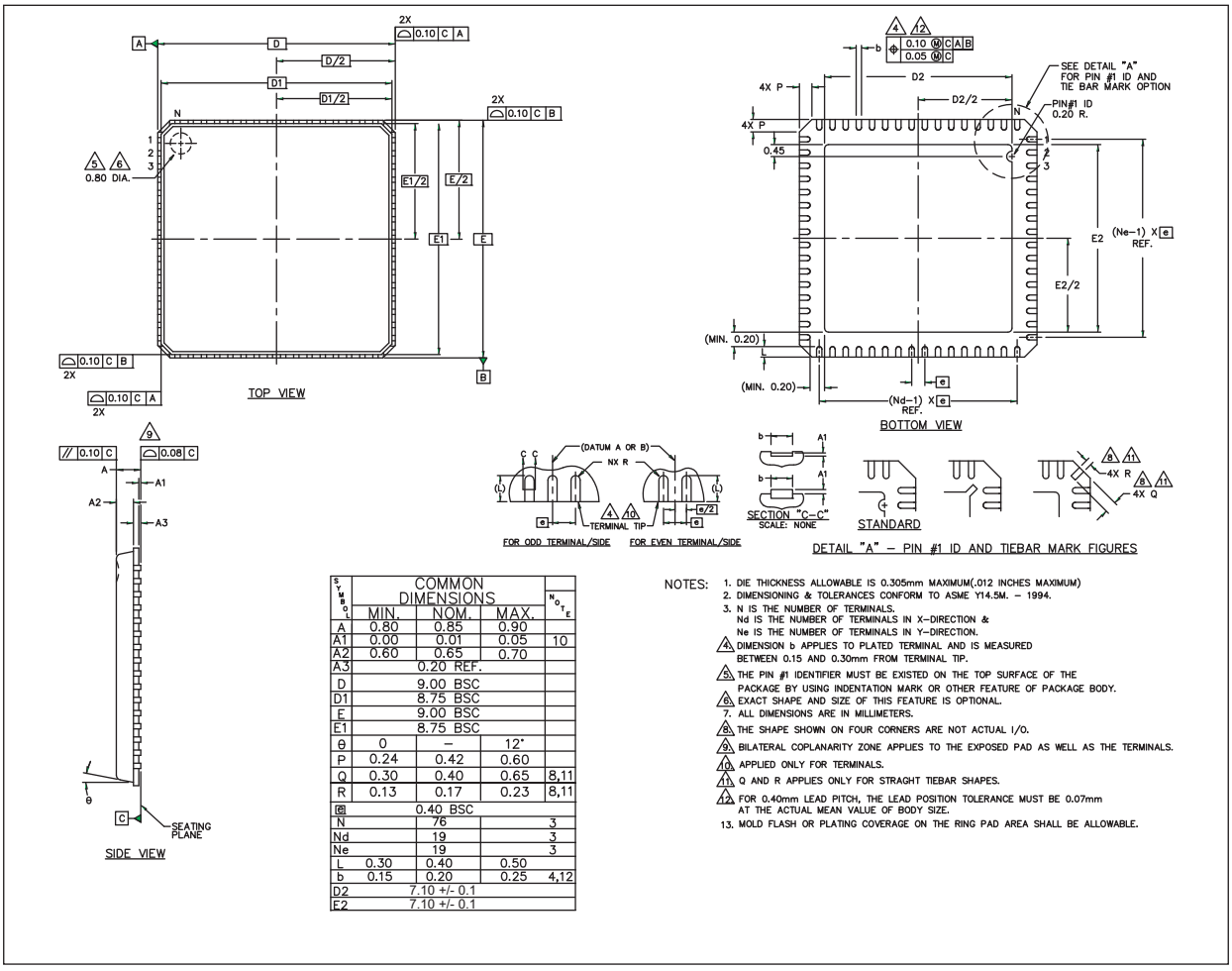


GENERAL NOTE: Pin 77 is the ground paddle and should be tied to system ground.

2.6 CX20709-21Z Package Dimensions

Figure 5 provides the package dimensions.

Figure 5. Package Dimensions: 76-Pin QFN



SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	10
A2	0.60	0.65	0.70	
A3		0.20 REF.		
D		9.00 BSC		
D1		8.75 BSC		
E		9.00 BSC		
E1		8.75 BSC		
θ	0	–	12°	
P	0.24	0.42	0.60	
Q	0.30	0.40	0.65	8,11
R	0.13	0.17	0.23	8,11
e		0.40 BSC		
N		76		3
Nd		19		3
Ne		19		3
L	0.30	0.40	0.50	
b	0.15	0.20	0.25	4,12
D2		7.10 +/- 0.1		
E2		7.10 +/- 0.1		

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
10. APPLIED ONLY FOR TERMINALS.
11. Q AND R APPLIES ONLY FOR STRAGHT TIEBAR SHAPES.
12. FOR 0.40mm LEAD PITCH, THE LEAD POSITION TOLERANCE MUST BE 0.07mm AT THE ACTUAL MEAN VALUE OF BODY SIZE.
13. MOLD FLASH OR PLATING COVERAGE ON THE RING PAD AREA SHALL BE ALLOWABLE.

2.6.1 Package Thermal Data

Table 35. Package Thermal Data

Die Power (W)		2.0	
Ambient Temperature (°C)		85	
Airflow (m/s)	**T_J (°C)**	**Θ_{JA} (°C/W)**	**Θ_{JC} (°C/W)**
0	122.4	18.7	6.6

Table 36. Test Board and Conditions for Thermal Data

Size (in inches)	7” x 8”
Motherboard Thickness (in inches)	0.062”
Motherboard Material	FR4
Number of Layers in Motherboard	4

3 CX20709-21Z Device Description

3.1 Analog Audio Input Paths

3.1.1 Analog-Digital Converters

Four identical Analog-Digital Converters (ADCs) are grouped into two stereo pairs, one for microphone in and another one that can be configured to support either microphone in or line in. Sample widths supported are 24 or 16 bits at sample rates of 8k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, 88.2k and 96k. A digital PGA with a gain range of -74 dB to +5 dB in 1 dB steps is at the output of each ADC.

3.1.2 Line Inputs

Four analog input buffers with adjustable gain settings range from -34.5 dB to +12 dB in 1.5 dB steps (32 settings). With the gain set at 0 dB, the line input buffers are capable of accepting a 1 V RMS input signal. These input buffers are arranged in two groups of three each. Each group feeds an ADC input multiplexer and mixer. The multiplexer can select between a mix of the input channels or any individual channel. Mixer inputs can be individually muted. Two of the buffers in each group share a common single-ended or differential mode control.

The line inputs have the following configuration options:

- Power on/off for any individual buffer
- Power on/off for the mixer/multiplexer
- Multiplexer input source select
- Individual buffer gain setting
- Line Input 2 Analog Pass Through to HP can be supported via API register control

3.1.3 Microphone Input

Up to four analog input buffers with adjustable gain settings range from 0 dB to 42 dB in 6 dB steps (eight settings). With the gain set at 0 dB, the microphone buffer can accept a 1 V RMS input signal.

NOTE: Line- in and mic-in support options:

a. Support 4 analog mic-in and no line-in.

b. Support up to 3 single-ended line-in with no mic-in

c. Support up to 2 single-ended line-in and 1 stereo mic-in

3.1.4 Microphone Bias Generator

The bias generator is capable of generating two programmable bias voltages, 2.64 V or 1.65 V (80% or 3.3 V or 50% of 3.3 V), to support two analog microphones. The bias voltages can be disabled, which puts the bias buffer in a low-power and high-impedance mode. The buffer output pads allow for a full 1 V RMS swing below ground without any impedance change.

3.1.5 Jack Sense

Jack sense is provided by a 4-bit Successive Approximation Register (SAR) and an externally located resistor divider network. Grounding a resistor indicates that an audio device is connected to the corresponding port. It is possible to map the four jack sense bits to any possible input or output port. The debounce time is adjustable with a default of 250 ms.

3.1.6 Monitor ADC

The monitor ADC consists of an input multiplexer and a 12-bit ADC. The multiplexer selects between two pins. One pin is intended to monitor a potentiometer connected to 3.3 V. The voltage reading is translated, by the controller firmware, into volume settings for the main stereo outputs. The second pin is intended for monitoring battery voltage levels. The measurement range is from 0 to 3.3 V. Sample conversion is initiated by the system controller.

3.2 Analog Audio Output Paths

3.2.1 Digital-Analog Converters

Three identical Digital-Analog Converters (DACs) are grouped as one stereo pair and a single DAC. Sample widths supported are 24 or 16 bits at sample rates of 8k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, 88.2k, and 96k. A digital PGA with a gain range of -74 dB to +5 dB in 1 dB steps is at the input of each DAC.

Twelve bi-quad filters are on the output of each DAC. Ten of the bi-quads are used to create a spectrum equalizer and two are available to create a high pass, low pass, or band pass filter to support 2.1 streaming (left, right and sub woofer). The coefficients for all twelve are user accessible. Also, at the output of each DAC chain, a sample peak accumulator is used for dynamic range compression feedback.

3.2.2 Differential/Single-ended Line Out (Stereo)

The line outputs can be configured for either single-ended or differential output. They can drive 1 V RMS into a 10k load and meet the DAC path performance requirements specified in Section 2.4. The line outs have the following configuration options:

- Power on/off
- Differential or single-ended operating mode
- 1 or 2 V RMS output level (differential mode)
- Mute on/off

3.2.3 2.5 W Class-D

These differential output drivers make up the CLASS-D speaker output. They can drive up to 2.5 W (when device is powered by fixed +5 V) into a rated 4 Ω speaker (3.2 Ω DC) and meet the speaker path performance requirements specified in Section 2.4. If powered by less than +5 V, gains and overcurrent thresholds must be adjusted accordingly. The Class-D outputs have the following configuration options:

- Power on/off
- 2.5 W per channel @ 5 V; 1.0 W per channel @ 3.3 V
- Spread spectrum, low EMI clocking
- Single channel operation
- Over current protection, under voltage protection and over temperature protection

3.2.4 Capless Headphone Driver

Two output drivers can be configured for either line out (10 kΩ load) or headphone out (32 Ω load). They can drive 50 mW into an 32 Ω load or 1 V RMS into a 10 kΩ load and meet the DAC path performance requirements specified in Section 2.4. The Capless Headphone outputs have the following configuration options:

- Power on/off
- Mute on/off

3.2.5 Differential/Single-ended Line Out (Mono)

This output driver can be configured for either single-ended or differential output. It is intended to act as a line output and can drive 1 V RMS into a 10k load and meet the DAC path performance requirements specified in Section 2.4. It can also drive a 600 Ω audio coupling transformer directly in differential mode. The mono line out has the following configuration options:

- Power on/off
- Differential or single-ended operating mode
- 1 V (Single-ended) or 2 V RMS output level (Differential Mode)
- Mute on/off.

3.3 Digital Audio

3.3.1 USB

The USB interface is a 2.0 full-speed interface exposing a UAC compliant client. Stereo record and stereo playback are supported at all sample rates up to 96 kHz and bit widths up to 24 bits.

The USB client interface supports two endpoints.

- EPs:
  - 0: IN-Status, OUT-Control
  - 1: IN-ADC, OUT-DAC
  - 2: OUT-DAC
  - 4: IN-HID
- PLL/SRC solution for clock synchronization
- < 2.5 mA Suspend mode
- 48 MHz crystal clock source is required

3.3.2 5-Wire PCM/I^{2}S/SPDIF_OUT (Digital Port 1) Interface

This five pin interface has several modes of operation. The first mode is as a five-wire I^{2}S interface. The fifth wire in this case is an independently controlled transmit frame clock. This allows for independent but related sample rates to be sent and received from the I^{2}S port. For example, it is possible to set the bit clock to support a 48k sample rate for playback through a pair of DACs and simultaneously record a 16k sample rate stream from a pair of ADCs. This is because the 48k and 16k have an integer relationship. The receive and transmit frame signal can be independently programmed for different bit counts.

The second mode is a traditional four-wire I^{2}S or PCM interface with the transmit word select configured to be an independent SPDIF output.

The third mode is a four-wire PCM interface. The PCM interface supports up to two slots of active input and up to three slots of active output out from a range of 1 to 32 slots.

The I^{2}S or PCM can be configured for master or slave modes, meaning clocking and sync or frame signals can be internally or externally generated. The maximum frequency of an external clock with a 50 percent duty cycle is 12.288 MHz.

The I^{2}S interface supports left-justified and right-justified data formats. Both the I^{2}S and PCM interfaces send or receive the MSB first.

SPDIF clocking is always internally generated. The SPDIF engine supports 16 or 24-bit PCM samples as well as AC3 data streams. The SPDIF header information is fully programmable. Sample rates of 44.1k, 48k, and 96k are supported.

This interface shares its power source with the four-wire PCM/ I^{2}S interface to allow for 1.8 or 3.3 V signal levels. A pass through pin allows the interface to be shared with another I^{2}S device. In pass through mode the transmit data pin is driven by the pass through pin instead of the internal interface engine.

3.3.3 4-Wire PCM/I^{2}S/ SPDIF_IN/Digital Microphone (Digital Port 2) Interface

This is a traditional four wire I^{2}S or PCM interface. The PCM interface supports up to two slots of active input and up to three slots of active output out from a range of 1 to 32 slots.

The I^{2}S or PCM can be configured for master or slave modes, which means clocking and sync or frame signals can be internally or externally generated. The maximum frequency of an external clock with a 50 percent duty cycle is 12.288 MHz. The I^{2}S interface supports I^{2}S, left justified and right justified data formats. Both the I^{2}S and PCM interfaces send or receive the MSB first.

This interface shares the power source with the five wire PCM/ I^{2}S interface to allow for 1.8 or 3.3 V signal levels. A pass through pin allows the interface to be shared with another I^{2}S device. In pass through mode the transmit data pin is driven by the pass through pin instead of the internal interface engine.

NOTE: Standard CX2070x firmware supports 3.3V SPDIF_IN signaling. For 0.6V SPDF_IN signaling, contact your local Conexant sales office for firmware patch and reference schematic.

3.3.4 Digital Microphone Interface

CX20709-21Z supports both conventional analog microphones and digital microphones.

The DMIC_IN shares the input pin with Digital Port 2 and SPDIF_IN. Hence, when DMIC_IN is in use, the SPDIF_IN and the Digital Port 2 (PCM or I^{2}S) are not available.

The CX20709-21Z device features a stereo digital microphone interface, to which one or two digital microphones can be attached. The CX2070x device provides a clock to the digital microphones, at pin I2S_PCM_2_CLK/DMIC_CLK, and latches the data sent by the digital microphones at pin I2S_PCM_2_RX_DAT/SPDIF_IN/DMIC_IN. The digital microphone function shares those two pins with SPDIF and with the I^{2}S/PCM interface; neither SPDIF_IN nor I2S/PCM are available when the digital microphone is in use.

The incoming data from the microphones can be sent to either Stream 1 or Stream 2. For Stream 1, it is multiplexed with Line1/Line2/Mic2; for Stream 2, it is multiplexed with Mic1.

When using the digital microphone interface, there is an available gain boost ranging from 0 to 48 dB, in 6 dB steps.

Available digital microphone clock frequencies are 1.536 MHz, 3.072 MHz, and 12 MHz. The left-channel microphone data is latched on the falling edge of the clock, and sent by the microphone on the rising edge of the clock. Conversely, the right-channel microphone data is latched on the rising edge of the clock, and sent by the microphone on the falling edge of the clock.

The interface is controlled using Digital Microphone Control register 0x1247; see the *CX2070x API Host Document* for a detailed description.

Figure 6. Digital Microphone Interface

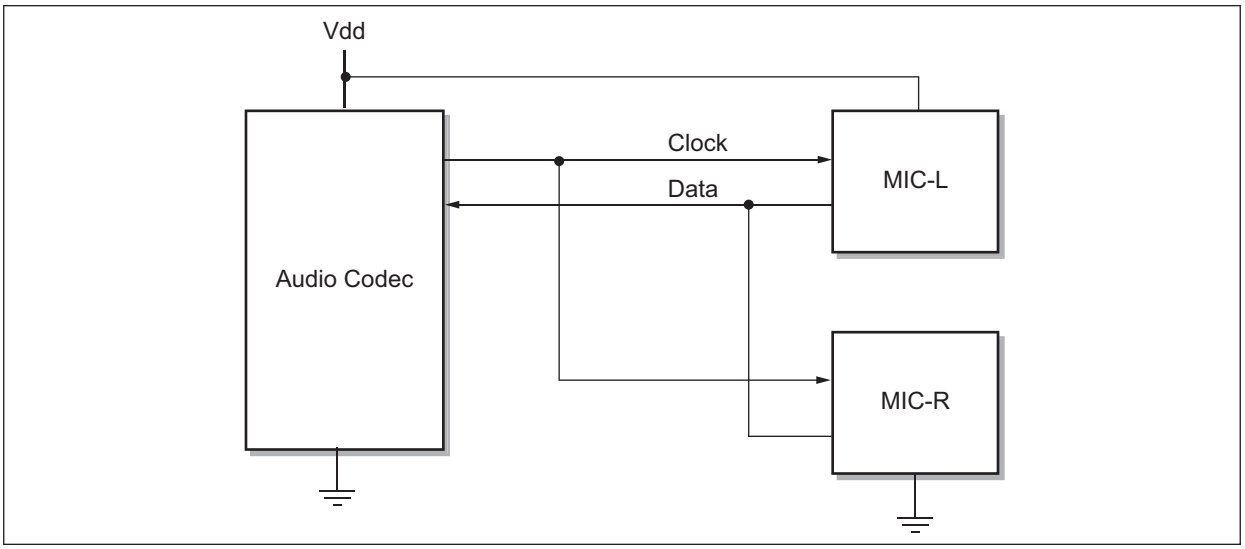


Figure 7. Digital Microphone Interface Timing

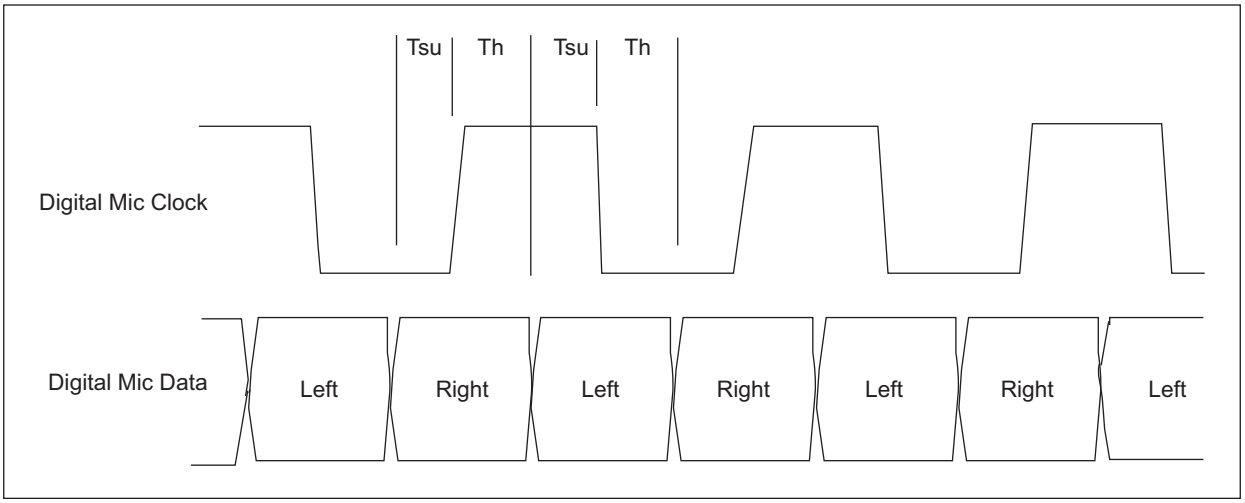


Table 37. Digital Microphone Interface Parameters

Parameter		Value	Units	Comments
Clock Frequency	F	1.536 3.072 12.00	MHz	
Output Low (max)	Vol	0.4	V	
Output High (min)	Voh	2.6	V	
Input Low (max)	Vil	0.94	V	
Input High (min)	Vih	1.20	V	
Setup (min)	Tsu	36	ns	The Setup and Hold parameters apply to both left channel (falling edge of clock) and right channel (rising edge of clock).
Hold (min)	Th	0	ns	

3.3.5 SPDIF Input Interface

For SPDIF input operation, see Section 3.3.2, 5-Wire PCM/I2S/SPDIF_OUT (Digital Port 1) Interface.

The SPDIF_IN shares the input pin with Digital Port 2 and Digital Mic. Hence, when SPDIF_IN is in use, the Digital Mic and the Digital Port 2 (PCM or I^2S) are not available.

3.3.6 I^2S Audio Interface Timing

The first digital port has five pins assigned to provide a bi-directional interface. They are CLK, TX_WS, TX_DAT, RX_WS, and RX DAT. (Refer to Table 38.) CLK can be either internally generated or externally supplied. Both TX_WS and RX_WS follow the direction programmed for CLK. If CLK is an input TX_WS and RX_WS are also inputs. If CLK is an output, TX_WS and RX_WS are also outputs. In Slave mode (CLK as input), we have:

- TX_WS and RX_WS are inputs.
- TX_WS & RX_WS are latched on the rising edge of CLK.
- TX_DAT is sent on the falling edge of CLK.
- RX_DAT is latched on the rising edge of CLK.

In Master mode (CLK as output), we have:

- TX_WS and RX_WS are outputs
- TX_WS & RX_WS are sent on the falling edge of CLK.
- TX_DAT is sent on the falling edge of CLK.
- RX_DAT is latched on the rising edge of CLK.

The second digital port has four pins assigned to provide a bi-directional interface. They are CLK, WS, TX_DAT and RX_DAT. (Refer to Table 38.) CLK can be either internally generated or externally supplied. WS follows the direction programmed for CLK. If CLK is an input, WS is also an input. If CLK is an output, WS is also an output. In Slave mode (CLK as input), we have:

- WS is an input.
- WS is latched on the rising edge of CLK.
- TX_DAT is sent on the falling edge of CLK.
- RX_DAT is latched on the rising edge of CLK.

In Master mode (CLK as output), we have:

- WS is an output.
- WS is sent on the falling edge of CLK.
- TX_DAT is sent on the falling edge of CLK.
- RX_DAT is latched on the rising edge of CLK.

Table 38. I^2S Audio Interface Parameters

Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
CLK	Frequency, CLK	Cl – 30 pF	256k		12.288	MHz
tsu1	Setup time, WS to CLK rising (in slave mode only)	14 pF	10			ns
th1	Hold time, WS from CLK rising (in slave mode only)	14 pF	5			ns
tsu2	Setup time, DAT to CLK rising	14 pF	10			ns
th2	Hold time, DAT from CLK rising	14 pF	5			ns
	WS frequency		8	48	96	kHz
	CLK duty cycle		40	50	60	%
	WS duty cycle		40	50	60	%
t_{D1}	Output delay time for TX_WS (for Digital Port 1)/ WS (for Digital Port 2) with respect to PCM[1,2]_CLK (in master mode only)	14 pF	—	—	5	ns
t_{D2}	Output delay time for PCM[1,2]_TXD with respect to PCM[1,2]_CLK	14 pF	—	—	12	ns

Figure 8. RX_WS/WS (Slave Mode) Setup and Hold

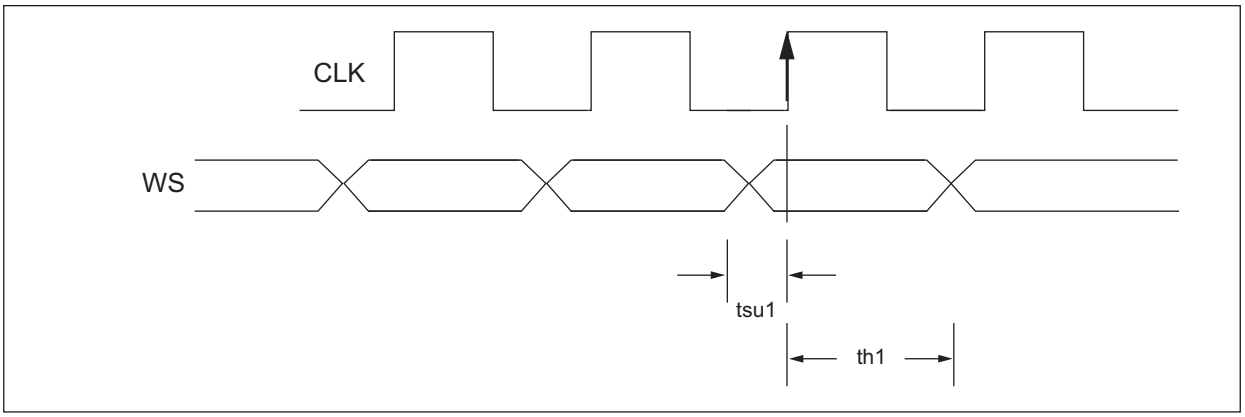


Figure 9. RX_DATA Setup and Hold

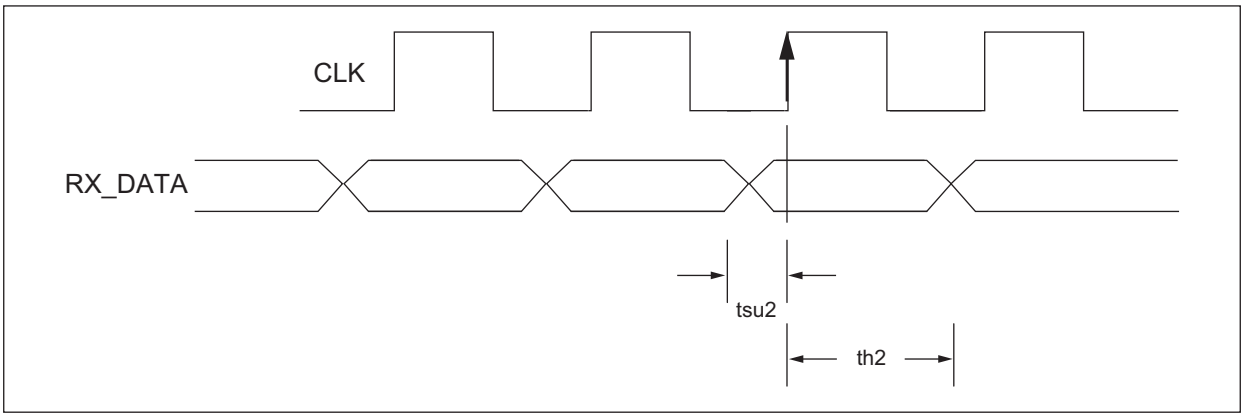
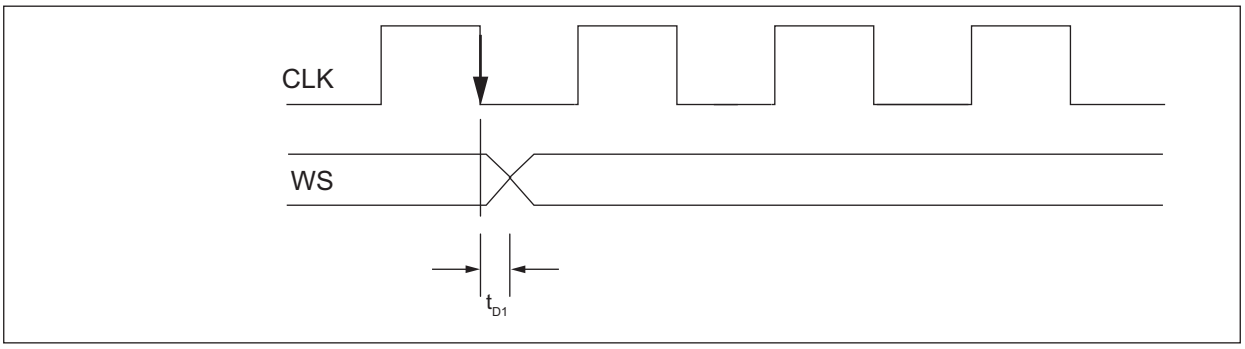
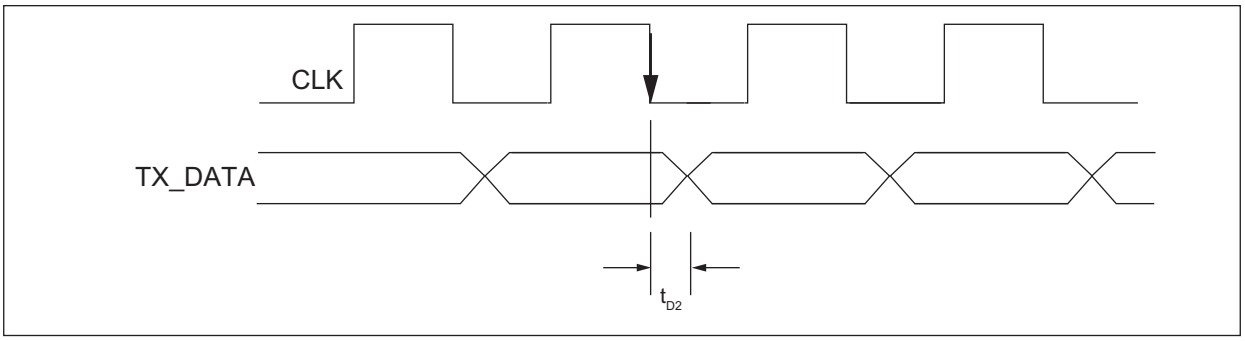


Figure 10. TX_WS /WS (Master Mode) Output Delay



NOTE: The I2S_PCM_1_CLK and I2S_PCM_2_CLK are hereinafter simply referred as CLK or BITCLK.

Figure 11. TX_DATA Output Delay



I^2S timing uses WS to define when the data being transmitted is for the left channel and when it is for the right channel. WS is low for the left channel and high for the right channel. WS need not be symmetrical. A bit clock (CLK) running at a minimum of 2 x (sample width) x sample frequency is used to clock in the data. There is a delay of one clock bit from the time the WS signal changes state to the first data bit on the data line. The data is written MSB first and is valid on the rising edge of the bit clock. Once the programmed sample width is taken any remaining bits are ignored.

Figure 12. I^2S Timing Diagram: Width of WS frame is wider than 2N bits. N=8, 16 or 24

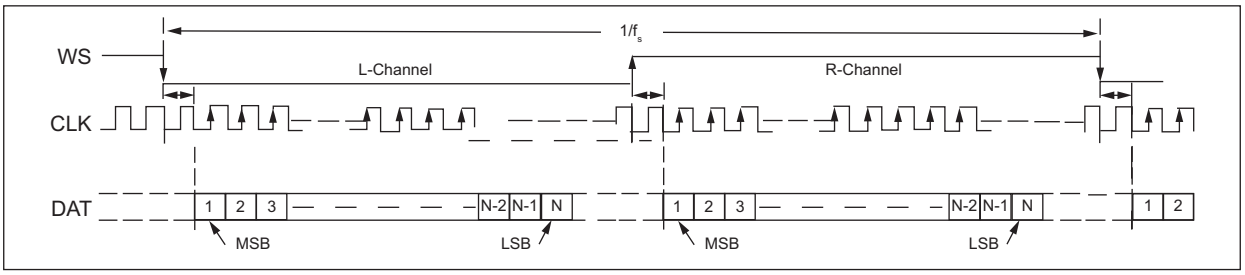
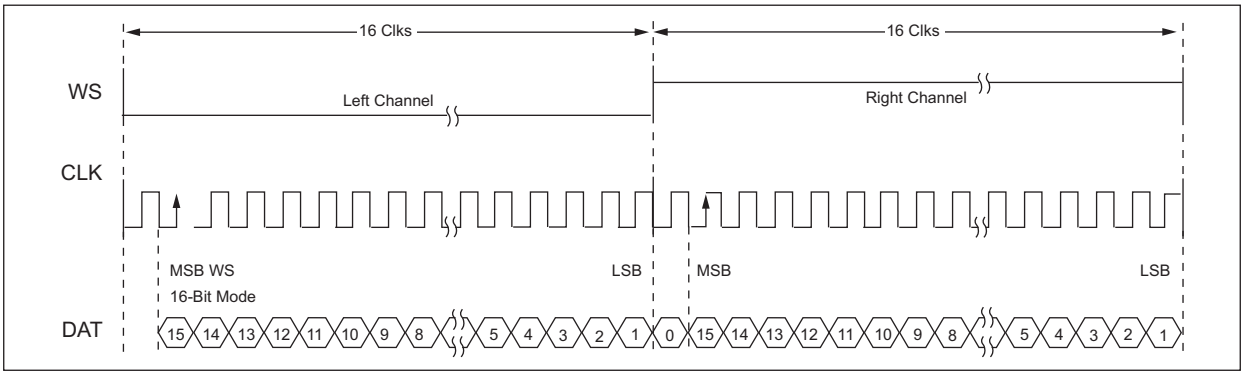


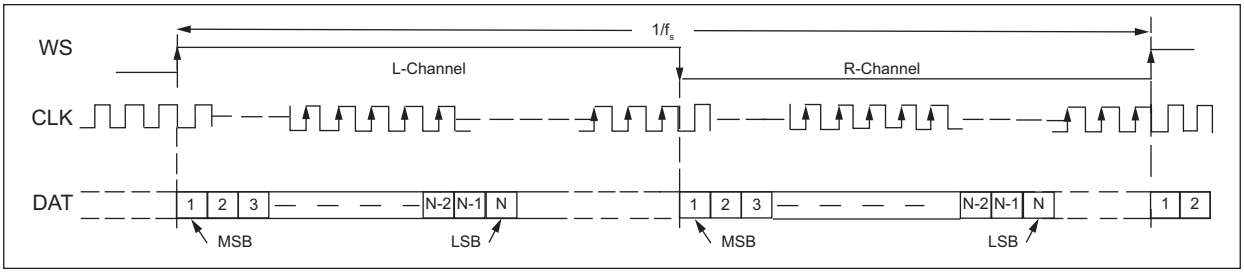
Figure 13. I^2S Timing Diagram 2: 16-Bit per Channel I2S



3.3.6.1 Left-Justified Timing

Left-justified timing uses WS clock to define when the data being transmitted is for the left channel and when it is for the right channel. WS is high for the left channel and low for the right channel. A bit clock running at a minimum of 2 x sample width x sample frequency is used to clock the data. The first data bit appears on the data lines at the same time WS toggles. The data is written MSB first and is valid on the rising edge of bit clock. Once the programmed sample width is taken, any remaining bits are ignored. If the WS toggles before the full word length is read, the remaining bits are zeroed.

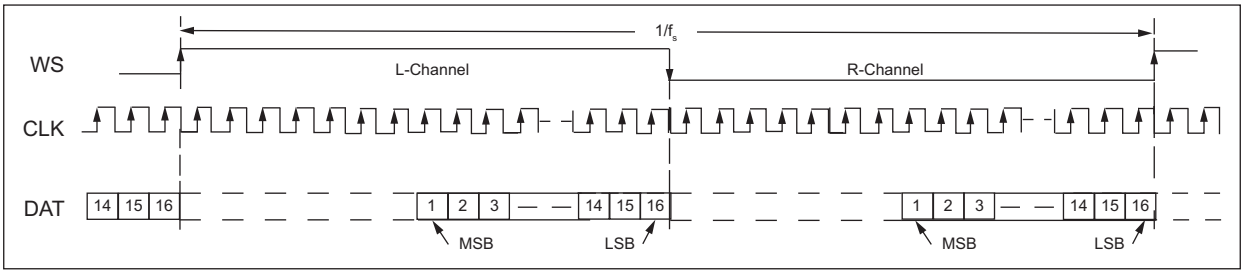
Figure 14. Left-Justified Timing Diagram



3.3.6.2 Right-Justified Timing

Right-justified timing uses WS clock to define when the data being transmitted is for the left channel and when it is for the right channel. WS is high for the left channel and low for the right channel. A bit clock running at a minimum of 2 x sample width x sample frequency is used to clock the data. Data is captured in a 24-bit shift register until WS toggles. Once WS toggles, the last 24, 16, or 8 bits are transferred to the channel indicated by the previous state of WS. In right-justified mode, the LSB of data is always clocked by the last bit clock before the WS transitions. The data is written MSB first and is valid on the rising edge of bit clock. All leading bits are ignored.

Figure 15. Right-Justified Timing Diagram



NOTE: For additional I^2S information, please refer to "I^2S Bus Specification" from NXP Semiconductor.

NOTE: For Right-Justified Timing or Left-Justified Timing, the WS is High for L-channel and Low for R-channel selection. They do not follow the convention of I^2S standard.

3.3.7 PCM Audio Interface Timing

The two PCM interfaces on CX20709-21Z support multiple audio streams divided into slots. Each slot is 8 bits wide and can support audio data of 8-bit A-Law/Mu-Law, 16- or 24-bit audio samples. 8-bit audio data takes up one slot per channel, while 16-bit audio takes 2 slots and similarly, 24-bit audio takes 3 slots per channel. CX20709-21Z PCM audio data are either in pairs or in 3 audio streams, supporting stereo audio (2-channel) or 2.1 audio (L, R and center), respectively. The audio streams are labeled as Stream 1 (L), Stream 2 (R) and Stream 3 (e.g., Center channel or sub-woofer), corresponding to their Stream Slot Control registers (namely, 0x0F57 through 0x0F5C and 0x0F62 through 0x0F67).

When the Stream 3 is unused, then Port 1 TX Stream 3 Slot Control Register (0x0F5C) and Port 2 TX Stream 3 Slot Control Register (0x0F67) may be left un-programmed.

Each PCM interface supports up to 32 8-bit slots. The user can use anywhere from 2 slots to all 32 slots for the transmission and reception of audio data.

The PCM Port 1 TX_DAT, TX_WS and Port 2 TX_DAT are 3-statable in master mode; the PCM Port 1 TX_DAT, TX_WS and Port 2 TX_DAT, WS are 3-statable in slave mode.

NOTE: 3-state functionality is not support in I^2S mode.

The following examples are used to illustrate two typical PCM applications:

3.3.7.1 PCM Example 1: Requirement

16-bit audio, L & R channel

PCM slots used: 8 slots (4 slots of data, 4 slots for stuffing)

Sample rate: 48 kHz

Digital Port 1, Master mode

3.3.7.2 PCM Example 1: PCM Register Setting

0x0F50 = 0xF2 ; Port 1 Clock - 3.072 MHz (8*8*48 kHz), Port 2 slave or unused

0x0F51 = 0xB1 ; PCM - Tx/Rx data delayed by one clock cycle

0x0F52 = 0x07 ; 64 TX clocks / frame = (7+1)*8

0x0F53 = 0x07 ; 64 RX clocks / frame = (7+1)*8

0x0F54 = 0x00 ; PCM TX sync width = 1 clock cycle ' (0+1)

0x0F55 = 0x00 ; PCM RX sync width = 1 clock cycle ' (0+1)

0x0F56 = 0x05 ; 16-bit RX sample and 16-bit TX sample

0x0F57 = 0x20 ; enable RX Stream1, occupying slots 0 & 1 (L channel)

0x0F58 = 0x24 ; enable RX Stream2, occupying slots 4 & 5 (R channel)

0x0F5A =0x20 ; enable TX Stream1, occupying slots 0 & 1 (L channel)

0x0F5B= 0x24 ; enable TX Stream2, occupying slots 4 & 5 (R channel)

Note that in the above example, we purposely use 8 slots instead of 4 slots. 4 slots would have been sufficient to accommodate the two 16-bit audio samples. The user

should be aware of the fact that there are 8 slots that are unused and are “wasted” or ignored. Also, if only 4 slots are used, then the clock rate can drop from 3.072 MHz down to 1.536 MHz. In addition, the TX/ RX Stream 2 slot will begin at Slot 2 (occupying Slot 2 and Slot 3).

The user may also choose different slots to start the Stream 2, say, Slots 2 and Slot 3 in the above case. This leaves slots 4 through 7 unused. The only requirement for slot allocation is that the audio data has to occupy contiguous slots should the sample size is large than 8 bits and TX slots for Stream 1, and Stream 2 *must* be distinct from each other. RX slots, however, may read from the same slot locations, thus, providing only L or only R audio PCM data at the receiving device.

3.3.7.3 PCM Example 2: Requirement

16-bit audio, L & R channel

PCM slots used: 4 slots (2 slots of L audio data, 2 slots of R audio data)

Sample rate: 48 kHz

Digital Port 1, Master mode

By eliminating the 4 'stuffing' slots, we have:

3.3.7.4 PCM Example 2: PCM Register Setting

0x0F50 = 0xF4 ; Port 1 Clock - 1.536 MHz, Port 2 slave or unused

0x0F51 = 0xB1 ; PCM - Tx/Rx data delayed by one clock cycle

0x0F52 = 0x03 ; 32 TX clocks / frame = (3+1)*8

0x0F53 = 0x03 ; 32 RX clocks / frame = (3+1)*8

0x0F54 = 0x00 ; PCM TX sync width = 1 clock cycle ' (0+1)

0x0F55 = 0x00 ; PCM RX sync width = 1 clock cycle ' (0+1)

0x0F56 = 0x05 ; 16-bit RX sample and 16-bit TX sample

0x0F57 = 0x20 ; enable RX Stream1, occupying slots 0 & 1 (L channel)

0x0F58 = 0x22 ; enable RX Stream2, occupying slots 2 & 3 (R channel)

0x0F5A =0x20 ; enable TX Stream1, occupying slots 0 & 1 (L channel)

0x0F5B= 0x22 ; enable TX Stream2, occupying slots 2 & 3 (R channel

Apply NewC thru the DINIT register. (Refer to CX20709-21Z Host API document.)

The first PCM port has five lines that make up the PCM interface: CLK, TX_WS, TX_DAT, RX_WS, and RX_DAT. In PCM mode, TX_WS and RX_WS act as the sync pulse. CLK, TX_WS, and RX_WS can either be internally generated or externally supplied.

The second PCM port has four lines that make up the PCM interface: CLK, WS, TX_DAT, and RX_DAT. In PCM mode WS is the sync pulse. Both CLK and WS can either be internally generated or externally supplied.

There are three modes of operation for PCM:

- Short frame mode
- Long frame mode
- Multi-slot mode

In short frame mode, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is one clock long. TX data is driven out on the rising edge of PCM_CLK after the PCM_SYNC pulse. RX data is strobed on the falling edge of PCM_CLK.

Figure 16. Short Frame Sync TX

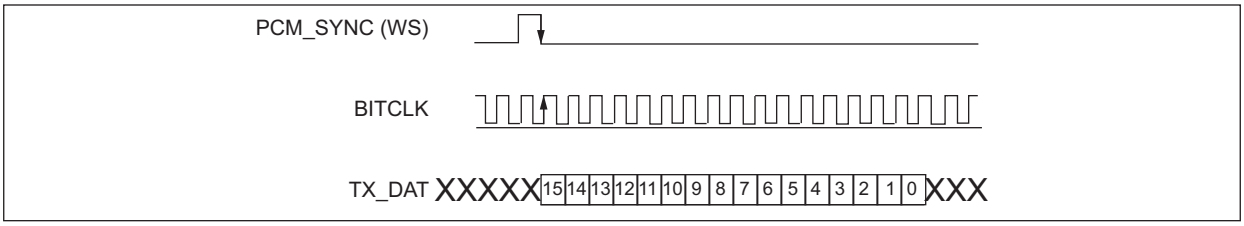
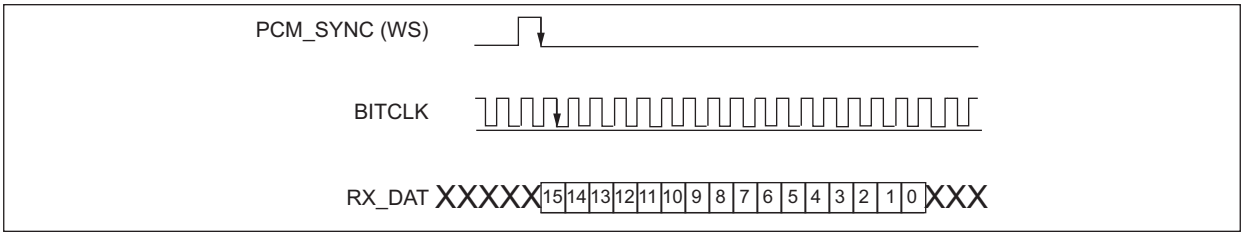


Figure 17. Short Frame Sync RX



In long frame mode, the rising edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is at least two clocks long. TX data is driven out on the rising edge of PCM_CLK coincident with the rising edge of PCM_SYNC. RX Data is strobed on the falling edge of PCM_CLK.

Figure 18. Long Frame Sync TX

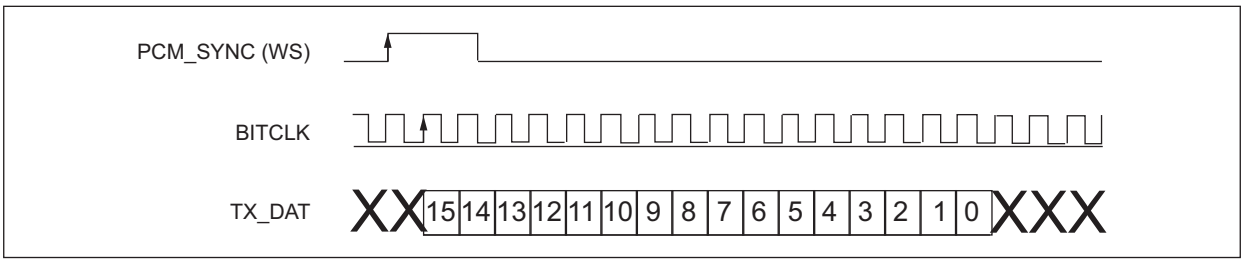
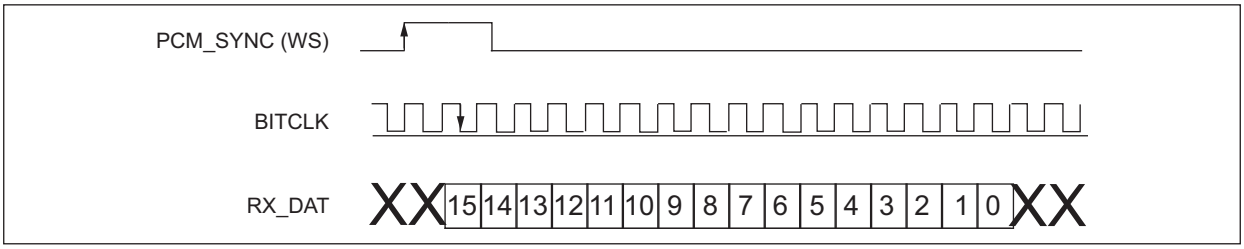


Figure 19. Long Frame Sync RX



In multi-slot mode, PCM_SYNC can be either long or short. Up to three streams of data can be sent or received. The position of the start of the PCM word is determined by the length of the sync pulse. Slots are determined by counting data width clocks (8, 16, or 24) from the first PCM word. (See the above two examples). In any case, unless the audio data is 8-bit A-Law/Mu-Law, stereo audio and 16-bit or 24-bit audio are always in multi-slot mode.

3.3.8 Master Clock to Codec: MCLK

CX20709-21Z can provide master clock to codecs that do not have their own clock. MCLK shares pin with I2C_EN. Upon power-up, CX20709-21Z will configure itself as an I^2C slave or SPI slave.

Once CX20709-21Z has reached full operation mode, the I2C_EN / MCLK pin can be programmed via API register to provide MCLK to an external codec.

The MCLK frequency can range from 2.048MHz all the way up to 24.576 MHz.

For details, refer to the *CX2070x Host API Document*.

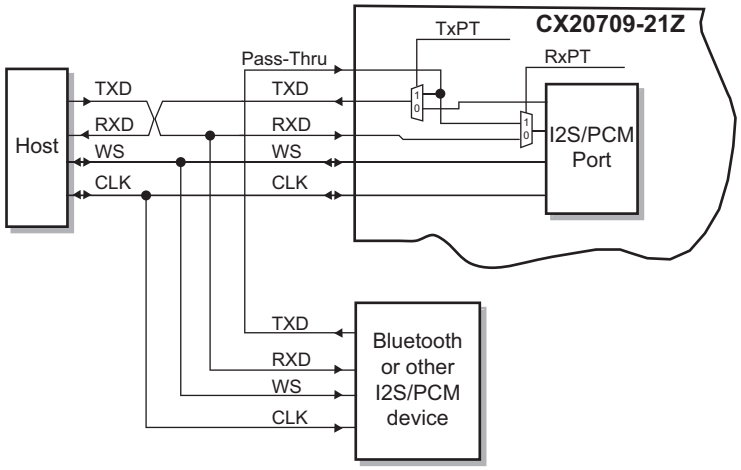
3.3.9 I^2S/PCM Pass-Through Mode

The PASS_THRU pin allows the TX data from another I^2S device to be routed through the PASS_THRU input to the TX output on the CX20709-21Z. This allows two slave devices to share the bus when normally the I^2S interface would be point-to-point. The other three signals are received from the host or controlled by the CX20709-21Z (depending on master or slave mode) so they can be tied together. The TX signals cannot be tied together because the CX20709-21Z TX in I^2S is a totem-pole output and is constantly driving a '0' or a '1'. The host uses the I^2C bus to tell the CX20709-21Z which TX data should be sent. (see Figure 20).

The Pass-Through mode is controlled by the following hardware registers:

- Port 1 Control 2 Register 0x0F56[5:4]
- Port 2 Sample Width Register 0x0F61[5:4].

Figure 20. I^2S/PCM Pass-Through Mode Diagram



GENERAL NOTE: Only 1 WS signal is shown in this diagram. If using the 5-wire interface, TX_WS and RX_WS should be tied together in Pass-Thru.

For PCM/I^2S Register programming, refer to Chapter 4, Registers.

NOTE: For CX20709-21Z PCM mode, the WS, BitClk, and TX Data can be three-stated, so pass-thru mode is optional when more than two devices are connected in the PCM bus. However, in I^2S mode, CX20709-21Z I^2S signals (WS, BitClk, and TX Data) are NOT three-statable.

3.3.10 Sound Bar

CX20709-21Z is capable of decoding incoming USB 5.1 sound bar audio and outputs to Stereo DAC, Mono DAC, I2S/PCM Digital Port 1 and Port 2.

For details, pleaser refer to CX2070x Host API Document.

3.4 Control Interfaces

CX20709-21Z supports: I2C, SPI, UART, and USB HID interfaces for serial communications with CX20709-21Z registers for CX20709-21Z command and control.

3.4.1 SPI/I2C

The SPI/I2C interface is used for controlling the codec. The Conexant SPoC Configuration Toolbox uses the I2C interface to read/write the CX20709-21Z registers. The CX20709-21Z I2C interface supports serial, 8-bit oriented, bi-directional data transfers of rates up to 100 kbps in the Standard-mode, or up to 400 kbps in the Fast-mode. I2C read/write operations are described below. For additional details, please refer to the I2C specification.

3.4.1.1 I2C Write Operation

For a host writing to the slave CX2070x device:

1. Send a start sequence
2. Send the I2C address of the slave with the R/W bit low
3. Send the internal register address you want to write to. Send high byte followed by low byte.
4. Send the data byte
5. [Optionally, send any further data bytes] -- Burst operation
6. Send the stop sequence.

Write Single Location

S	Device Address	W (0)	A	ADDR byte 1	A	ADDR byte 0	A	DATA byte 0	A	P

Write Auto increment

S	Device Address	W (0)	A	start ADDR byte 1	A	start ADDR byte 0	A	DATA [n]	A	DATA [n+1]	A	DATA [n+2]	A	DATA [n+3]	A	P

3.4.1.2 I²C Read Operation

For a host reading from the slave CX2070X device:

1. Send a start sequence
2. Send I²C address with the R/W bit low
3. Send the internal register address you want to read. Send high byte followed by low byte.
4. Send a start sequence again (repeated start)
5. Send I²C address with the R/W bit high
6. Read data byte
7. [Optionally, send any further data bytes] -- Burst operation
8. Send the stop sequence.

Read Single Location

S	Device Address	W (0)	A	ADDR byte 1	A	ADDR byte 0	A	Sr	Device Address	R (1)	A	DATA byte 0	N	P

Read Auto increment

S	Device Address	W (0)	A	start ADDR byte 1	A	start ADDR byte 0	A	Sr	Device Address	R (1)	A	DATA [n]	A	DATA [n+1]	A	DATA [n+2]	A	DATA [n+3]	N	P

Read Continuing Auto increment

S	Device Address	R	A	DATA [n+4] byte 1	A	DATA [n+5] byte 0	A	DATA [n+6] byte 1	A	DATA [n+7] byte 0	N	P

3.4.2 CX20709-21Z SPI Interface

3.4.2.1 SPI/I²C Interface I/Os

CX20709-21Z is a SPI slave device.

I2C_SPI_SCL: CX20709-21Z SPI Serial Clock input, provided by SPI Master

I2C_SDA/SPI_MOSI: CX20709-21Z SPI Serial In (driven by SPI Master)

SPI_MISO: CX20709-21Z SPI Serial Output.

I2C_EN: I²C Enable. Selects I²C or SPI interface. Connect to VDDO1 for I²C mode, 0 V for SPI mode.

I2C_SPI_CSN – I2C_ SPI_CSN = 0 enables I²C/SPI; I2C_SPI_CSN = 1 disables I²C/SPI access. I2C_SPI_CSN is usually controlled by SPI host.

3.4.2.2 I²C/SPI Clock

The I²C and SPI modules share the same pin interface and thus, the same clock input, pin SCL. Pin I2C_EN selects the interface to be I²C or SPI. If I²C_EN is set to 1, the I²C module is active while the SPI is not. In the same manner, when I2C_EN is set to 0, and the I²C module is turned off.

The maximum SPI clock rate is 24 MHz, recommended maximum operating frequency is 9 MHz.

3.4.2.3 General Description: SPI Interface

The SPI slave controller is used to provide the serial interface to write to CX20709-21Z registers. It supports 13-bit addressing mode for all register read/writes. Data can be written in single or burst mode. Register read/write commands from external host or SPI master received are converted to appropriate commands to perform read/write from CX20709-21Z registers.

- Supports 8-bit register read/write through SPI slave interface
- Supports single and burst mode

3.4.2.4 SPI Register Read/Write Operation

The host can initiate register read or write to CX20709-21Z registers first by writing the control word 000xxxxxxxxxxxx or 100xxxxxxxxxxxx respectively after the falling edge of I2C_SPI_CSN.

The SPI interface logic decodes host commands:

- Write address and data are registered and written to CX20709-21Z registers.
- Read address is transferred to CX20709-21Z for register reads.

The CX20709-21Z responds by sending data back to SPI interface, which serializes the data and sends it to host over SPI interface.

Note that until data is received from CX20709-21Z, to meet SPI protocol, dummy data is sent as first byte, and when actual data is received from CX20709-21Z it is sent as second byte.

- Register read/write transfers can be 8/13-bit address modes.
- MOSI Input serial data is latched on the rising edge of SCK.
- MISO Output data is sent on the falling edge of SCK.
- Read/Write access is valid during CSN=0.

3.4.2.5 SPI Timing Information

Figure 21. SPI Timing

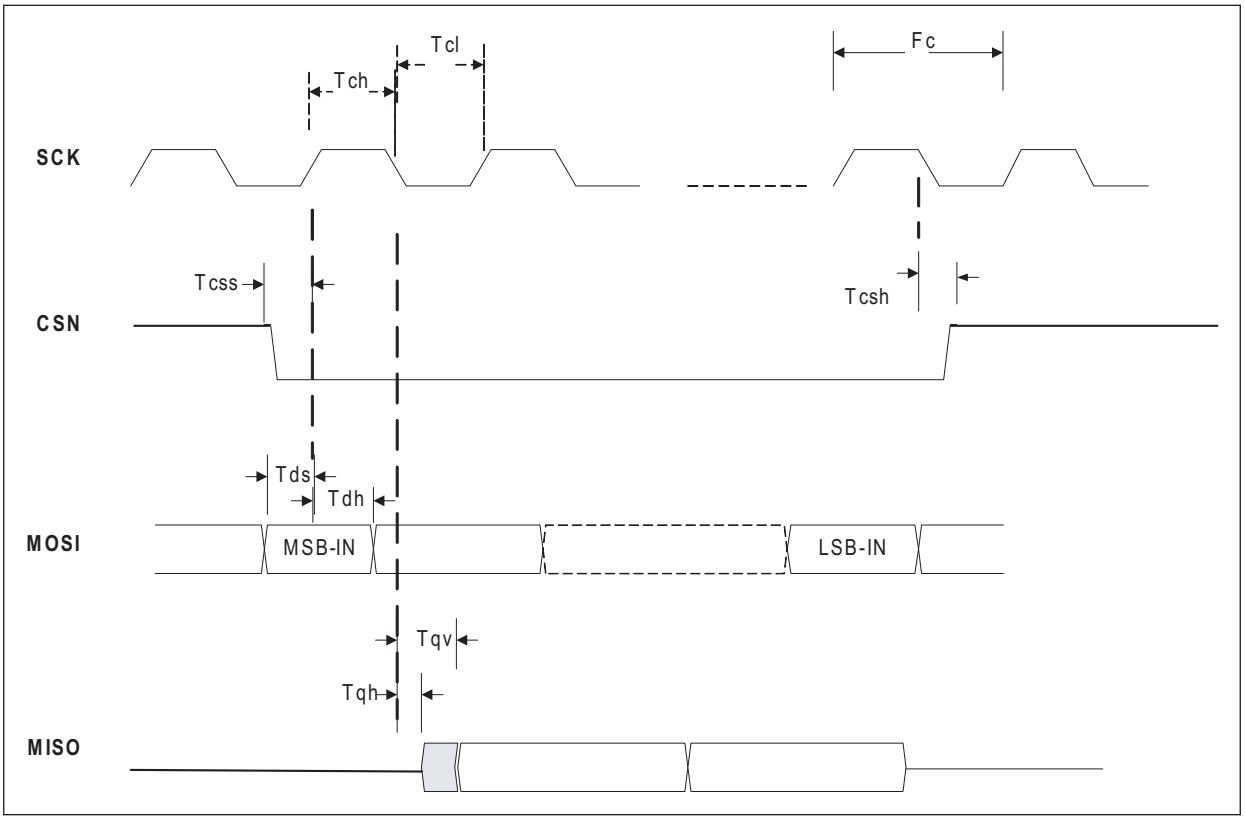


Table 39. Timing Parameters

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Fc	Clock Frequency			24	MHz
Tch	Clock High	18			ns
Tcl	Clock Low	18			ns
Tcss	Chip select Setup Time	7			ns
Tcsh	Chip select Hold Time	7			ns
Tds	Data-In Setup Time	5			ns
Tdh	Data-In Hold Time	5			ns
Tqv	Clock Low to output Valid			15	ns
Tqh	Output Hold Time	0			ns

Table 40. Control Word Format

Control Word	Description
0000xxxxxxxxxxxx	Read eight or sixteen bit register at address xxxxxx (Dummy data is sent as first byte for First Read)
1000xxxxxxxxxxx	Write to eight or sixteen bit register at address xxxxxx

3.4.2.6 SPI Read/Write Timing

The SPI commands are sent by the master on the SPI_MOSI pin at the rising edge of I2C_SPI_SCL. The commands are 3 bytes wide. CX20709-21Z addresses are 13 bits wide.

Write: 100---xxxxxxxxxxxxx---yyyyyyyy (The 13 bits following 100 is the address). Then followed by the 8 bits (yyyyyyyy) data being written.

Read: 000---xxxxxxxxxxxxx---00000000 (The 13 bits following 000 is the address).

Once the read is issued, wait for eight clock cycles and the data will be placed on the SPI_MISO line at the subsequent falling edge of I2C_SPI_SCL.

Figure 22. SPI Read Timing

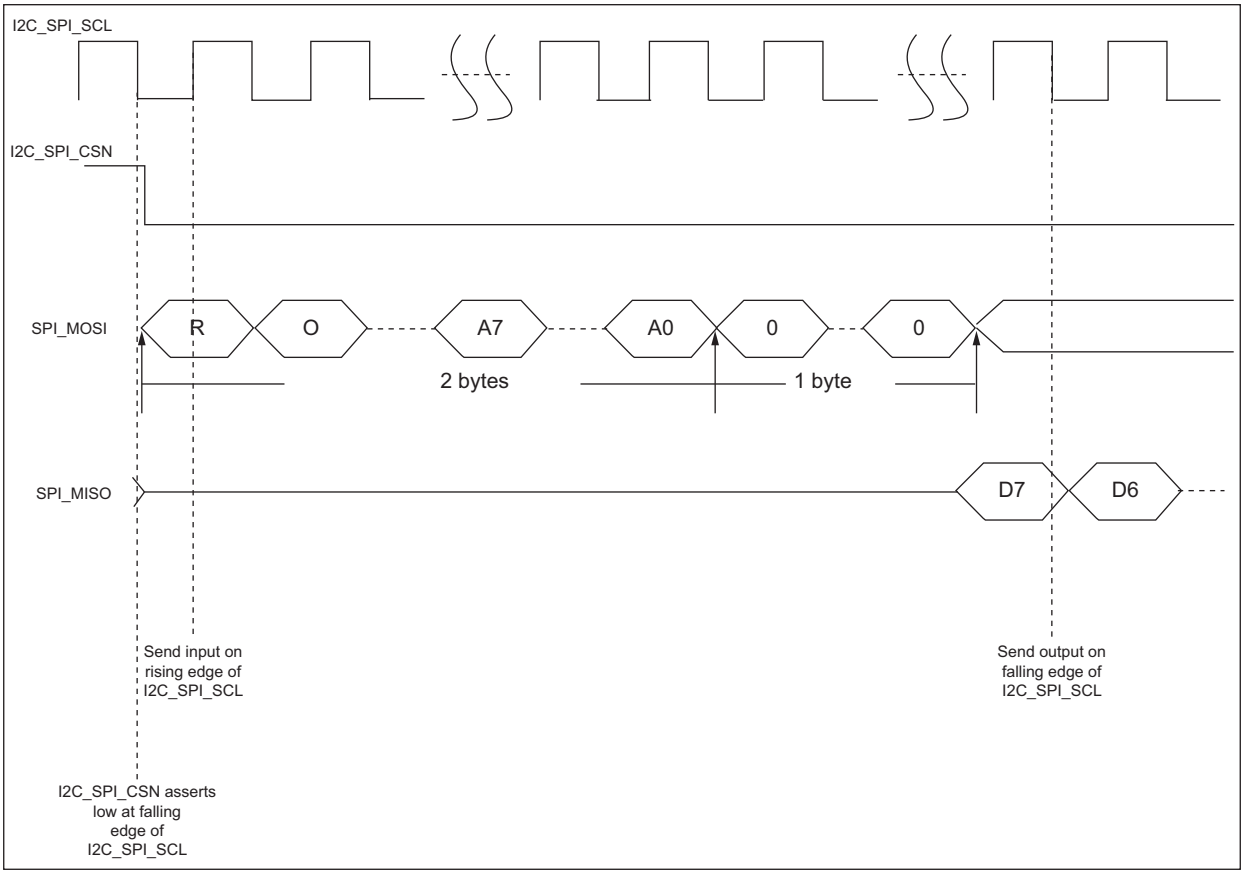


Figure 23. SPI Write Timing

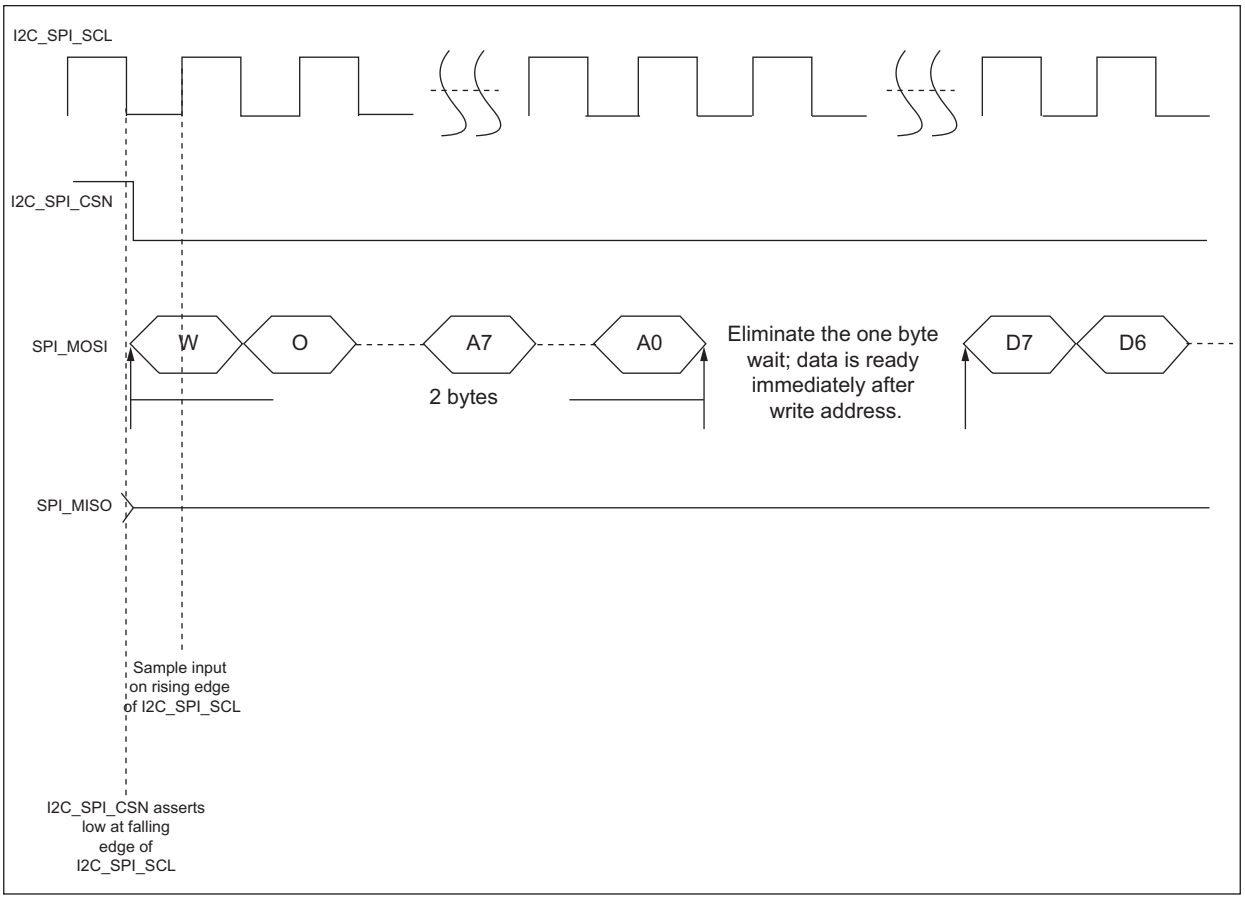
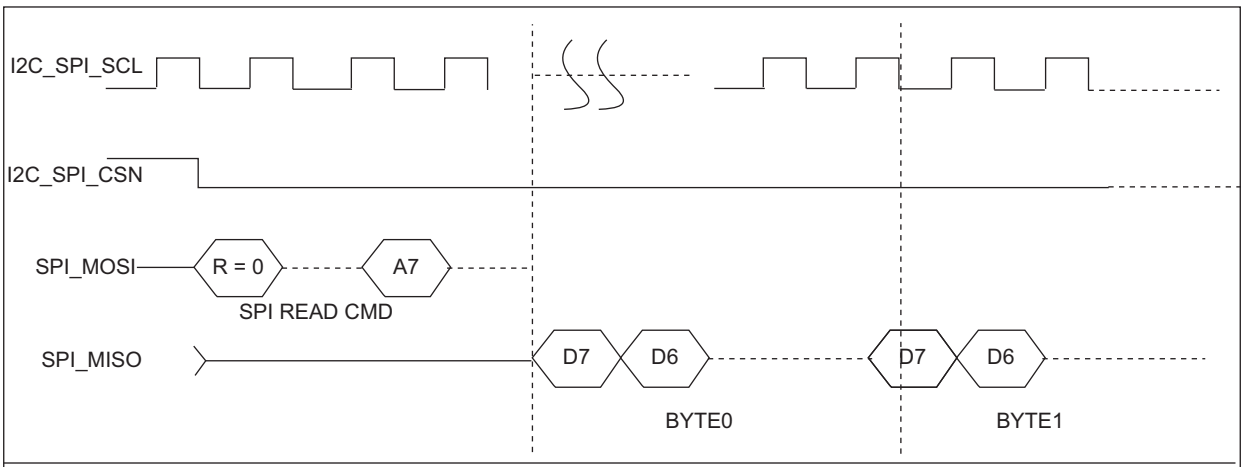
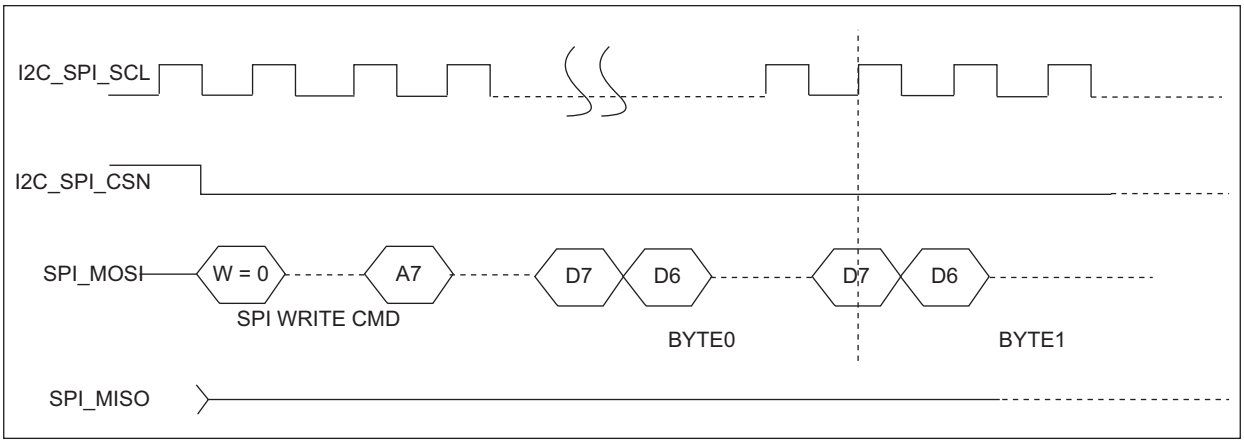


Figure 24. SPI Burst Read



GENERAL NOTE: After read address is presented, there is an 8-clockk-cycle wait time before valid data will come out from SPI_MISO (HSOMI).

Figure 25. SPI Burst Write



As long as I2C_SPI_CSN is asserted, the transactions are valid. If I2C_SPI_CSN stays asserted beyond 1 byte of data, the next data byte will be written to the next address location in an auto increment mode. The same is true in the case of reads. As long as I2C_SPI_CSN is asserted, registers will be read in auto increment mode.

3.4.3 GPIO

There are eight general purpose GPIO pins available. These are configured and controlled by the controller. There are pre-defined uses for these pins, but through code patching many other uses are possible. The GPIO block is powered by its own supply allowing 1.8 V or 3.3 V signaling. On reset the GPIO are configured as inputs to minimize power. GPIO can be configured as a wake source. This allows the analog, DSP, and controller to wake from a low-power state.

GPIO1 can also be configured as SPDIF_OUT.

3.4.4 EEPROM

An I^2C master interface is dedicated for loading USB strings, controller patches, and DSP patches from an external EEPROM. An external 16kx8 (128k bit) EEPROM is supported for CX20709-21Z.

CX20709-21Z firmware patch codes can be implemented in the EEPROM for download to CX20709-21Z RAM upon power-up or hardware reset.

The EEPROM interface has two I^2C interface pins: NVCLK and NVDAT. CX20709-21Z acts as an I^2C master, reading external EEPROM data via the NVCLK and NVDAT pins (equivalent to SCL and SDA). NVCLK and NVDAT require external pull-up resistors interfacing to the EEPROM.

The EEPROM write data can be obtained from CX20709-21Z internal RAM while EEPROM patch data is read upon power-up or hardware reset from an external NVRAM.

3.4.5 UART

The UART is a serial communication device that communicates with the CX20709-21Z registers. The pins are: UART_RX, UART_TX and the GPIO0 also serves as CTS. It operates at 115,200 bps, no parity bit, 8 data bits and 1 stop bit. For file transfer, the CTS should always be used to prevent UART buffer overflow.

3.4.6 Clock Source/Crystal

A 48 MHz crystal or oscillator is required for CX20709-21Z to operate in USB mode. Either a 24 MHz or 48 MHz crystal or oscillator may be used for non USB operations. The CX20709-21Z defaults to a 48 MHz clock, the Host0 RAM location register, 0x004D[5], selects between the 48 MHz or 24 MHz clock source.

The crystal (clock source) tolerance is ± 200 ppm over temperature and voltage.

3.5 DSP

The CX20709-21Z DSP has 100 MIPs of processing power, and sufficient memory to support speakerphone, 2.1-channel audio, and 3D algorithms. The complete list of required algorithms is AEC, NR, Beam Forming, ALC, LEC, Digital Crossover, Equalizer, DRC, and 3D processing. The DSP is capable of mixing two stereo streams coming from any of the digital sources with one analog stream. The resulting mix can be sent to any digital or analog interface. Mixing will be done at 48 kHz and the sample rate converted to the requested output sample rate.

3.5.1 CX20709-21Z DSP Stream Routing

CX20709-21Z inputs and outputs are governed by audio streams. The following describe the audio stream routing and behavior of CX20709-21Z as governed by CX20709-21Z Firmware Version 5:

1. CX20709-21Z has four inputs streams, namely: Stream 1, 2, 3, & 4, plus a Function Generator Stream; and five output streams: Stream 5, 6, 7, 8, & 9.
2. Stream 1 is comprised of the two Line Inputs and a 2nd set of mic or Line input (Line In 1, 2, & Mic 2). It can also be used by the digital mic as an input.
3. Stream 2 is the microphone input stream, with a sampling rate of 8k,16k, 32k, or 48ksps for narrow-band or wide-band phone applications. It can also be used by the digital mic as an input.
4. Stream 3 is sourced from Digital Port 1 (5-wire), Digital Port 2 (4-wire, SPDIF input or 2nd USB playback stream); the audio stream of Digital Port 1 or Digital Port 2 is either in I^2S or PCM format.
5. Stream 4 is sourced from Digital Port 1 (5-wire), Digital Port 2 (4-wire) or USB playback stream; the audio stream of Digital Port 1 or Digital Port 2 is either in I^2S or PCM format.
6. Stream 5 is the Digital Port 1 output which also provides ASRC for sampling rate translation.
7. Stream 6 is the Digital Port 2 output which also provides ASRC for sampling rate translation.
8. Stream 7 outputs to either:
   a. SPDIF, or
   b. Stereo DAC to headphone, Line Out or Class-D with Equalizer.
9. Stream 8 outputs to the Mono DAC. Stream 8 sums the left and right signals into a mono stream:
   a. which also has a crossover equalizer, upon activation, can drive a Sub Woofer via an external amplifier. Sub Woofer output cutoff frequency is user selectable via the writing of API registers. Conexant recommends a low-pass cutoff frequency of 400 Hz or below for meaningful sub-woofer output.
   b. OR, MONO_OUT (DAC3), it can be configured as single-ended or differential line output.
10. Stream 9: USB recording stream. It is sent to an USB host.

11. There is also a built-in Function Generator (selectable sampling rate of 16k, 32k, or 48ksps) that can be routed to any of the 5 output streams, namely: Stream 5, 6, 7, 8, or 9.
12. The Inputs streams are sent out to the output steams via one of the three processing internal blocks. These blocks are:
    a. Playback Processing Block (PB) that contains the following functional blocks:
        i. 3D processing
        ii. DRC
        iii. In-Bound Noise Reduction
        iv. Line Echo Canceller (LEC)
        v. Mixer 0: It allows mixing of up to four different inputs.
        vi. Volume Control
    b. Mixer 1 Block (MX1). It allows mixing of up to four different inputs. No processing except stream mixing is performed.
    c. Voice Processing Block (VP). This blocks consists of the following functional blocks:
        i. Acoustic Echo Canceller (AEC)
        ii. AGC
        iii. Beam Forming
        iv. Debug Select
        v. DRC
        vi. Mic EQ
        vii. Noise Reduction
13. The Output Streams can accept outputs from one of the above three internal processing blocks or directly from the output of any of the input streams, i.e. Stream 1, 2, 3, 4 or Function Generator block output. The use is cautioned to ensure that the input sampling rate matches to that of the output sampling rate of the input streams.
14. For further details, please refer to the *CX2070x: Host API Document*.
15. For line echo cancellation, the microphone MUST be used (Stream 2) in conjunction with the Playback Processing (PB) block. After PB, the most common stream routing would be Mono Output, i.e. Stream 8. If the Mono Output is configured as a differential line-driver, it may drive an external 600 Ohm transformer to interface with PSTN telephone lines. However, the user may choose other output options, and is thus not limited to Stream 8 only.

Figure 26. CX20709-21Z Input Streams and Function Generator Block

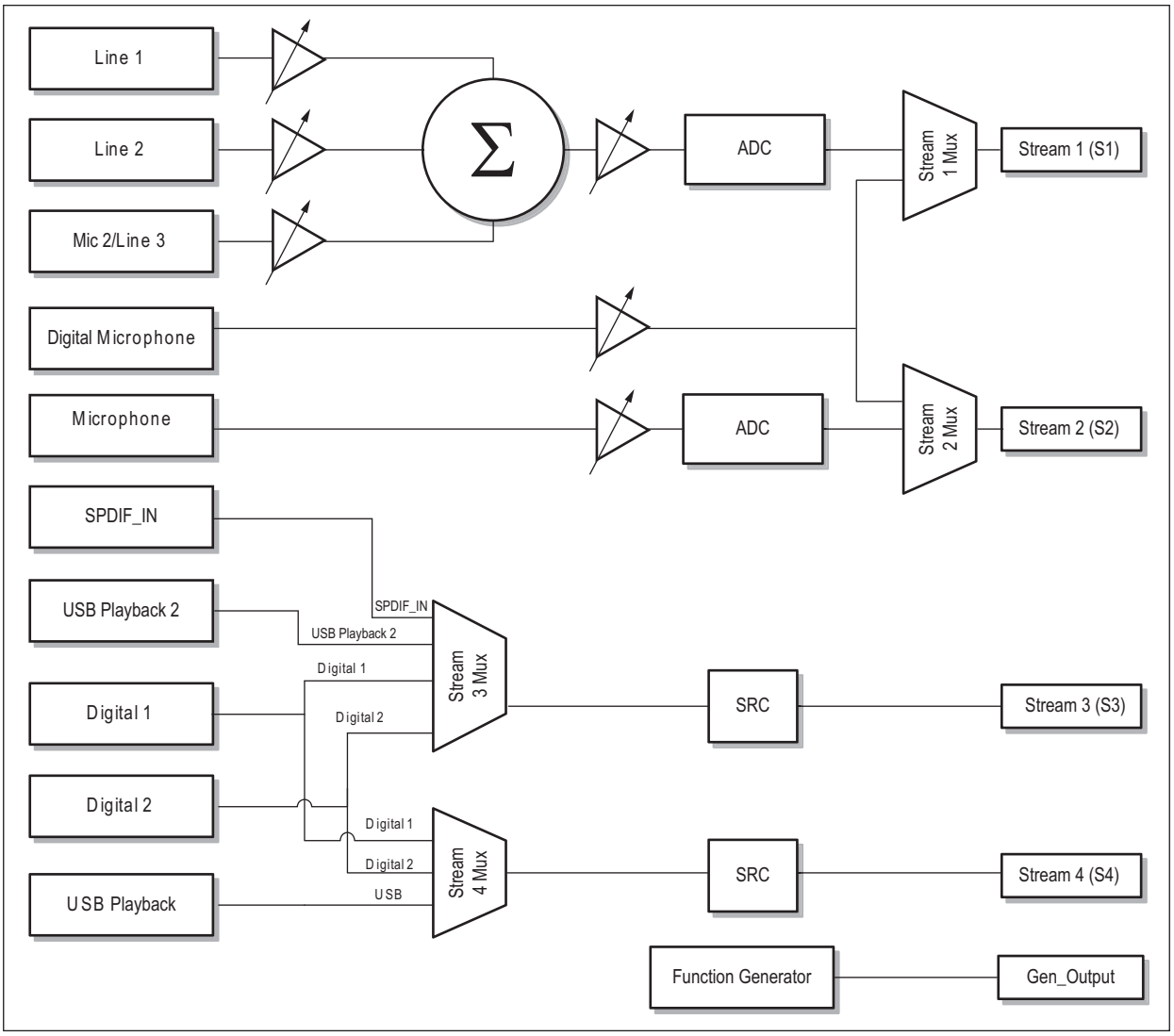


Figure 27. CX20709-21Z Processing Blocks and Mixer Block

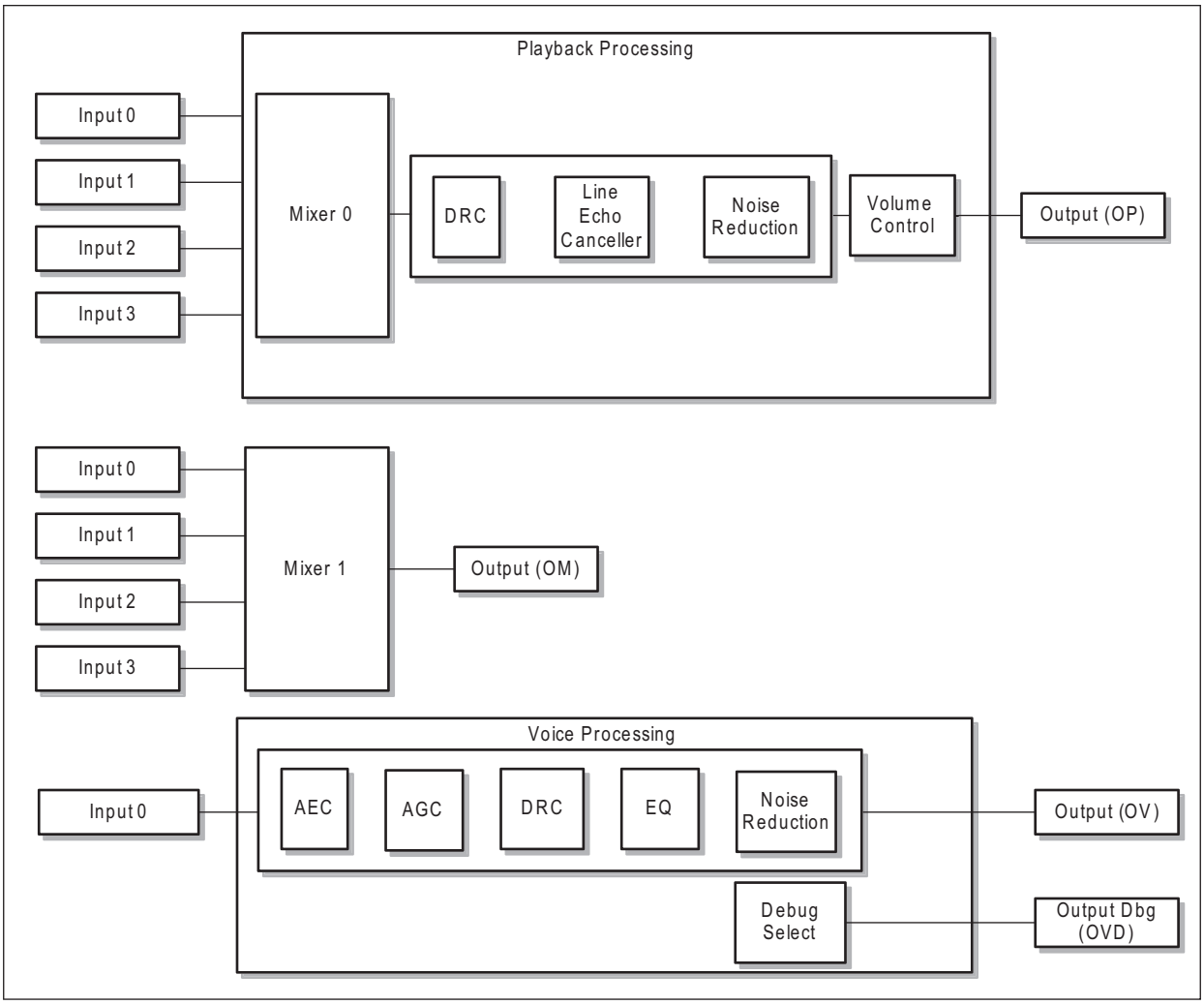
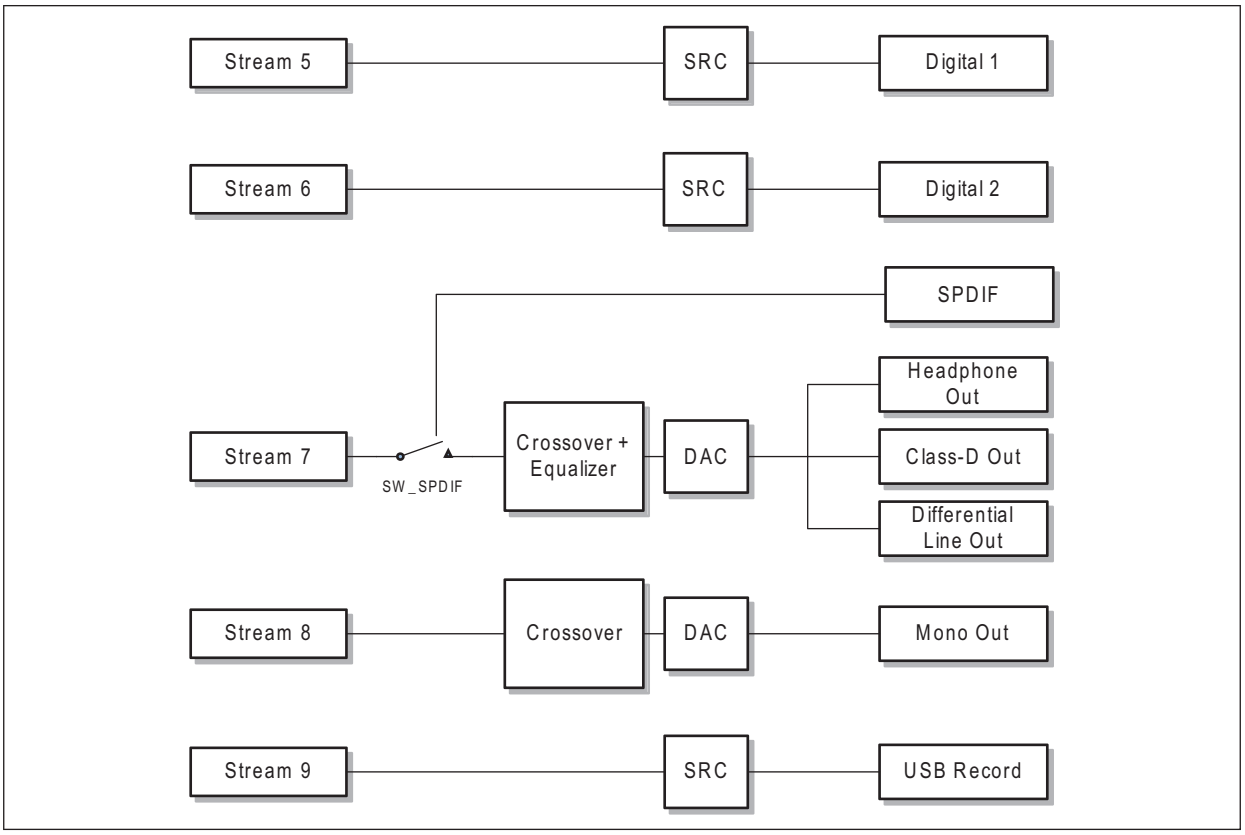


Figure 28. CX20709-21Z Output Streams

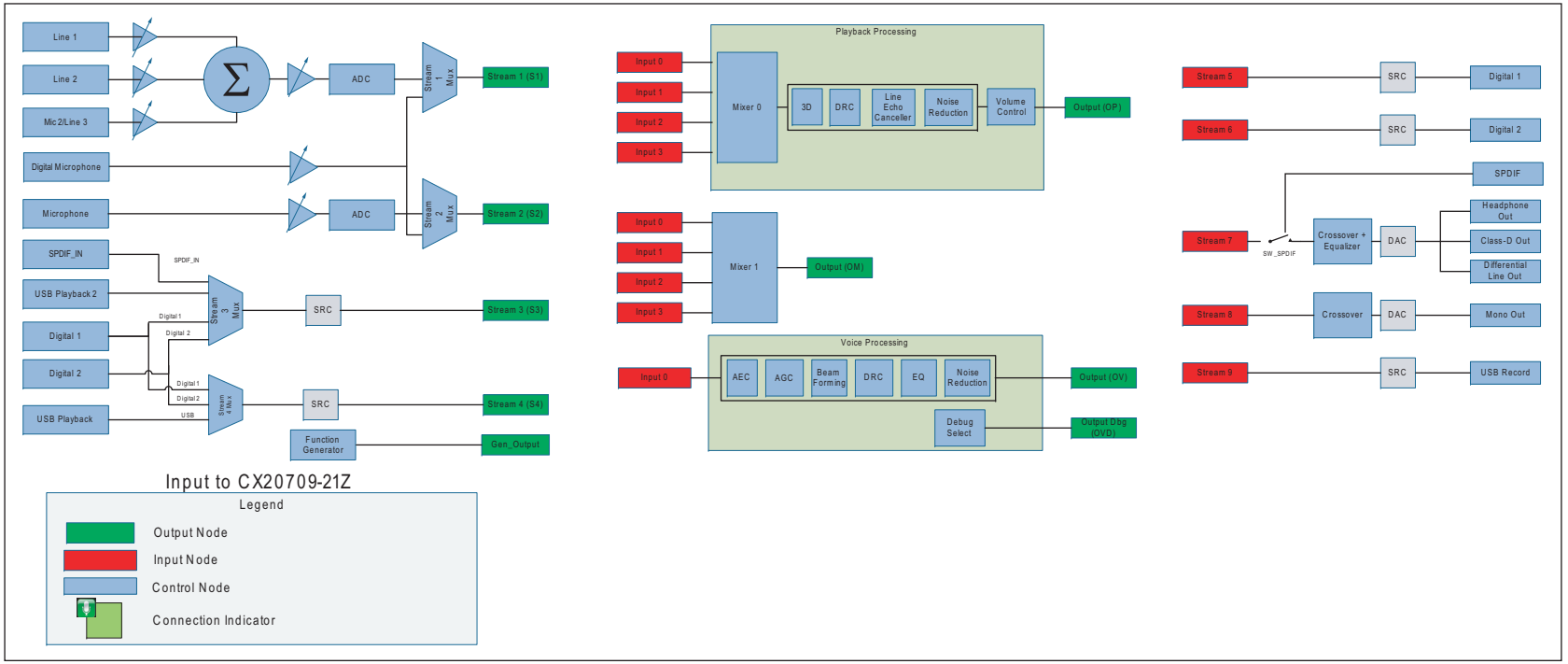


NOTE: In I^2S/PCM Mode, CX20709-21Z will operate in the following modes:

- ✓ DSP mode, either as I^2S/PCM master or slave.
- ✓ Pass-Thru mode (non-DSP), I^2S/PCM master, or as I^2S/PCM slave if the master codec uses the MCLK generated by CX20709-21Z.

NOTE: ASRC or SRC refers to the asynchronous sample rate conversion function of CX20709-21Z in DSP Mode.

Figure 29. CX20709-21Z DSP Diagram



Any Input Stream output (Stream 1, 2, 3, 4 and Function Generator) can be connected directly to the input node of any Output Stream (Stream 5, 6, 7, 8, 9); or to any Processing Block/Multiplexer input node. The validity of the connection is subject to proper rate matching with or without the use of ASRC.

There is a limit of 4 Input Streams and 5 Output Streams. An input node can only accept one input. However, any output node may be connected to up to 4 output nodes.

For a description on the various sources and destination of the stream routing, refer to the *CX20709-21Z Host API Document*.

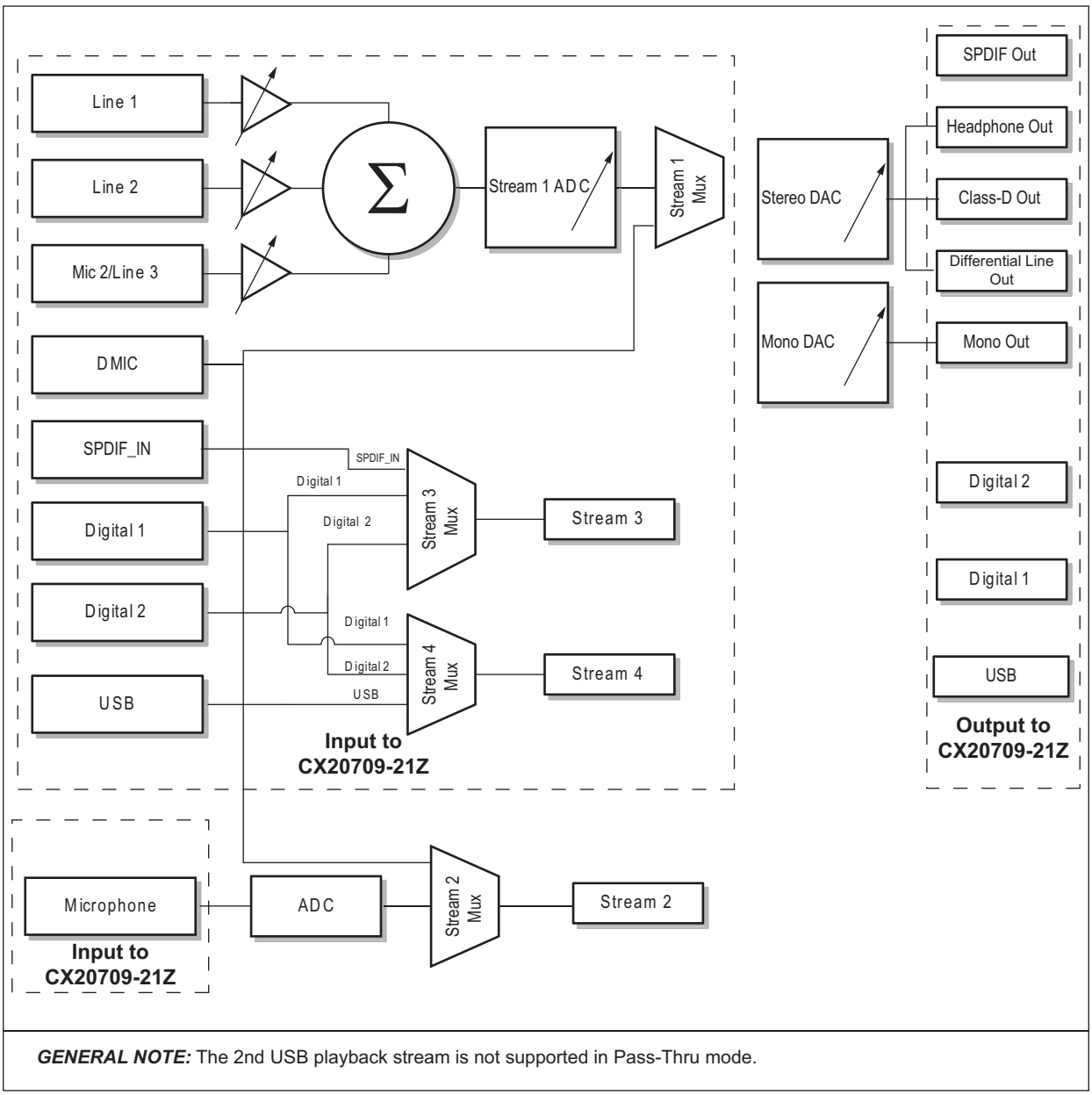
3.6 Pass-Thru Mode

In Pass-Thru (non-DSP) mode, any input stream can be routed to any output stream, as long as the input stream and the output stream are of the same rate. In the absence of ASRC in Pass-Thru mode, if there is a rate mismatch in the audio streams (e.g., input vs. output), there will be distortion in the output.

An example of a valid Pass-Thru mode audio route is: Stream 2 (mic input) can be routed to the DAC and playback through the Class-D speaker.

Note that the only DSP function that is supported in Pass-Thru mode is the equalizer at the DAC (refer to Figure 30).

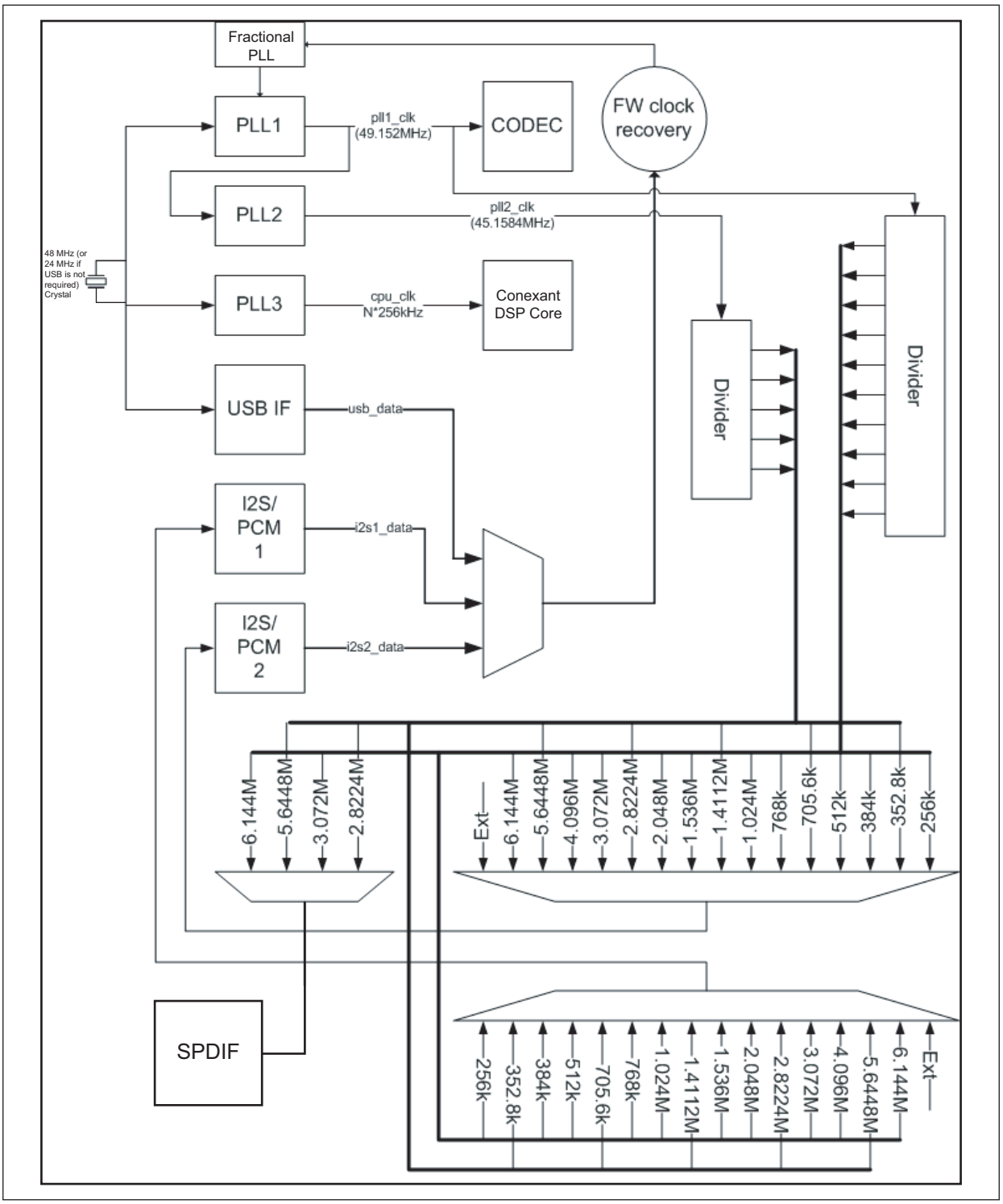
Figure 30. Pass-Thru (non-DSP) Audio Stream Routing Diagram



GENERAL NOTE: The 2nd USB playback stream is not supported in Pass-Thru mode.

3.7 Internal Clocking

Figure 31. Internal Clocking



4 CX20709-21Z Registers

4.1 Register Map

All CX2070x hardware registers are controlled by the firmware except for the I^2S/ PCM configuration registers (namely: 0x0F50 through 0x0F6A). For a detailed description of the functionality and application of the firmware registers, please refer to the *CX2070x-21Z Host API Document* corresponding to the pertinent firmware revision.

Table 41. Register List *(1 of 2)*

Register Name	Offset (Byte)	Default
Digital Audio Interface (I^2S and PCM) Control Registers		
Clock Divider	0xF50	0xFF
Port 1 Control	0xF51	0
Port 1 TX Clocks per Frame	0xF52	0
Port 1 RX Clocks per Frame	0xF53	0
Port 1 TX Sync Width	0xF54	0
Port 1 RX Sync Width	0xF55	0
Port 1 Control 2	0xF56	0x0A
Port 1 RX Stream 1 Slot Control	0xF57	0
Port 1 RX Stream 2 Slot Control	0xF58	0
Port 1 RX Stream 3 Slot Control	0xF59	0
Port 1 TX Stream 1 Slot Control	0xF5A	0
Port 1 TX Stream 2 Slot Control	0xF5B	0
Port 1 TX Stream 3 Slot Control	0xF5C	0
Port 1 Bit Count Delay	0xF5D	0
Port 2 Control	0xF5E	0
Port 2 Clocks per Frame	0xF5F	0
Port 2 Sync Width	0xF60	0

Table 41. Register List *(2 of 2)*

Register Name	Offset (Byte)	Default
Digital Audio Interface (I^2S and PCM) Control Registers (continued)		
Port 2 Sample Width	0xF61	0x01
Port 2 RX Stream 1 Slot Control	0xF62	0
Port 2 RX Stream 2 Slot Control	0xF63	0
Port 2 RX Stream 3 Slot Control	0xF64	0
Port 2 TX Stream 1 Slot Control	0xF65	0
Port 2 TX Stream 2 Slot Control	0xF66	0
Port 2 TX Stream 3 Slot Control	0xF67	0
Port 2 Bit Count Delay	0xF68	0
Port 1 TX Stream 4 Slot Control	0x0F69	0
Port 2 TX Stream 4 Slot Control	0x0F6A	0

4.2 Register Details

Clock Divider (0x0F50)

Bits	Name	Default	R/W	Description
7:4	Port 2 Clock Div Select	0	R/W	0x0 = 6.144 MHz 0x1 = 4.096 MHz 0x2 = 3.072 MHz 0x3 = 2.048 MHz 0x4 = 1.536 MHz 0x5 = 1.024 MHz 0x6 = 768 kHz 0x7 = 512 kHz 0x8 = 384 kHz 0x9 = 256 kHz 0xa = 5.644 MHz 0xb = 2.822 MHz 0xc = 1.411 MHz 0xd = 705 kHz 0xe = 352 kHz 0xf = external clock enabled
3:0	Port 1 Clock Div Select	0	R/W	0x0 = 6.144 MHz 0x1 = 4.096 MHz 0x2 = 3.072 MHz 0x3 = 2.048 MHz 0x4 = 1.536 MHz 0x5 = 1.024 MHz 0x6 = 768kHz 0x7 = 512 kHz 0x8 = 384 kHz 0x9 = 256 kHz 0xa = 5.644 MHz 0xb = 2.822 MHz 0xc = 1.411 MHz 0xd = 705 kHz 0xe = 352 kHz 0xf = external clock enabled

Port 1 Control (0x0F51)

Bits	Name	Default	R/W	Description
7	Delay	0	R/W	0 = I^2S - Left Justified Data not delayed PCM – TX/RX data start in same cycle as Frame Sync, without any delay. 1 = I^2S - Left Justified Data delayed 1 bit PCM – TX/RX data delayed by One cycle
6	Right Justify	0	R/W	0 = Left Justify Mode (I^2S)/MSB first (PCM) 1 = Right Justify mode (I^2S)/LSB first (PCM)
5	RX En	0	R/W	1 = Port 1 RX Enabled 0 = Port 1 RX Disabled
4	TX EN	0	R/W	1 = Port 1 TX Enabled 0 = Port 1 TX Disabled
3	RX Bitclk Polarity	0	R/W	**I^2S Mode** 0 = RX Data Strobed with Rising Edge of Bit Clock 1 = RX Data Strobed with Falling Edge of Bit Clock **PCM Mode** 0 = RX Data Strobed with Falling Edge of Bit Clock 1 = RX Data Strobed with Rising Edge of Bit Clock
2	TX Bitclk Polarity	0	R/W	**I^2S Mode** 0 = TX Data Sent on Falling Edge of Bit Clock 1 = TX Data Sent on Rising Edge of Bit Clock **PCM Mode** 0 = TX Data Sent on Rising Edge of Bit Clock 1 = TX Data Sent on Falling Edge of Bit Clock
1	WS Pol	0	R/W	0: WS Low for Left channel; WS High for Right channel (I^2S Only) 1: WS High for Left channel; WS Low for Right channel (I^2S Only)
0	I^2S PCM	0	R/W	0 = I^2S mode 1 = PCM Mode

Port 1 TX Clocks per Frame (0x0F52)

Bits	Name	Default	R/W	Description
7:5	Reserved	0	R	
4:0	TX Clocks per Frame	0	R/W	TX Clocks per Frame It is (N+1)*8 00000 – 8 Clocks per Frame 00001 – 16 Clocks per Frame 00010 – 24 Clocks per Frame 00011 – 32 Clocks per Frame ……. ……. 11111 – 256 Clocks per Frame

Port 1 RX Clocks per Frame (0x0F53)

Bits	Name	Default	R/W	Description
7:5	Reserved	0	R	
4:0	RX Clocks per Frame	0	R/W	RX Clocks per Frame It is (N+1)*8 00000 – 8 Clocks per Frame 00001 – 16 Clocks per Frame 00010 – 24 Clocks per Frame 00011 – 32 Clocks per Frame ……. ……. 11111 – 256 Clocks per Frame

Port 1 TX Sync Width (0x0F54)

Bits	Name	Default	R/W	Description
7	Reserved	0	R	
6:0	TX Sync Length	0	R/W	TX Sync Width. Number of bit clock cycles RX Frame Sync would be valid. 0000000 – 1 Cycle 0000001 – 2 Cycle …….. …….. 1111111 – 128 Cycles

Port 1 RX Sync Width (0x0F55)

Bits	Name	Default	R/W	Description
7	Reserved	0	R	
6:0	RX Sync Length	0	R/W	RX Sync Width Number of bit clock cycles TX Frame Sync would be valid. 0000000 – 1 Cycle 0000001 – 2 Cycle …….. …….. 1111111 – 128 Cycles

Port 1 Control 2 (0x0F56)

Bits	Name	Default	R/W	Description
7-6	Reserved	0		
5	P1 TX PT	0	R/W	Port 1 TX PassThru 0 = TX pin outputs TX data 1 = TX pin outputs PassThru Input
4	P1 RX Pt	0	R/W	Port 1 RX PassThru 0 = RX receives RX pin data 1 = RX receives PassThru data
3:2	RX Sample Size	1	R/W	RX Sample Size 00 = 8-bit 01 = 16-bit 10 = 24-bit truncated to 16 bits 11 = 24-bit
1:0	TX Sample Size	1	R/W	TX Sample Size 00 = 8-bit 01 = 16-bit 10 = 24-bit truncated to 16 bits 11 = 24-bit

Port 1 RX Stream 1 Slot Control (0x0F57)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	RX Stream 1 Enable	0	R/W	0 = Disable, 1= Enable RX Steam 1
4:0	RX Stream 1	0	R/W	PCM Slot Number for RX Stream 1 Each Slot is 8 bits. All the Enabled RX steams should be configured to Unique Slot Nos. Note: If RX Sample Size is 16 or 24, it uses two or three consecutive slots respectively. RX slots nos. should be allocated accordingly.

Port 1 RX Stream 2 Slot Control (0x0F58)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	RX Stream 2 Enable	0	R/W	0 = Disable, 1= Enable RX Steam 2
4:0	RX Stream 2	0	R/W	PCM Slot Number for RX Stream 2. See PCM steam1 for slot allocation Description.

Port 1 TX Stream 1 Slot Control (0x0F5A)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	TX Stream 1 Enable	0	R/W	0 = Disable, 1= Enable TX Steam 1
4:0	TX Stream 1	0	R/W	PCM Slot Number for TX Stream 1 Each Slot is 8 bits. All the Enabled TX steams should be configured to Unique Slot Nos. Note: If TX Sample Size is 16 or 24, it uses two or three consecutive slots respectively. TX slots nos. should be allocated accordingly.

Port 1 TX Stream 2 Slot Control (0x0F5B)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	TX Stream 2 Enable	0	R/W	0 = Disable, 1= Enable TX Steam 2
4:0	TX Stream 2	0	R/W	PCM Slot Number for TX Stream 2 See TX steam1 for slot allocation Description.

Port 1 TX Stream 3 Slot Control (0x0F5C)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	TX Stream 3 Enable	0	R/W	0 = Disable, 1= Enable TX Steam 3
4:0	TX Stream 3	0	R/W	PCM Slot Number for TX Stream 3 See TX steam1 for slot allocation Description.

Port 1 Bit Count Delay (0x0F5D)

Bits	Name	Default	R/W	Description
7	Reserved	0	R	
6:0	Bit Count Delay	0	R/W	I^2S Bit Count Delay (used for right justify mode)

Port 2 Control 1 (0x0F5E)

Bits	Name	Default	R/W	Description
7	Delay	0	R/W	0 = I^2S - Left Justified Data not delayed PCM – TX/RX data start in same cycle as Frame Sync, without any delay. 1 = I^2S - Left Justified Data delayed 1 bit PCM – TX/RX data delayed by One cycle
6	Right Justify	0	R/W	0 = Left Justify Mode (I^2S) / MSB first (PCM) 1 = Right Justify mode (I^2S) / LSB first (PCM)
5	RX En	0	R/W	0 = Port 2 RX Disabled 1 = Port 2 RX Enabled
4	TX En	0	R/W	0 = Port 2 TX Disabled 1 = Port 2 TX Enabled
3	RX Bitclk Polarity	0	R/W	**I^2S Mode** 0 = RX Data Strobed with Rising Edge of Bit Clock 1 = RX Data Strobed with Falling Edge of Bit Clock **PCM Mode** 0 = RX Data Strobed with Falling Edge of Bit Clock 1 = RX Data Strobed with Rising Edge of Bit Clock
2	TX Bitclk Polarity	0	R/W	**I^2S Mode** 0 = TX Data Sent on Falling Edge of Bit Clock 1 = TX Data Sent on Rising Edge of Bit Clock **PCM Mode** 0 = TX Data Sent on Rising Edge of Bit Clock 1 = TX Data Sent on Falling Edge of Bit Clock
1	WS Pol	0	R/W	0: WS Low for Left channel; WS High for Right channel (I^2S only) 1: WS High for Left channel; WS Low for Right channel (I^2S only)
0	I2S PCM	0	R/W	0 = I^2S mode 1 = PCM Mode

Port 2 Clocks per Frame (0x0F5F)

Bits	Name	Default	R/W	Description
7:5	Reserved	0	R	
4:0	Clocks per Frame	0	R/W	Clocks per Frame It is (N+1)*8 00000 – 8 Clocks per Frame 00001 – 16 Clocks per Frame 00010 – 24 Clocks per Frame 00011 – 32 Clocks per Frame ……. ……. 11111 – 256 Clocks per Frame

Port 2 Sync Width (0x0F60)

Bits	Name	Default	R/W	Description
7	Reserved	0	R	
6:0	Sync Length	0	R/W	Sync Width Number of bit clock cycles Frame Sync would be valid. 0000000 – 1 Cycle 0000001 – 2 Cycle …….. …….. 1111111 – 128 Cycles

Port 2 Sample Width (0x0F61)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	P2 TX PT	0	R/W	Port 2 TX PassThru 0 = TX pin outputs TX data 1 = TX pin outputs PassThru Input
4	P2 RX Pt	0	R/W	Port 2 RX PassThru 0 = RX receives RX pin data 1 = RX receives PassThru data
3:2	Reserved	0	R	
1:0	Sample Size	1	R/W	Sample Size 00 = 8-bit 01 = 16-bit 1x = 24-bit

Port 2 RX Stream 1 Slot Control (0x0F62)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	RX Stream 1 Enable	0	R/W	0 = Disable, 1= Enable RX Steam 1
4:0	RX Stream 1	0	R/W	PCM Slot Number for RX Stream 1 Each Slot is 8 bits. All the Enabled RX steams should be configured to Unique Slot Nos. Note: If RX Sample Size is 16 or 24, it uses two or three consecutive slots respectively. RX slots nos. should be allocated accordingly.

Port 2 RX Stream 2 Slot Control (0x0F63)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	RX Stream 2 Enable	0	R/W	0 = Disable, 1= Enable RX Steam 2
4:0	RX Stream 2	0	R/W	PCM Slot Number for RX Stream 2 See RX Steam1 for slot allocation description

Port 2 TX Stream 1 Slot Control (0x0F65)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	TX Stream 1 Enable	0	R/W	0 = Disable, 1= Enable TX Steam 1
4:0	TX Stream 1	0	R/W	PCM Slot Number for TX Stream 1 Each Slot is 8 bits. All the Enabled TX steams should be configured to Unique Slot Nos. Note: If TX Sample Size is 16 or 24, it uses two or three consecutive slots respectively. TX slots nos. should be allocated accordingly.

Port 2 Tx Stream 2 Slot Control (0x0F66)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	TX Stream 2 Enable	0	R/W	0 = Disable, 1= Enable TX Steam 2
4:0	TX Stream 2	0	R/W	PCM Slot Number for TX Stream 2 See TX Steam1 for slot allocation description

Port 2 TX Stream 3 Slot Control (0x0F67)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	TX Stream 3 Enable	0	R/W	0 = Disable, 1= Enable TX Steam 3
4:0	TX Stream 3	0	R/W	PCM Slot Number for TX Stream 3 See TX Steam1 for slot allocation description

Port 2 Bit Count Delay (0x0F68)

Bits	Name	Default	R/W	Description
7	Reserved	0	R	
6:0	Bit Count Delay	0	R/W	Port 2 I^2S Bit Count Delay (used for right justify mode) 0: 1 bit delay 1: 2 bits delay : : k: (k+1) bits delay

Port 1 TX Stream 4 Slot Control (0x0F69)

Bits	Name	Default	R/W	Description
Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	TX Stream 4 Enable	0	R/W	0 = Disable, 1= Enable TX Steam 4 (controlled by FW)
4:0	TX Stream 4	0	R/W	PCM Slot Number for TX Stream 4 See TX Steam1 for slot allocation description

Port 2 TX Stream 4 Slot Control (0x0F6A)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	TX Stream 4 Enable	0	R/W	0 = Disable, 1= Enable TX Steam 4 (controlled by FW)
4:0	TX Stream 4	0	R/W	PCM Slot Number for TX Stream 4 See TX Steam1 for slot allocation description

NOTE: The RX/TX Stream Slot Control Registers are only applicable to PCM. They are not applicable to I^2S.

5 CX20709-12Z Hardware Interface

5.1 Pin Assignments

Table 42 provides the pin assignments.

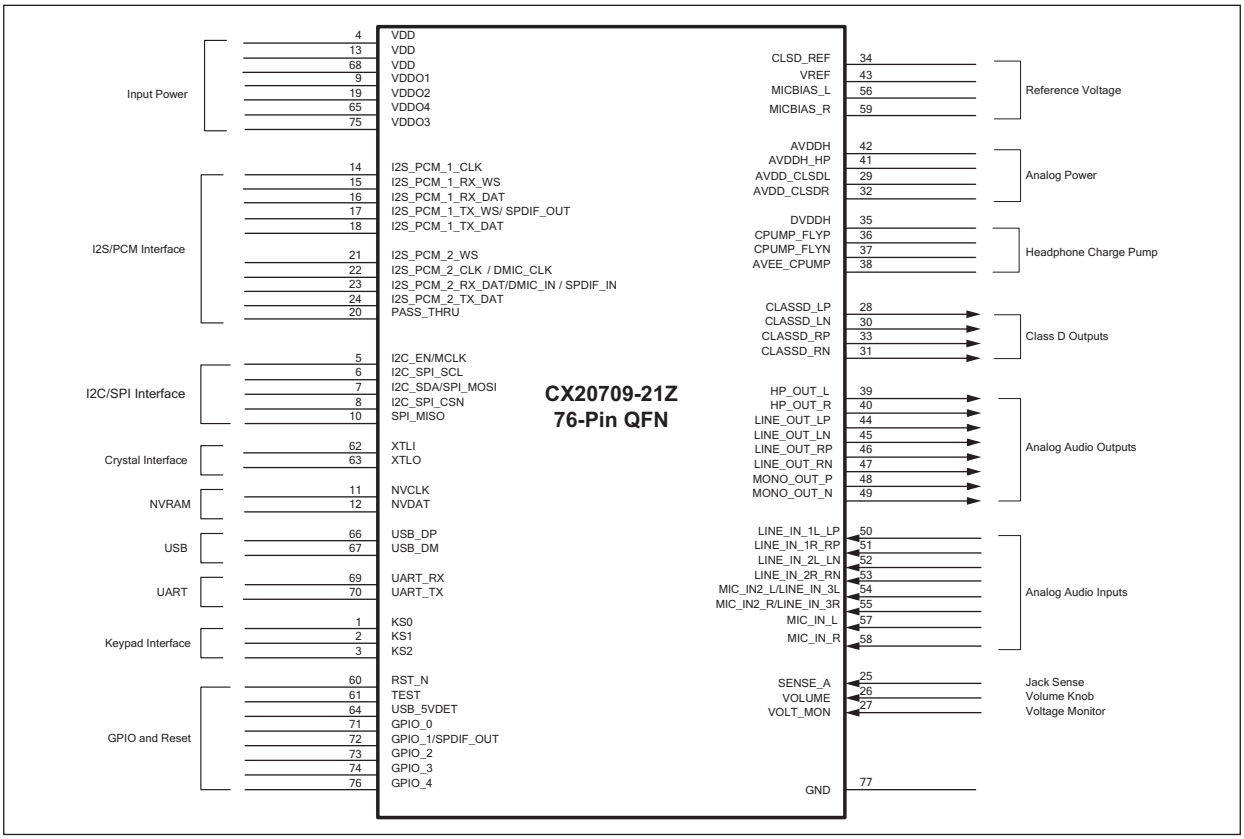
Table 42. Pin Assignments and Signal Definitions

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	KS0	20	PASS_THRU	39	HP_OUT_L	58	MIC_IN_R
2	KS1	21	I2S_PCM_2_WS	40	HP_OUT_R	59	MIC_BIAS_R
3	KS2	22	I2S_PCM_2_CLK	41	AVDDH_HP	60	RST_N
4	VDD	23	I2S_PCM_2_RX_DAT	42	AVDDH	61	TEST
5	I2C_EN	24	I2S_PCM_2_TX_DAT	43	VREF	62	XTLI
6	I2C_SPI_SCL	25	SENSE_A	44	LINE_OUT_LP	63	XTLO
7	I2C_SDA/SPI_MOSI	26	VOLUME	45	LINE_OUT_LN	64	USB_5VDET
8	I2C_SPI_CSN	27	VOLT_MON	46	LINE_OUT_RP	65	VDDO4
9	VDDO1	28	CLASSD_LP	47	LINE_OUT_RN	66	USB_DP
10	SPI_MISO	29	AVDD_CLSDL	48	MONO_OUT_P	67	USB_DM
11	NVCLK	30	CLASSD_LN	49	MONO_OUT_N	68	VDD
12	NVDAT	31	CLASSD_RN	50	LINE_IN_1L_LP	69	UART_RX
13	VDD	32	AVDD_CLSDR	51	LINE_IN_1R_RP	70	UART_TX
14	I2S_PCM_1_CLK	33	CLASSD_RP	52	LINE_IN_2L_LN	71	GPIO_0
15	I2S_PCM_1_RX_WS	34	CLSD_REF	53	LINE_IN_2R_RN	72	GPIO_1
16	I2S_PCM_1_RX_DAT	35	DVDDH	54	LINE_IN_3L	73	GPIO_2
17	I2S_PCM_1_TX_WS	36	CPUMP_FLYP	55	LINE_IN_3R	74	GPIO_3
18	I2S_PCM_1_TX_DAT	37	CPUMP_FLYN	56	MICBIAS_L	75	VDDO3
19	VDDO2	38	AVEE_CPUMP	57	MIC_IN_L	76	GPIO_4
GENERAL NOTES: The device also has a ground paddle referred to as pin 77 in this document.							

5.2 CX20709-12Z Hardware Interface Signals

Figure 32 shows the signals for the hardware interface. Table 42 provides a list of the CX20709-12Z hardware signal definitions.

Figure 32. CX20709-12Z Hardware Interface Signals



5.3 Signal Definitions

Table 43. CX20709-12Z Hardware Signal Definitions *(1 of 4)*

Label	Pin	I/O Type	Signal Name/Description
Crystal Signals			
XTLI	62	Digital In	**Crystal In**. Connect XTALI to a 48.0 MHz crystal circuit.
XTLO	63	Digital Out	**Crystal Out.** Connect XTALO to the crystal circuit return.
I^2S/PCM Interface			
I2S_PCM_1_CLK	14	Digital I/O	**Digital Port 1.** I^2S/PCM Bit Clock.
I2S_PCM_1_RX_WS	15	Digital I/O	**Digital Port 1.** I^2S/PCM Receive Word Select.
I2S_PCM_1_RX_DAT	16	Digital In	**Digital Port 1.** I^2S/PCM Receive Word Data.
I2S_PCM_1_TX_WS	17	Digital I/O	**Digital Port 1.** I^2S/PCM Transmit Word Select. This pin can optionally be defined as the SPDIF output.
I2S_PCM_1_TX_DAT	18	Digital Out	**Digital Port 1.** I^2S/PCM Transmit Word Data**.**
PASS_THRU	20	Digital In	**I^2S Pass Through.** This allows the interface to be shared with another I^2S device. In pass through mode, the transmit data pin is driven by the pass through pin instead of the internal interface engine.
I2S_PCM_2_WS	21	Digital I/O	**Digital Port 2.** I^2S/PCM Word Select.
I2S_PCM_2_CLK	22	Digital I/O	**Digital Port 2.** I^2S/PCM Bit Clock.
I2S_PCM_2_RX_DAT	23	Digital In	**Digital Port 2.** I^2S/PCM Receive Word Data.
I2S_PCM_2_TX_DAT	24	Digital Out	**Digital Port 2.** I^2S/PCM Transmit Word Data.
I^2C/SPI Interface			
I2C_EN	5	Digital In	**I^2C Enable.** Selects I^2C or SPI interface. Connect to VDDO1 for I^2C mode, 0V for SPI mode.
I2C_SPI_SCL	6	Digital I/O	**I^2C/SPI Clock.**
I2C_SDA/SPI_MOSI	7	Digital I/O	**I^2C/SPI Data.**
I2C_SPI_CSN	8	Digital In	**I^2C/SPI Chip Select.** I2C_ SPI_CSN=0 enables I2C/SPI. I2C_SPI_CSN=1 disables I2C/SPI access.
SPI_MISO	10	Digital I/O	**SPI Data to Host.** In I^2C mode, this pin is used to select between I^2C slave address of 14H and 54H, respectively.
USB			
USB_DP	66	Digital I/O	**USB Data Positive.**
USB_DM	67	Digital I/O	**USB Data Negative.**

***Table 43. CX20709-12Z Hardware Signal Definitions** (2 of 4)*

Label	Pin	I/O Type	Signal Name/Description
Control Signals			
RST_N	60	Digital In	**Reset.** Active low input asserted to initialize registers, sequencers, and signals to a consistent reset state. RST_N should remain low for 5ms after all power rails have become stable. Then RST_N should go to VDDO4.
TEST	61	Digital In	**TEST.** Connect to ground through 0 Ω resistor.
USB_5VDET	64	Digital In	**USB 5V Detect.** USB +5V VBUS signal should be connected to a resistor divider to reduce the level to 3.3 V at this pin.
GPIO_0	71	Digital I/O	**GPIO.** If using the UART interface, this pin should be used as the UART CTS signal.
GPIO_1	72	Digital I/O	**GPIO.** Pin can be configured as the SPDIF output.
GPIO_2	73	Digital I/O	**GPIO.**
GPIO_3	74	Digital I/O	**GPIO.**
GPIO_4	76	Digital I/O	**GPIO.**
SENSE_A	25	Analog In	**Jack Sense.** Connect to external resistor network to sense up to 4 jacks.
VOLUME	26	Analog In	**Analog Volume Control.** Connect to potentiometer. When set to 3.3 V, volume is maximum.
VOLT_MON	27	Analog In	**Voltage Monitor.** This pin can be used to monitor an external battery voltage.
Button Interface			
KS[0:2]	1, 2, 3	Digital I/O	**Keypad Scan I/O.** These pins can be used to form a button matrix or can be used as GPIO.
UART Interface			
UART_RX	69	Digital In	**UART Receive.**
UART_TX	70	Digital Out	**UART Transmit.**
NVRAM Signals			
NVCLK	11	Digital I/O	**NVRAM Clock.** Connect to external NVRAM clock signal.
NVDAT	12	Digital I/O	**NVRAM Data.** Connect to external NVRAM data signal. Connect to VDDO1 via 10 kΩ resistor.

***Table 43. CX20709-12Z Hardware Signal Definitions** (3 of 4)*

Label	Pin	I/O Type	Signal Name/Description
Analog Audio Inputs			
LINE_IN_1L_LP	50	Analog In	**Line Input Left 1/Positive.** In single-ended mode, this pin is the left input for line input 1. In differential mode, this pin is the left positive input and is paired with pin 52.
LINE_IN_1R_RP	51	Analog In	**Line Input Right 1/Positive.** In single-ended mode, this pin is the right input for line input 1. In differential mode, this pin is the right positive input and is paired with pin 53.
LINE_IN_2L_LN	52	Analog In	**Line Input Left** 2/Negative. In single-ended mode, this pin is the left input for line input 2. In differential mode, this pin is the left negative input and is paired with pin 50.
LINE_IN_2R_RN	53	Analog In	**Line Input Right** 2/Negative. In single-ended mode, this pin is the right input for line input 2. In differential mode, this pin is the right negative input and is paired with pin 51.
LINE_IN_3L_L/R	54, 55	Analog In	**Left and Right Line Input 3.** Can be used as a single-ended input or combined with one of the other line inputs for a differential input.
MIC_IN_L/R	57, 58	Analog In	**Left and Right Microphone Inputs.** L Mic is used in both DSP mode and Pass-Thru mode. R Mic is used in either: 1. Pass-Thru mode or 2. Beam-Forming in DSP mode. It is not enabled in DSP mode unless it is used in Beam Forming. Both L & R mics are active (stereophonic) in Pass-Thru mode.
Analog Audio Outputs			
CLASSD_LP/N	28, 30	Analog Out	**Class-D Left Differential Output.**
CLASSD_RN/P	31, 33	Analog Out	**Class-D Right Differential Output.**
HP_OUT_L/R	39, 40	Analog Out	Headphone Out. 50 mW Capless headphone output
LINE_OUT_LP/N	44, 45	Analog Out	**Line Out Left.** Can be configured as single-ended or differential. In single-ended mode, the output is on the positive pin.
LINE_OUT_RP/N	46, 47	Analog Out	**Line Out Right.** Can be configured as single-ended or differential. In single-ended mode, the output is on the positive pin.
MONO_OUT_P/N	48, 49	Analog Out	**Mono Out.** Can be configured as single-ended or differential. In single-ended mode, the output is on the positive pin. Can be used as a subwoofer output or to drive a 600 Ω load for intercom applications.
Headphone Charge Pump			
DVDDH	35	Power	**3.3 V Power for HP & Class-D digital circuits.** Requires 3.3 V external power supply.
CPUMP_FLYP	36	Power	**Charge Pump Positive Transfer Charge.** Connect to CPUMP_FLYN through a 1 μF capacitor.
CPUMP_FLYN	37	Power	**Charge Pump Negative Transfer Charge.** Connect to CPUMP_FLYP through a 1 μF capacitor.

***Table 43. CX20709-12Z Hardware Signal Definitions** (4 of 4)*

Label	Pin	I/O Type	Signal Name/Description
AVEE_CPUMP	38	Power	**Charge Pump Negative Power Supply.** Internally generated negative charge pump power. Connect to 10 μF and 0.1 μF external filtering capacitors.
Digital Power			
VDD	4, 13, 68	Power	**VDD.** Requires 1.8 V external power supply.
VDDO1	9	Power	**VDDO1.** Power for I^2C and NVRAM interfaces. Requires 1.8 V or 3.3 V external power supply.
VDDO2	19	Power	**VDDO2.** Power for PCM interfaces. Requires 1.8 V or 3.3 V external power supply.
VDDO3	75	Power	**VDDO3.** Power for GPIO. Requires 1.8 V or 3.3 V external power supply.
VDDO4	65	Power	**VDDO4.** Power for crystal and reset blocks. Requires 3.3 V external power supply.
Analog Power			
AVDDH	42	Power	**AVDDH.** Requires 3.3 V external power supply.
AVDDH_HP	41	Power	**AVDDH_HP.** Headphone power. Connect to 3.3 V.
AVDD_CLSDL	29	Power	**Class-D Left Channel Input Power.** This pin can be powered by 3.3 V or 5.0 V. If 3.3 V, maximum speaker power output is 1.0 W per channel. If 5V, maximum speaker power output is 2.5 W per channel.
AVDD_CLSDR	32	Power	**Class-D Right Channel Input Power.** This pin can be powered by 3.3 V or 5.0 V. If 3.3 V, maximum speaker power output is 1.0 W per channel. If 5 V, maximum speaker power output is 2.5 W per channel.
Reference Voltage			
CLSD_REF	34	Power	**Class-D Reference Voltage.** Internally generated supply that is 1.7 V if Class-D power on Pins: 29, 32 = 5 V 350 mV if Class-D power on Pins: 29, 32 = 3.3 V, depending on Class-D input power on pins 29 and 32.
VREF	43	Power	**VREF.** Internally generated 1.65 V supply.
MICBIAS_L	56	Power	**Left Microphone Bias.** Can be programmed to be 50% or 80% of 3.3 V.
MICBIAS_R	59	Power	**Right Microphone Bias.** Can be programmed to be 50% or 80% of 3.3 V.
Ground Signal			
GROUND	77	Ground	**Ground.** Connect the device paddle to ground on the PCB.

5.4 Electrical Characteristics

5.4.1 Power Supplies

Table 44. General

Parameter	Minimum	Nominal	Maximum	Unit	Comments
1.8 V supply voltage	1.71	1.8	1.89	V	VDD, VDDO
3.3 V supply voltage	3.15	3.3	3.45	V	AVDDH, AVDDH_HP, DVDDH, VDDO
Speaker driver supply voltage 5 V mode 3.3 V mode	 4.75 3.15	 5.0 3.3	 5.25 3.45	V	AVDD_CLDL, AVDD_CLDR

5.4.2 Absolute Maximum Ratings

Table 45. Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Unit	Comments
1.8 V supply voltage	-0.4		1.98	V	VDD, VDDO
3.3 V supply voltage	-0.4		3.60	V	AVDDH, AVDDH_HP, DVDDH, VDDO
Speaker driver supply voltage 5 V mode 3.3 V mode	 -0.4 -0.4		 5.5 3.6	V	AVDD_CLDL, AVDD_CLDR
Pin Voltage					
Input or Hi-Z Output	-0.4		VDDO+0.4	V	
Storage Temperature Range	-40		150	°C	Non operating temperature
Operating Temperature Range	-40		85	°C	
Temperature	-40	27	125	°C	Junction temperature

GENERAL NOTES:

1. Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.These are stress ratings only and functional operation under these conditions or at any other condition beyond those indicated for normal operation is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5.4.3 Analog Inputs and Outputs

Table 46. Line Inputs

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Gain	-34.5		12	dB	
Full scale input signal		1		Vrms	AC-coupled, 0 dB gain
Dynamic Range(1)		87		dBFS	A-weighted, 20 to 20 kHz
THD+N at -3 dB FS		-84		dBFS	20 to 20 kHz
Input resistance	5		15	kΩ	15k with 0 dB gain, 5k otherwise

Table 47. Mic Inputs

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Gain	0		42	dB	
Full scale input signal		1		Vrms	AC-coupled, 0 dB gain
Dynamic Range(1)		87		dBFS	A-weighted, 20 to 20 kHz Boost = 18 dB
THD+N at -3 dB FS		-80		dBFS	20 to 20 kHz Boost = 18 dB
Input resistance	5		15	kΩ	15k with 0 dB gain, 5k otherwise

Table 48. Sub Outputs

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Full scale output signal Single-ended mode Differential mode	 1	1	 2	Vrms	AC-coupled, programmable when differential
Output load	500			Ω	
Dynamic Range(1)	95			dBFS	A-weighted, 20 to 20 kHz
THD+N 500 Ω load, at -3 dB FS 10 kΩ load, at 0 dB FS			 -75 -85	dBFS	20 to 20 kHz
Crosstalk			-70	dB	

Table 49. Line Output

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Full scale output signal Single-ended mode Differential mode	 1	1	 2	Vrms	AC-coupled, programmable when differential
Output load	10			kΩ	
Dynamic Range(1)	92			dBFS	A-weighted, 20 to 20 kHz
THD+N at 0 dB FS			-85	dBFS	20 to 20 kHz into 10 kΩ load
Crosstalk			-70	dB	

Table 50. Headphone Output

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Full scale output signal		1.25		Vrms	
Output offset	-3	0	3	mV	
Output load	16	32		Ω	Can drive -3 dBFS into 16 Ω without clipping.
Dynamic Range(1)	95			dBFS	A-weighted, 20 to 20 kHz
THD+N at 0 dB FS			-80	dBFS	20 to 20 kHz into 32 Ω
Crosstalk			-70	dB	

Table 51. Charge Pump

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Input voltage	3	3.3	3.6	V	DVDDH
Output voltage	-2		-2.8	V	AVEE_CPUMP
Clock frequency		500		kHz	

Table 52. Speaker Output

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Full scale output signal 5 V mode 3.3 V mode		 2.8 2.1		Vrms	
Output load		4		Ω	
Dynamic Range(1)	85			dBFS	A-weighted, 20 to 20 kHz
THD+N at -3 dB FS			-60	dBFS	20 to 20 kHz into 4 Ω.

Table 53. Microphone Bias

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Output voltage	1.65		2.65	V	Programmable to be 50% or 80% of supply.

Table 54. Jack Sensing

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Input voltage	0		3.3	V	
Pad sampling interval		10		ms	
SAR clock rate		500		kHz	

Table 55. Monitor ADC

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Input voltage	0		3.3	V	

FOOTNOTES:

(1) Dynamic Range is the ratio of the full scale signal level to the RMS noise floor, in the presence of signal, expressed in dB FS. It should be measured by performing a THD+N measurement with a -60 dBFS signal.

(2) Performance data valid over full operating temperature range, -40 to 85 °C.

5.4.4 Digital Inputs and Outputs

Table 56. CX20709-12Z Digital I/O Pad Cells

3.3 V/V.1.8 V Input Pad Cells	
Signal Name	**Supply Level**
I2C_EN	VDDO1=3.3V / 1.8V
I2C_SPI_CSN	VDDO1=3.3V / 1.8V
I2S_PCM_1_RX_DAT	VDDO2=3.3V / 1.8V
I2S_PCM_2_RX_DAT	VDDO2=3.3V / 1.8V
PASS_THRU	VDDO2=3.3V / 1.8V
UART_RX	VDDO3=3.3V / 1.8V
RST_N	VDDO4=3.3V Schmitt & Pull-Up
TEST	VDDO4=3.3V
USB_5VDET	VDDO4=3.3V

3.3 V/V.1.8 V Output Pad Cells	
Signal Name	**Supply Level**
I2S_PCM_1_TX_DAT	VDDO2=3.3V / 1.8V
I2S_PCM_2_TX_DAT	VDDO2=3.3V / 1.8V
UART_TX	VDDO3=3.3V / 1.8V

I2C I/Os	
Signal Name	**Supply Level**
I2C_SPI_SCL	VDDO1=3.3V / 1.8V
I2C_SDA/SPI_MOSI	VDDO1=3.3V / 1.8V

3.3 V/1.8 V I/Os	
Signal Name	**Supply Level**
I2S_PCM_1_CLK	VDDO2=3.3V / 1.8V
I2S_PCM_1_RX_WS	VDDO2=3.3V / 1.8V
I2S_PCM_1_TX_WS	VDDO2=3.3V / 1.8V
I2S_PCM_2_WS	VDDO2=3.3V / 1.8V
I2S_PCM_2_CLK	VDDO2=3.3V / 1.8V
GPIO_[4:0]	VDDO3=3.3V / 1.8V
KS[2:0]	VDDO3=3.3V / 1.8V
NVDAT	VDDO1=3.3V / 1.8V
NVCLK	VDDO1=3.3V / 1.8V
SPI_MISO	VDDO1=3.3V / 1.8V

Oscillator	
Signal Name	**Supply Level**
XTLI	VDDO4=3.3V
XTLO	VDDO4=3.3V

USB I/O Pads	
Signal Name	**Supply Level**
USB_DP	VDDO4=3.3V
USB_DM	VDDO4=3.3V

The above table lists all CX20709-12Z digital IO pad cells. Their electrical characteristics are listed in Section 5.4.4.1.

5.4.4.1 3.3 V/1.8 V I/Os: I2S_PCM_1_CLK, I2S_PCM_1_RX_WS, I2S_PCM_1_TX_WS, I2S_PCM_2_WS, I2S_PCM_2_CLK, GPIO_[4:0], KS[2:0], NVDAT, NVCLK, SPI_MISO

NOTE: 3.3V/1.8V interface levels. These pads are not 5 V-tolerant.

Table 57. 3.3 V I/O Electrical Characteristics

		Minimum	Maximum	Units	Conditions[1]
Output Mode					OEN = 0
Output Low Voltage	VOL		0.4	VDC	IOL = + 9.2 mA
Output High Voltage	VOH	VDDO-0.4		VDC	IOH = –9.2 mA
Output Impedance (2)	Z7	12	45	Ω	
Input Mode					
Input Low Voltage - TTL	VIL		0.8	VDC	
Input High Voltage - TTL	VIH	2.0		VDC	
Input Current	IIL	–1	1	μA	OEN = 1

GENERAL NOTES: VDDO= 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = -40C to +125C.

Table 58. 3.3 V I/O Switching Characteristics

		C_L=7 pF	C_L=20 pF	C_L=50 pF	Units	Conditions[1]
Max Slew Rate (3)	SR7	6.2	3.1	1.8	V/ns	
Max Transition Time (3)	tT7	0.7	1.2	2.4	ns	

GENERAL NOTES:
1. VDDO= 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = -40C to +125C.
2. Slew rates and transition times are for the voltage transition between 25% and 75% of VDDO.

Table 59. 1.8 V I/O Electrical Characteristics

		Minimum	Maximum	Units	Conditions[1]
Output Mode					OEN = 0
Output Low Voltage	VOL7		0.45	VDC	IOL = +5.7mA
Output High Voltage	VOH7	VDDO-0.45		VDC	IOH = –5.7 mA
Output Impedance(2)	Z7	12	95	Ω	
Input Mode					
Input Low Voltage - CMOS	VILC	0	35	%VDDO	
Input High Voltage-CMOS	VIHC	65	100	%VDDO	
Input Current	IIL	-1	1	µA	OEN=1
GENERAL NOTES: VDDO= 1.65 V to 1.95 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.					

Table 60. 1.8 V I/O Switching Characteristics

		C_L=7 pF	C_L=20 pF	C_L=50 pF	Units	Conditions[1]
Max Slew Rate (3)	SR7	2.1	1.2	0.7	V/ns	
Max Transition Time (3)	tT7	0.9	1.5	3	ns	

GENERAL NOTES:
1. OEN is internally driven by CX20709-12Z.
2. Output impedances are for reference only, they are not tested.
3. Switching characteristics are for reference only, they are not tested.
4. VDDO= 1.65 V to 1.95 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.
5. Slew rates and transition times are for the voltage transition between 25% and 75% of VDD.

5.4.4.2 3.3 V/1.8 V Output Pad Cells: I2S_PCM_1_TX_DAT, I2S_PCM_2_TX_DAT, UART_TX, SPI_MISO

NOTE: 3.3 V/1.8 V interface levels. These pads are not 5 V-tolerant.

Table 61. 3.3 V Output Pad Electrical Characteristics

		Minimum	Maximum	Units	Conditions[1]
Output Mode					
Output Low Voltage	VOL		0.4	VDC	IOL = +9.2 mA
Output High Voltage	VOH	VDDO-0.4		VDC	IOH = –9.2 mA
Output Impedance (2)	Z7	12	45	Ω	
GENERAL NOTES: VDDO = 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.					

Table 62. 3.3 V Output Pad Switching Characteristics

		C_L = 7 pF	C_L = 20 pF	C_L = 50 pF	Units	Conditions[1]
Max Slew Rate (3)	SR7	6.2	3.1	1.8	V/ns	
Max Transition Time (3)	tT7	0.7	1.2	2.4	ns	

GENERAL NOTES:
1. VDDO= 3.0V to 3.6V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.
2. Slew rates and transition times are for the voltage transition between 25% and 75% of VDDO.

Table 63. 1.8 V Output Pad Electrical Characteristics

		Minimum	Maximum	Units	Conditions[1]
Output Mode					
Output Low Voltage	VOL7		0.45	VDC	IOL =+ 5.7 mA
Output High Voltage	VOH7	VDDO-0.45		VDC	IOH = -5.7 mA
Output Impedance (2)	Z7	12	95	Ω	
GENERAL NOTES: VDDO= 1.65 V to 1.95 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.					

Table 64. 1.8 V Output Pad Switching Characteristics

		C_L = 7 pF	C_L = 20 pF	C_L = 50 pF	Units	Conditions[1]
Max Slew Rate (3)	SR7	2.1	1.2	0.7	V/ns	
Max Transition Time (3)	tT7	0.9	1.5	3	ns	

GENERAL NOTES:
1. VDDO= 1.65V to 1.95V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.
2. Slew rates and transition times are for the voltage transition between 25% and 75% of VDDO.
3. Output impedances are for reference only, they are not tested.
4. Switching characteristics are for reference only, they are not tested.

5.4.4.3 3.3 V/1.8 V Input Pad Cells: I2C_EN, I2C_SPI_CSN, I2S_PCM_1_RX_DAT, I2S_PCM_2_RX_DAT, PASS_THRU, UART_RX

NOTE: 3.3 V/1.8 V interface levels. These pads are not 5 V-tolerant.

Table 65. 3.3 V Input Pad Cells Electrical Characteristics

		Minimum	Maximum	Units
Input Mode				
Input Low Voltage - TTL	VIL	0	0.8	VDC
Input High Voltage - TTL	VIH	2.0	VDDO	VDC
Input Current	IIL	–1	1	µA

GENERAL NOTES: VDDO = 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.

Table 66. 1.8 V Input Pad Cells Electrical Characteristics

		Minimum	Maximum	Units
Input Mode				
Input Low Voltage - CMOS	VILC	0	35	%VDDO
Input High Voltage- CMOS	VIHC	65	100	%VDDO
Input Current	IIL	–1	1	µA

GENERAL NOTES: VDDO= 1.65 V to 1.95 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C

5.4.4.4 Input Pad Cells: TEST, USB_5VDET (VDDO4=3.3V)

NOTE: 3.3 V interface levels. These pads are not 5 V-tolerant.

Table 67. 3.3 V Input Pad Cells Electrical Characteristics

		Minimum	Maximum	Units
Input Mode				
Input Low Voltage - TTL	VIL	0	0.8	VDC
Input High Voltage - TTL	VIH	2.0	VDDO	VDC
Input Current	IIL	–1	1	µA
GENERAL NOTES: VDDO = 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.				

5.4.4.5 RST_N (3.3 V Input with Schmidt and Pull-Up)

RST_N is a relatively low speed input pad cell with Schmitt trigger (hysteresis) input receiver.

Features:

- 3.3 V interface level. These pads are not 5 V-tolerant.
- Weak pull-up 3.3 V operation.

Table 68. 3.3 V RST_N Electrical Characteristics

		Minimum	Maximum	Units	Conditions (1)
Input Mode					
Input Low Voltage - Hysteresis	VILS	0	30	%VDDO	
Input High Voltage - Hysteresis	VIHS	70	0	%VDDO	
Input Hysteresis	VHYS	0.5		VDC	
Input Current - Pull-Up2	IPU2	–30	–6	µA	VIN=VSS
Pull-Up Resistance2	RPU2	130	315	kΩ	VIN=VSS

GENERAL NOTES:
1. VDDO = 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C.
2. Input pad with hysteresis and internal weak pull-up.

5.4.4.6 XTLI/XTLO (XTAL Oscillator)VDDO4 = 3.3V

3.3 V Crystal Oscillator Pad Cell

XTLI

XTLO

Features:

- Input receiver from XTLO to chip core has 150-250 mV hysteresis to help prevent parasitic feedback paths.
- Internal 1MΩ feedback resistor from XTLO to XTLI.

Table 69. XTLI/XTLO Electrical Characteristics

		Minimum	Maximum	Units	Conditions (1)
Output					
XTLO Output Low Voltage	VOL		0.4	VDC	XTLI=VDDO IOL=+1.5 mA
XTLO Output High Voltage	VOH	VDDO-0.4		VDC	XTLII=VSS IOH=-7.3 mA
XTLO Bias Voltage	VBXO	20	7.5	%VDDO	XTLI=HiZ IOL=IOH=0
XTLO Output Impedance (2)	Z0	300	1200	%VDDO	XTLI=VBXI XTLO=VBXO± 50 mV
Input					
XTLI Input Low Voltage	VIL	0	30	%VDDO	
XTLI Input High Voltage	VIH	70	100	%VDDO	
XTLI Low Input Current	IIL	–8	–1	μA	XTLI=VSS (XO=VDDO)
XTLI High Input Current	IIH	1	8	μA	XTLI=VDDO (XO=VSS)
XTLI Bias Voltage	VBXI	45	55	%VDDO	XTLI=HiZ IOL=IOH=0
XTLI Input Capacitance (2)	CIN		2	pF	XTLI=VBXI

GENERAL NOTES:
1. 3.6 V unless otherwise specified. Junction Temperature Tj = no external components.
2. Output impedance and input capacitance are for reference only, they are not tested.
3. The input capacitance is for the die only and does not include the capacitance of the packaging.

5.4.4.7 I2C I/Os: I2C_SPI_SCL, I2C_SDA/SPI_MOSI

Features:

- 3.3 V/1.8 V interface levels. These pads are not 5 V-tolerant
- Supports Standard and Fast Modes; not Hs Mode.
- Select either I^2C mode or SPI mode.

Note: VBUS is the voltage to which the external pull-up for the I^2C bus is connected. VBUS must be 3.3 V.

I^2C	Conditions
0 (SPI Mode)	The output buffer is push-pull and will drive PAD both low and high.
	The output buffer has normal GPIO delay.
	The output buffer has normal GPIO rise and fall times.
	The input receiver has normal GPIO delays.
	The input has reduced input levels and hysteresis so that it meets VIL>30% VDDO and VIH<70% VDDO for both 3.3 V$\pm$10% and 1.8 V$\pm$10% VDDO ranges.
1 (I2C mode)	The output buffer is open drain and will only drive PAD low.
	The output buffer has a long delay.
	The output buffer has a long fall time as required by the i^2c specification.
	The input receiver has a glitch rejection filter to reject pulses less than 50 ns as required by the i^2c specification. This makes the input receiver delay very long; at least 50 ns and up to about 150 ns for the 3.3 V operation. Maximum delay for the 1.8 V operation can be as high as 400 ns.
	The input levels are consistent with the i^2c specification.

Table 70. 3.3 V I2C_SPI_SCL, I2C_SDA/SPI_MOSI Electrical Characteristics

		Minimum	Maximum	Units	Conditions (1)
Output Mode					OEN=0
Output Low Voltage	VOL0		0.4	VDC	I2C=X IOL=+3.0 mA
Output High Voltage	VOH0	VDDO-0.4		VDC	I2C=0 IOH=-3. 0mA
Output Impedance (2)	Z0		45	Ω	I2C=0
Maximum SSO (per VDDO/VSSO pin)	SSO		6		I2C=0
Input Mode					OEN=1
Input Low Voltage	VIL	0	30	%VDDO	I2C=0
I^2C Input Low Voltage – 3.3 V Bus	VIL3	0	30	%VDDO	I2C=1 VDDO=VBUS=3.3V ±10%
Input High Voltage	VIH	70	100	%VDDO	I2C=0
I^2C Input High Voltage - 3.3 V Bus	VIH3	70	100	%VDDO	I2C=1 VDDO=VBUS=3.3V ±10%
Input Hysteresis	VHYS	5		%VDDO	
Input Hysteresis - 3.3 V Bus	VHYS3	5		%VDDO	I2C=1 VDDO=VBUS=3.3V ±10%
Input Current	ILL	–1	1	μA	I2C = 1 VIN=VSS
GENERAL NOTES: VDDO= 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C					

Table 71. 1.8 V I2C_SPI_SCL, I2C_SDA/SPI_MOSI Electrical Characteristics

		Minimum	Maximum	Units	Conditions (1)
Output Mode					OEN=0
Output Low Voltage	VOL1		0.2VDDO	VDC	I2C=X IOL=+3.0 mA
Output High Voltage	VOH1	VDDO-VOL1		VDC	I2C=0 IOH=-3. 0mA
Output Impedance (2)	Z0		96	Ω	I2C=0
Maximum SSO (per VDDO/VSSO pin)	SSO		6		I2C=0
Input Mode					OEN=1
Input Low Voltage – Hysteresis	VIL	0	30	%VDDO	I2C=0
I^2C Input Low Voltage - Hysteresis 1.8 V Bus	VIL1PS	0	30	%VDDO	I2C=1 VDDO=VBUS=1.8V ±10%
Input High Voltage - Hysteresis	VIH	70	100	%VDDO	I2C=0
I^2C Input High Voltage - 1.8 V Bus	VIH3	70	100	%VDDO	I2C=1 VDDO=VBUS=1.8V ±10%
Input Hysteresis	VHYS	10		%VDDO	
Input Hysteresis - 1.8 V Bus	VHYSIPS3	10		%VDDO	I2C=1 VDDO=VBUS=3.3V ±10%
Input Current	ILL	–1	1	μA	I2C = 1 VIN=VSS

GENERAL NOTES:

1. OEN & I2C are internal signals that control the mode of the driver and receiver.
2. Output impedances are for reference only, they are not tested.
3. VDDO= 1.65V to 1.95V unless otherwise specified. Junction Temperature Tj = -40 °C to +125 °C.
4. OEN: Active Low Output enable for the 3-state buffer driving PAD, controlled by core logic. Not accessible to user.
5. I2C: Mode control; selects either I2C mode or GPIO mode.

5.4.4.8 USB I/O Pads: USB_DP, USB_DM

USB_DP, USB_DM is a full-speed USB pad cell.

Features:

- Designed for Rs = 22 Ω (±1% tolerance) external series resistor on DM and DP.
- Internally designed, selectable Pull-up Resistor (Rpu) to VDDO on DP

Table 72. USB I/O Rpu Control

Bus State	Minimum (Ω)	Typical (Ω)	Maximum (Ω)	Conditions (3)
Transmitting		OPEN		
Receiving	1425	2237	3090	
Idle	900	1237	1575	

***Table 73. USB I/O Electrical Characteristics** (1 of 2)*

		Minimum	Maximum	Units	Conditions (1)
Output Mode					TXEN=1
Output Low Voltage	VOL0		0.4	VDC	IOL= +10 mA
USB “DC Drive”	VOLDC		0.3	VDC	R=1.5 kΩ to VDDO
USB “DC Drive” (2)	VOLDC1		0.3	VDC	IOL= +2.32 mA
USB “AC Drive“(2)	VOLAC		27	%VDDO	IOL=VDDO×+6.10 mA
Output High Voltage	VOH	VDDO-0.4		VDC	IOH= –10 mA
USB “DC Drive”	VOLDC	2.8		VDC	R=15 kΩ to VSS
USB “DC Drive” (2)	VOLDC1	2.8		VDC	IOH= -0.20 mA
USB “AC Drive “(2)	VOHAC	73		%VDDO	IOH=VDDO × –6.10 mA
Output Impedance (3)	ZO	14	36	Ω	Rs = 0
Output Impedance (2) (3)	Z22	28	44	Ω	
Single-Ended Inputs					
Input Low Voltage	VIL	0	0.8	VDC	
Input High Voltage	VIH	2.0	VDDO	VDC	
Differential Inputs					
Differential Input Voltage	VDI	0.2		VDC	
Common Mode Voltage	VCM	0.8	2.5	VDC	

Table 73. USB I/O Electrical Characteristics *(2 of 2)*

		Minimum	Maximum	Units	Conditions (1)
Input Low Condition	VCM_min < DP < DP+VDI < DM < VCM_max				
Input High Condition	VCM_min < DM < DM+VDI < DP < VCM_max				
Input Current		–1	1	μA	TXEN = 0
GENERAL NOTES: VDDO= 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = –40 °C to +125 °C					

NOTES:

1) Rpu and TXEN are internal signals that control the mode of the driver, receiver (s) and pull-up resistor. Not accessible to user.

2) Based on USB Full Speed Mode V/I Characteristics.

3) Output impedance is for reference only and is not tested.

4) TXEN INPUT Output enable for the 3-state buffer driving DM and DP. Active high. Controlled from the chip core. Not accessible to user.

5) Rpu INPUT Pull-up resistor select from the chip core. Not accessible to user.

6) VDDO = 3.0 V to 3.6 V unless otherwise specified. Junction Temperature Tj = -40 °C to +125 °C.

7) Slew rates and transition times are for the voltage transition between 25% and 75% of VDDO.

5.4.5 Power Consumption

Table 74. CX2070x-12Z Power Consumption *(1 of 3)*

Scenario	AVDDH (3.3 V) (mA)	DVDDH (3.3 V) (mA)	AVDDH _HP (3.3 V) (mA)	AVDD_ CLASSD (5 V) (mA)	DVDD (1.8 V) (mA)	DVDDO (3.3 V) (mA)	Power (mW)
USB							
Suspend	0.23	0.38	0.28	3.60	0.00	1.09	24.56
Idle	2.74	0.38	0.28	4.90	67.60	4.55	172.46
Mono Record from Microphone NR on, AGC on	10.33	0.41	0.28	4.90	82.40	5.55	227.53
Stereo Record from Line In NR on	9.28	0.41	0.31	5.20	79.70	5.51	220.65
Full Duplex Mono mic record, playback to HP 5mW/ch (0.405 mVrms @ 33 Ω) NR on, AGC on	14.38	16.64	15.62	5.20	91.20	5.67	362.78
Stereo Playback to Headphone Zero Amplitude Disabled AGC, NR, AEC	6.77	9.23	8.26	4.90	74.70	4.64	254.31
Stereo Playback to Headphone 5mW per channel(0.405 mV @ 33 Ω) Disabled AGC, NR, AEC	6.77	16.77	15.74	4.90	76.50	4.64	307.13
Stereo Playback to Headphone 10mW per channel(0.575 mV@ 33 Ω) Disabled AGC, NR, AEC	6.77	21.44	20.36	4.90	76.50	4.63	337.73
Stereo Playback to Headphone 33 mW per channel (1.05 Vrms @ 33 Ω) Disabled AGC, NR, AEC	6.77	34.67	33.54	5.10	76.50	4.65	425.97
Stereo Playback to Line Out (1.0 Vrms per channel) Disabled AGC, NR, AEC	6.18	0.41	0.31	5.10	76.40	4.66	201.16
Stereo Playback to Class D Zero Signal Disabled AGC, NR, AEC	16.00	1.13	0.28	15.30	75.10	4.64	284.43
Stereo Playback to Class D 256 mW per channel, 1000 Hz, Sine Wave Disabled AGC, NR, AEC	15.97	1.13	0.28	142.40	77.10	4.63	923.42
Stereo Playback to Class D 1.0 W per channel, 497 Hz, Square Wave Disabled AGC, NR, AEC	15.97	1.10	0.31	393.80	76.30	4.62	2178.95

***Table 74. CX2070x-12Z Power Consumption** (2 of 3)*

Scenario	AVDDH (3.3 V) (mA)	DVDDH (3.3 V) (mA)	AVDDH _HP (3.3 V) (mA)	AVDD_ CLASSD (5 V) (mA)	DVDD (1.8 V) (mA)	DVDDO (3.3 V) (mA)	Power (mW)
I^2S							
Suspend Sleep Enabled (0x117E, Bit 7 = 1)	2.77	0.41	0.31	5.20	0.00	0.48	39.09
Suspend Deep Sleep Enabled (0x117E, Bits 6 and 7 = 1)	0.23	0.41	0.31	3.80	0.00	0.45	23.63
Idle All streams off	2.74	0.38	0.28	5.10	67.70	4.06	172.00
Idle All streams off CPX optimized, 0x117E = 0x24 (CPX = 3 MHz)	2.74	0.41	0.31	5.20	51.80	4.06	144.05
Stereo Record from Microphone Stream 2 --> VP --> Stream 5, Other streams off NR on, AGC on	10.36	0.41	0.31	5.10	80.60	3.99	220.31
Stereo Record from Line In, Single Ended Stream 1 --> VP --> Stream 5, Other streams off	9.28	0.44	0.31	5.20	86.10	3.98	227.21
Full Duplex Microphone to I2S1, I2S1 to HP 5mW per channel (0.405 mVrms @ 33 Ω) AGC on, NR on	14.38	16.64	15.62	5.10	90.40	3.96	355.20
Stereo Playback to Headphone Zero Amplitude Disabled AGC, NR, AEC	6.79	9.23	8.26	5.10	75.40	3.95	254.39
Stereo Playback to Headphone 33 mW per channel (1.05 Vrms @ 33 Ω) Disabled AGC, NR, AEC	6.77	33.33	32.18	5.10	76.40	3.93	414.53
Stereo Playback to Headphone 10mW per channel (0.575 mV @ 33 Ω) Disabled AGC, NR, AEC	6.77	21.41	20.36	5.10	76.40	3.94	336.21
Stereo Playback to Line Out 1.0 Vrms sine wave per channel Disabled AGC, NR, AEC	6.18	0.41	0.31	5.10	76.40	3.94	198.79
Stereo Playback to Class D Zero Signal Disabled AGC, NR, AEC	16.00	1.13	0.31	15.70	75.40	3.95	284.79

Table 74. CX2070x-12Z Power Consumption *(3 of 3)*

Scenario	AVDDH (3.3 V) (mA)	DVDDH (3.3 V) (mA)	AVDDH _HP (3.3 V) (mA)	AVDD_ CLASSD (5 V) (mA)	DVDD (1.8 V) (mA)	DVDDO (3.3 V) (mA)	Power (mW)
Stereo Playback to Class D 254 mW (1.009 Vrms) per channel Disabled AGC, NR, AEC	16.00	1.13	0.31	134.90	76.40	3.93	882.54
Stereo Playback to Class D 2.0 W (2.83 Vrms), per channel Disabled AGC, NR, AEC	15.92	1.10	0.28	1031.00	76.60	3.92	5362.92

GENERAL NOTES:
1. Typical condition: 25 ^{o}C, 1.8 V, 3.3 V, and 5.0 V
2. Class-D speaker load: 4 Ω
3. All power figures include the 4 Ω external speaker load and/or the 33 Ω headphone load.

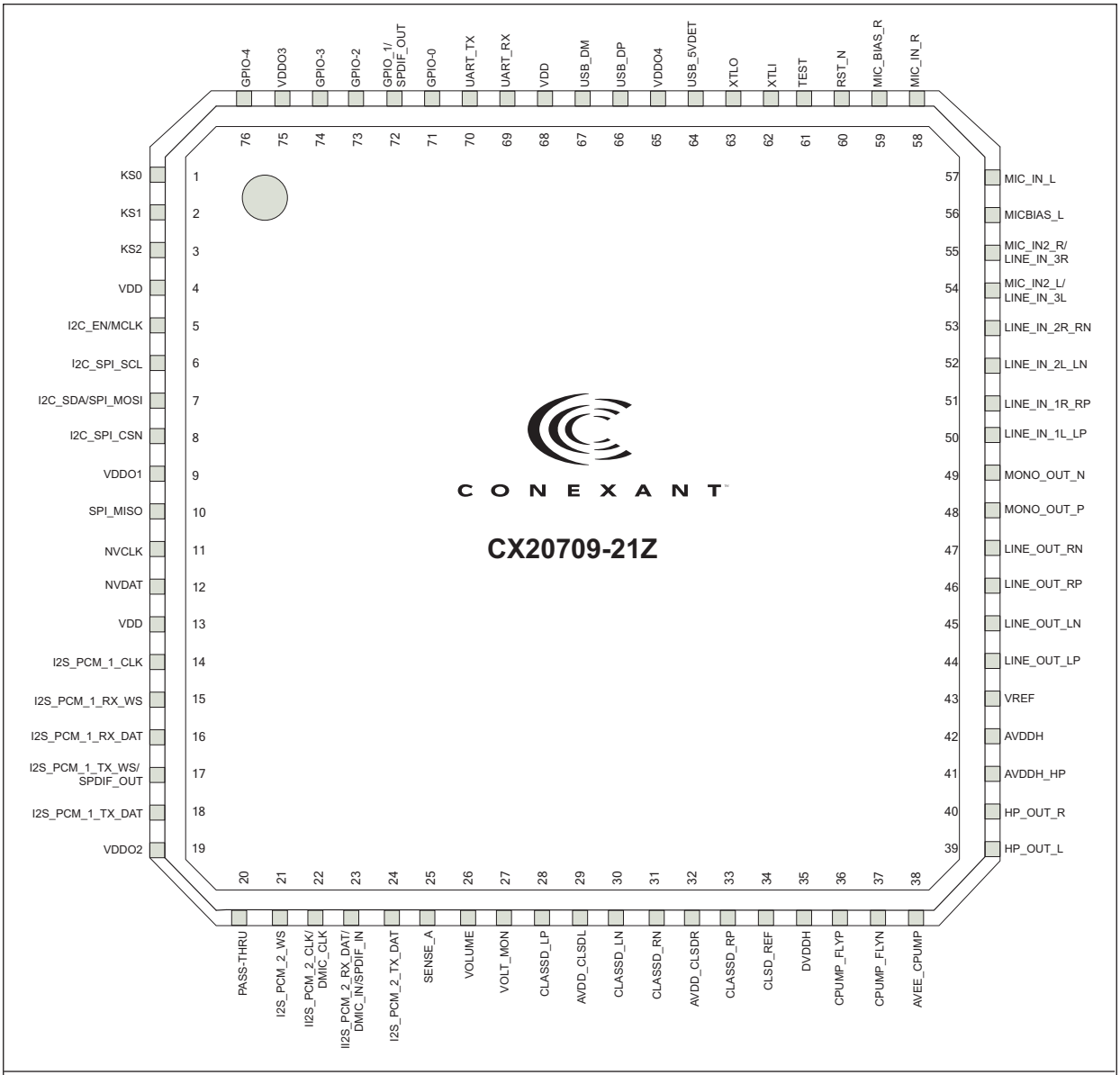
5.4.6 CX20709-12Z Power Sequencing

Please refer to APN-202411-XXX, Application Note 8 - *CX2070x Layout Guide* for CX20709-12Z power sequencing.

5.5 CX20709-12Z Pin Diagram

Figure 33 provides a diagram of the 76-pin QFN.

Figure 33. CX20709-12Z 76-Pin QFN Diagram

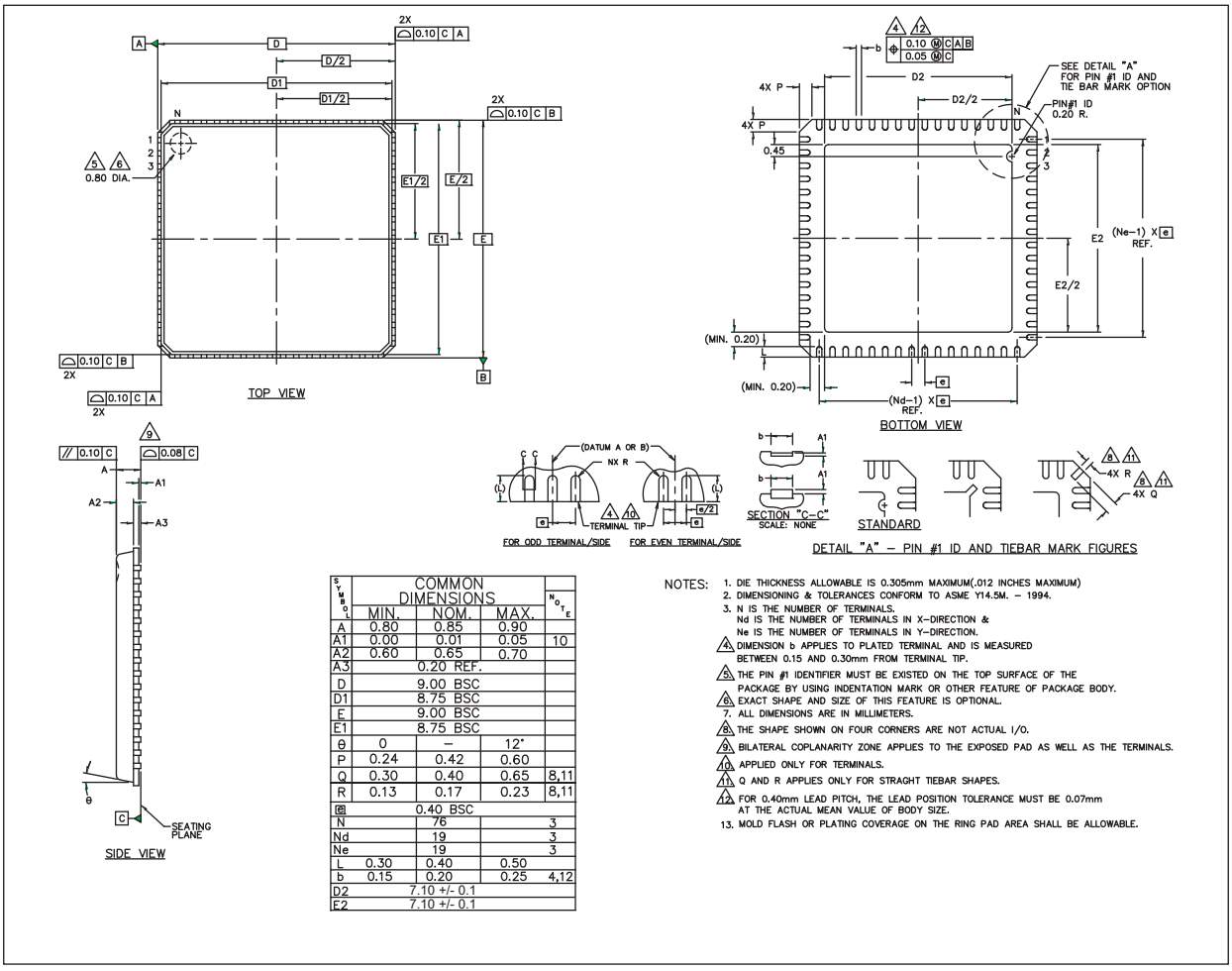


GENERAL NOTE: Pin 77 is the ground paddle and should be tied to system ground.

5.6 CX20709-12Z Package Dimensions

Figure 34 provides the package dimensions.

Figure 34. Package Dimensions: 76-Pin QFN



SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	10
A2	0.60	0.65	0.70	
A3		0.20 REF.		
D		9.00 BSC		
D1		8.75 BSC		
E		9.00 BSC		
E1		8.75 BSC		
θ	0	–	12°	
P	0.24	0.42	0.60	
Q	0.30	0.40	0.65	8,11
R	0.13	0.17	0.23	8,11
e		0.40 BSC		
N		76		3
Nd		19		3
Ne		19		3
L	0.30	0.40	0.50	
b	0.15	0.20	0.25	4,12
D2		7.10 +/- 0.1		
E2		7.10 +/- 0.1		

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
10. APPLIED ONLY FOR TERMINALS.
11. Q AND R APPLIES ONLY FOR STRAGHT TIEBAR SHAPES.
12. FOR 0.40mm LEAD PITCH, THE LEAD POSITION TOLERANCE MUST BE 0.07mm AT THE ACTUAL MEAN VALUE OF BODY SIZE.
13. MOLD FLASH OR PLATING COVERAGE ON THE RING PAD AREA SHALL BE ALLOWABLE.

5.6.1 Package Thermal Data

Table 75. Package Thermal Data

Die Power (W)		2.0	
Ambient Temperature (°C)		85	
Airflow (m/s)	**T_J (°C)**	**Θ_{JA} (°C/W)**	**Θ_{JC} (°C/W)**
0	122.4	18.7	6.6

Table 76. Test Board and Conditions for Thermal Data

Size (in inches)	7” x 8”
Motherboard Thickness (in inches)	0.062”
Motherboard Material	FR4
Number of Layers in Motherboard	4

6 CX20709-12Z Device Description

6.1 Analog Audio Input Paths

6.1.1 Analog-Digital Converters

Four identical Analog-Digital Converters (ADCs) are grouped into two stereo pairs, one for mic and one for line in. Sample widths supported are 24 or 16 bits at sample rates of 8k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, 88.2k and 96k. A digital PGA with a gain range of -74 db to +5 db in 1 db steps is at the output of each ADC.

6.1.2 Line Inputs

Six analog input buffers with adjustable gain settings range from -34.5 db to +12 db in 1.5 db steps (32 settings). With the gain set at 0 db, the line input buffers are capable of accepting a 1 V RMS input signal. These input buffers are arranged in two groups of three each. Each group feeds an ADC input multiplexer and mixer. The multiplexer can select between a mix of the input channels or any individual channel. Mixer inputs can be individually muted. Two of the buffers in each group share a common single-ended or differential mode control.

The line inputs have the following configuration options:

- Power on/off for any individual buffer
- Power on/off for the mixer/multiplexer
- Multiplexer input source select
- Individual buffer gain setting

6.1.3 Microphone Input

Two analog input buffers with adjustable gain settings range from 0 db to 42 db in 6 db steps (eight settings). With the gain set at 0 db, the microphone buffer can accept a 1 V RMS input signal.

6.1.4 Microphone Bias Generator

The bias generator is capable of generating two programmable bias voltages, 2.64 V or 1.65 V (80% or 3.3 V or 50% of 3.3 V), to support two analog microphones. The bias voltages can be disabled, which puts the bias buffer in a low-power and high-impedance mode. The buffer output pads allow for a full 1 V RMS swing below ground without any impedance change.

6.1.5 Jack Sense

Jack sense is provided by a 4-bit Successive Approximation Register (SAR) and an externally located resistor divider network. Grounding a resistor indicates that an audio device is connected to the corresponding port. It is possible to map the four jack sense bits to any possible input or output port. The debounce time is adjustable with a default of 250 ms.

6.1.6 Monitor ADC

The monitor ADC consists of an input multiplexer and a 12-bit ADC. The multiplexer selects between two pins. One pin is intended to monitor a potentiometer connected to 3.3 V. The voltage reading is translated, by the controller firmware, into volume settings for the main stereo outputs. The second pin is intended for monitoring battery voltage levels. The measurement range is from 0 to 3.3 V. Sample conversion is initiated by the system controller.

6.2 Analog Audio Output Paths

6.2.1 Digital-Analog Converters

Three identical Digital-Analog Converters (DACs) are grouped as one stereo pair and a single DAC. Sample widths supported are 24 or 16 bits at sample rates of 8k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, 88.2k, and 96k. A digital PGA with a gain range of -74 db to +5 db in 1 db steps is at the input of each DAC.

Twelve bi-quad filters are on the output of each DAC. Ten of the bi-quads are used to create a spectrum equalizer and two are available to create a high pass, low pass, or band pass filter to support 2.1 streaming (left, right and sub woofer). The coefficients for all twelve are user accessible. Also at the output of each DAC chain is a sample peak accumulator used for dynamic range compression feedback.

6.2.2 Differential/Single-ended Line Out (Stereo)

The line outputs can be configured for either single-ended or differential output. They can drive 1 V RMS into a 10k load and meet the DAC path performance requirements specified in Section 2.4. The line outs have the following configuration options:

- Power on/off
- Differential or single-ended operating mode
- 1 or 2 V RMS output level (differential mode)
- Mute on/off

6.2.3 2.5 W Class-D

These differential output drivers make up the CLASS-D speaker output. They can drive up to 2.5 W (when device is powered by fixed +5 V) into a rated 4 Ω speaker (3.2 Ω DC) and meet the speaker path performance requirements specified in Section 2.4. If powered by less than +5 V, gains and overcurrent thresholds must be adjusted accordingly. The Class-D outputs have the following configuration options:

- Power on/off
- 2.5 W per channel @ 5 V; 1.0 W per channel @ 3.3 V
- Spread spectrum, low EMI clocking
- Single channel operation
- Over current protection, under voltage protection and over temperature protection

6.2.4 Capless Headphone Driver

Two output drivers can be configured for either line out (10 kΩ load) or headphone out (32 Ω load). They can drive 50 mW into an 32 Ω load or 1 V RMS into a 10 kΩ load and meet the DAC path performance requirements specified in Section 2.4. The Capless Headphone outputs have the following configuration options:

- Power on/off
- Mute on/off

6.2.5 Differential/Single-ended Line Out (Mono)

This output driver can be configured for either single-ended or differential output. It is intended to act as a line output and can drive 1 V RMS into a 10k load and meet the DAC path performance requirements specified in Section 2.4. It can also drive a 600 Ω audio coupling transformer directly in differential mode. The mono line out has the following configuration options:

- Power on/off
- Differential or single-ended operating mode
- 1 V (Single-ended) or 2 V RMS output level (Differential Mode)
- Mute on/off.

6.3 Digital Audio

6.3.1 USB

The USB interface is a 2.0 full-speed interface exposing a UAC compliant client. Stereo record and stereo playback are supported at all sample rates up to 96 kHz and bit widths up to 24 bits.

6.3.2 5-Wire PCM/I^{2}S/SPDIF (Digital Port 1) Interface

This five pin interface has several modes of operation. The first mode is as a five-wire I^{2}S interface. The fifth wire in this case is an independently controlled transmit frame clock. This allows for independent but related sample rates to be sent and received from the I^{2}S port. For example, it is possible to set the bit clock to support a 48k sample rate for playback through a pair of DACs and simultaneously record a 16k sample rate stream from a pair of ADCs. This is because the 48k and 16k have an integer relationship. The receive and transmit frame signal can be independently programmed for different bit counts.

The second mode is a traditional four-wire I^{2}S or PCM interface with the transmit word select configured to be an independent SPDIF output.

The third mode is a four-wire PCM interface. The PCM interface supports up to two slots of active input and up to three slots of active output out from a range of 1 to 32 slots.

The I^{2}S or PCM can be configured for master or slave modes, meaning clocking and sync or frame signals can be internally or externally generated. The maximum frequency of an external clock with a 50 percent duty cycle is 12.288 MHz.

The I^{2}S interface supports left-justified and right-justified data formats. Both the I^{2}S and PCM interfaces send or receive the MSB first.

SPDIF clocking is always internally generated. The SPDIF engine supports 16 or 24-bit PCM samples as well as AC3 data streams. The SPDIF header information is fully programmable. Sample rates of 44.1k, 48k, and 96k are supported.

This interface shares its power source with the four-wire PCM/ I^{2}S interface to allow for 1.8 or 3.3 V signal levels. A pass through pin allows the interface to be shared with another I^{2}S device. In pass through mode the transmit data pin is driven by the pass through pin instead of the internal interface engine.

6.3.3 4-Wire PCM/I^{2}S (Digital Port 2) Interface

This is a traditional four wire I^{2}S or PCM interface. The PCM interface supports up to two slots of active input and up to three slots of active output out from a range of 1 to 32 slots.

The I^{2}S or PCM can be configured for master or slave modes, meaning clocking and sync or frame signals can be internally or externally generated. The maximum frequency of an external clock with a 50 percent duty cycle is 12.288 MHz. The I^{2}S interface supports I^{2}S, left justified and right justified data formats. Both the I^{2}S and PCM interfaces send or receive the MSB first.

This interface shares the power source with the five wire PCM/ I^{2}S interface to allow for 1.8 or 3.3 V signal levels. A pass through pin allows the interface to be shared with another I^{2}S device. In pass through mode the transmit data pin is driven by the pass through pin instead of the internal interface engine.

6.3.4 I^{2}S Audio Interface Timing

The first digital port has five pins assigned to provide a bi-directional interface. They are CLK, TX_WS, TX_DAT, RX_WS, and RX DAT. (Refer to Table 77.) CLK can be either internally generated or externally supplied. Both TX_WS and RX_WS follow the direction programmed for CLK. If CLK is an input TX_WS and RX_WS are also inputs. If CLK is an output, TX_WS and RX_WS are also outputs. In Slave mode (CLK as input), we have:

- TX_WS and RX_WS are inputs.
- TX_WS & RX_WS are latched on the falling edge of CLK.
- TX_DAT is sent on the falling edge of CLK.
- RX_DAT is latched on the rising edge of CLK.

In Master mode (CLK as output), we have:

- TX_WS and RX_WS are outputs
- TX_WS & RX_WS are sent on the falling edge of CLK.
- TX_DAT is sent on the falling edge of CLK.
- RX_DAT is latched on the rising edge of CLK.

The second digital port has four pins assigned to provide a bi-directional interface. They are CLK, WS, TX_DAT and RX_DAT. (Refer to Table 77.) CLK can be either internally generated or externally supplied. WS follows the direction programmed for CLK. If CLK is an input, WS is also an input. If CLK is an output, WS is also an output. In Slave mode (CLK as input), we have:

- WS is an input.
- WS is latched on the falling edge of CLK.
- TX_DAT is sent on the falling edge of CLK.
- RX_DAT is latched on the rising edge of CLK.

In Master mode (CLK as output), we have:

- WS is an output.
- WS is sent on the falling edge of CLK.
- TX_DAT is sent on the falling edge of CLK.
- RX_DAT is latched on the rising edge of CLK.

Table 77. I^2S Audio Interface Parameters

Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
CLK	Frequency, CLK	Cl – 30 pF	256k		12.288	MHz
tsu1	Setup time, WS to CLK falling (in slave mode only)	14 pF	10			ns
th1	Hold time, WS from CLK falling (in slave mode only)	14 pF	5			ns
tsu2	Setup time, DAT to CLK rising	14 pF	10			ns
th2	Hold time, DAT from CLK rising	14 pF	5			ns
	WS frequency		8	48	96	kHz
	CLK duty cycle		40	50	60	%
	WS duty cycle		40	50	60	%
t_{D1}	Output delay time for TX_WS (for Digital Port 1)/ WS (for Digital Port 2) with respect to PCM[1,2]_CLK (in master mode only)	14 pF	—	—	5	ns
t_{D2}	Output delay time for PCM[1,2]_TXD with respect to PCM[1,2]_CLK	14 pF	—	—	12	ns

Figure 35. RX_WS/WS (Slave Mode) Setup and Hold

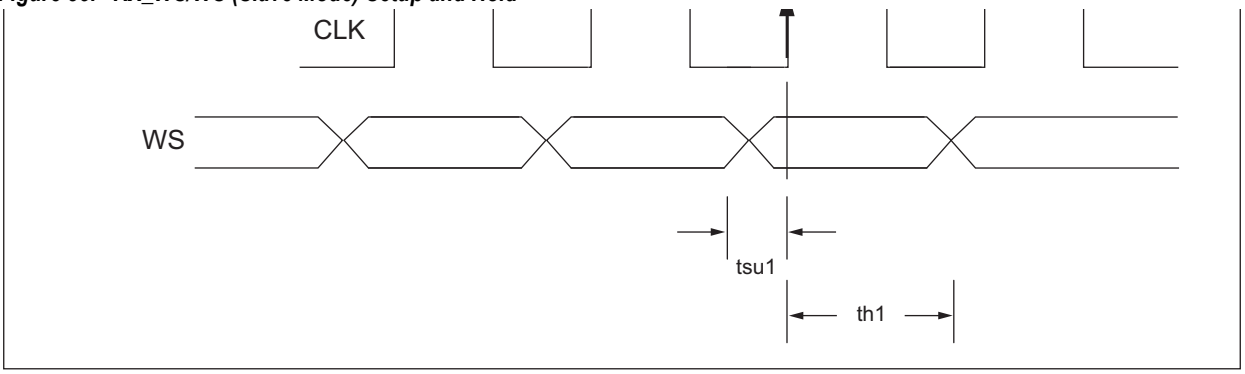


Figure 36. RX_DATA Setup and Hold

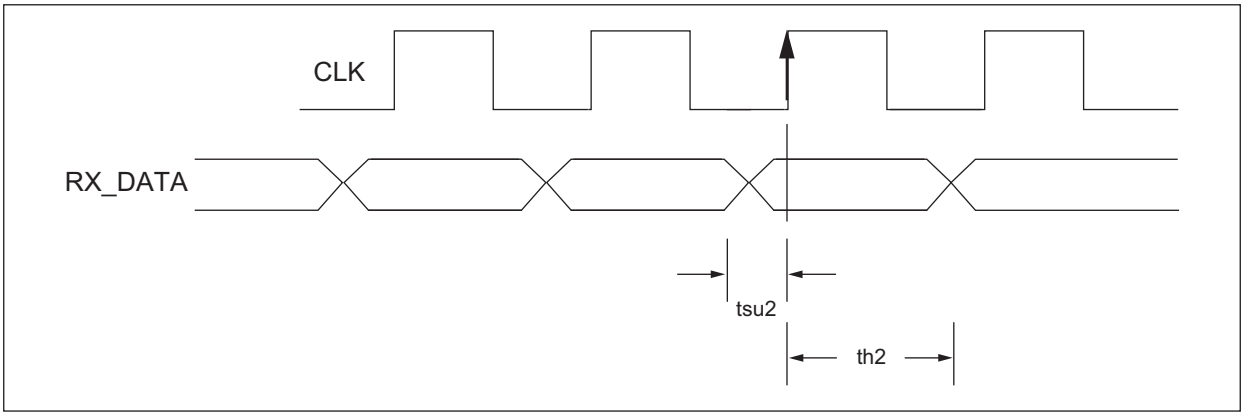
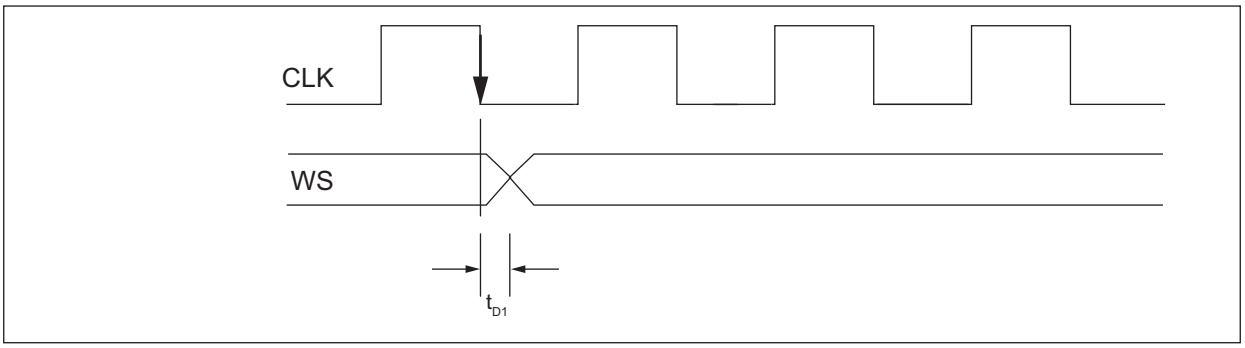
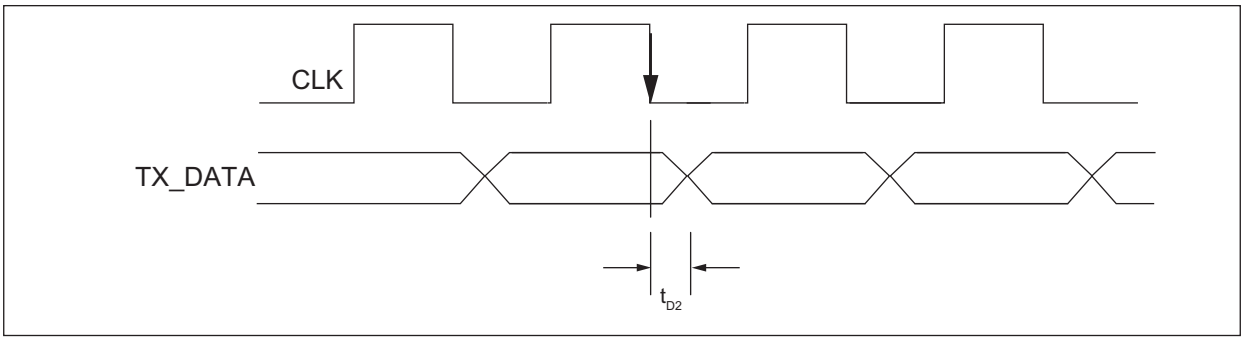


Figure 37. TX_WS /WS (Master Mode) Output Delay



NOTE: The I2S_PCM_1_CLK and I2S_PCM_2_CLK are hereinafter simply referred as CLK or BITCLK.

Figure 38. TX_DATA Output Delay



I^2S timing uses WS to define when the data being transmitted is for the left channel and when it is for the right channel. WS is low for the left channel and high for the right channel. WS need not be symmetrical. A bit clock (CLK) running at a minimum of 2 x (sample width) x sample frequency is used to clock in the data. There is a delay of one clock bit from the time the WS signal changes state to the first data bit on the data line. The data is written MSB first and is valid on the rising edge of the bit clock. Once the programmed sample width is taken any remaining bits are ignored.

Figure 39. I^2S Timing Diagram: Width of WS frame is wider than 2N bits. N=8, 16 or 24

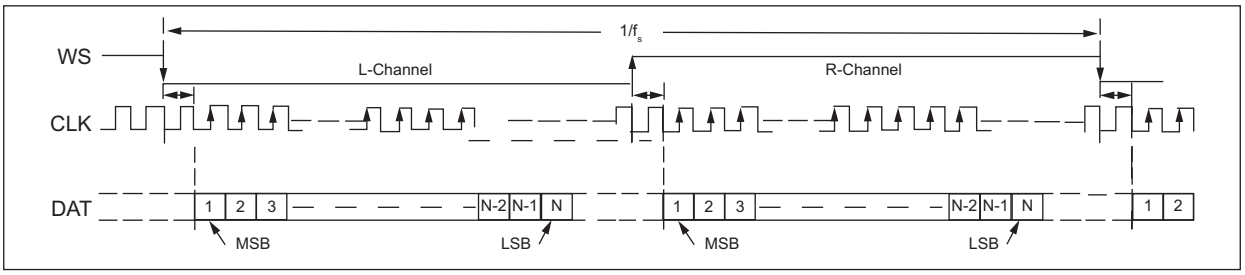
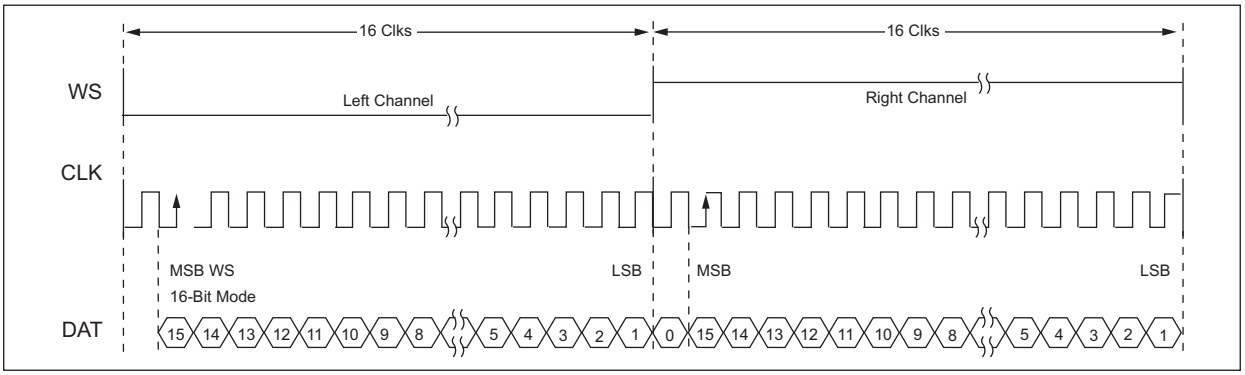


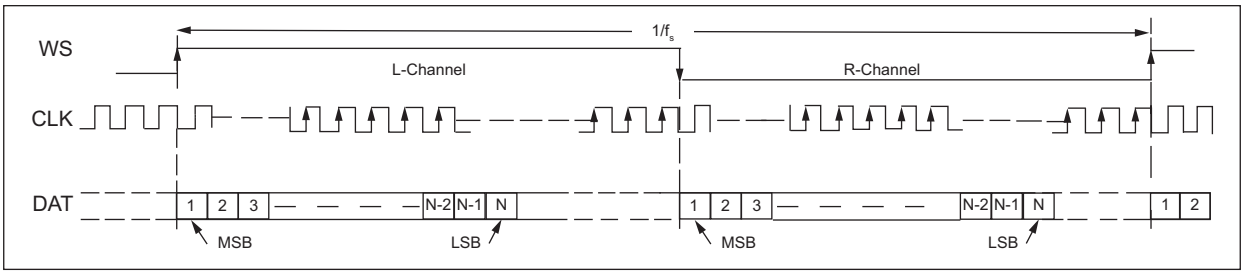
Figure 40. I^2S Timing Diagram 2: 16-Bit per Channel I2S



6.3.4.1 Left-Justified Timing

Left-justified timing uses WS clock to define when the data being transmitted is for the left channel and when it is for the right channel. WS is high for the left channel and low for the right channel. A bit clock running at a minimum of 2 x sample width x sample frequency is used to clock the data. The first data bit appears on the data lines at the same time WS toggles. The data is written MSB first and is valid on the rising edge of bit clock. Once the programmed sample width is taken, any remaining bits are ignored. If the WS toggles before the full word length is read, the remaining bits are zeroed.

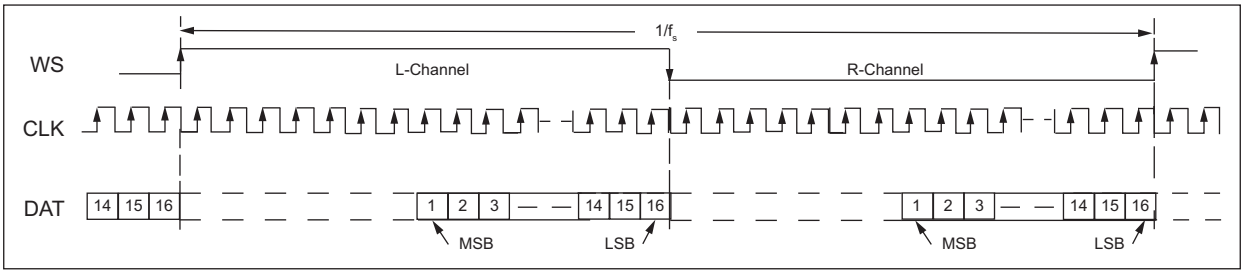
Figure 41. Left-Justified Timing Diagram



6.3.4.2 Right-Justified Timing

Right-justified timing uses WS clock to define when the data being transmitted is for the left channel and when it is for the right channel. WS is high for the left channel and low for the right channel. A bit clock running at a minimum of 2 x sample width x sample frequency is used to clock the data. Data is captured in a 24-bit shift register until WS toggles. Once WS toggles, the last 24, 16, or 8 bits are transferred to the channel indicated by the previous state of WS. In right-justified mode, the LSB of data is always clocked by the last bit clock before the WS transitions. The data is written MSB first and is valid on the rising edge of bit clock. All leading bits are ignored.

Figure 42. Right-Justified Timing Diagram



NOTE: For additional I^2S information, please refer to "I^2S Bus Specification" from NXP Semiconductor.

NOTE: For Right-Justified Timing or Left-Justified Timing, the WS is High for L-channel and Low for R-channel selection. They do not follow the convention of I^2S standard.

6.3.5 PCM Audio Interface Timing

The two PCM interfaces on CX20709-12Z support multiple audio streams divided into slots. Each slot is 8 bits wide and can support audio data of 8-bit A-Law/Mu-Law, 16- or 24-bit audio samples. 8-bit audio data takes up one slot per channel, while 16-bit audio takes 2 slots and similarly, 24-bit audio takes 3 slots per channel. CX20709-12Z PCM audio data are either in pairs or in 3 audio streams, supporting stereo audio (2-channel) or 2.1 audio (L, R and center), respectively. The audio streams are labeled as Stream 1 (L), Stream 2 (R) and Stream 3 (e.g., Center channel or sub-woofer), corresponding to their Stream Slot Control registers (namely, 0x0F57 through 0x0F5C and 0x0F62 through 0x0F67).

When the Stream 3 is unused, then Port 1 TX Stream 3 Slot Control Register (0x0F5C) and Port 2 TX Stream 3 Slot Control Register (0x0F67) may be left un-programmed.

Each PCM interface supports up to 32 8-bit slots. The user can use anywhere from 2 slots to all 32 slots for the transmission and reception of audio data.

The following examples are used to illustrate two typical PCM applications:

6.3.5.1 PCM Example 1: Requirement

16-bit audio, L & R channel

PCM slots used: 8 slots (4 slots of data, 4 slots for stuffing)

Sample rate: 48 kHz

Digital Port 1, Master mode

6.3.5.2 PCM Example 1: PCM Register Setting

0x0F50 = 0xF2 ; Port 1 Clock - 3.072 MHz (8*8*48 kHz), Port 2 slave or unused

0x0F51 = 0xB1 ; PCM - Tx/Rx data delayed by one clock cycle

0x0F52 = 0x07 ; 64 TX clocks / frame = (7+1)*8

0x0F53 = 0x07 ; 64 RX clocks / frame = (7+1)*8

0x0F54 = 0x00 ; PCM TX sync width = 1 clock cycle ' (0+1)

0x0F55 = 0x00 ; PCM RX sync width = 1 clock cycle ' (0+1)

0x0F56 = 0x05 ; 16-bit RX sample and 16-bit TX sample

0x0F57 = 0x20 ; enable RX Stream1, occupying slots 0 & 1 (L channel)

0x0F58 = 0x24 ; enable RX Stream2, occupying slots 4 & 5 (R channel)

0x0F5A =0x20 ; enable TX Stream1, occupying slots 0 & 1 (L channel)

0x0F5B= 0x24 ; enable TX Stream2, occupying slots 4 & 5 (R channel)

Note that in the above example, we purposely use 8 slots instead of 4 slots. 4 slots would have been sufficient to accommodate the two 16-bit audio samples. The user should be aware of the fact that there are 8 slots that are unused and are “wasted” or ignored. Also, if only 4 slots are used, then the clock rate can drop from 3.072 MHz down to 1.536 MHz. In addition, the TX/ RX Stream 2 slot will begin at Slot 2 (occupying Slot 2 and Slot 3).

The user may also choose different slots to start the Stream 2, say, Slots 2 and Slot 3 in the above case. This leaves slots 4 through 7 unused. The only requirement for slot allocation is that the audio data has to occupy contiguous slots should the sample size is large than 8 bits and TX slots for Stream 1, and Stream 2 *must* be distinct from each other. RX slots, however, may read from the same slot locations, thus, providing only L or only R audio PCM data at the receiving device.

6.3.5.3 PCM Example 2: Requirement

16-bit audio, L & R channel

PCM slots used: 4 slots (2 slots of L audio data, 2 slots of R audio data)

Sample rate: 48 kHz

Digital Port 1, Master mode

By eliminating the 4 'stuffing' slots, we have:

6.3.5.4 PCM Example 2: PCM Register Setting

0x0F50 = 0xF4 ; Port 1 Clock - 1.536 MHz, Port 2 slave or unused

0x0F51 = 0xB1 ; PCM - Tx/Rx data delayed by one clock cycle

0x0F52 = 0x03 ; 32 TX clocks / frame = (3+1)*8

0x0F53 = 0x03 ; 32 RX clocks / frame = (3+1)*8

0x0F54 = 0x00 ; PCM TX sync width = 1 clock cycle ' (0+1)

0x0F55 = 0x00 ; PCM RX sync width = 1 clock cycle ' (0+1)

0x0F56 = 0x05 ; 16-bit RX sample and 16-bit TX sample

0x0F57 = 0x20 ; enable RX Stream1, occupying slots 0 & 1 (L channel)

0x0F58 = 0x22 ; enable RX Stream2, occupying slots 2 & 3 (R channel)

0x0F5A =0x20 ; enable TX Stream1, occupying slots 0 & 1 (L channel)

0x0F5B= 0x22 ; enable TX Stream2, occupying slots 2 & 3 (R channel

Apply NewC thru the DINIT register. (Refer to CX20709-12Z Host API document.)

The first PCM port has five lines that make up the PCM interface: CLK, TX_WS, TX_DAT, RX_WS, and RX_DAT. In PCM mode, TX_WS and RX_WS act as the sync pulse. CLK, TX_WS, and RX_WS can either be internally generated or externally supplied.

The second PCM port has four lines that make up the PCM interface: CLK, WS, TX_DAT, and RX_DAT. In PCM mode WS is the sync pulse. Both CLK and WS can either be internally generated or externally supplied.

There are three modes of operation for PCM:

- Short frame mode
- Long frame mode
- Multi-slot mode

In short frame mode, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is one clock long. TX data is driven out on the rising edge of PCM_CLK after the PCM_SYNC pulse. RX data is strobed on the falling edge of PCM_CLK.

Figure 43. Short Frame Sync TX

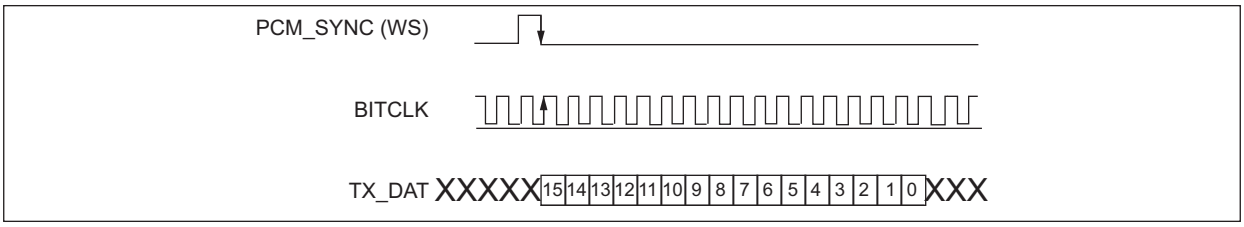
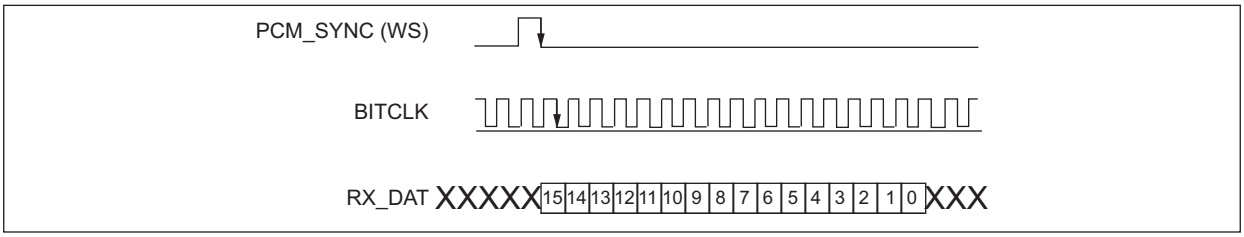


Figure 44. Short Frame Sync RX



In long frame mode, the rising edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is at least two clocks long. TX data is driven out on the rising edge of PCM_CLK coincident with the rising edge of PCM_SYNC. RX Data is strobed on the falling edge of PCM_CLK.

Figure 45. Long Frame Sync TX

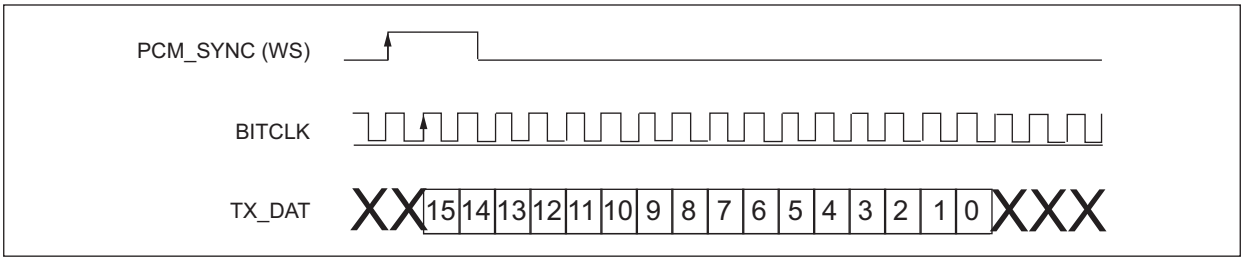
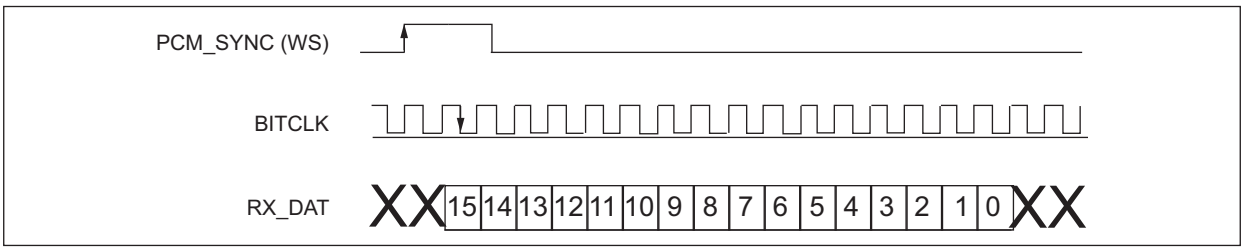


Figure 46. Long Frame Sync RX



In multi-slot mode, PCM_SYNC can be either long or short. Up to three streams of data can be sent or received. The position of the start of the PCM word is determined by the length of the sync pulse. Slots are determined by counting data width clocks (8, 16, or 24) from the first PCM word. (See the above two examples). In any case, unless the audio data is 8-bit A-Law/Mu-Law, stereo audio and 16-bit or 24-bit audio are always in multi-slot mode.

NOTES:

CX20709-12Z Firmware Version 3xx or earlier does not support A-Law / Mu-Law. CX20709-12Z Firmware Version 4xx provides A-Law / Mu-Law support.

Current CX20709-12Z firmware supports only Multi-Slot mode, single-slot mode is not yet supported.

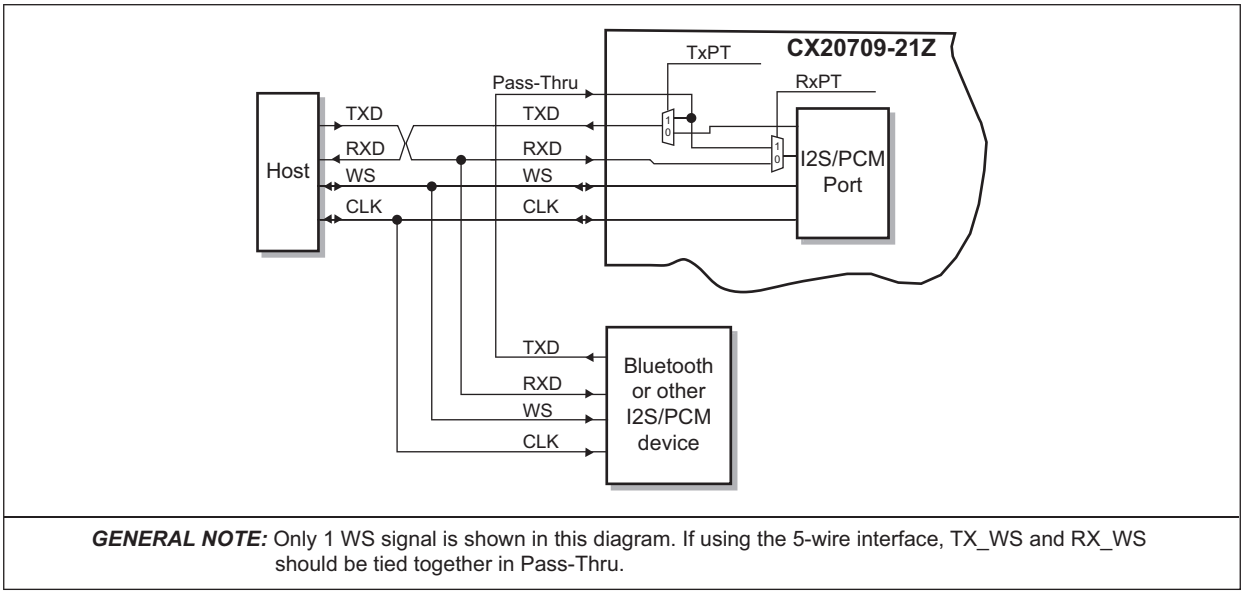
6.3.6 I²S/PCM Pass-Through Mode

The PASS_THRU pin allows the TX data from another I²S/PCM device to be routed through the PASS_THRU input to the TX output on the CX20709-12Z. This allows two slave devices to share the bus when normally the I²S/PCM interface would be point-to-point. The other three signals are received from the host or controlled by the CX20709-12Z (depending on master or slave mode) so they can be tied together. The TX signals cannot be tied together because the CX20709-12Z TX is a totem-pole output and is constantly driving a '0' or a '1'. The host uses the I²C bus to tell the CX20709-12Z which TX data should be sent. (see Figure 47).

The Pass-Through mode is controlled by the following hardware registers:

- Port 1 Control 2 Register 0x0F56[5:4]
- Port 2 Sample Width Register 0x0F61[5:4].

Figure 47. I²S/PCM Pass-Through Mode Diagram



GENERAL NOTE: Only 1 WS signal is shown in this diagram. If using the 5-wire interface, TX_WS and RX_WS should be tied together in Pass-Thru.

For PCM/I²S Register programming, refer to Chapter 4, Registers.

6.4 Control Interfaces

CX20709-12Z supports: I2C, SPI, UART, and USB HID interfaces for serial communications with CX20709-12Z registers for CX20709-12Z command and control.

6.4.1 SPI/I2C

The SPI/I2C interface is used for controlling the codec. The Conexant SPoC Configuration Toolbox uses the I2C interface to read/write the CX20709-12Z registers. The CX20709-12Z I2C interface supports serial, 8-bit oriented, bi-directional data transfers of rates up to 100 kbps in the Standard-mode, or up to 400 kbps in the Fast-mode. I2C read/write operations are described below. For additional details, please refer to the I2C specification.

6.4.1.1 I2C Write Operation

For a host writing to the slave CX2070x device:

1. Send a start sequence
2. Send the I2C address of the slave with the R/W bit low
3. Send the internal register address you want to write to. Send high byte followed by low byte.
4. Send the data byte
5. [Optionally, send any further data bytes] -- Burst operation
6. Send the stop sequence.

Write Single Location

S	Device Address	W (0)	A	ADDR byte 1	A	ADDR byte 0	A	DATA byte 0	A	P

Write Auto increment

S	Device Address	W (0)	A	start ADDR byte 1	A	start ADDR byte 0	A	DATA [n]	A	DATA [n+1]	A	DATA [n+2]	A	DATA [n+3]	A	P

6.4.1.2 I2C Read Operation

For a host reading from the slave CX2070X device:

1. Send a start sequence
2. Send I2C address with the R/W bit low
3. Send the internal register address you want to read. Send high byte followed by low byte.
4. Send a start sequence again (repeated start)
5. Send I2C address with the R/W bit high
6. Read data byte
7. [Optionally, send any further data bytes] -- Burst operation
8. Send the stop sequence.

Read Single Location

S	Device Address	W (0)	A	ADDR byte 1	A	ADDR byte 0	A	Sr	Device Address	R (1)	A	DATA byte 0	N	P

Read Auto increment

S	Device Address	W (0)	A	start ADDR byte 1	A	start ADDR byte 0	A	Sr	Device Address	R (1)	A	DATA [n]	A	DATA [n+1]	A	DATA [n+2]	A	DATA [n+3]	N	P

Read Continuing Auto increment

S	Device Address	R	A	DATA [n+4] byte 1	A	DATA [n+5] byte 0	A	DATA [n+6] byte 1	A	DATA [n+7] byte 0	N	P

6.4.2 CX20709-12Z SPI Interface

6.4.2.1 SPI/I²C Interface I/Os

CX20709-12Z is a SPI slave device.

I2C_SPI_SCL: CX20709-12Z SPI Serial Clock input, provided by SPI Master

I2C_SDA/SPI_MOSI: CX20709-12Z SPI Serial In (driven by SPI Master)

SPI_MISO: CX20709-12Z SPI Serial Output.

I2C_EN: I²C Enable. Selects I²C or SPI interface. Connect to VDDO1 for I²C mode, 0 V for SPI mode.

I2C_SPI_CSN – I2C_ SPI_CSN = 0 enables I²C/SPI; I2C_SPI_CSN = 1 disables I²C/SPI access. I2C_SPI_CSN is usually controlled by SPI host.

6.4.2.2 I²C/SPI Clock

The I²C and SPI modules share the same pin interface and thus, the same clock input, pin SCL. Pin I2C_EN selects the interface to be I²C or SPI. If I²C_EN is set to 1, the I²C module is active while the SPI is not. In the same manner, when I2C_EN is set to 0, and the I²C module is turned off.

The maximum SPI clock rate is 24 MHz, recommended maximum operating frequency is 9 MHz.

6.4.2.3 General Description: SPI Interface

The SPI slave controller is used to provide the serial interface to write to CX20709-12Z registers. It supports 13-bit addressing mode for all register read/writes. Data can be written in single or burst mode. Register read/write commands from external host or SPI master received are converted to appropriate commands to perform read/write from CX20709-12Z registers.

- Supports 8-bit register read/write through SPI slave interface
- Supports single and burst mode

6.4.2.4 SPI Register Read/Write Operation

The host can initiate register read or write to CX20709-12Z registers first by writing the control word 000xxxxxxxxxxxx or 100xxxxxxxxxxxx respectively after the falling edge of I2C_SPI_CSN.

The SPI interface logic decodes host commands:

- Write address and data are registered and written to CX20709-12Z registers.
- Read address is transferred to CX20709-12Z for register reads.

The CX20709-12Z responds by sending data back to SPI interface, which serializes the data and sends it to host over SPI interface.

Note that until data is received from CX20709-12Z, to meet SPI protocol, dummy data is sent as first byte, and when actual data is received from CX20709-12Z it is sent as second byte.

- Register read/write transfers can be 8/13-bit address modes.
- MOSI Input serial data is latched on the rising edge of SCK.
- MISO Output data is sent on the falling edge of SCK.
- Read/Write access is valid during CSN=0.

6.4.2.5 SPI Timing Information

Figure 48. SPI Timing

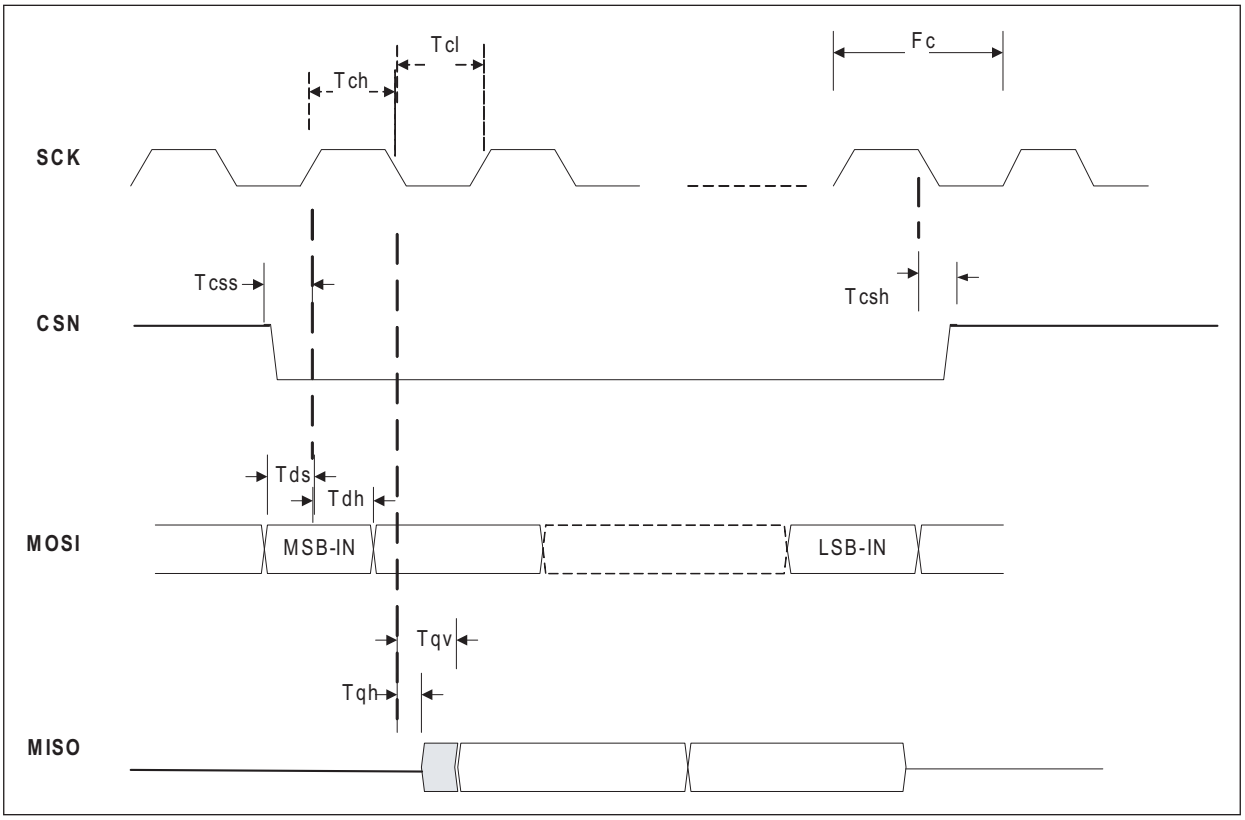


Table 78. Timing Parameters

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Fc	Clock Frequency			24	MHz
Tch	Clock High	18			ns
Tcl	Clock Low	18			ns
Tcss	Chip select Setup Time	7			ns
Tcsh	Chip select Hold Time	7			ns
Tds	Data-In Setup Time	5			ns
Tdh	Data-In Hold Time	5			ns
Tqv	Clock Low to output Valid			15	ns
Tqh	Output Hold Time	0			ns

Table 79. Control Word Format

Control Word	Description
0000xxxxxxxxxxxx	Read eight or sixteen bit register at address xxxxxx (Dummy data is sent as first byte for First Read)
1000xxxxxxxxxxx	Write to eight or sixteen bit register at address xxxxxx

6.4.2.6 SPI Read/Write Timing

The SPI commands are sent by the master on the SPI_MOSI pin at the rising edge of I2C_SPI_SCL. The commands are 3 bytes wide. CX20709-12Z addresses are 13 bits wide.

Write: 100---xxxxxxxxxxxxx---yyyyyyyy (The 13 bits following 100 is the address). Then followed by the 8 bits (yyyyyyyy) data being written.

Read: 000---xxxxxxxxxxxxx---00000000 (The 13 bits following 000 is the address).

Once the read is issued, wait for eight clock cycles and the data will be placed on the SPI_MISO line at the subsequent falling edge of I2C_SPI_SCL.

Figure 49. SPI Read Timing

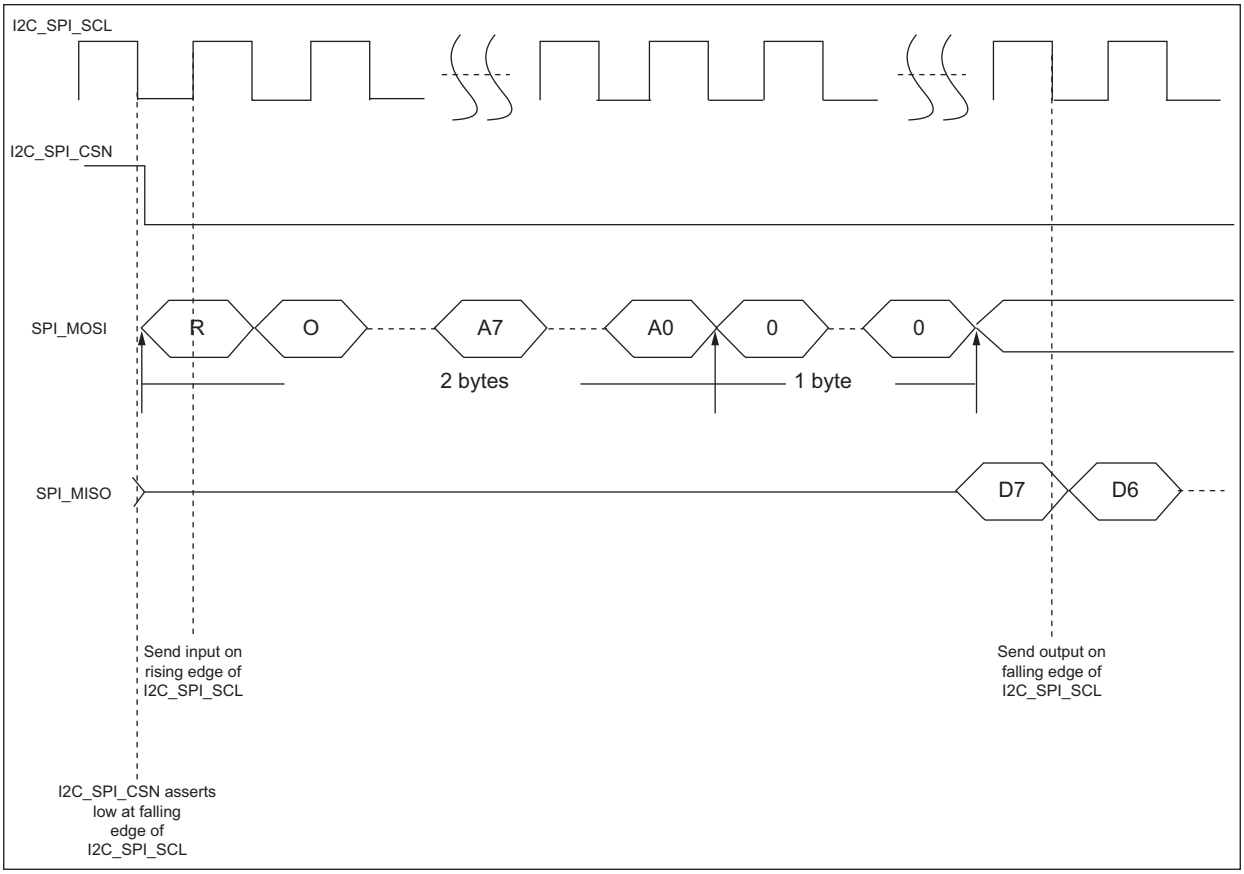


Figure 50. SPI Write Timing

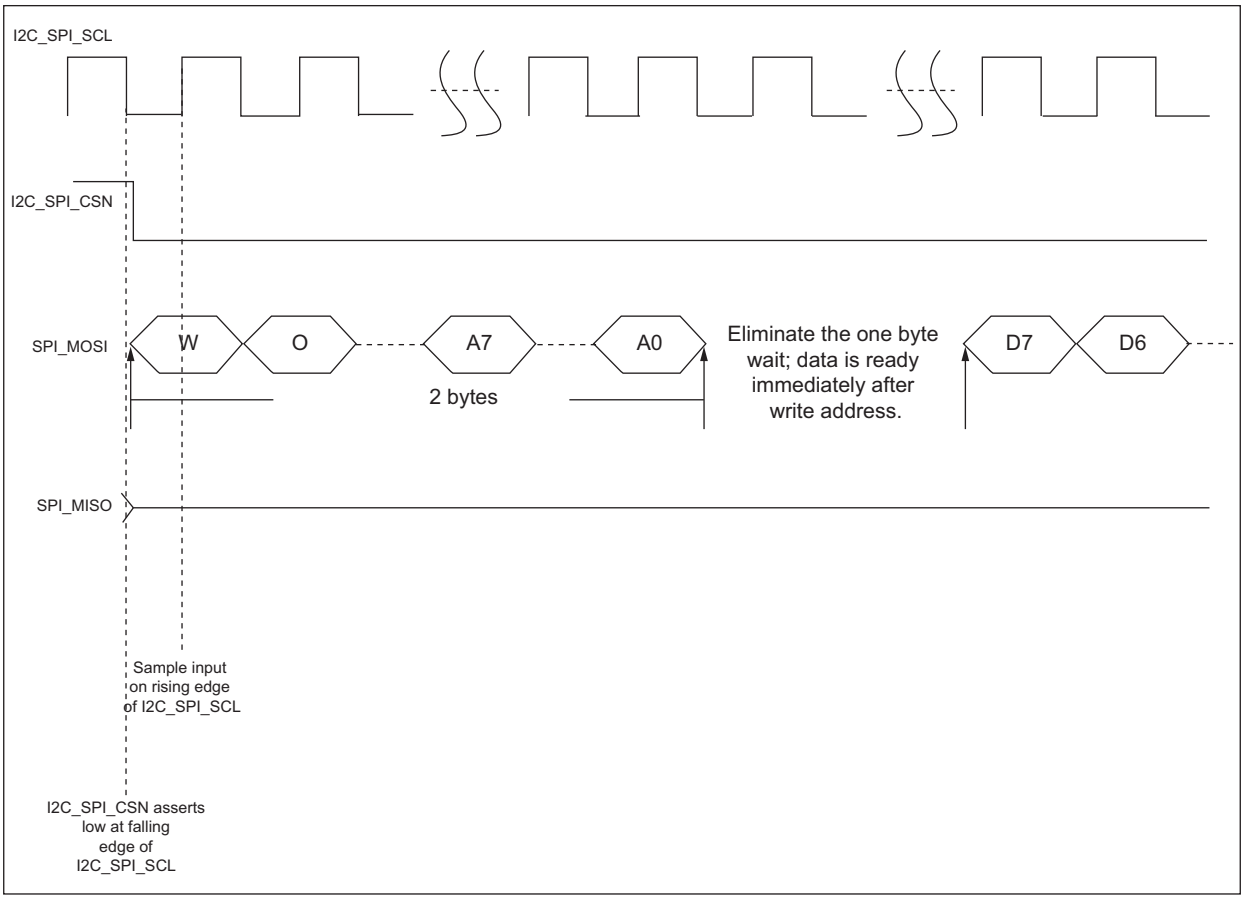
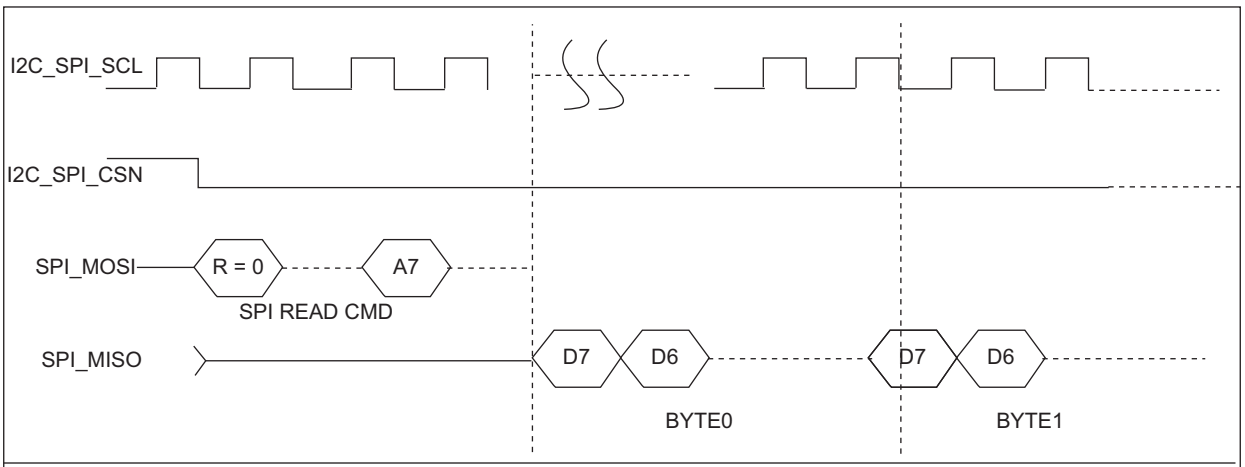
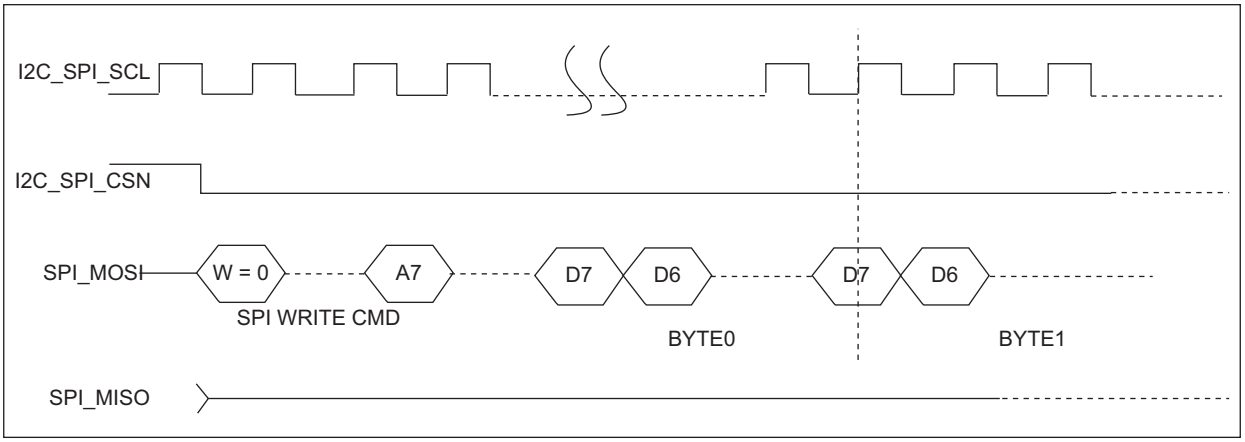


Figure 51. SPI Burst Read



GENERAL NOTE: After read address is presented, there is an 8-clockk-cycle wait time before valid data will come out from SPI_MISO (HSOMI).

Figure 52. SPI Burst Write



As long as I2C_SPI_CSN is asserted, the transactions are valid. If I2C_SPI_CSN stays asserted beyond 1 byte of data, the next data byte will be written to the next address location in an auto increment mode. The same is true in the case of reads. As long as I2C_SPI_CSN is asserted, registers will be read in auto increment mode.

6.4.3 GPIO

There are eight general purpose GPIO pins available. These are configured and controlled by the controller. There are pre-defined uses for these pins, but through code patching many other uses are possible. The GPIO block is powered by its own supply allowing 1.8 V or 3.3 V signaling. On reset the GPIO are configured as inputs to minimize power. GPIO can be configured as a wake source. This allows the analog, DSP, and controller to wake from a low-power state.

6.4.4 EEPROM

An I^2C master interface is dedicated for loading USB strings, controller patches, and DSP patches from an external EEPROM. An external 128kx8 (1-M bit) EEPROM is required for CX20709-12Z to operate.

CX20709-12Z firmware can be stored in the EEPROM for download to CX20709-12Z RAM upon power-up or hardware reset.

The EEPROM interface has two I^2C interface pins: NVCLK and NVDAT. CX20709-12Z acts as an I^2C master, reading external EEPROM data via the NVCLK and NVDAT pins (equivalent to SCL and SDA). NVCLK and NVDAT require external pull-up resistors interfacing to the EEPROM.

The EEPROM write data is obtained from CX20709-12Z internal RAM while EEPROM data is read upon power-up or hardware reset from an external 1Mb (128k x 8) NVRAM.

6.4.5 UART

The UART is a serial communication device that communicates with the CX20709-12Z registers. The pins are: UART_RX, UART_TX and the GPIO0 also serves as CTS. It operates at 115,200 bps, no parity bit, 8 data bits and 1 stop bit. For file transfer, the CTS should always be used to prevent UART buffer overflow.

6.4.6 Clock Source/Crystal

A 48 MHz crystal or oscillator is required for CX20709-12Z to operate.

The crystal (clock source) tolerance is + 200 ppm over temperature and voltage.

6.5 DSP

The CX20709-12Z DSP has 100 MIPs of processing power, and sufficient memory to support speakerphone, 2.1-channel audio, and 3D algorithms. The complete list of required algorithms is AEC, NR, Beam Forming, ALC, LEC, Digital Crossover, Equalizer, DRC, and 3D processing. The DSP is capable of mixing two stereo streams coming from any of the digital sources with one analog stream. The resulting mix can be sent to any digital or analog interface. Mixing will be done at 48 kHz and the sample rate converted to the requested output sample rate.

6.5.1 CX20709-12Z DSP Stream Routing

CX20709-12Z inputs and outputs are governed by audio streams. The following describe the audio stream routing and behavior of CX20709-12Z as governed by CX20709-12Z Firmware Version 5 and 4:

1. CX20709-12Z has four inputs streams, namely: Stream 1, 2, 3, & 4, plus a Function Generator Stream; and five output streams: Stream 5, 6, 7, 8, & 9.
2. Stream 1 is comprised of the three Line Inputs (Line In 1, 2, & 3).
3. Stream 2 is the microphone input stream, with a sampling rate of 8k or 16 kHz, for narrow-band or wide-band phone applications.
4. Stream 3 is sourced from Digital Port 1 (5-wire) or Digital Port 2 (4-wire); the audio stream is either in I2S or PCM format.
5. Stream 4 is sourced from Digital Port 1 (5-wire), Digital Port 2 (4-wire) or USB playback stream; the audio stream of Digital Port 1 or Digital Port 2 is either in I2S or PCM format.
6. Stream 5 is the Digital Port 1 output which also provides ASRC for sampling rate translation.
7. Stream 6 is the Digital Port 2 output which also provides ASRC for sampling rate translation.
8. Stream 7 outputs to either:
    a. SPDIF, or
    b. Stereo DAC to headphone, Line Out or Class-D with Equalizer.
9. Stream 8 outputs to the Mono DAC. Stream 8 sums the left and right signals into a mono stream:
    a. which also has a crossover equalizer, upon activation, can drive a Sub Woofer via an external amplifier. Sub Woofer output cutoff frequency is user selectable via the writing of API registers. Conexant recommends a low-pass cutoff frequency of 400 Hz or below for meaningful sub-woofer output.
    b. OR, MONO_OUT (DAC3), it can be configured as single-ended or differential line output.
10. Stream 9: USB recording stream. It is sent to an USB host.
11. There is also a built-in Function Generator (fixed sampling rate of 48 kHz) that can be routed to any of the 5 output streams, namely: Stream 5, 6, 7, 8, or 9.
12. The Inputs streams are sent out to the output steams via one of the three processing internal blocks. These blocks are:

a. Playback Processing Block (PB) that contains the following functional blocks:
   i. DRC
   ii. Line Echo Canceller (LEC)
   iii. Noise Reduction
   iv. Volume Control and
   v. 3D processing
   vi. Mixer 0: It allows mixing of up to four different inputs.

b. Mixer 1 Block (MX1). It allows mixing of up to four different inputs. No processing except stream mixing is performed.

c. Voice Processing Block (VP). This blocks consists of the following functional blocks:
   i. Acoustic Echo Canceller (AEC)
   ii. Beam Forming
   iii. Noise Reduction
   iv. DRC
   v. Mic EQ
   vi. AGC and
   vii. Debug Select

13. The Output Streams can accept outputs from one of the above three internal processing blocks or directly from the output of any of the input streams, i.e. Stream 1, 2, 3, 4 or Function Generator block output. The user is cautioned to ensure that the input sampling rate matches to that of the output sampling rate of the input streams.

14. For further details, please refer to the *CX2070x: Host API Document*.

15. For line echo cancellation, the microphone MUST be used (Stream 2) in conjunction with the Playback Processing (PB) block. After PB, the most common stream routing would be Mono Output, i.e. Stream 8. If the Mono Output is configured as a differential line-driver, it may drive an external 600 Ohm transformer to interface with PSTN telephone lines. However, the user may choose other output options, and is thus not limited to Stream 8 only.

Figure 53. CX20709-12Z Input Streams and Function Generator Block

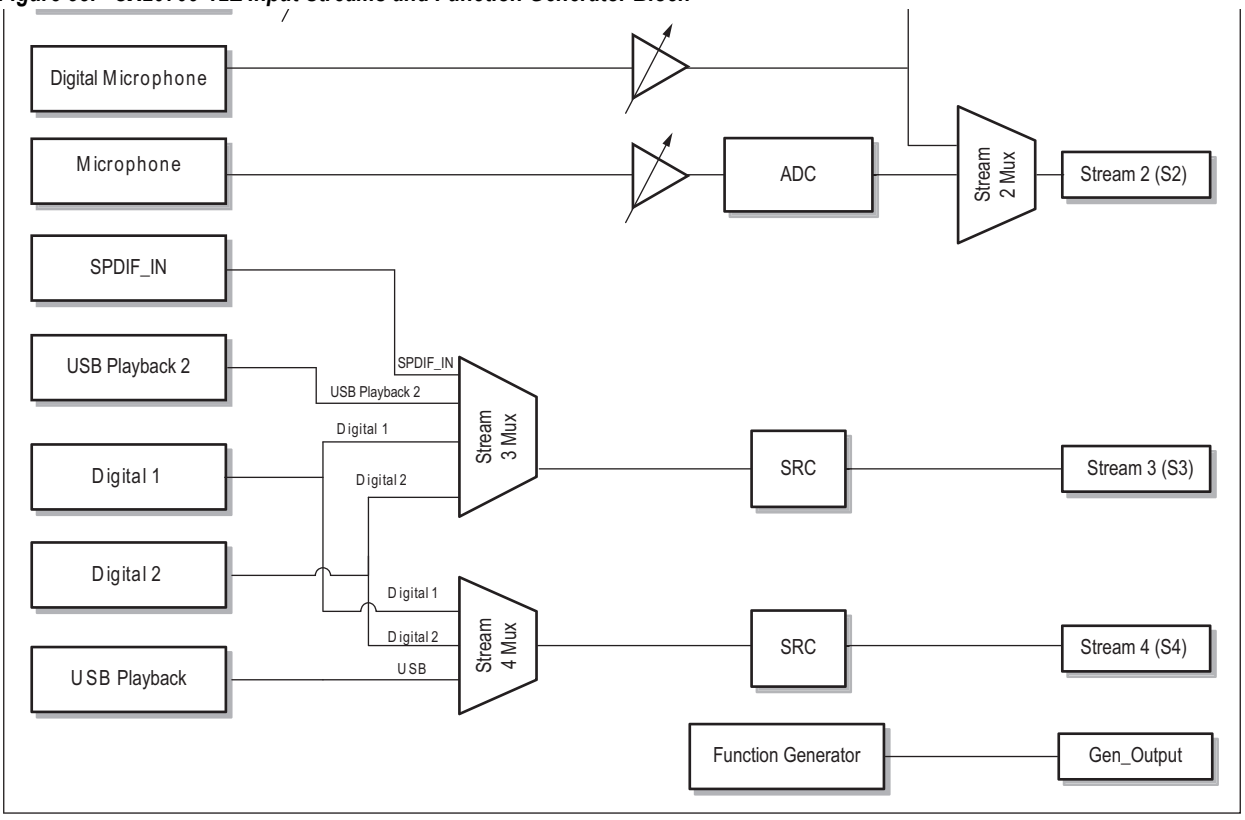


Figure 54. CX20709-12Z Processing Blocks and Mixer Block

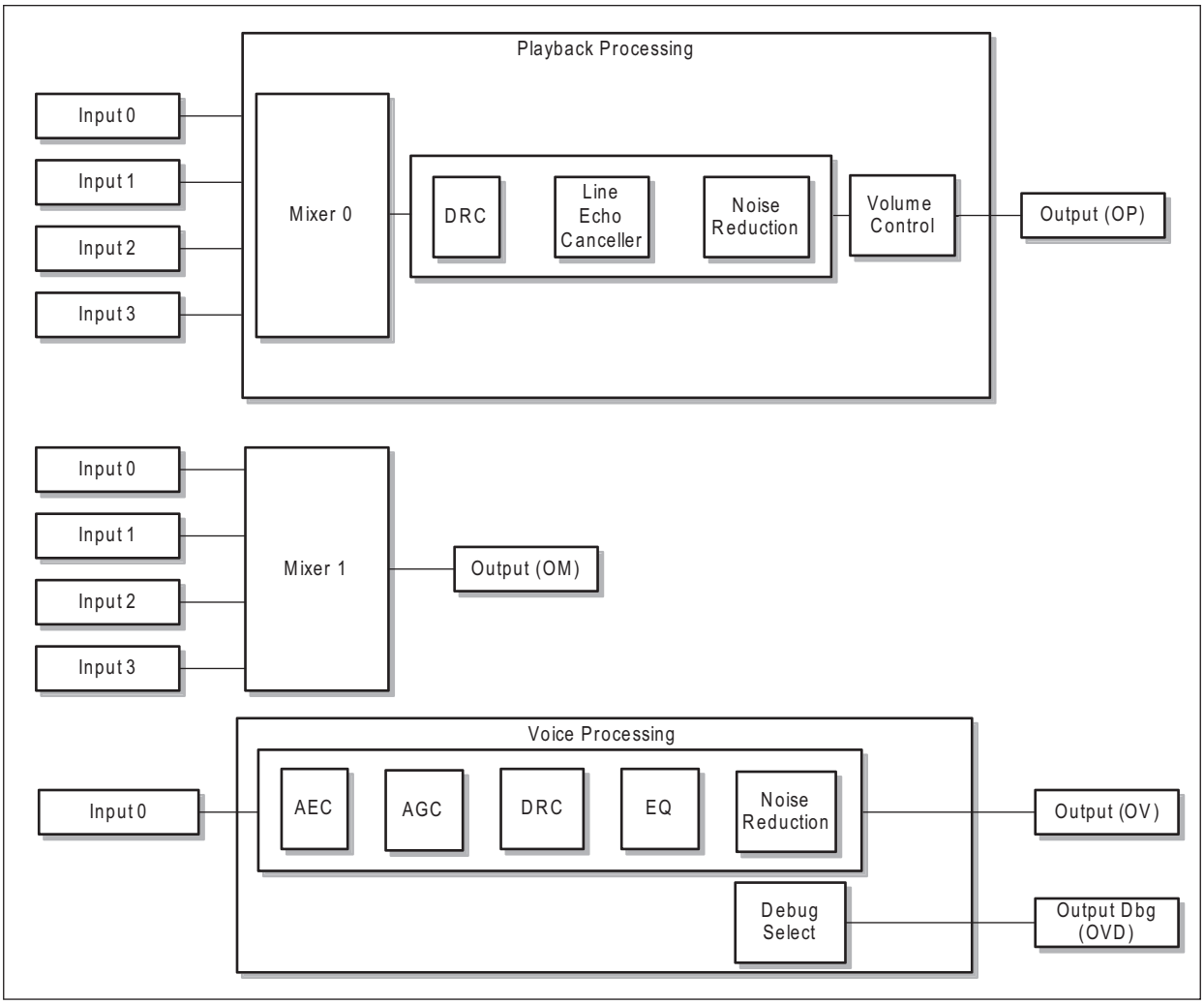
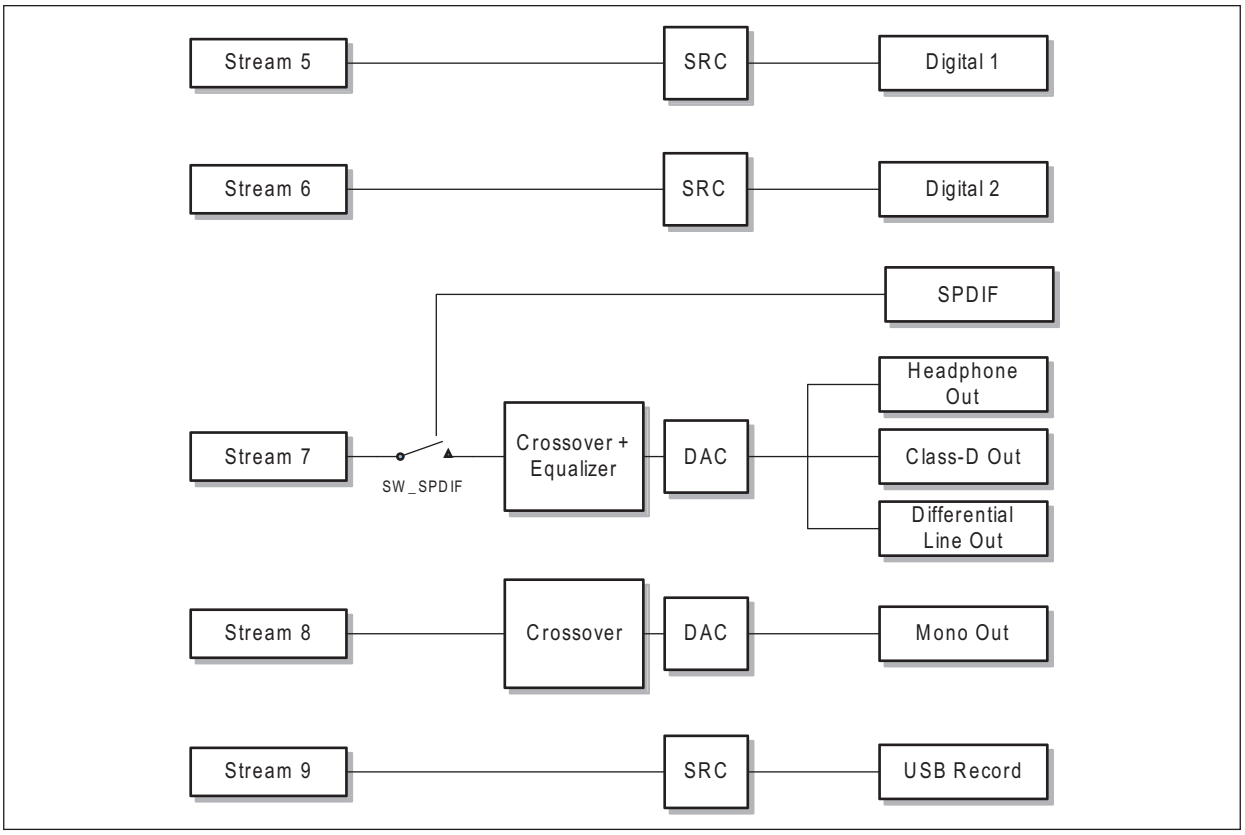


Figure 55. CX20709-12Z Output Streams

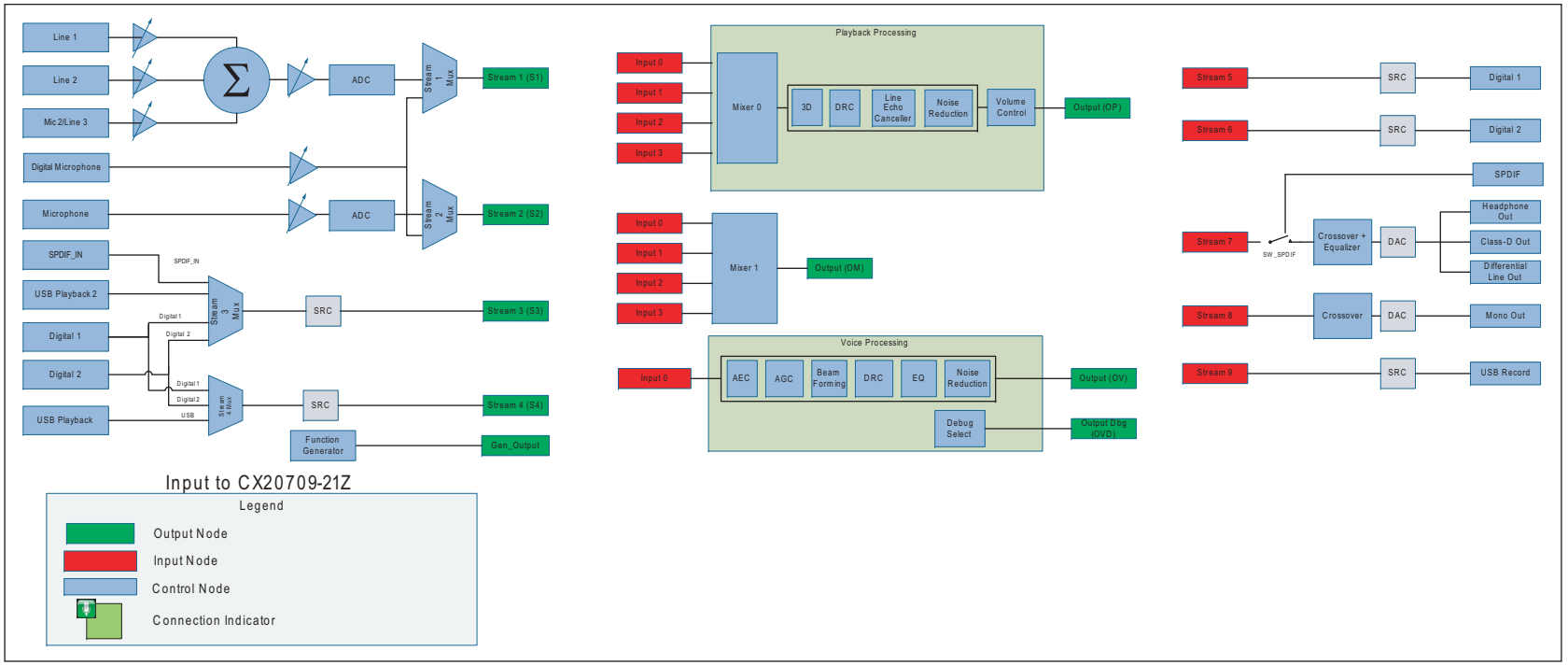


NOTE: In I^2S/PCM Mode, CX20709-12Z will operate in the following modes:

- ✓ DSP mode, either as I^2S/PCM master or slave.
- ✓ Pass-Thru mode (non-DSP), ONLY as I^2S/PCM master.

NOTE: ASRC or SRC refers to the asynchronous sample rate conversion function of CX20709-12Z in DSP Mode.

Figure 56. CX20709-12Z DSP Diagram



Any Input Stream output (Stream 1, 2, 3, 4 and Function Generator) can be connected directly to the input node of any Output Stream (Stream 5, 6, 7, 8, 9); or to any Processing Block/Multiplexer input node. The validity of the connection is subject to proper rate matching with or without the use of ASRC.

There is a limit of 4 Input Streams and 5 Output Streams. An input node can only accept one input. However, any output node may be connected to up to 4 output nodes.

For a description on the various sources and destination of the stream routing, refer to the *CX2070x Host API Document* for CX20709-12Z.

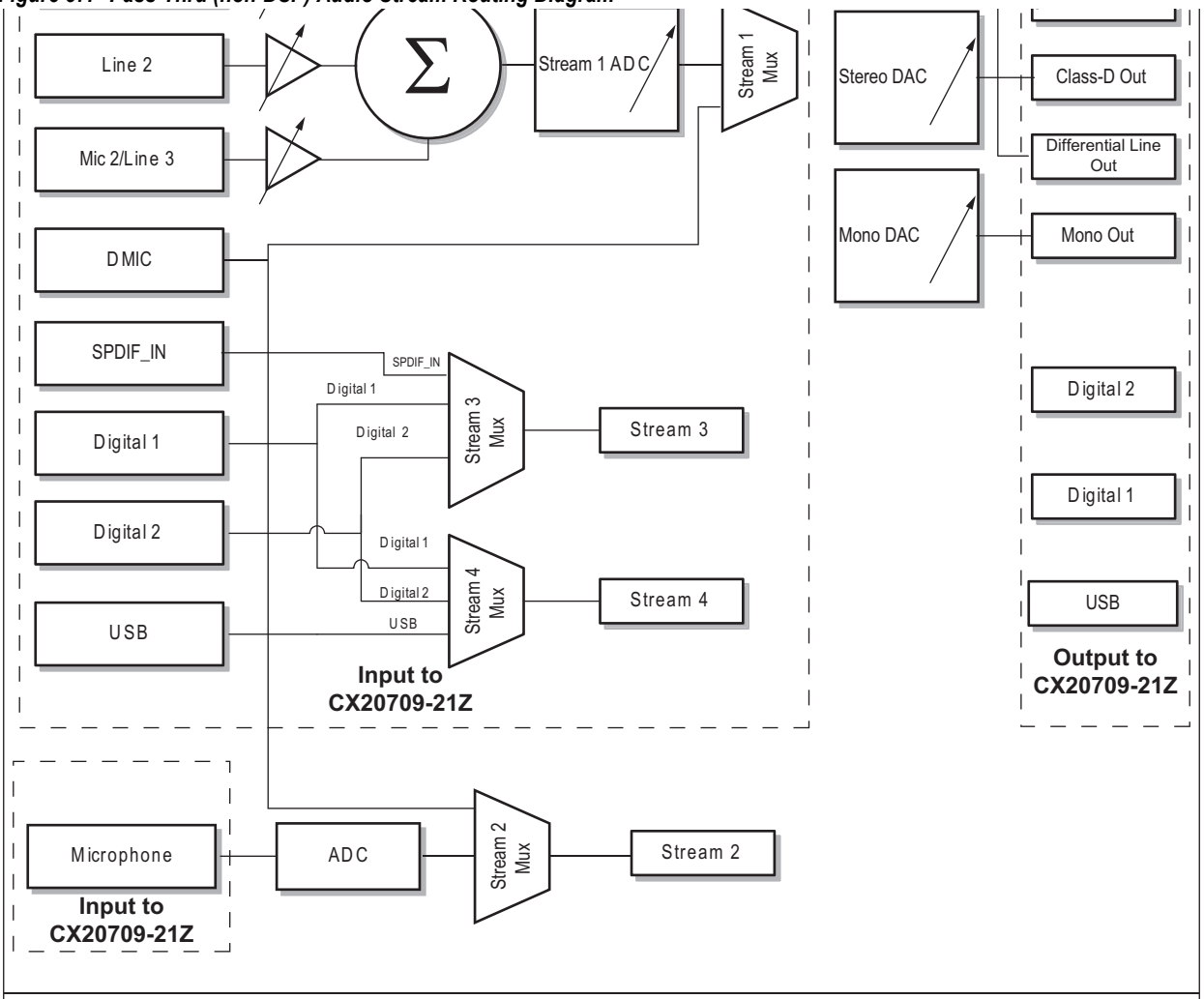
6.6 Pass-Thru Mode

In Pass-Thru (non-DSP) mode, any input stream can be routed to any output stream, as long as the input stream and the output stream are of the same rate. In the absence of ASRC in Pass-Thru mode, if there is a rate mismatch in the audio streams (e.g., input vs. output), there will be distortion in the output.

An example of a valid Pass-Thru mode audio route is: Stream 2 (mic input) can be routed to the DAC and playback through the Class-D speaker.

Note that the only DSP function that is supported in Pass-Thru mode is the equalizer at the DAC (refer to Figure 57).

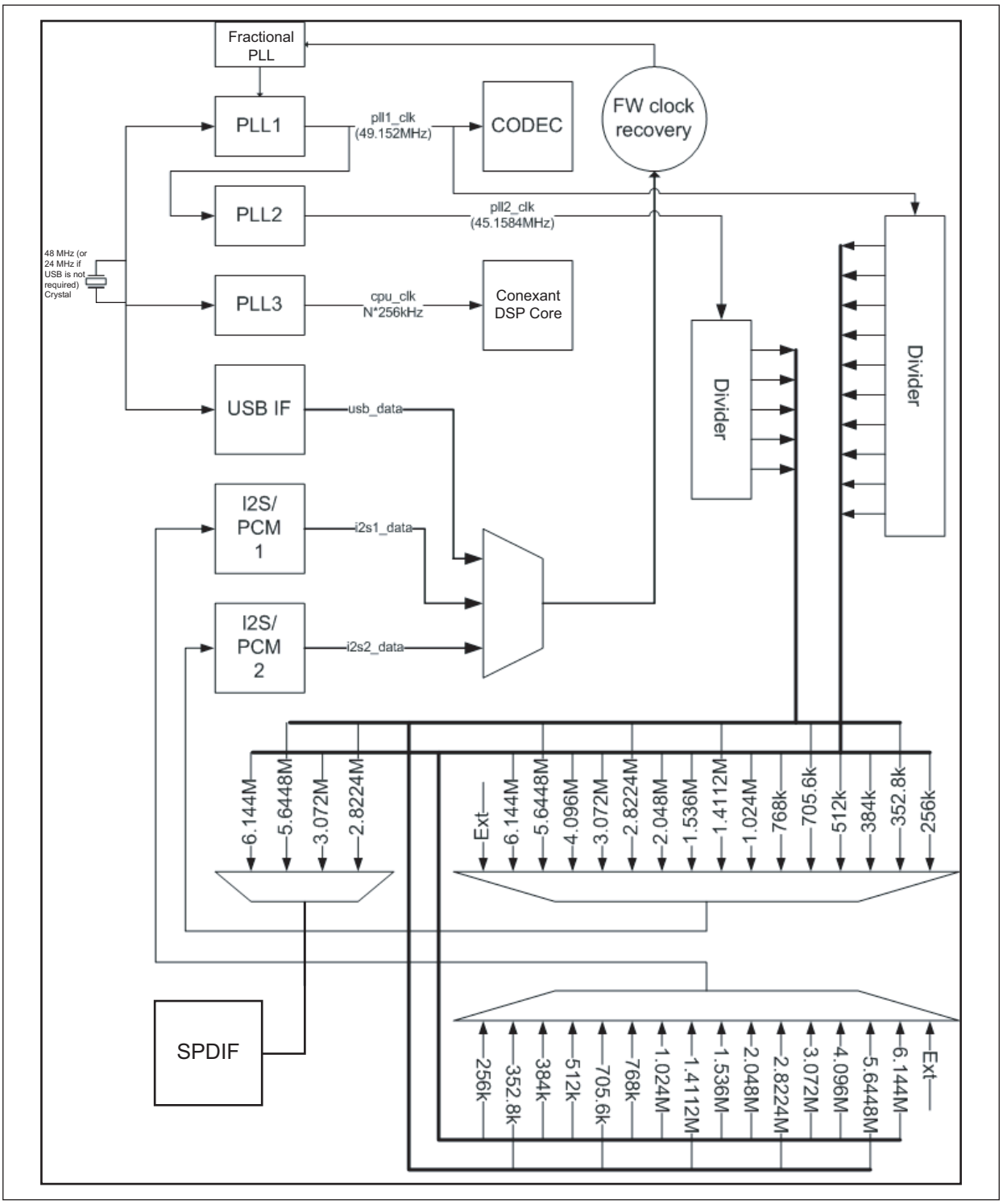
Figure 57. Pass-Thru (non-DSP) Audio Stream Routing Diagram



GENERAL NOTE: The 2nd USB playback stream is not supported in Pass-Thru mode.

6.7 Internal Clocking

Figure 58. Internal Clocking



7 CX20709-12Z Registers

7.1 Register Map

All CX2070x hardware registers are controlled by the firmware except for the I^2S/ PCM configuration registers (namely: 0x0F50 through 0x0F68). For a detailed description of the functionality and application of the firmware registers, please refer to the *CX2070x Host API Document* corresponding to the pertinent firmware revision.

Table 80. Register List *(1 of 2)*

Register Name	Offset (Byte)	Default
Digital Audio Interface (I^2S and PCM) Control Registers		
Clock Divider	0xF50	0xFF
Port 1 Control	0xF51	0
Port 1 TX Clocks per Frame	0xF52	0
Port 1 RX Clocks per Frame	0xF53	0
Port 1 TX Sync Width	0xF54	0
Port 1 RX Sync Width	0xF55	0
Port 1 Control 2	0xF56	0x0A
Port 1 RX Stream 1 Slot Control	0xF57	0
Port 1 RX Stream 2 Slot Control	0xF58	0
Port 1 RX Stream 3 Slot Control	0xF59	0
Port 1 TX Stream 1 Slot Control	0xF5A	0
Port 1 TX Stream 2 Slot Control	0xF5B	0
Port 1 TX Stream 3 Slot Control	0xF5C	0
Port 1 Bit Count Delay	0xF5D	0
Port 2 Control	0xF5E	0
Port 2 Clocks per Frame	0xF5F	0
Port 2 Sync Width	0xF60	0

Table 80. Register List *(2 of 2)*

Register Name	Offset (Byte)	Default
Digital Audio Interface (I^2S and PCM) Control Registers (continued)		
Port 2 Sample Width	0xF61	0x01
Port 2 RX Stream 1 Slot Control	0xF62	0
Port 2 RX Stream 2 Slot Control	0xF63	0
Port 2 RX Stream 3 Slot Control	0xF64	0
Port 2 TX Stream 1 Slot Control	0xF65	0
Port 2 TX Stream 2 Slot Control	0xF66	0
Port 2 TX Stream 3 Slot Control	0xF67	0
Port 2 Bit Count Delay	0xF68	0

7.2 Register Details

Clock Divider (0x0F50)

Bits	Name	Default	R/W	Description
7:4	Port 2 Clock Div Select	0	R/W	0x0 = 6.144 MHz 0x1 = 4.096 MHz 0x2 = 3.072 MHz 0x3 = 2.048 MHz 0x4 = 1.536 MHz 0x5 = 1.024 MHz 0x6 = 768 kHz 0x7 = 512 kHz 0x8 = 384 kHz 0x9 = 256 kHz 0xa = 5.644 MHz 0xb = 2.822 MHz 0xc = 1.411 MHz 0xd = 705 kHz 0xe = 352 kHz 0xf = external clock enabled
3:0	Port 1 Clock Div Select	0	R/W	0x0 = 6.144 MHz 0x1 = 4.096 MHz 0x2 = 3.072 MHz 0x3 = 2.048 MHz 0x4 = 1.536 MHz 0x5 = 1.024 MHz 0x6 = 768kHz 0x7 = 512 kHz 0x8 = 384 kHz 0x9 = 256 kHz 0xa = 5.644 MHz 0xb = 2.822 MHz 0xc = 1.411 MHz 0xd = 705 kHz 0xe = 352 kHz 0xf = external clock enabled

Port 1 Control (0x0F51)

Bits	Name	Default	R/W	Description
7	Delay	0	R/W	0 = I^2S - Left Justified Data not delayed PCM – TX/RX data start in same cycle as Frame Sync, without any delay. 1 = I^2S - Left Justified Data delayed 1 bit PCM – TX/RX data delayed by One cycle
6	Right Justify	0	R/W	0 = Left Justify Mode (I^2S)/MSB first (PCM) 1 = Right Justify mode (I^2S)/LSB first (PCM)
5	RX En	0	R/W	1 = Port 1 RX Enabled 0 = Port 1 RX Disabled
4	TX EN	0	R/W	1 = Port 1 TX Enabled 0 = Port 1 TX Disabled
3	Reserved	0	R	
2	Bitclk Pol	0	R/W	**I^2S Mode** 0 = TX Data Sent on Falling Edge of Bit Clock 0 = RX Data Strobed with Rising Edge of Bit Clock 0 = WS (slave mode) Strobed with Falling Edge of Bit Clock & WS (master mode) Sent on Falling Edge of Bit Clock 1 = TX Data Sent on Rising Edge of Bit Clock 1 = RX Data Strobed with Falling Edge of Bit Clock 1 = WS (slave mode) Strobed with Rising Edge of Bit Clock & WS (master mode) Sent on Rising Edge of Bit Clock **PCM Mode** 0 = TX Data Sent on Rising Edge of Bit Clock 0 = RX Data Strobed with Falling Edge of Bit Clock 0 = WS (slave mode) Strobed with Falling Edge of Bit Clock & WS (master mode) Sent on Rising Edge of Bit Clock 1 = TX Data Sent on Falling Edge of Bit Clock 1 = RX Data Strobed with Rising Edge of Bit Clock 1 = WS (slave mode) Strobed with Rising Edge of Bit Clock & WS (master mode) Sent on Falling Edge of Bit Clock
1	WS Pol	0	R/W	0: WS Low for Left channel; WS High for Right channel (I^2S Only) 1: WS High for Left channel; WS Low for Right channel (I^2S Only)
0	I^2S PCM	0	R/W	0 = I^2S mode 1 = PCM Mode

Port 1 TX Clocks per Frame (0x0F52)

Bits	Name	Default	R/W	Description
7:5	Reserved	0	R	
4:0	TX Clocks per Frame	0	R/W	TX Clocks per Frame It is (N+1)*8 00000 – 8 Clocks per Frame 00001 – 16 Clocks per Frame 00010 – 24 Clocks per Frame 00011 – 32 Clocks per Frame ……. ……. 11111 – 256 Clocks per Frame

Port 1 RX Clocks per Frame (0x0F53)

Bits	Name	Default	R/W	Description
7:5	Reserved	0	R	
4:0	RX Clocks per Frame	0	R/W	RX Clocks per Frame It is (N+1)*8 00000 – 8 Clocks per Frame 00001 – 16 Clocks per Frame 00010 – 24 Clocks per Frame 00011 – 32 Clocks per Frame ……. ……. 11111 – 256 Clocks per Frame

Port 1 TX Sync Width (0x0F54)

Bits	Name	Default	R/W	Description
7	Reserved	0	R	
6:0	TX Sync Length	0	R/W	TX Sync Width. Number of bit clock cycles RX Frame Sync would be valid. 0000000 – 1 Cycle 0000001 – 2 Cycle …….. …….. 1111111 – 128 Cycles

Port 1 RX Sync Width (0x0F55)

Bits	Name	Default	R/W	Description
7	Reserved	0	R	
6:0	RX Sync Length	0	R/W	RX Sync Width Number of bit clock cycles TX Frame Sync would be valid. 0000000 – 1 Cycle 0000001 – 2 Cycle …….. …….. 1111111 – 128 Cycles

Port 1 Control 2 (0x0F56)

Bits	Name	Default	R/W	Description
7-6	Reserved	0		
5	P1 TX PT	0	R/W	Port 1 TX PassThru 0 = TX pin outputs TX data 1 = TX pin outputs PassThru Input
4	P1 RX Pt	0	R/W	Port 1 RX PassThru 0 = RX receives RX pin data 1 = RX receives PassThru data
3:2	RX Sample Size	1	R/W	RX Sample Size 00 = 8-bit 01 = 16-bit 10 = 24-bit truncated to 16 bits 11 = 24-bit
1:0	TX Sample Size	1	R/W	TX Sample Size 00 = 8-bit 01 = 16-bit 10 = 24-bit truncated to 16 bits 11 = 24-bit

Port 1 RX Stream 1 Slot Control (0x0F57)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	RX Stream 1 Enable	0	R/W	0 = Disable, 1= Enable RX Steam 1
4:0	RX Stream 1	0	R/W	PCM Slot Number for RX Stream 1 Each Slot is 8 bits. All the Enabled RX steams should be configured to Unique Slot Nos. Note: If RX Sample Size is 16 or 24, it uses two or three consecutive slots respectively. RX slots nos. should be allocated accordingly.

Port 1 RX Stream 2 Slot Control (0x0F58)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	RX Stream 2 Enable	0	R/W	0 = Disable, 1= Enable RX Steam 2
4:0	RX Stream 2	0	R/W	PCM Slot Number for RX Stream 2. See PCM steam1 for slot allocation Description.

Port 1 TX Stream 1 Slot Control (0x0F5A)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	TX Stream 1 Enable	0	R/W	0 = Disable, 1= Enable TX Steam 1
4:0	TX Stream 1	0	R/W	PCM Slot Number for TX Stream 1 Each Slot is 8 bits. All the Enabled TX steams should be configured to Unique Slot Nos. Note: If TX Sample Size is 16 or 24, it uses two or three consecutive slots respectively. TX slots nos. should be allocated accordingly.

Port 1 TX Stream 2 Slot Control (0x0F5B)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	TX Stream 2 Enable	0	R/W	0 = Disable, 1= Enable TX Steam 2
4:0	TX Stream 2	0	R/W	PCM Slot Number for TX Stream 2 See TX steam1 for slot allocation Description.

Port 1 TX Stream 3 Slot Control (0x0F5C)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	TX Stream 3 Enable	0	R/W	0 = Disable, 1= Enable TX Steam 3
4:0	TX Stream 3	0	R/W	PCM Slot Number for TX Stream 3 See TX steam1 for slot allocation Description.

Port 1 Bit Count Delay (0x0F5D)

Bits	Name	Default	R/W	Description
7	Reserved	0	R	
6:0	Bit Count Delay	0	R/W	I^2S Bit Count Delay (used for right justify mode)

Port 2 Control 1 (0x0F5E)

Bits	Name	Default	R/W	Description
7	Delay	0	R/W	0 = I^2S - Left Justified Data not delayed PCM – TX/RX data start in same cycle as Frame Sync, without any delay. 1 = I^2S - Left Justified Data delayed 1 bit PCM – TX/RX data delayed by One cycle
6	Right Justify	0	R/W	0 = Left Justify Mode (I^2S) / MSB first (PCM) 1 = Right Justify mode (I^2S) / LSB first (PCM)
5	RX En	0	R/W	0 = Port 2 RX Disabled 1 = Port 2 RX Enabled
4	TX En	0	R/W	0 = Port 2 TX Disabled 1 = Port 2 TX Enabled
3	Reserved	0	R	
2	Bitclk Pol	0	R/W	**I^2S Mode** 0 = TX Data Sent on Falling Edge of Bit Clock 0 = RX Data Strobed with Rising Edge of Bit Clock 0 = WS (slave mode) Strobed with Falling Edge of Bit Clock & WS (master mode) Sent on Falling Edge of Bit Clock 1 = TX Data Sent on Rising Edge of Bit Clock 1 = RX Data Strobed with Falling Edge of Bit Clock 1 = WS (slave mode) Strobed with Rising Edge of Bit Clock & WS (master mode) Sent on Rising Edge of Bit Clock **PCM Mode** 0 = TX Data Sent on Rising Edge of Bit Clock 0 = RX Data Strobed with Falling Edge of Bit Clock 0 = WS (slave mode) Strobed with Falling Edge of Bit Clock & WS (master mode) Sent on Rising Edge of Bit Clock 1 = TX Data Sent on Falling Edge of Bit Clock 1 = RX Data Strobed with Rising Edge of Bit Clock 1 = WS (slave mode) Strobed with Rising Edge of Bit Clock & WS (master mode) Sent on Falling Edge of Bit Clock
1	WS Pol	0	R/W	0: WS Low for Left channel; WS High for Right channel (I^2S only) 1: WS High for Left channel; WS Low for Right channel (I^2S only)
0	I2S PCM	0	R/W	0 = I^2S mode 1 = PCM Mode

Port 2 Clocks per Frame (0x0F5F)

Bits	Name	Default	R/W	Description
7:5	Reserved	0	R	
4:0	Clocks per Frame	0	R/W	Clocks per Frame It is (N+1)*8 00000 – 8 Clocks per Frame 00001 – 16 Clocks per Frame 00010 – 24 Clocks per Frame 00011 – 32 Clocks per Frame ……. ……. 11111 – 256 Clocks per Frame

Port 2 Sync Width (0x0F60)

Bits	Name	Default	R/W	Description
7	Reserved	0	R	
6:0	Sync Length	0	R/W	Sync Width Number of bit clock cycles Frame Sync would be valid. 0000000 – 1 Cycle 0000001 – 2 Cycle …….. …….. 1111111 – 128 Cycles

Port 2 Sample Width (0x0F61)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	P2 TX PT	0	R/W	Port 2 TX PassThru 0 = TX pin outputs TX data 1 = TX pin outputs PassThru Input
4	P2 RX Pt	0	R/W	Port 2 RX PassThru 0 = RX receives RX pin data 1 = RX receives PassThru data
3:2	Reserved	0	R	
1:0	Sample Size	1	R/W	Sample Size 00 = 8-bit 01 = 16-bit 1x = 24-bit

Port 2 RX Stream 1 Slot Control (0x0F62)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	RX Stream 1 Enable	0	R/W	0 = Disable, 1= Enable RX Steam 1
4:0	RX Stream 1	0	R/W	PCM Slot Number for RX Stream 1 Each Slot is 8 bits. All the Enabled RX steams should be configured to Unique Slot Nos. Note: If RX Sample Size is 16 or 24, it uses two or three consecutive slots respectively. RX slots nos. should be allocated accordingly.

Port 2 RX Stream 2 Slot Control (0x0F63)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	RX Stream 2 Enable	0	R/W	0 = Disable, 1= Enable RX Steam 2
4:0	RX Stream 2	0	R/W	PCM Slot Number for RX Stream 2 See RX Steam1 for slot allocation description

Port 2 TX Stream 1 Slot Control (0x0F65)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	TX Stream 1 Enable	0	R/W	0 = Disable, 1= Enable TX Steam 1
4:0	TX Stream 1	0	R/W	PCM Slot Number for TX Stream 1 Each Slot is 8 bits. All the Enabled TX steams should be configured to Unique Slot Nos. Note: If TX Sample Size is 16 or 24, it uses two or three consecutive slots respectively. TX slots nos. should be allocated accordingly.

Port 2 Tx Stream 2 Slot Control (0x0F66)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	TX Stream 2 Enable	0	R/W	0 = Disable, 1= Enable TX Steam 2
4:0	TX Stream 2	0	R/W	PCM Slot Number for TX Stream 2 See TX Steam1 for slot allocation description

Port 2 TX Stream 3 Slot Control (0x0F67)

Bits	Name	Default	R/W	Description
7:6	Reserved	0	R	
5	TX Stream 3 Enable	0	R/W	0 = Disable, 1= Enable TX Steam 3
4:0	TX Stream 3	0	R/W	PCM Slot Number for TX Stream 3 See TX Steam1 for slot allocation description

NOTE: The RX/TX Stream Slot Control Registers are only applicable to PCM. They are not applicable to I^2S.

Port 2 Bit Count Delay (0x0F68)

Bits	Name	Default	R/W	Description
7	Reserved	0	R	
6:0	Bit Count Delay	0	R/W	Port 2 I^2S Bit Count Delay (used for right justify mode)

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