OptiPHY™-F155 Quad OC-3/STM-1ATM/ POS PHY

Data Sheet

CX29704

500034A
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MINDSPEED™

Ordering Information

Model Number	Manufacturing Part Number	Package	Operating Temperature
CX29704	29704-11	27 × 27, 272-Pin PBGA	–40 to 85 °C

Revision History

Revision	Level	Date	Description
A	Preliminary	June 2001	Formerly Conexant document number 101344A.

CX29704

OptiPHY™-F155 Quad OC-3/STM-1ATM/POS PHY

The CX29704 is an integrated circuit that implements four-channel mapping functions for SONET/SDH processing and ATM/Packet-Over-SONET(POS)/SDH at 155.52 Mbps. The component contains both the PMD and the TC sublayers and provides an UTOPIA Level 2 interface to the ATM layer or, optionally, a POS interface to the link layer.

The CX29704 is fully compliant with the SONET/SDH, B-ISDN ATM Forum User Network Interface requirements and standards and compliant with Point-to-Point Protocol (PPP) over SONET/SDH (RFC 1619/1662 of the IETF). The PMD sublayer is based on Mindspeed Technologies, Incorporated's technology for high-speed clock and data recovery. The UTOPIA Level 2/POS interfaces provide variable modes of operation when interfacing the ATM layer or link layer in order to facilitate the connection of the CX29704 to different ATM layer or packet over SONET/SDH link layer devices. The primary applications of the CX29704 are ATM switches, routers, and WAN switches supporting POS/SDH.

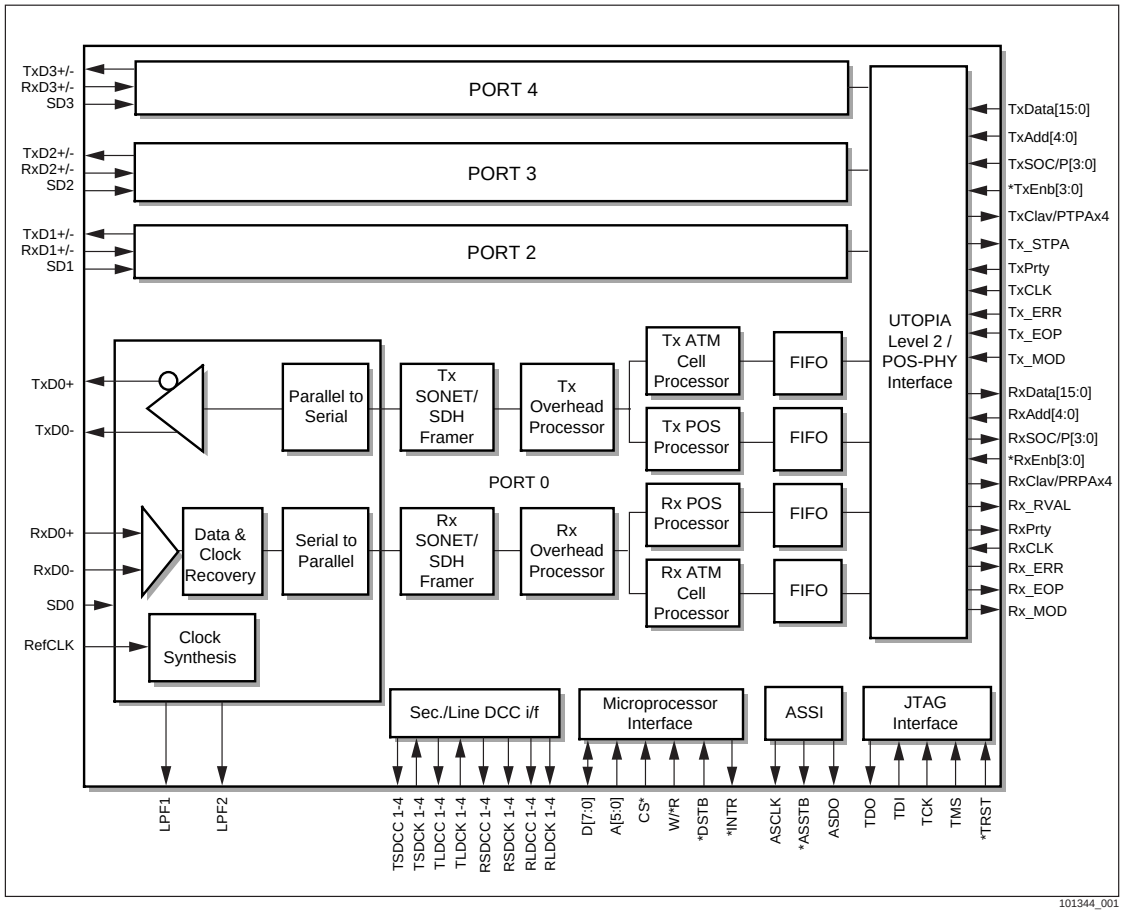
This Data Sheet provides a detailed description of the component. For additional information, please contact Customer Support at Mindspeed Technologies, Inc.

Distinguishing Features

- Single chip four port ATM User Network Interface operating at 155.52 Mbps
- Supports Packet Over SONET(POS)/SDH applications
- Compliant with ATM Forum User Network Interface V 3.1 Specification and with the physical layer specification for B-ISDN according to ITU-T recommendation I.432
- Compliant with the Point-to-Point Protocol (PPP) over SONET/SDH specification (RFC 1619/1662 of the IETF)

—continued—

Functional Block Diagram



–Continued Distinguishing Features–

- Processes 155.52 Mbps STS-3c/STM-1 data streams
- On-chip clock and data recovery and clock synthesis
- Complies with Bellcore GR-253-CORE Jitter criteria
- Supports capture and insertion of all SONET/SDH overhead bytes
- Dedicated serial port for insertion/ extraction of the DCC overhead bytes (D1–D12).
- Optical transceiver interface
- Provides UTOPIA Level 2 Interface according to the ATM Forum UTOPIA Level 2 Specification
- Provides POS interface to a link layer device
- Supports Normal and Hot selection
- Dual-port mapping in conjunction with SONET/SDH APS mechanism facilitates quick recovery at Failure Protection State
- Supports 4-cell FIFO buffers for both receive and transmit directions in ATM mode
- Supports 256-byte FIFO buffers for both receive and transmit directions in POS mode
- Enhanced SONET/SDH bit error-rate monitoring
- Provides 16-bit microprocessor bus interface for configuration, control, and status indications
- Boundary Scan (JTAG) support in accordance with IEEE 1149.1 for test board purposes
- PECL- and TTL-compatible input
- TTL and CMOS output
- 272-pin PBGA, 27 × 27 mm
- Industrial temperature range (–40 °C to +85 °C)
- 3.3 V, 0.35 µm CMOS technology with 5 V input tolerance

Applications

- Switches
- Routers
- DSLAMs
- Cellular base station infrastructure

Table of Contents

List of Figures

List of Tables

1.0 ATM Layer Applications

Figure 1-1 illustrates a multiport ATM Layer Device interfacing two CX29704 ICs according to UTOPIA Level 2 specifications. This configuration enables connection of up to eight CX29704 ICs to one multiport ATM Layer Device. The modes of operation shown in Figure 1-1 are Multiplexed Status mode and One Rx/Tx CLAV mode. Both modes receive and transmit cells from and to one PHY port at a time. In Multiplexed Status mode, the ATM layer device polls the Receive and Transmit FIFO status of four PHY ports simultaneously. In this mode, several multiport devices share the same UTOPIA bus. When any specific device port is polled for status, all ports within this PHY device provide their status by the Clav[3:0] pins.

In One Rx/Tx CLAV mode, the ATM Layer device polls the Receive or Transmit FIFO status of a single PHY port at a time by using the address pins to select the port. The polled port provides its status on the Rx/TxClav[0] pin. One Rx/Tx CLAV mode uses the Rx/TxClav[0] pin to obtain the status of any port. This mode does not use the signals TxClav[3:1] and RxClav[3:1].

Figure 1-1. Interfacing Two CX29704 to One Multiport ATM Layer Device

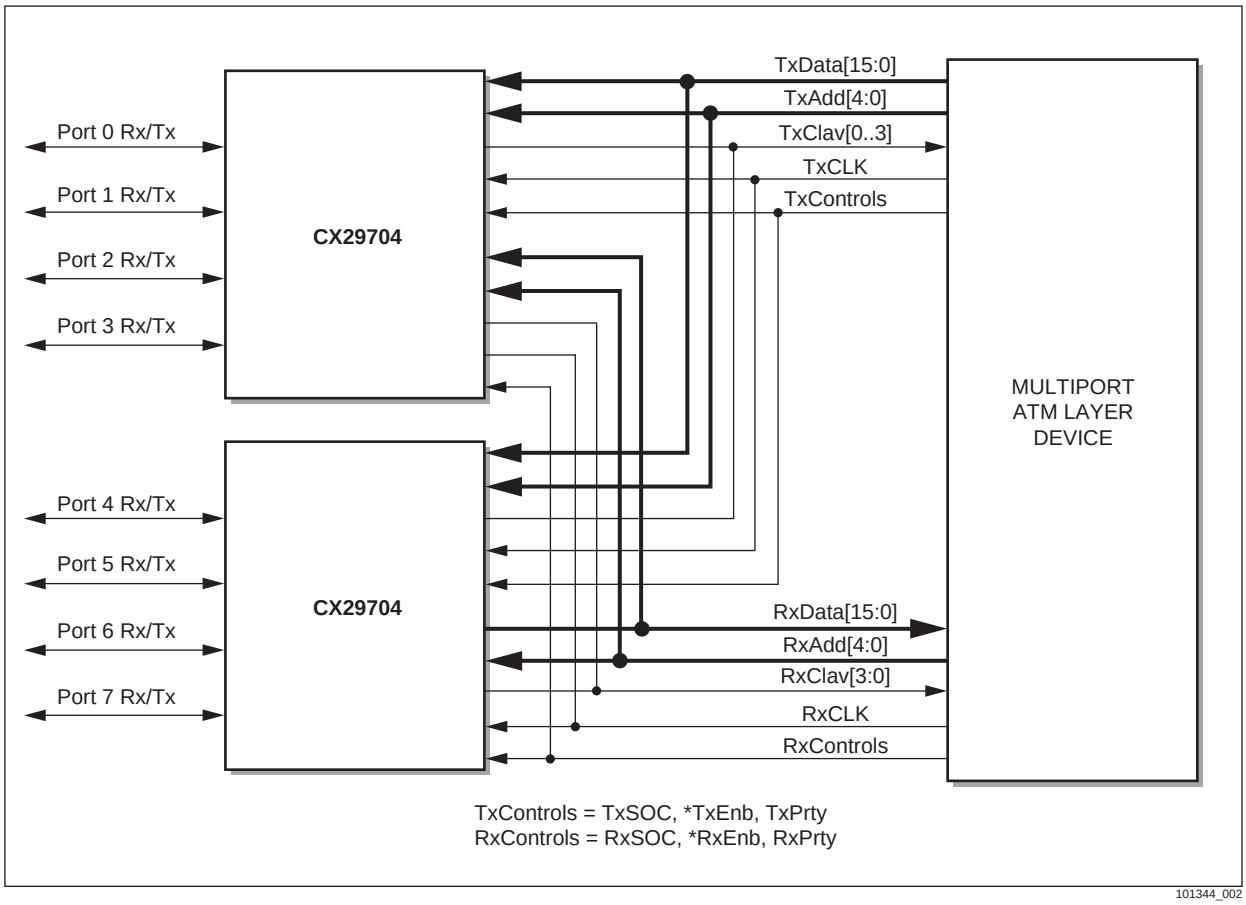
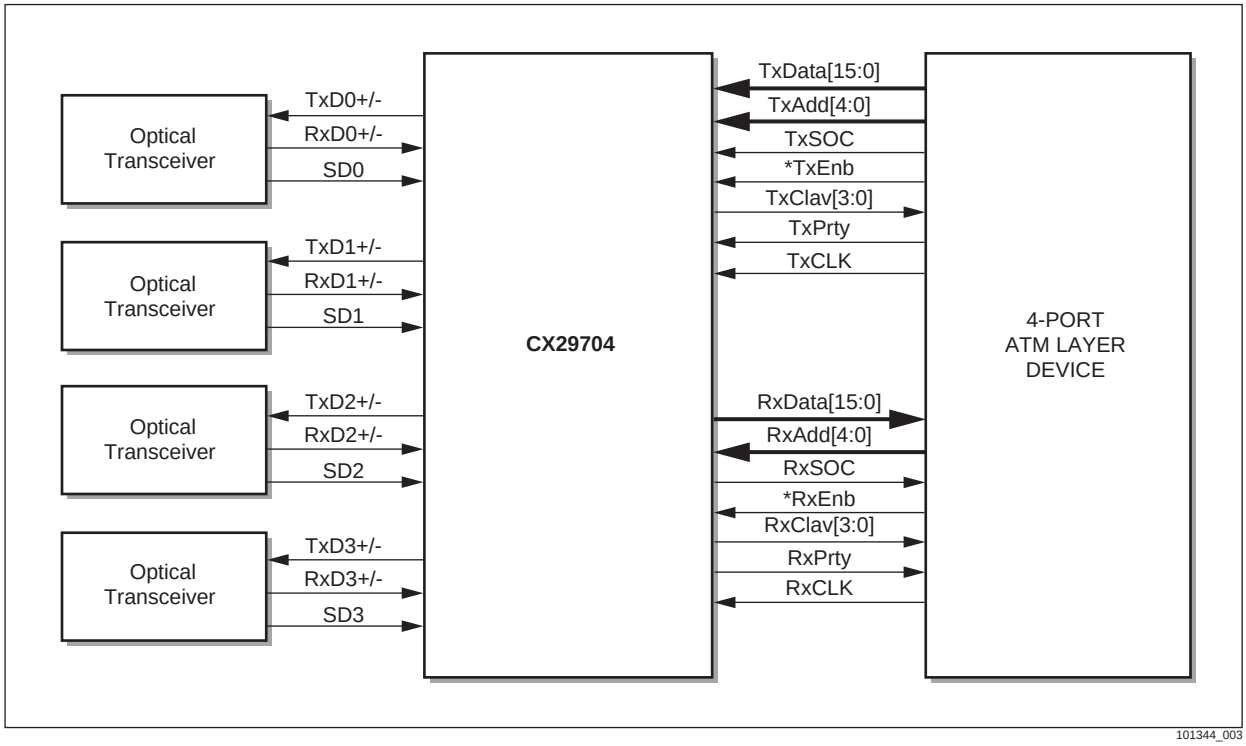


Figure 1-2 demonstrates the connection of one CX29704 to one 4-port ATM Layer device according to the UTOPIA Level 2 Specification. The connection is performed using Direct Status Indication mode, where there is a direct per port indication of the FIFO status by dedicated RxClav and TxClav signals. Cell transmission is made to or from one PHY port at a time. Receive and transmit channels function simultaneously and independently. This mode supports a 16-bit data bus.

Figure 1-2. Using Direct Status Indication to Interface One CX29704 to One 4-port ATM Layer Device



2.0 POS Layer Applications

Figure 2-1 illustrates a multiport POS Layer Device interfacing two CX29704 ICs according to the POS interface. This configuration enables the connection of up to eight CX29704 ICs to one multiport POS Layer Device. The modes of operation shown in Figure 2-1 are Selected Status mode and Polling Status mode. Both modes receive and transmit packets from and to one PHY port at a time. In the Selected Status mode, the POS Link Layer device polls the Receive and Transmit FIFO status of four different PHY ports per poll. Polling is performed using signals DTPA/DRPA[3:0]. DTPA/DRPA[i] indicates the FIFO associated with port i. In the Selected Status mode, the POS Layer Device polls the Receive or Transmit FIFO status of a single PHY port at a time, using the PTPA/STPA or PRPA/RVAL signals and the address pin to select the desired port.

Figure 2-1. Interfacing Two CX29704 to One Multiport POS Layer Device

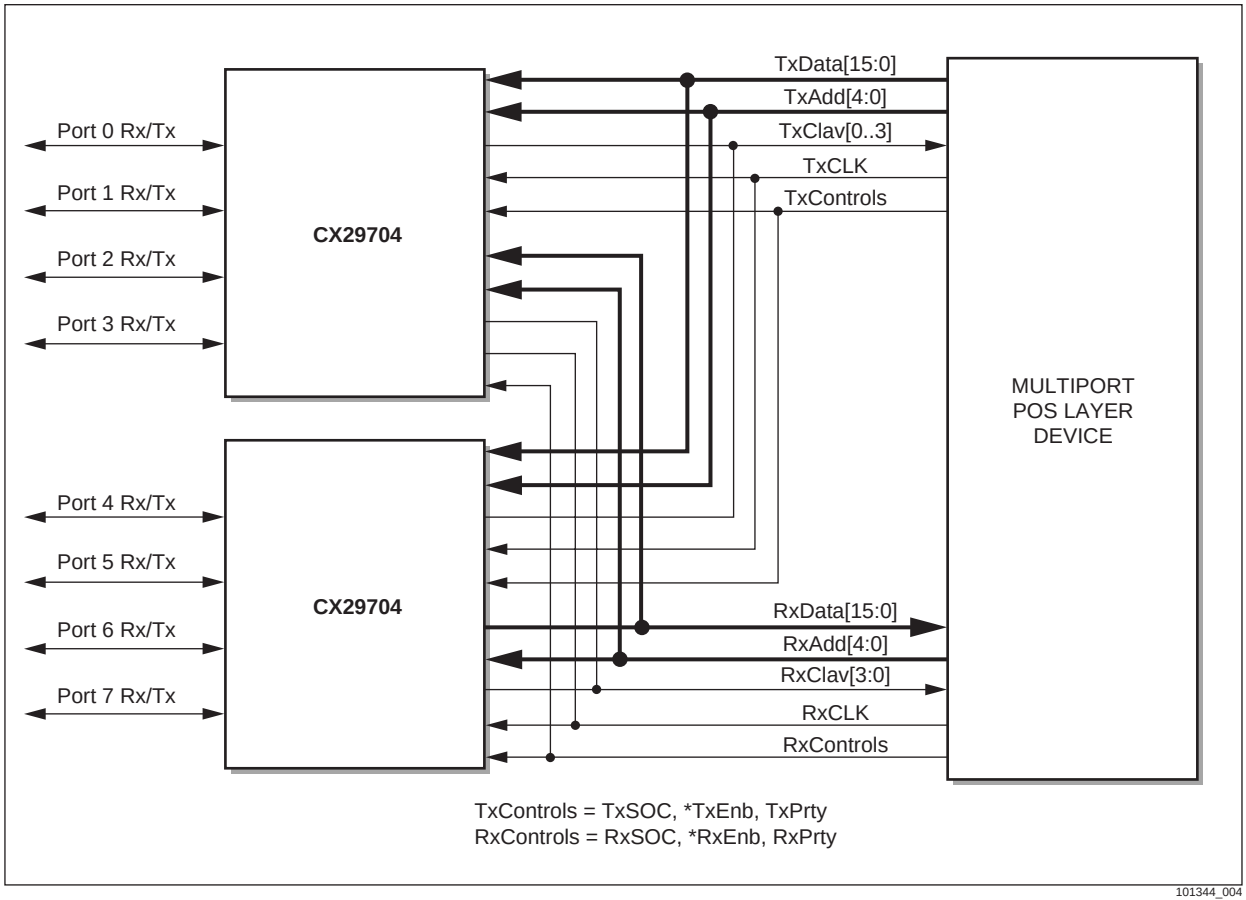
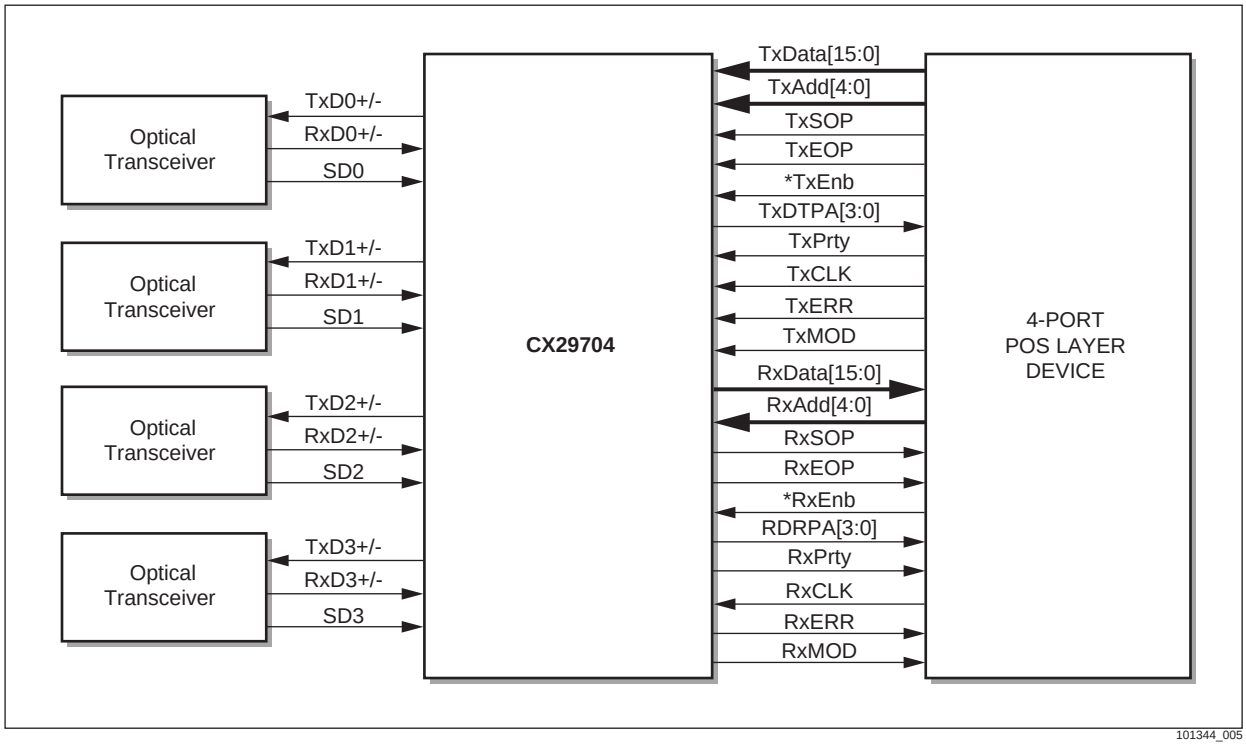


Figure 2-2 demonstrates the connection of one CX29704 to one 4-port POS link layer device according to POS Interface Level 2. The connection is performed using the Direct Status Indication mode, where there is a direct per-port indication by a dedicated pin of the FIFO status. Data transmission is made to or from one PHY port at a time. Receive and transmit channels work simultaneously and independently. This mode supports a 16-bit data bus.

Figure 2-2. Using Direct Status Indication to Interface One CX29704 to One 4-port POS Layer Device



3.0 Pin Description

3.1 UTOPIA Level 2 Interface (ATM Mode)

Table 3-1. UTOPIA Level 2 Interface (ATM Mode) (1 of 4)

Name	No.	I/O	Type	Functional Description
TxData[15:0] (ATM mode)	R3 P4 T1 R2 R1 P2 P1 N3 N1 M4 M3 M2 L4 L3 L2 L1	I	T	UTOPIA Transmit Data. Cell data is transmitted from the ATM layer to the PHY layer. Data is sampled on the rising edge of TxClk and is valid only when *TxEnb is asserted.
TxData[15:0] (POS mode)	R3 P4 T1 R2 R1 P2 P1 N3 N1 M4 M3 M2 L4 L3 L2 L1	I	T	POS Interface Transmit Data. Packet/data is transmitted from the link layer to the PHY layer. Data is sampled on the rising edge of TxClk and is valid only when *TxEnb is asserted.

Table 3-1. UTOPIA Level 2 Interface (ATM Mode) (2 of 4)

Name	No.	I/O	Type	Functional Description
TxAdd[4:0] (ATM mode)	H3 H2 J4 J3 J2	I	T	UTOPIA Transmit Address. The address is driven from the ATM layer to the PHY layer and selects the port that receives the next cell(s). When using the modes One Rx/Tx CLAV or Multiplexed Status Polling, it is also used to poll the status of the transmit FIFOs. Address is sampled on the rising edge of TxClk.
TxAdd[4:0] (POS mode)	H3 H2 J4 J3 J2	I	T	POS Interface Transmit Address. The address is driven from the link layer to the PHY layer and selects the port that receives the next data packet. It is also used to poll the status of the transmit FIFOs through the PTPA pin. Address is sampled on the rising edge of TxClk.
TxSOC (ATM mode)	F1	I	T	UTOPIA Transmit Start Of Cell (SOC). TxSOC is asserted when TxData contains the first word of a cell. An interrupt is generated when TxSOC is asserted when already receiving a cell from the UTOPIA interface. TxSOC is sampled on the rising edge of TxClk.
TxSOP (POS mode)	F1	I	T	POS Interface Transmit Start Of Packet (SOP). TxSOP is asserted when TxData contains the first word of a packet. TxSOP is sampled on the rising edge of TxClk.
*TxEnb (ATM mode)	G2	I	T	UTOPIA Transmit Data Enable (active-low). *TxEnb indicates that TxData[15:0] contains valid cell data. *TxEnb is sampled on the rising edge of TxClk.
*TxEnb (POS mode)	G2	I	T	POS Interface Transmit Data Enable (active-low). *TxEnb indicates that TxData[15:0] contains valid packet data. *TxEnb is sampled on the rising edge of TxClk.
TxClav[3:0] (ATM mode)	G4 F3 E1 E2	O	High-Z	UTOPIA Transmit Cell Available. Supports Cell-Level Handshake. Indicates that the transmit FIFO can accept a complete cell. The mode One Rx/Tx CLAV requires only TxClav[0]. TxClav[3:0] are updated on the rising edge of TxClk.
DTPA [3:0] (POS mode)	G4 F3 E1 E2	O	High-Z	POS Interface Direct Transmit Packet Available (DTPA). Transition HIGH indicates that a (predefined) minimum number of bytes is available in the corresponding FIFO. Once HIGH, the DTPA pin indicates that the FIFO is not full. Transition LOW indicates that the FIFO is full or almost full (programmable by the user). DTPA[3:0] is updated on the rising edge of TxClk.
PTPA (POS mode)	G4	O	High-Z	Polled Transmit Packet Available (PTPA). The PTPA [0] and DTPA [0] are physically the same pin with different functionality according to the selected mode. When operating in single TPA pin mode, DTPA pin [0] acts as PTPA. Transition HIGH indicates that a predefined number of bytes (in the Tx-FLL) is valid in the polled Tx FIFO. Transition LOW indicates that the FIFO is full or nearly full (as programmed in the Tx-FHL Register). PTPA is driven by the PHY when its address is polled on the address pins. Otherwise, it must be high-Zed.
TxPrty (ATM mode)	G3	I	T	UTOPIA Transmit Parity. TxPrty indicates odd parity of TxData[15:0]. Interrupt is optionally generated when a mismatch is found. The use of this pin is optional since cells with parity errors are transmitted. TxPrty is sampled on the rising edge of TxClk.
TxPrty (POS mode)	G3	I	T	POS Interface Transmit Parity. TxPrty indicates parity of TxData[15:0]. TxPrty is sampled on the rising edge of TxClk.

Table 3-1. UTOPIA Level 2 Interface (ATM Mode) (3 of 4)

Name	No.	I/O	Type	Functional Description
TxClk (ATM mode)	K2	I	T	UTOPIA Transmit Clock. Driven by the ATM layer. TxData[15:0], TxAdd[4:0], TxSOC, *TxEnb and TxPrty signals are sampled on the rising edge of this clock. TxClav[3:0] is updated on the rising edge of this clock.
TxClk (POS mode)	K2	I	T	POS Interface Transmit Clock. Driven by the link layer. TxData[15:0], TxAdd[4:0], TxSOP, *TxEnb and TxPrty, TxEOP, TxMOD, TxERR signals are sampled on the rising edge of this clock. DTPA[3:0] is updated on the rising edge of this clock.
RxData[15:0] (ATM mode)	A5 B6 A6 B7 A7 B8 A8 D9 C9 A9 D10 C10 C11 B11 A13 C13	O	High-Z	UTOPIA Receive Data. Cell data is transferred from the PHY layer to the ATM layer. Data is updated on the rising edge of RxClk and is valid only when *RxEnb is sampled while asserted.
RxData[15:0] (POS mode)	A5 B6 A6 B7 A7 B8 A8 D9 C9 A9 D10 C10 C11 B11 A13 C13	O	High-Z	POS Interface Receive Data. Packet data is transferred from the PHY layer to the link layer. Data is updated on the rising edge of RxClk and is valid only when *RxEnb is sampled while asserted.
RxAdd[4:0] (ATM mode)	B3 C4 B5 C6 D7	I	T	UTOPIA Receive Address. The ATM layer drives the address to the PHY layer and selects the port from which the next cell(s) is taken. When using modes One Rx/Tx CLAV or Multiplexed Status Polling, it is also used to poll the status of the receive FIFOs. Address is sampled on the rising edge of RxClk.
RxAdd[4:0] (POS mode)	B3 C4 B5 C6 D7	I	T	POS Interface Receive Address. The link address layer drives the PHY layer and selects the port from which the next packet-data is taken. It is also used to poll the status of the receive FIFOs using the PRPA pin. Address is sampled on the rising edge of RxClk.

Table 3-1. UTOPIA Level 2 Interface (ATM Mode) (4 of 4)

Name	No.	I/O	Type	Functional Description
RxSOC (ATM mode)	A16	O	High-Z	UTOPIA Receive Start Of Cell. RxSOC is asserted when RxData[15:0] contains the first word of the cell. RxSOC is updated on the rising edge of RxClk.
RxSOP (POS mode)	A16	O	High-Z	POS Interface Receive Start Of Packet. RxSOP is asserted when RDAT[15:0] contains the first word of the packet. RxSOP is updated on the rising edge of RxClk.
*RxEnb (ATM mode)	C17	I	T	UTOPIA Receive Data Enable (active-low). When asserted, it indicates that the PHY port has permission to transfer valid cell data, if available. *RxEnb is sampled on the rising edge of RxClk.
*RxEnb (POS mode)	C17	I	T	POS Interface Receive Data Enable (active-low). When asserted, it indicates that the PHY port has permission to transfer valid packet data, if available. *RxEnb is sampled on the rising edge of RxClk.
RxClav[3:0] (ATM mode)	A14 B14 C14 D14	O	High-Z	UTOPIA Receive Cell Available. Support Cell Level Handshake indicates that the receive FIFO has a complete cell available. The mode One Rx/Tx CLAV requires only RxClav[0]. RxClav[3:0] are sampled on the rising edge of RxClk.
DRPA[3:0] (POS mode)	A14 B14 C14 D14	O	High-Z	POS Interface Receive Packet Available. Indicates that the receive FIFO has at least one End-Of-Packet available or a predefined number of bytes. DRPA[3:0] are sampled on the rising edge of RxClk.
PRPA (POS mode)	A14	O	High-Z	Received Polled Packet Available. Indicates that data is valid in the polled Rx FIFO. Logic 1 indicates at least one End-Of-Packet or a predefined number of bytes is available in the FIFO. Logic 0 indicates there is no End-Of-Packet in the FIFO and the number of valid bytes is below the predefined threshold. The PHY drives the PRPA when its address is selected on the address pins. Otherwise, it must be high-Zed. This pin is physically the same pin as DTPA[0], which functions according to the POS Interface configuration
RxPrty (ATM mode)	B15	O	High-Z	UTOPIA Receive Parity. RxPrty indicates odd parity of RxData[15:0]. RxPrty is updated on the rising edge of TxClk.
RxPrty (POS mode)	B15	O	High-Z	POS Interface Receive Parity. RxPrty indicates parity of RxData[15:0]. RxPrty is updated on the rising edge of RxClk.
RxClk (ATM mode)	C12	I	T	UTOPIA Receive Clock. Driven by the ATM layer. RxData[15:0], RxSOC, RxClav, and RxPrty signals are updated on the rising edge of this clock. RxAdd[4:0] and *RxEnb are sampled on the rising edge of this clock.
RxClk (POS mode)	C12	I	T	POS Interface Receive Clock. Driven by the link layer. RxData[15:0], RxSOP, DRPA, RxPrty, RxSOP, RxEOP, RxMOD, and RxERR signals are updated on the rising edge of this clock. RxAdd[4:0] and *RxEnb are sampled on the rising edge of this clock.
NOTE(S): I = Input, O = Output, E = PECL, T = TTL				

3.2 PIN Description (POS Mode)

Table 3-2. PIN Description (POS Mode)

Name	No.	I/O	Type	Functional Description
STPA	E3	O	High-Z	Tx Selected Packet Available. Transition HIGH indicates that the number of words are less than the value predefined by the Tx-FLL in the selected FIFO (the FIFO to which data is currently being sent). Transition LOW indicates that the number of words (32-bit) are more than the value predefined in the Tx-FHL in the selected FIFO. The PHY drives the STPA when its address is selected on the address pins. Otherwise, it must be high-Zed.
TxMOD (POS mode)	C1	I	T	Transmit Word Modulo. Indicates the length of the current word being transmitted. TxMOD should always be LOW, except during the last word transfer of a packet (TxEOP). Logic 1 indicates that only the eight MSBs of the last word are valid. Logic 0 indicates that all 16 bits of the last word of a packet are valid.
TxEOP (POS mode)	E4	I	T	Transmit End-Of-Packet. Marks the end of a packet on the data bus. When TxEOP is HIGH, it indicates that the last word of a packet is present on the data bus (TDAT). Assertion of both TxEOP and TxSOP is legal, and is used to indicate one- or two-byte-long packets.
TxERR (POS mode)	D3	I	T	Transmit Error. Indicates the current packet is aborted and should be discarded. TxERR should be asserted only during the last word of a packet.
RVAL (POS mode)	C16	O	High-Z	Receive Signal Validity. The RVAL indicates the validity of the receive data. When the RVAL is HIGH, receive data pins are valid. Otherwise, the receive signals must be discarded. RVAL transitions LOW on a FIFO empty condition or on End-Of-Packet. No transaction with the receive FIFO can be performed while the RVAL is deasserted. RVAL allows monitoring of the selected FIFO during a data transfer. The monitoring of other FIFOs is done with the DRPA pins. After deassertion the RVAL will be reasserted after the current FIFO is deselected. RVAL is driven by the PHY when its address is selected on the address pins. Otherwise, it must be high-Zed.
RxMOD (POS mode)	D16	O	High-Z	Receive Word Modulo. Indicates the length of the current word being received. RxMOD should always be LOW, except during the last word transfer of a packet (RxEOP). Logic 1 indicates that only the eight MSBs of the last word are valid. Logic 0 indicates that all 16 bits of the last word of a packet are valid.
RxEOP (POS mode)	B16	O	High-Z	Receive End-Of-Packet. Marks the end of a packet on the data bus. When RxEOP is HIGH, it indicates that the last word of a packet is present on the data bus (TDAT). Assertion of both RxEOP and RxSOP is legal and is used to indicate one- or two-byte-long packets.
RxERR (POS mode)	A18	O	High-Z	Receive Error. Indicates the current packet is aborted and should be discarded. RxERR should be asserted only during the transfer of the last word of a packet.
NOTE(S): I = Input, O = Output, E = PECL, T = TTL				

3.3 Line Interface Pins

Table 3-3. Line Interface Pins

Name	No.	I/O	Type	Functional Description
RxD0+ RxD0– RxD1+ RxD1– RxD2+ RxD2– RxD3+ RxD3–	V3 Y1 W6 V7 Y14 Y15 W18 V18	I	E	Line Receive Data. Ports 0–3 differential data inputs. These inputs contain NRZ encoded data. Ports 0–3 receive clocks are recovered from these inputs.
TxD0+ TxD0– TxD1+ TxD1– TxD2+ TxD2– TxD3+ TxD3–	Y4 W5 V9 Y9 Y17 W17 T17 U20	O	E	Line Transmit Data. Port 0–3 differential data outputs. These outputs contain NRZ encoded data.
SD0, SD1, SD2, SD3	T3 U2 T20 R18	I	E	Signal Detect. Single-ended PECL input. This signal indicates the presence of a valid signal from the optical transceiver per port. Active-High. A Low signal indicates a loss of signal.
RefCLK	W12	I	E	Reference Clock Inputs
PCAP0, PCAP1, PCAP2, PCAP3,	Y2 Y7 W15 Y20	—	—	External PLL capacitor. These pins are provided to connect the external capacitor of the internal PLLs.
NCAP0, NCAP1, NCAP2, NCAP3,	W4 V8 Y16 W20	—	—	External PLL capacitor. These pins are provided to connect the external capacitor to the internal PLLs.
REXT0, REXT1	Y10 Y11	—	—	External PLL resistor. These pins are provided to connect an external resistor for the internal PLL.
PHYBPSS	U1	I	T	Analog test mode. Reserved for manufacturer's testing. Should be connected to GND.
RECCLK0, RECCLK1, RECCLK2, RECCLK3	V1 T4 T18 T19	O	T	Recovered clock divided by 8. This is a 19.44 MHz clock optionally active for each port or optionally an 8 kHz clock synchronized with each frame received.

3.4 Data Communication Channel Interface Pins

Table 3-4. Data Communication Channel Interface Pins

Name	No.	I/O	Type	Functional Description
RSDCD1–4	T2 D5 C15 J20	O	T	The received section-DCC bytes (D1–D3) are serialized out using these pins, clocked by RSDCC1–4. A dedicated pin is available for each port. Per-port disabling of this pin is optional.
RSDCC1–4	P3 A4 A15 H19	O	T	The received section DCC (D1–D3) clock. This is a 216 kHz clock (50% duty cycle), which is active for part of the frame time, and produces a nominal rate of 192 kHz to update the RSDCD1–4 pins. A dedicated pin is available for each port. Per-port disabling of this pin is optional.
RLDCD1–4	M1 B2 D12 D20	O	T	The received line-DCC bytes (D4–D12) are serialized out using these pins, clocked by RLDCC1–4. A dedicated pin is available for each port. Per port disabling of this pin is optional.
RLDCC1–4	N2 D1 A17 F19	O	T	The received line DCC (D4–D12) clock. This is a 648 kHz clock (50% duty cycle), which is active for part of the frame time and produces a nominal rate of 576 kHz to update the RLDCD1–4 pins. A dedicated pin is available for each port. Per port disabling of this pin is optional.
TSDCD1–4	F2 C7 D18 P17	I	I	The transmit section-DCC bytes (D1–D3) are serialized using these pins, clocked by TSDCC1–4. A dedicated pin is available for each port. Per-port disabling of this pin is optional.
TSDCC1–4	G1 B10 C18 N18	O	T	The transmit section DCC (D1–D3) clock. This is a 216 kHz clock (50% duty cycle), which is active for part of the frame time, and produces a nominal rate of 192 kHz to sample the TSDCD1–4 pins. A dedicated pin is available for each port. Per-port disabling of this pin is optional.
TLDCD1–4	K1 C8 B13 K20	I	I	The transmit line-DCC bytes (D4–D12) are serialized using these pins, clocked by TLDCC1–4. A dedicated pin is for each port. Per-port disabling of this pin is optional.
TLDCC1–4	H1 B9 B17 M19	O	T	The transmitted line DCC (D4–D12) clock. This is a 648 kHz clock (50% duty cycle) that is active for part of the frame time and produces a nominal rate of 576 kHz to sample the TLDCD1–4 pins. A dedicated pin is available for each port. Per-port disabling of this pin is optional.

3.5 Microprocessor Interface Pins

Table 3-5. Microprocessor Interface Pins

Name	No.	I/O	Type	Functional Description
D[15:0]	G20 H18 H20 J17 J18 J19 K17 K18 K19 L20 L18 L19 M20 M18 M17 N20	I/O	T	Microprocessor interface data bus
A[8:0]	C19 E17 C20 D19 E18 E19 F18 G17 E20	I	T	Microprocessor interface address bus
*CS	G18	I	T	Chip Select (active-low)
W/*R	G19	I	T	Write/Read control signal (High = Write, Low = Read).
*DSTRB	F20	I	T	Data strobe (active-low).
*READY	B20	O	High-Z	Ready (active-low) In Read cycle, when asserted, indicates to the microprocessor that the data on D[15:0] is valid and ready to be read. In Write cycle, when asserted, signals the μP that the Write cycle was completed.
*INTR	A19	O	Open Drain	Interrupt signal (active-low, open drain). When asserted, interrupt is active; Hi-Z when not asserted. This pin requires an external pullup. The Interrupt request is deasserted three cycles after all the Interrupt registers are read.

3.6 Alarms Status Serial Interface Pins

Table 3-6. Alarms Status Serial Interface Pins

Name	No.	I/O	Type	Functional Description
ASDO	N19	O	T	Alarms Status Data Out
*ASSTB	P20	O	T	Alarms Status Strobe (active-low)
ASCLK	P19	O	T	Alarms Status Clock
ASENB	P18	I	T	Alarms Status Enable When tied to VSS, ASDO and *ASCLK are disabled.

3.7 JTAG Interface Pins

Table 3-7. JTAG Interface Pins

Name	No.	I/O	Type	Functional Description
TDO	C3	O	High-Z	Test data output (when in JTAG mode). Leave unconnected when JTAG is not used.
TDI	A2	I	T	Test data input (when in JTAG mode). Tie to VDD when JTAG is not used (TMS is Low).
TCK	B4	I	T	Test Clock pin (when in JTAG mode). Tie to VDD when JTAG is not used.
TMS	C5	I	T	Test Mode Select pin. High = JTAG mode, Low = Normal mode.
*TRST	A3	I	T	Test Reset pin (when in JTAG mode). Tie to VSS when JTAG is not used (active-Low).

3.8 Scan Interface Pins

Table 3-8. Scan Interface Pins

Name	No.	I/O	Type	Functional Description
TM	B12	I	T	Test Mode. Engineering only. Enables scan mode testing. Active-high (Should be tied to VSS).
SCANEN	A12	I	T	Scan Enable. Engineering only. Enables scan shift in/out of the device. Active-high (Should be tied to VSS).

3.9 General Pins

Table 3-9. General Pins

Name	No.	I/O	Type	Functional Description
*RESET	B18	I	T	Device reset. Sets the CX29704 to its default initial state. When asserted, all outputs that may be in Hi-Z state return to this initial state. If the device is in power-down mode during power-up reset, a reset sequence should be reactivated when power down is released. This pin is active-low.

3.10 Power and Ground

Table 3-10. Power and Ground (1 of 2)

Name	No.	Type	Functional Description
VDD	C2 J1 R19 B19 A11 D6 D11 D15 F4 F17 K4 L17 R4 R17 U6 U10 U15	Power	Digital power.
VSS	D2 K3 R20 A20 A10 A1 D4 D8 D13 D17 H4 H17 J9–J12 K9–K12 L9–L12 M9–M12 N4 N17 U4 U8 U13 U17	Ground	Digital ground.

Table 3-10. Power and Ground (2 of 2)

Name	No.	Type	Functional Description
VDDD	U5 Y3 Y8 U9 V15 W16 U19 U18	Digital Power	Digital power for the line interface. Should be separated from the Digital Power pins (VDD) on the application board.
VDDA	W2 V4 Y6 W8 W10 V10 V12 U12 W14 U14 Y19 V19	Analog Power	Analog power.
VSSD	U3 V2 Y5 V6 U11 Y13 W13 Y18 U16	Digital Ground	Digital ground for the line interface. Should be separated from the Digital Ground pins (VSS) on the application board.
VSSA	W1 W3 V5 U7 W7 W9 W11 V11 Y12 V13 V14 V16 V17 W19 V20	Analog Ground	Analog ground.

4.0 Functional Description

4.1 Line Interface

4.1.1 Clock Synthesis

The Clock Synthesis block is responsible for generating a 155.52 MHz clock signal using a 19.44 MHz reference clock multiplied by 8. This 155.52 MHz synthesized clock output feeds into the Data and Clock Recovery block.

4.1.2 Data and Clock Recovery

This block performs data retiming and clock recovery from the incoming serial data stream. The 155 MHz clock is synthesized using a 19.44 reference clock. This synthesized clock is then provided to each port as the reference clock. Each port phase locks onto the data stream using the 155 MHz synthesized clock as a reference input and generates the recovered clock and data outputs.

4.1.3 LOCK Condition

The CX29704 constantly monitors for a LOCK state between the synthesized clock and the recovered clock. A LOCK state occurs when there is less than ±1000 PPM shift between the clocks. An Out-of-LOCK state is indicated as a Loss Of Signal (LOS) alarm (see Section 4.2.1.3).

4.1.4 Serial-to-Parallel

The Serial-to-Parallel block converts the incoming serial bit data into 8-bit (octet) parallel data.

4.1.5 Parallel-to-Serial

The Parallel-to-Serial block serializes and transmits the data from the framer clock.

4.1.6 Data Transmission

There are two modes of operation. By default, transmitted data is driven to the transceiver by the Clock and Data Recovery Block using the synthesized clock.

The user can also choose to drive data with the recovered clock by setting the Tx Timing Bit in Configuration Register A (Table 6-4 (Add: 0x02, 0x42, 0x82, 0xC2)) to a value of 1.

If no data is present at the input data stream (LOS indication), or the signal detect input (SD pin) is low, the transmission clock automatically switches to the synthesized lock. Once the cause for the clock switch (LOS or SD) is terminated, the transmit clock source returns to its configured source.

4.2 Receive

4.2.1 Rx SONET/SDH Framer

The framer performs framing and generates Loss Of Signal (LOS), Loss Of Frame (LOF), and Severe Error Framing (SEF) alarms.

4.2.1.1 Framing and Severe Error Framing (SEF)

On each frame, the framer compares the expected framing pattern (A1, A2) with the framing bytes received on incoming data in order to ensure frame alignment. An SEF defect is declared when four consecutive framing patterns contain errors. When an SEF defect is detected, the SONET/SDH framer begins searching for a framing pattern. When the framer recognizes two successive error-free framing patterns, the SEF defect is terminated.

An SEF Defect Generation/Termination status bit, with Interrupt, is provided (Bit 1 in Table 6-15).

4.2.1.2 Loss Of Frame (LOF)

The in-frame timer is activated if there is no SEF defect. The timer stops and is reset to zero when an SEF defect is detected. The SEF timer is activated when an SEF defect is present. The timer stops when the SEF defect is terminated. It is reset to zero when the SEF defect is absent continuously for 3 ms (the in-frame counter reaches 3 ms).

An LOF defect is detected when the SEF timer reaches the 3 ms threshold. The LOF defect is terminated when the in-frame counter reaches 3 ms. While the port is in LOF state, no values are captured in the device overhead bytes, and the last value before the LOF occurred remains in the overhead bytes.

An LOF Defect Generation/Termination status bit, with Interrupt, is provided (Bit 2 in Table 6-15).

4.2.1.3 Loss Of Signal (LOS)

An LOS defect is declared when the incoming data stream (before descrambling) contains an all-0s pattern for 20 µs or the Signal Detect (SD) signal indicates non-valid signal from the optical transceiver for 20 µs or an Out-of-LOCK condition was detected for 20 µs. The LOS defect is terminated when the incoming data stream contains two consecutive valid framing patterns and no LOS defect is detected in the intervening time and the Signal Detect (SD) signal indicates a valid signal from the optical transceiver and the device is in LOCK condition. While the port is in LOS state, no values are captured into the device overhead bytes, and the last value before the LOS occurred remains in the overhead bytes.

An LOS Defect status bit is provided (Bit 0 in Table 6-15 (Add: 0x12, 0x52, 0x92, 0xD2)).

4.2.2 Rx Overhead Processor

The overhead processor processes all section, line, and path overhead bytes and performs frame descrambling.

4.2.2.1 Frame Descrambler

Descrambling is performed using a 127-sequence-long, self-synchronous descrambler. The generating polynomial for the descrambler is $1+X^6+X^7$**.** The descrambler is set to all-1s on the Most Significant Bit (MSB) of the third byte following the J0 byte. The framing bytes (A1, A2), the section trace byte (J0), and the section growth bytes (Z0) are not descrambled.

Descrambler operation may optionally be bypassed.

4.2.2.2 Section Overhead

Section Error Monitor (B1)

The Section Error Monitor performs error monitoring on the entire frame by calculating the BIP-8 error code of the incoming frame before descrambling. The result is compared with the B1 overhead byte of the next frame. Any difference between matching bits indicates that a section bit interleaved parity error has occurred. The first bit of the B1 byte should reflect the even parity over the first bit of every byte in the entire frame. These parity bit errors are accumulated in a 16-bit saturating counter that can be read through the microprocessor interface. To avoid the possibility of loss of events, the counter should be polled at least once per second. An interrupt is generated upon detection of an error.

4.2.2.3 Section Data Communication Channel Extraction (D1–D3)

The three Section DCC overhead bytes (D1–D3) are captured and serially transmitted using a 216 kHz clock (with effective rate of 192 kHz). Certain systems require a serial port to extract the Section DCC bytes and implement management functions. This port can be optionally disabled.

4.2.2.4 Section Trace/Growth (J0/Z0)

The Section Trace bytes are captured and can be read through the microprocessor port. The data is not kept in the message format as the J1; however, the data is available in general purpose registers (Table 6-58).

4.2.2.5 Order Wire Byte (E1)

The Order Wire Byte, formerly used to facilitate a voice channel, is captured on the receive path and can be read through the microprocessor port.

4.2.2.6 Section User Channel (F1)

The Section User Channel byte is captured on the receive path and can be read through the microprocessor port.

4.2.2.7 Line Overhead

Automatic Protection Switching (APS) (K1, K2)

The K1 and K2 overhead bytes are used for handshaking between network elements that support APS when transmission failure occurs to determine whether or not to switch from the failed working channel to the protection channel.

Bits 0–2 of the K2 overhead byte are used for Alarm Indication Signal-Line (AIS-L) and Remote Defect Indication-Line (RDI-L) alarms which are described later in this chapter.

These bytes are available through the microprocessor interface for receive and transmit. In the receive path, the K1 and K2 bytes are captured when three consecutive identical new-frame values are received. APS Inconsistent State is entered when in 12 frames, no three consecutive frames are received with identical K1 byte. The APS state machine exits the Inconsistent State when three consecutive frames contain an identical K1 byte.

An interrupt is generated upon capture of new values of K1 and K2 bytes. An APS Inconsistent State status bit (Table 6-7 (Add: 0x5, 0x45, 0x85, 0xC5)) is provided and an Interrupt is generated when entering or exiting this state.

4.2.2.8 Line Error Monitor (B2)

The Line Error Monitor performs error searching on the entire frame (excluding the section overhead bytes) by calculating the BIP-24 error code of the incoming frame after descrambling. The result is compared with the B2 overhead bytes of the next frame. Any difference between matching bits indicates a line bit interleaved parity error has occurred. The first bit of the first B2 byte should reflect the even parity over the first bit of every three bytes in the entire frame. These parity errors are accumulated in a 32-bit saturating counter that can be read through the microprocessor interface. Interrupt generation upon detection of an error is optional.

A dedicated mechanism for enhanced Bit Error Rate (BER) monitoring is provided. The user can program a threshold of errors (number of line BIP-24 errors found) and the period during which this counting is done. The Period register is a 32-bit counter that counts the 19.44 MHz clock. For instance, a period of one second should be programmed to the Period register as a 0x128A180 value. The user should also program the threshold of errors (16-bit register), above which an interrupt is generated. When the period counter reaches the zero value (end of period), the error counter is reset to zero and the counting begins again. If the number of BIP-24 errors found in this period is greater than the threshold, an interrupt is generated to reflect this condition. The number of errors is counted based on the individual/frame counting mode, as specified in the Port Configuration register.

Table 4-1. Line Error Monitor

BER	Detect Time (ms)	B2 BER Period Register	B2 BER Threshold Register
10^{-3}	1	0x4BF0	0x9A
10^{-4}	2	0x97E0	0x1F
10^{-5}	16	0x4BF00	0x18
10^{-6}	128	0x25F800	0x13
10^{-7}	2,048	0x25F8000	0x1F
10^{-8}	16,384	0x12FC0000	0x18
10^{-9}	131,072	0x97E00000	0x13

4.2.2.9 Alarm Indication Signal-Line (AIS-L) Detection

An AIS-L defect is detected on the incoming signal when bits 0, 1, and 2 of the K2 byte contain the 111 pattern in five consecutive frames. The AIS-L defect is terminated when bits 0, 1, and 2 of the K2 byte contain any pattern other than 111 in five consecutive frames. AIS-L Defect status bit is provided and Interrupt upon generation and termination is optional.

4.2.2.10 Remote Defect Indication-Line (RDI-L) Detection

RDI-L defect is detected on the incoming signal when bits 0, 1, and 2 of the K2 byte in five consecutive frames contain the 110 pattern. RDI-L defect is terminated when bits 0, 1, and 2 of the K2 byte contain any pattern other than

110 in five consecutive frames. RDI-L Defect Status Generation/Termination bit is provided. Generation of an interrupt is optional.

4.2.2.11 Remote Error Indication-Line (REI-L) Accumulation and Transmission

The number of REI-L BIP-24 errors detected in the last received frame is accumulated in a 32-bit counter that can be read through the microprocessor port. Interrupt generation upon detection of an error is optional. On the transmit path, the number of errors found on the previous frame is transmitted through the M1 byte back to the transmitter.

4.2.2.12 Section Data Communication Channel Extraction (D4–D12)

The nine line DCC overhead bytes (D4–D12) are captured and serially transmitted out of the chip using a 648 kHz clock (with an effective rate of 576 kHz). This port can be optionally disabled.

4.2.2.13 Synchronization Status (S1)

The S1 bytes carry the synchronization status of the SONET/SDH device. The target is to allow the selection of the best clock from the available sources. Bits [0:3] of the Synchronization Status Message register can be optionally read via the microprocessor port on the receive path and transmitted with a non-default value on the transmit path.

4.2.2.14 Order Wire Byte (E2)

The Order Wire byte, formerly used to facilitate a voice channel, is captured on the receive path and can be read through the microprocessor port.

4.2.2.15 Path Overhead

STS SPE Pointer Interpretation (H1, H2, H3)

During normal operation, the pointer value (H1, H2) represents the offset from the H3 byte to the first byte of the STS SPE (J1). Any consistent new value received three successive times replaces the current value. If an increment is detected, the byte following the H3 is considered a positive stuff byte, and the pointer value is incremented by one. If a decrement is detected, then H3 is considered a negative stuff byte, and the pointer value is decremented by one. If a set New Data Flag (NDF) is detected, the new pointer value replaces the old pointer value.

4.2.2.16 Pointers Interpretation Model (LOP, AIS-P)

The pointer interpretation can be modeled as a finite state-machine, holding three-states: NORM, AIS, LOP. The transition between the states occurs after detecting three consecutive events of the same type (with the exception of transition from AIS_state to NORM_state by Norm_NDF). The following events drive the transition:

- NORM_point—Normal NDF and offset value in range with valid concatenation values.
- NDF_enable/Set_NDF—NDF enabled AND offset value in range.
- AIS_ind—11111111 11111111 (in H1 and H2 bytes).
- Incr_ind—Normal NDF AND majority of I bits inverted AND no majority of D bits inverted AND previous NDF_enable, incr_ind or decr_ind.
- Decr_ind—Normal NDF AND majority of D bits inverted AND no majority of I bits inverted AND previous NDF_enable, incr_ind or decr_ind.
- Inv_point—Any other OR norm_point with an offset value not equal to the active offset is defined as Invalid-Pointer.

The transitions indicated in the state diagram are defined as follows:

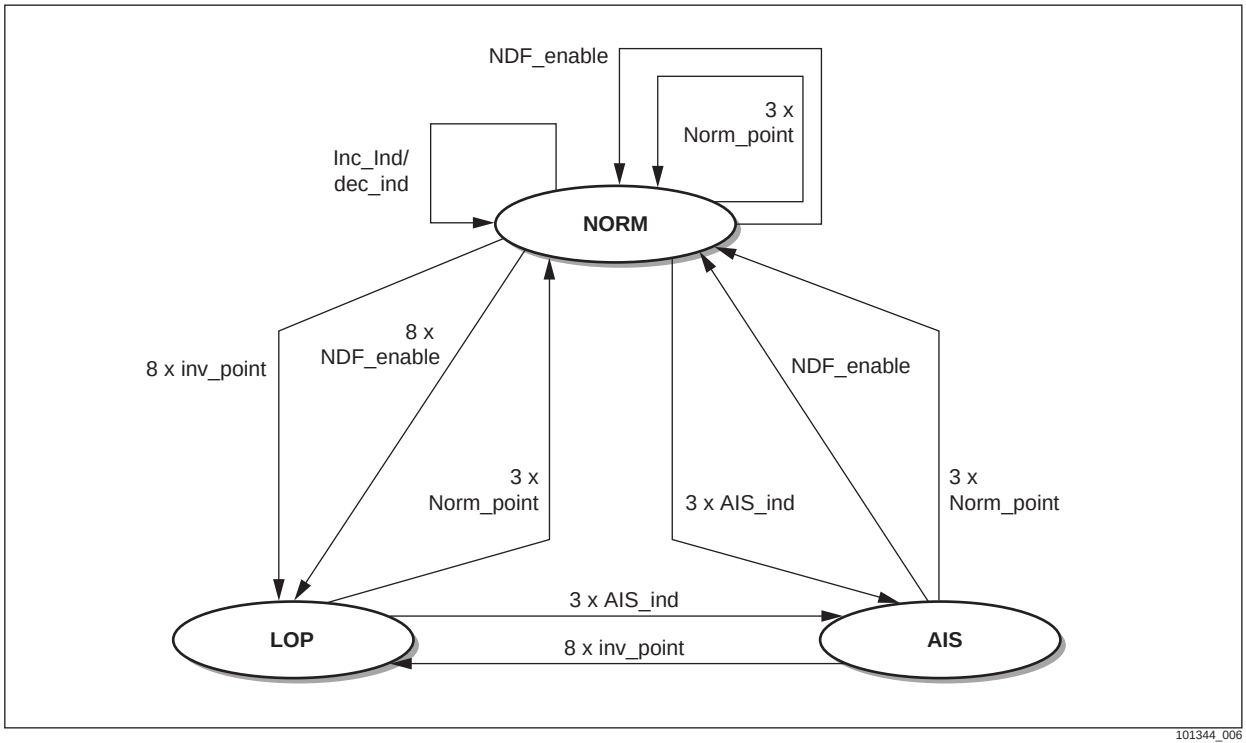
- Inc_ind/dec_ind—Offset adjustment (increment or decrement indication).
- 3 x norm_point—Three consecutive equal norm_point indications.
- NDF_enable—Single NDF_enable indication.
- 3 x AIS_ind—Three consecutive frames with AIS indications.

- 8 x inv_point—Eight consecutive inv_point (SDH mode only).
- 8 x NDF_enable—Eight consecutive NDF_enable.

NOTE(S):

1. Active offset is defined as the accepted current phase of the VC in the NORM_state and is undefined in the other states.
2. NDF enabled is equal to 1001, 0001, 1101, 1011, 1000.
3. Normal NDF is equal to 0110, 1110, 0010, 0100, 0111.
4. The transitions from NORM to NORM do not represent changes of state but imply offset changes.
5. 3 x norm_point takes precedence over 8 x inv_point.

Figure 4-1. Port Interpretation State Diagram



An LOP failure is defined as a transition of the pointer interpreter from the NORM_state to the LOP_state or the AIS_state.

As seen, LOP-P defect is declared if no valid pointer is found in eight consecutive frames or if eight consecutive NDFs are detected. LOP-P is not detected when the pointer contains an all-1s pattern or when AIS-P is detected. An LOP-P defect is terminated when there is a valid pointer with normal NDF in three consecutive frames. LOP-P defect status bit is provided and Interrupt upon generation and termination is optional.

4.2.2.17 Path Error Monitor (B3) and REI-P

This block performs error monitoring on the entire STS SPE by calculating the BIP-8 error code of the incoming SPE after descrambling. The result is compared with the B3 overhead byte of the next frame. Any difference between matching bits indicates that a path bit interleaved parity error has occurred. The first bit of the B3 byte should reflect the even parity over the first bit of every byte in the entire SPE. These parity bit errors are accumulated in a 16-bit saturating counter that can be read through the microprocessor interface. Bits 4–7 of the transmitted

G1 overhead byte are allocated to the REI-P count transmitted on the last frame. To avoid losing events, the counter should be polled at least once per second. Interrupt generation upon detection of an error is optional.

4.2.2.18 Remote Defect Indication-Path (RDI-P) Detection

The following error monitors are provided by the multioption ERDI-P indication. For enhanced RDI-P (ERDI-P), a defect is detected on the incoming signal when a defect sequence is received in bits 1–3 of the G1 overhead byte for ten consecutive frames. The RDI-P defect is terminated when a no-defect sequence is received in bits 1–3 of G1 for ten consecutive frames. ERDI-P defect declaration is terminated when a 000 or 001 (SONET mode); or 011, 001, or 000 (SDH mode) is received in bits 1–3 of G1 for ten consecutive frames.

Table 4-2. ERDI-P Defect Coding

G1 bits 1,2,3	Priority of ERDI-P codes (for SONET)	Interpretation	
—	—	SONET	SDH
000	NA	No defects	No defects
100	NA	AIS-P, LOP-P, LOS, LOF, AIS-L (1-bit RDI-P)	AIS-P, LOP, UNEQ, LOS, LOF, AIS-L
010	3	PLM-P, LCD-P	LCD
110	2	UNEQ-P	UNEQ
001	4	No defects	No defects
101	1	AIS-P, LOP-P, LOS, LOF, AIS-L	AIS-P, LOP, LOS, LOF, AIS-L
011	—	NA	No defect
111	—	NA	AIS-P, LOP, UNEQ, LOS, LOF, AIS-L

An RDI-P Defect Status Generation/Termination bit is provided, and Interrupt is optional. Upon defect detection, the RX-RDIP register should be read to determine what generated this event.

For PLM and UNEQ descriptions, refer to the STS Path Signal Label (C2) in Section 4.2.2.21.

4.2.2.19 Remote Error Indication-Path (REI-P) Accumulation

REI-P (SPE BIP-8 errors detected by B3) are accumulated in a 16-bit saturating counter. The number of errors detected over the last frame is transmitted back by G1 overhead byte. Bits 4–7 of the G1 byte contain the number of REI-P errors detected over the last frame by the transmitting device. The legal values of the 4-bit field are 0–8. Any other value is considered as zero. Interrupt generation upon detection of an indication is optional.

4.2.2.20 Rx Path Trace Buffer (J1)

A 16-byte (SDH mode) or 64-byte (SONET mode) array is available for receiving through the path identifier byte J1. Data to the array is written or read via the Path Trace Address register and the Path Trace Data register.

An interrupt is generated whenever a new message is received for two successive frames. The Rx Path Trace array can be read by reading the 16 or 64 bytes from the registers that compose this array. The selection of which part (i.e., register) of the array will be read is determined by the Rx Path Trace address. To

begin reading the array, an address is loaded to the Rx Path Trace address. Generally, this is the first address of the array. The R/W bit should be set to 1 (Read mode) and the Rx/Tx bit of the register set to 1 (reading the receive buffer).

A 16-bit microprocessor read cycle should be performed from the address mapped to the Rx Path Trace array. After this reading cycle, the Path Trace address is auto-incremented to point to the next 16 bits of the array. The next reading cycle is from the same address of the microprocessor port but with an auto-incremented pointer (Rx Path Trace address). After 8 read cycles (SDH mode) or 31 read cycles (SONET mode), the reading is completed and the Rx Path Trace address is loaded with its initial value. The identifier is received using the J1 overhead byte on each frame. The first byte of the identifier (one in MSB for SDH mode or the first byte after CR (0x0D) and LF(0x0A) for SONET mode) is located in the LSB of the word in address 0x0 and the second byte on the MSB. Each byte received is compared with the appropriate byte in the previous identifier. When two new identical consecutive identifiers are received, an interrupt is generated.

To summarize the process of reading the Path Trace message, the following steps are required:

1. Receive an interrupt that points to a new message.
2. Load the Path Trace address with the first address in the array.
3. Read the first 16-bit word of the array (after which the address register is auto-incremented).
4. Repeat Step 3, if required.

4.2.2.21 STS Path Signal Label (C2)

The Path Signal label indicates the type of content being carried to the network by the SPE. A value of 0x13 indicates ATM transport, a value of 0xCF indicates non-scrambled POS/SDH data, and a value of 0x16 indicates a scrambled POS/SDH data.

Path Label Mismatch (PLM)—PLM defect sets when C2, different than 0x13 for ATM mode, (In the range of 02–FE except FC) is received for five consecutive frames. A PLM defect is cleared when C2 is found with a matched value in five consecutive frames (five consecutive frames with any value that does not create a PLM error). A PLM defect is set when C2 is different than 0xCF (for unscrambled POS mode) or different than 0x16 (or scrambled POS) is received during five consecutive frames. A PLM defect is cleared when during five consecutive frames C2 is found with a matched value.

UNEQ (UNEQuipped)—UNEQ defect is set when C2 = 00, during five consecutive frames. A UNEQ defect is cleared when C2 does not equal 00 during five consecutive frames.

Receiving an FF value in C2 does not cause the detection of a new UNEQ or PLM defect, nor does it cause an existing UNEQ or PLM defect to be terminated.

4.2.2.22 Path User Channel Byte (F2)

The receive path captures the Path User Channel Byte (F2) and is read through the microprocessor port.

4.2.2.23 Path Growth Byte (F3)

The receive path captures the Path Growth Byte (F3) and is read through the microprocessor port.

4.2.2.24 Path Growth Bytes (Z4–Z5)

The receive path captures the Path Growth Bytes (Z4–Z5) and is read through the microprocessor port.

4.2.3 Rx ATM Cell Processor

This processor operates in ATM mode only.

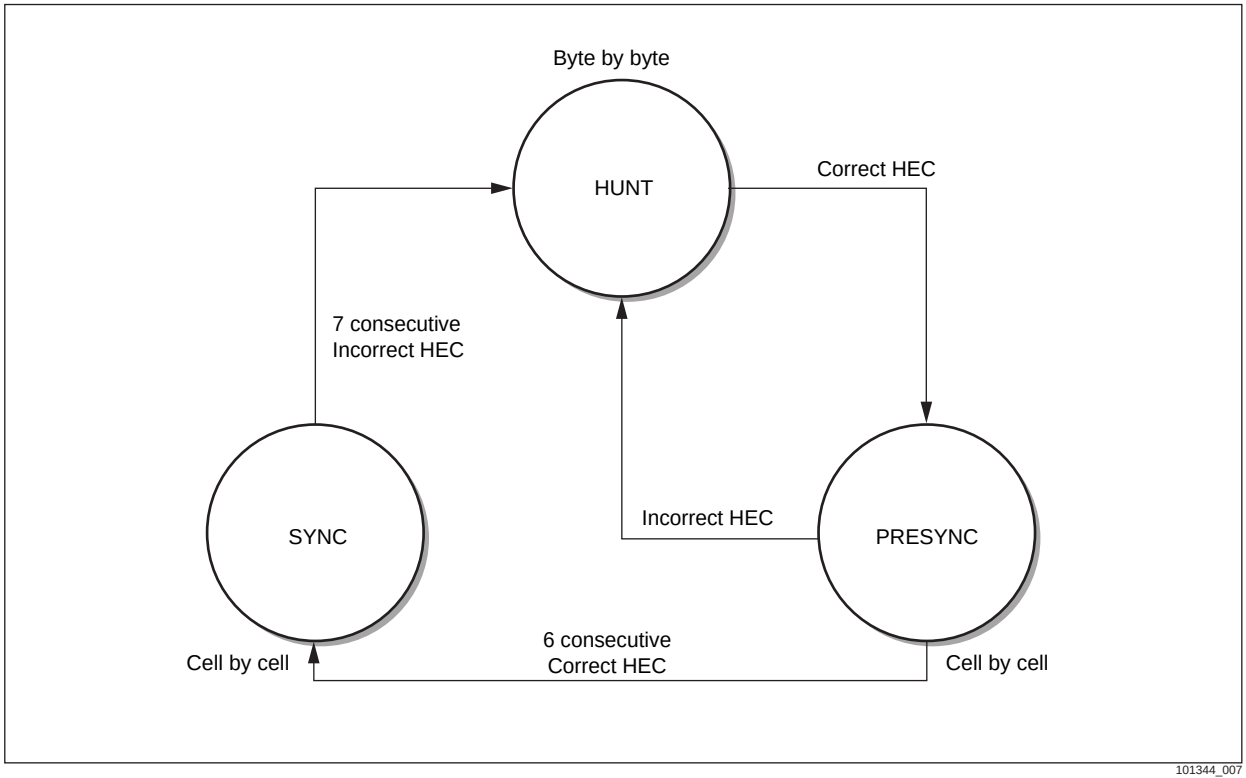
The ATM cell processor performs cell delineation, cell descrambling, idle/unassigned cell filtering and header error detection or correction.

4.2.3.1 Cell Delineation

The Cell Delineation function enables the identification of cell boundaries. This process is achieved with the following three states:

1. HUNT State—Processes the incoming data byte by byte to find a match between the calculation of HEC for an assumed header field and the assumed HEC field. Once this match is found, the system enters the PRESYNC state.
2. PRESYNC State—Searches for six consecutive correct HECs on a cell by cell basis. If an incorrect HEC is found, the process returns to the HUNT state.
3. SYNC State—The only state that enables transmission of cells to the ATM layer. If an incorrect HEC is found seven consecutive times, the cell delineation is assumed to be lost and the process returns to the HUNT state.

Figure 4-2. Cell Delineation State Machine



4.2.3.2 Out of Cell Delineation (OCD)

An OCD is declared when the cell delineation state machine is found in the HUNT or PRESYNC state. OCD is terminated when the cell delineation state machine is in the SYNC state or when LCD defect is declared.

An OCD Defect Status (upon generation and termination) bit is provided (Table 6-21 (Add: 0x18, 0x58, 0x98, 0xD8)) along with an Interrupt.

4.2.3.3 Loss of Cell Delineation (LCD)

An LCD defect is declared when an OCD anomaly persists for 4 ms. An LCD defect is terminated when the cell delineation state machine enters the SYNC state for at least 4 ms.

An LCD Defect Status bit is provided (Table 6-21 (Add: 0x18, 0x58, 0x98, 0xD8)), and an Interrupt upon generation and termination is optional.

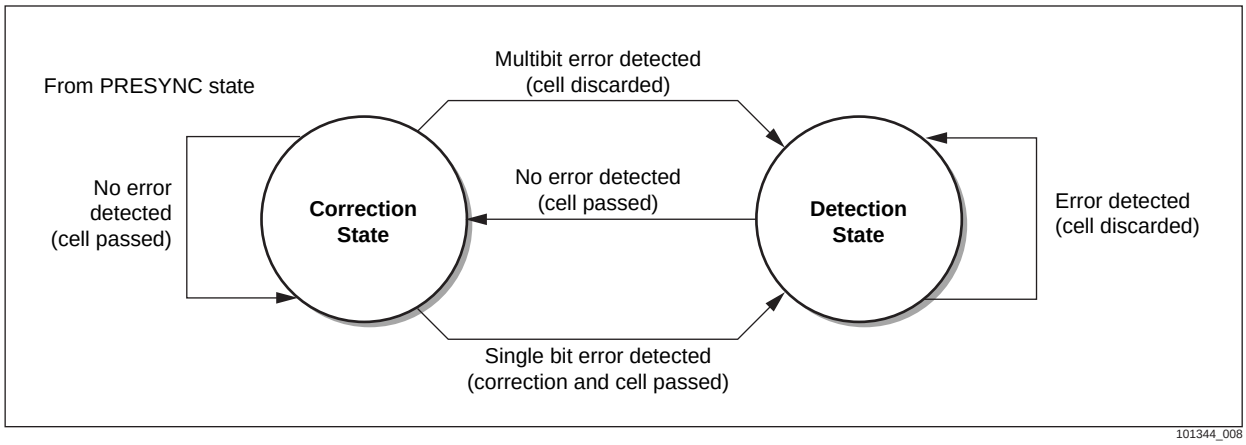
4.2.3.4 HEC Verification

There are two states of operation for HEC verification:

1. Detection State—The HEC is calculated and the result is compared with the polynomial found on the HEC octet after subtracting the polynomial $X^6 + X^4 + X^2 + 1$. If these polynomials are not the same, the cell is discarded.
2. Correction State—This procedure is similar to the Detection state except that when a single bit error is detected in the Correction state, correction is performed. The cell is then passed and the state machine enters the Detection state.

When in the SYNC state, the Correction state is entered. If an error is detected, the state machine enters the Detection state. As long as errors exist, the state machine remains in the Detection state. If no errors are detected, the state machine returns to the Correction state. Disabling the Correction state (i.e., working in the Detection state only) is optional.

Figure 4-3. Correction Mode State Machine



4.2.3.5 Cell Descrambling

Cell level descrambling is performed by using the self-synchronous descrambler polynomial $X^{43} + 1$.

The descrambler operates only on the information field and is suspended during the five octets of the header and when in HUNT state. The descrambling operation can be optionally bypassed.

4.2.3.6 Cell Filtering

Idle/unassigned and bad header cells are filtered by not being passed to the Rx FIFO.

4.2.3.7 Performance Counters

To provide the system with specific knowledge on the quality of the physical connections, four dedicated counters are available to be read through the microprocessor port. Each counter is reset to zero value upon reading its content.

- 16-bit counter—accumulates the number of uncorrectable HEC errors found
- 16-bit counter—accumulates the number the cells with correctable HEC errors
- 32-bit counter—accumulates the number of error-free cells put in the Rx FIFO
- 32-bit counter—accumulates the number of transmitted cells (excluding idle/unassigned cells)

4.2.4 POS Rx Packet Processor

This processor operates only in POS mode.

The Rx packet processor performs frame delineation, packet extraction, FCS error detection and payload descrambling. After processing the frame, only the information part passes to the POS interface.

Table 4-3. The Rx Frame Format

Flag	Information	FCS	Flag	Interframe Fill Or Next Information
0x7E	Variable Length	16/32 bits	0x7E	—

4.2.4.1 Descrambling

The self-synchronous descrambler, using the polynomial $X^{43} + 1$, operates on the POS data stream. Descrambling is done directly on the data stream coming from SONET/SDH SPE (before any preprocessing). By default, the descrambler is enabled.

4.2.4.2 Frame Delineation

Frame delineation is achieved by searching for the flag character (0x7E) in the descrambled data stream. The flags are removed upon detection.

4.2.4.3 Byte Destuffing

Byte destuffing is performed by searching for a Control Escape character (0x7D) in the data stream. When such a character is detected, it is removed, and the following byte is Exclusive-ORed with the value 0x20. Table 4-4 lists the Character Escape Map.

Table 4-4. Character Escape Map—Byte Destuffing

Sequence	Escaped
7E	7D–E5
7D	7D–5E
Abort	7D–7E

4.2.4.4 Frame Check Sequence (FCS) Verification

The FCS value is verified on the entire information field after descrambling and byte destuffing. The FCS value is generated by a CRC-CCITT (two-byte) or CRC-32 (four-byte) calculation. If an error is found, the packet is marked as a defective packet that should be discarded. FCS calculation and insertion can optionally be disabled.

The CRC-CCITT is two-bytes long and is calculated by the polynomial $1+ X^5 + X^{12} + X^{16}$. The CRC-32 is four-bytes long and is calculated by the polynomial $1+ X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$.

4.2.4.5 Performance Counters

To provide the system with specific knowledge on the quality of the physical connections, the following five dedicated counters can be read through the microprocessor port:

- 16-bit counter—accumulates the number of FCS errors found.
- 16-bit counter—accumulates the number the packets violating the minimum length-limit of a packet.
- 16-bit counter—accumulates the number the packets violating the maximum length-limit of a packet.
- 16-bit counter—accumulates the number of aborted packets.
- 32-bit counter—accumulates the number of error-free packets.

Each counter is reset to a zero value upon reading its content.

When a packet violates the minimum-length criteria, it is marked as defective and passed to the FIFO. When a packet violates the maximum length criteria, it is marked as a defective packet and the following bytes are discarded. The packet that violates the maximum length criteria is marked with the assertion of the POS Interface Error pin while being read from the FIFO by the link layer. The maximum and minimum packet length is defined in the Rx-Max_Pack_Length and Rx-Min_Pack_length registers. A packet is also considered defective if it does not include at least one data byte in addition to the FCS field (when the FCS verification option is enabled).

4.2.5 Rx ATM Interface Cell FIFO

The Rx ATM Interface Cell FIFO compensates for temporary timing differences between the physical and ATM layer. The ATM cells are inserted into the Rx FIFO using the recovered clock divided by eight. The ATM cells are drawn from the Rx FIFO using the UTOPIA Level 2 Interface Rx clock. The FIFO has a four-cell capacity and provides FIFO management used by the UTOPIA interface. The FIFO can be reset by software via the port FIFO Control/Status register.

4.2.6 Rx POS Interface FIFO

The Rx POS Interface FIFO can store up to 256 bytes of data, plus additional management information. The FIFO logic functionality includes flagging the availability status of the data in the FIFO, as well as flagging FIFO overrun and underrun. When an overrun is encountered, the writing of data to the FIFO is disabled. Writing to the FIFO resumes after the existing FIFO data is read and a "Start-of-Packet" is detected in the receive path. Thus, the first data word to be written after an overrun state is the start of a packet. When the POS-interface tries to read data from an empty FIFO an underrun occurs and invalid data is read; however, data is written to the FIFO as soon as it becomes available. An interrupt upon overrun/underrun detection is optional.

The FIFO threshold is the number of bytes available in the FIFO. The FIFO flags the link layer that free bytes are available, and that the number of available bytes in the FIFO is more than the value held by the Rx_FHL Register. The available data indication terminates when the number of available bytes in the FIFO is less than value held by the Rx_FLL Register. (The FHL and FLL registers specify the number of bytes in 32-bit granularity.) When a Packet-Abort command is detected on the receive path, the packet is marked with an error flag, and no more data is written to the FIFO until a "Start-Of-Packet" is detected.

4.3 Transmit

4.3.1 Tx ATM Interface Cell FIFO

This block compensates for temporary timing differences between the physical layer and the ATM layer. The ATM cells are inserted into the Tx FIFO using the UTOPIA Level 2 Interface Tx clock. The ATM cells are drawn from the Tx FIFO using the recovered clock (divided by eight) or the reference clock. The Tx ATM Interface FIFO has a four-cell capacity and provides the FIFO management used by the UTOPIA interface.

4.3.2 Tx POS Interface FIFO

The Tx POS Interface FIFO can store up to 256 bytes plus additional management information. The FIFO logic functionality includes flagging the availability status of the data in the FIFO, and flagging FIFO overrun and underrun. When an overrun is detected, the current packet continues to be transmitted. To avoid redundant packet abortion, an "Abort-Sequence" is transmitted only when the overran word is transmitted. After transmission of an "Abort-Sequence," no new data is transmitted until a "Start-Of-Packet" is detected in the FIFO. The detection of the overrun state does not force the transmission of an automatic "Abort-Sequence". In a case where the current (or any other) packet is completely transmitted, no packet abort is transmitted. In case of underrun (an empty FIFO state during which a packet is transmitted), an abort sequence is transmitted and all the bytes associated with this packet are replaced by a Flag sequence. Data transmission resumes after a "Start-of-Packet" is detected. Generation of an interrupt upon overrun/underrun detection is optional.

The Threshold registers (Tx-FHL and Tx-FLL) determine the minimum/maximum number of double (four-byte) words in the FIFO. The Threshold registers also determine under what conditions the FIFO flags the link-layer as available/unavailable for writing. When the number of words in the FIFO is greater than Tx-FHL (in four-byte granularity), the FIFO flags the link layer to stop sending data. When the number of words in the FIFO is less than Tx-FLL, the FIFO flags the link layer that it is ready for data to be written. The transmission of packets starts whenever the number of words in the FIFO is greater than the number held by the Tx-thresh. This register is used to avoid underrun of the FIFO and allows the user to determine the FIFO characteristics. The Tx-IFF (Inter-Fill Flag) determines the number of flags that separate each two packets on the transmission side. Although the value held in the FHL and FLL registers is in double (four-byte) word boundaries, the packet can also be in byte boundaries.

4.3.3 Tx ATM Cell Processor

The cell processor performs HEC insertion, cell scrambling, and cell rate decoupling to prepare the cells for encapsulation in the SONET/SDH frame.

4.3.3.1 Header Error Check (HEC) Insertion

The HEC is calculated as follows:

$$\frac{(\text{content of the header}) \times X^8}{X^8 + X^2 + X + 1}$$

The result residue is added (Modulo 2) to the co-set polynomial $X^6 + X^4 + X^2 + 1$ and inserted into the HEC octet of the ATM cell.

4.3.3.2 Cell Scrambling

Cell-level scrambling is performed using the self-synchronous scrambler polynomial $X^{43} + 1$. The scrambler operates only on the information field. At reset, the scrambler is initialized to an all-1s state. The scrambling operation can be bypassed.

4.3.3.3 Cell Rate Decoupling

Idle/Unassigned cells are generated when there are no cells available in the Tx FIFO.

4.3.4 POS—Tx Packet Processor

The Tx packet processor performs frame generation, frame encapsulation, FCS error-code calculation, byte-stuffing, and payload scrambling. The FCS, byte-stuffing, and scrambler can be either disabled or enabled independently.

Table 4-5. The Tx Frame Format

Flag	Information	FCS	Flag	Interframe Fill Or Next Information
0x7E	Variable Length	16/32 bits	0x7E	—

4.3.4.1 Flag Generator

The frame generator inserts the “Flag-Sequence” whenever an end of packet is encountered, the transmit FIFO is empty or an error has occurred, and no new “Start-Of-Packet” is detected.

4.3.4.2 FCS Insertion

The FCS value is calculated over the entire frame before byte-stuffing and scrambling. The CRC-CCITT is two bytes long, calculated by the polynomial $1 + X^5 + X^{12} + X^{16}$. The CRC-32 is four bytes long, calculated by the polynomial $1+ X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$. The FCS bytes are merged into the frame before the closing flag.

4.3.4.3 Byte Stuffing

For enabling transparency, two characters need to be escaped: the Flag Sequence and the Escape character. When an escape operation is performed on a character, it is exclusively ORed (XOR operation) with the value of 0x20 and an Escape character (0x7D) precedes it. This operation is performed only after the FCS calculation.

Table 4-6. Character Escape Map—Byte Stuffing

Sequence	Escaped
7E	7D–5E
7D	7D–5D
Abort	7D–7E

4.3.4.4 Scrambling

The Scrambler will optionally scramble the entire packet including the flags and FCS value using the polynomial $X^{43} + 1$. On reset, the Scrambler is set to all-1s. The default state is Scrambler Enabled.

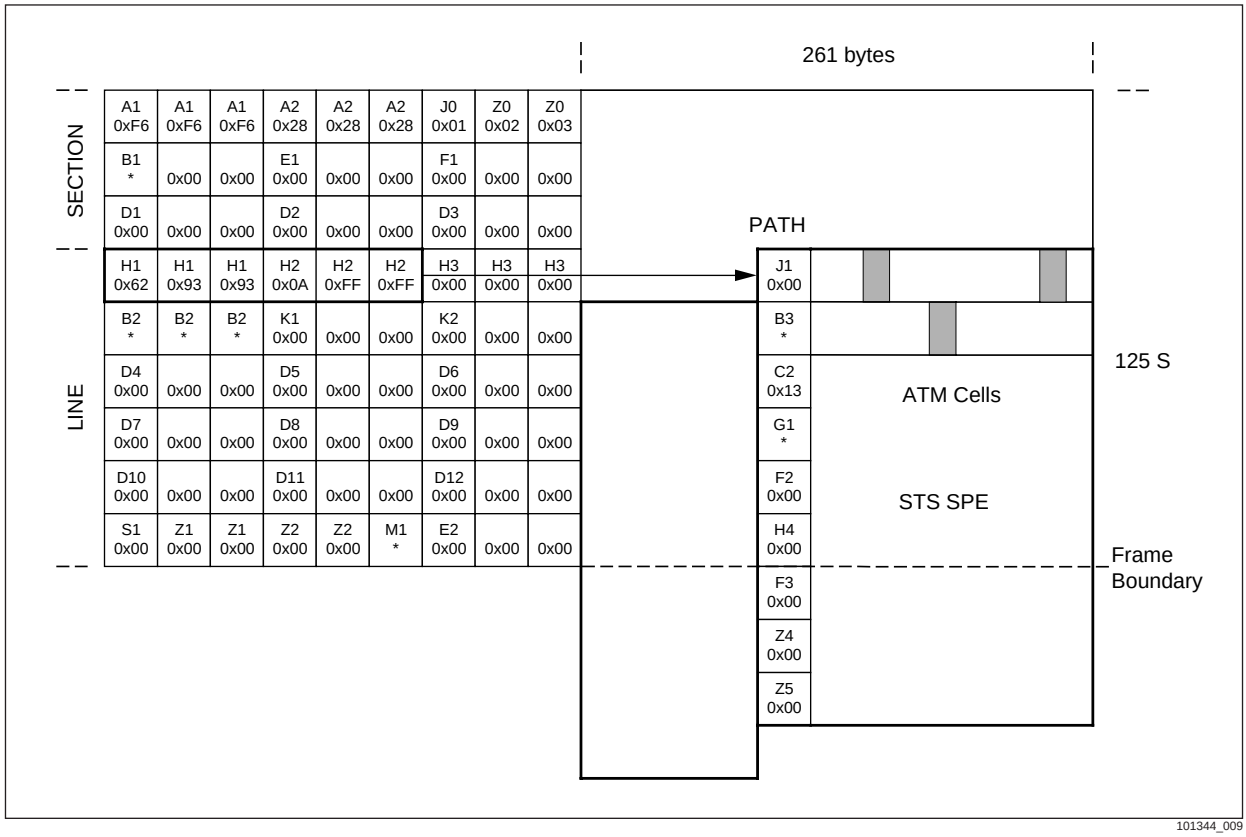
4.3.5 Tx Overhead Processor

The overhead processor calculates the necessary path, line, and section overhead bytes and inserts them, together with the ATM cells or packet data, into the STS-3c/STM-1 frame format. Frame scrambling is also performed in this processor.

4.3.5.1 Overhead Byte Default Values and STS-3c/STM-1 Frame Format

Figure 4-4 illustrates the STS-3c/STM-1 frame format and overhead byte default values.

Figure 4-4. STS-3c/STM-1 Frame Format and Overhead Byte Default Values



The SS bits within the H1 overhead bytes are undefined by the SONET Standard and are transmitted with a default value of 00. In SDH applications, these bits are set to the 10 value. Thus, in SDH mode the default value of the first H1 byte is 0x6A and the default value of the other two H1 overhead bytes is 0x9B. Overhead bytes marked with the value * are variables and are calculated according to the frame contents.

4.3.5.2 Path

STS SPE Pointer Generation

On the transmit path, the SPE pointers (H1, H2) are locked to the value of 0x20A, pointing to row 1, column 4, of the next frame. A normal New Data Flag (NDF) is associated with this constant value.

4.3.5.3 B3 Insertion

The Bit Interleaved Parity (BIP)-8 error code of the outgoing STS SPE before scrambling is calculated and inserted into the B3 overhead byte of the next frame. The first bit of B3 reflects the even parity over the first bit of every byte in the entire STS SPE. The B3 byte can be inserted inverted for diagnostic purposes.

4.3.5.4 Remote Defect Indication-Path (RDI-P) Generation

Enhanced RDI-P (ERDI-P) is supported on the transmit path (transmitted over bytes 1–3 of G1 overhead byte). Transmitting a single-bit RDI or totally disabling the transmission of RDI-P is optional. By default, RDI-P transmission is disabled. RDI-P is generated per Table 4-7.

Table 4-7. ERDI-P Defect Coding

G1 bits 1,2,3	Priority of ERDI-P codes (for SONET)	Trigger	
—	—	SONET	SDH
000	NA	No defects	No defects
010	3	PLM-P, LCD-P	LCD
110	2	UNEQ-P	UNEQ
001	4	No defects	No defects
101	1	AIS-P, LOP-P, LOS, LOF, AIS-L	AIS-P, LOP, LOS, LOF, AIS-L

ERDI-P is generated for at least 10 frames. It is deactivated by inserting the no-defect sequence into the G1 overhead byte for at least 10 frames. Generation of RDI-P defects can be controlled manually by the Tx-ERDIP register. In SONET mode, the value of G1 bits 1–3 are transmitted according to the Tx-ERDI-P register according to a trigger event with higher priority. In SDH mode, the register value is sent as is. When a defect occurs while another event is being transmitted, the first event transmission (using overhead byte G1) terminates first, and then the next defect transmission begins.

A single-bit RDI-P is generated (upon configuration) per Table 4-8.

Table 4-8. RDI-P Defect Coding

G1 bits 1,2,3	Interpretation	
—	SONET	SDH
000	No defects	No defects
100	AIS-P, LOP-P, LOS, LOF, AIS-L	AIS-P, LOP, UNEQ, LOS, LOF, AIS-L

4.3.5.5 Remote Error Indication-Path (REI-P) Insertion

Remote Error Indication on Path (REI-P) is transmitted by inserting the number of path BIP-8 errors detected over the last frame into bits 4–7 of the G1 overhead byte.

4.3.5.6 Tx-Path Trace Buffer (J1)

A 16-byte (SDH mode) or 64-byte (SONET mode) array is available for transmission through the path identifier byte (J1). Data to the array is written or read via the Tx Path Trace Address register and the Tx Path Trace Data register.

To load the array with the transmitted value, the user must first disable the J1 transmission logic by setting the appropriate bit in the Path Trace Address register to logic 0. While in that state, the default value is transmitted. The transmit J1 is loaded with new data by writing the 16 or 64 bytes that make up this array to the registers. The selection of which register array data will be written is done by the Tx Path Trace address. Once the transmission is disabled, and an address is loaded to the Tx Path Trace address, the R/W and Rx/Tx bits should be set to 0 (writing data to the transmit buffer). A 16-bit write should then be performed on the microprocessor bus to the address mapped to the Tx Trace array. After this writing cycle, the Tx Path Trace address is auto-incremented to point to the next 16 bits of the array. After 8 (SDH) writing cycles or 32 (SONET) writing cycles, the Enable/Disable bit should be set to 1. This allows transmission of the array data by the J1 overhead byte.

To summarize, the process of loading the array with values requires the following steps:

1. Disable the transmission.
2. Load the Path Trace address with the first address in the array.
3. Write a 16-bit word to the address of the Tx Path Trace array, after which the address register is auto-incremented.
4. Repeat Step 3 if required.
5. Enable the transmission.

4.3.5.7 STS Path Signal Label (C2)

The Path Signal label indicates the content being carried by the SPE to the network. A value of 0x13 indicates ATM transport. A value of 0xCF indicates non-scrambled POS/SDH data. A value of 0x16 indicates scrambled POS/SDH data. The default value is 0x13 (ATM Transport).

4.3.5.8 Path User Channel Byte (F2)

A default value (0x00) is used on the transmit path of the Path User Channel Overhead byte. Transmitting a non-default value by loading the transmitted value to the associated register is optional.

4.3.5.9 Path Growth Byte (F3)

A default value (0x00) is used on the transmit path of the Path Growth Overhead byte. Transmitting a non-default value by loading the transmitted value to the associated register is optional.

4.3.5.10 Path Growth Bytes (Z4–Z5)

A default value (0x00) is used on the transmit path of these overhead bytes. Transmitting a non-default value by loading the transmitted value to the associated register is optional.

4.3.5.11 Line *B2 Insertion*

The BIP-24 error code of the non-scrambled outgoing frame (excluding the section overhead bytes) is calculated and inserted into the B2 overhead byte of the next frame before scrambling. The first bit of the first B2 byte reflects the even parity over the first bit of every three bytes in the entire frame, and so on. The B2 bytes can be inserted inverted for diagnostic purposes.

4.3.5.12 Remote Defect Indication-Line (RDI-L) Generation

RDI-L is generated within 125 µs of LOS, LOF, or AIS-L defect detection on the incoming signal. The RDI-L is generated by inserting the pattern 110 in bits 0, 1, and 2 of the K2 overhead byte.

RDI-L is terminated within 125 µs of termination of the defect that caused it to be generated by inserting the pattern 000 in bits 0, 1, and 2 of the K2 overhead byte.

4.3.5.13 Remote Error Indication-Line (REI-L) Insertion

REI-L is transmitted by inserting the number of line BIP-24 errors detected over the last frame into the M1 transmitted overhead byte.

4.3.5.14 Line Data Communication Channel Insertion (D4–D12)

The nine Line DCC overhead bytes (D4–D12) are optionally transmitted serially through a dedicated port with a 648-kHz clock (which is partially active and produces a 576-kHz clock). The chip samples the data on the data pin on the rising edge of the serial clock. The data is transmitted as DCC overhead bytes of the next frame. Disabling this port is optional.

4.3.5.15 Synchronization Status (S1)

The S1 bytes carry the synchronization status of the SONET/SDH device. The target is to allow selecting of the best clock from the available sources. Only bits 4–7 of the BellCore standard are currently defined. Defining the value (other than the default (0x00)) is accomplished by loading that value to the associated register.

4.3.5.16 Order Wire Byte (E2)

The Order Wire byte was formerly used to facilitate a voice channel. A default value (0x00) is used on the transmit path of this overhead byte. Transmitting a non-default value by loading the transmitted value to the associated register is optional.

4.3.5.17 Section *B1 Insertion*

The BIP-8 error code of the outgoing scrambled frame is calculated and inserted into the B1 overhead byte of the next frame before scrambling. The first bit of B1 reflects the even parity over the first bit of every byte in the entire frame. The B1 byte may be optionally inserted inverted for diagnostic purposes.

4.3.5.18 Frame Scrambler

Scrambling is performed using a self-synchronous scrambler sequence length of 127. The generating polynomial for the scrambler is $1 + X^6 + X^7$**.** The scrambler is set to all-1s on the MSB of the third byte following the J0 byte.

The Framing bytes (A1, A2), the Section Trace byte (J0), and the Section Growth bytes (Z0) are not scrambled.

The Scrambler operation can be bypassed.

4.3.5.19 Section Data Communication Channel Extraction (D1–D3)

The three Section DCC overhead bytes (D1–D3) can optionally be transmitted serially through a dedicated port with a 216-kHz clock (partly active to produce a 192-kHz nominal clock). The chip samples the data on the data-pin on the rising edge of the serial clock. Data is transmitted as DCC overhead bytes of the next frame. Disabling this port is optional.

4.3.5.20 Section Trace/Growth (J0/Z0)

A default value is transmitted on this overhead byte (01, 02, 03). As an option, the value of J0 can be changed at the transmit path by loading any value to the associated register through the microprocessor port.

4.3.5.21 Order Wire Byte (E1)

A default value of (0x00) is used on the transmit path of this overhead byte. Transmitting a non-default value by loading the transmitted value to the associated register is optional.

4.3.5.22 Section User Channel (F1)

A default value (0x00) is used on the transmit path of this overhead byte. Transmitting a non-default value is optional, by loading the transmitted value to the associated register.

4.3.6 TX SONET/SDH Framer

The Framer inserts the Framing bytes (A1, A2) and the Section Trace and Growth bytes (J0, Z0) into the STS-3c/STM-1 frame.

4.3.7 Parallel to Serial

The parallel-to-serial block converts the outgoing 8-bit parallel data into serial data.

4.3.8 Performance Monitor

To provide management monitoring functions on the physical line, dedicated counters are provided for SONET/SDH cell and packet levels.

The SONET/SDH frame counter allows the user to read the number of frames that were received or transmitted since the last time this counter was read.

4.4 UTOPIA/POS Interface

The interface to the higher layer is a mixed-mode interface that simultaneously and independently serves four ports, allowing each port to function in a different mode. If the port is configured as an ATM port, the interface to the higher layer is a standard UTOPIA Level 2 interface. If the port is configured as a POS port, the interface is POS. The following sections describe these modes.

4.4.1 UTOPIA Level 2 Interface

The interface to the ATM layer is a standard UTOPIA Level 2 interface. Variable modes of operation are available for both single and multiport ATM Layer device connections.

Table 4-9. Recommended Mode of Operation Based on the Number of Ports Supported by the ATM Layer Device

No. of Ports Supported by the ATM Layer Device	1–4 Ports	5–31 Ports
Recommended Mode of Operation	Direct Status Indication One Rx/Tx CLAV	Multiplexed Status Polling One Rx/Tx CLAV

The UTOPIA Level 2 bus is a standard bus in which the PHY device functions as a slave. When one Rx FIFO is filled with a complete cell, the Cell Available (CLAV) indication is asserted by the FIFO. Depending on the mode of operation (Direct Status, Multiplexed Status, or One CLAV), the indication is driven out. As a result, the ATM Layer starts to read or write data to the port. For a detailed description of the UTOPIA Level 2 Interface, see the ATM Forum Standard (7/95).

4.4.1.1 Direct Status Indication

In this mode, each port has a dedicated pin for obtaining the fill status of its FIFO. Regardless of the address driven on the Rx/Tx address bus, the status of all Rx/Tx FIFOs is reported through corresponding pins. This mode of operation is recommended when using a single PHY device.

4.4.1.2 Multiplexed Status Polling

In this mode, each port has a dedicated pin for reporting FIFO status. This status is driven out even if the Rx/Tx address bus only one of the ports within the same PHY-IC. Thus, if one Rx port is selected by the RxADD bus, all four ports drive their Status CLAV pins. The same is true for the transmit port of the UTOPIA interface.

NOTE: In this mode of operation, all ports within the same PHY device must be mapped to addresses that have three identical MSBits. Practically, when performing selection in this mode, the two LSBits of the address bus are discarded. This mode is recommended when using multiple PHY devices functioning with the same ATM Layer device.

4.4.1.3 One Rx/Tx CLAV

In One Rx/Tx CLAV mode, all four ports within the same PHY device share the same pin for reporting their status. After selecting a specific port (by the Tx/Rx address bus), the associated port drives its FIFO status on the shared CLAV pin (Clav[0]). This mode of operation is suited for both single- and multi-PHY devices functioning with a single ATM Layer device.

4.4.2 POS-PHY: Normal Selection and Hot Selection Rx Modes of Operation

The receive path supports both Normal Selection and Hot Selection of the ports. In Normal Selection mode, the selection of a port is established by driving the port's address and setting the RxENB pin high for one cycle. Data is available on the data bus one clock cycle after the assertion of RxENB. This is similar to the timing of the UTOPIA Level 2 bus.

In Hot Selection mode, port selection is established by changing the address on the RxADR bus without toggling the RxENB pin. This provides better performance on the POS interface by saving an idle-cycle. System designers can determine the proper mode depending upon the system design.

NOTE: In Hot Selection mode, no polling is performed and the use of four Direct Status pins (DRPA [3:0]) is required. Also, for reliable operation of the system when reading data from one PHY-IC to another PHY-IC, it is highly recommended to use Normal Selection mode, using the idle cycle to avoid conflicts on the shared bus caused by different varying timing behavior of different ICs. In Normal Selection mode, several pins can be saved by using the polling mode, which allows status to be given through a shared pin (PRPA). An idle-cycle is required, however, when switching between different ports.

4.5 POS/SDH Interface

To support packet transfer over SONET/SDH, the CX29704 provides an extension to the UTOPIA Level 2 interface. This extension includes additional pins and dual modes of interfacing to a link layer. Both Selected Status and Polling Status modes are available for the link layer to obtain Tx/Rx FIFO status of the chip.

The Start Of Packet (SOP) and End Of Packet (EOP) signals are used to determine packet boundaries. The Rx/TxMOD pins determine the number of valid bits (8 or 16) in the last word of the packet being transferred. The Rx/TxERR pins are used in case any type of error occurs during the current transfer. Such an error may be of a parity or CRC type. If an error occurs in the transmit path, an Abort sequence is transmitted, followed by Flag Sequences until a new SOP is available. On the receive path, when any CRC, RUNT (less than one byte of an information packet), or Abort Sequence error is detected, the Rx ERR pin is asserted to flag the link layer to discard the current packet.

4.5.1 Transmit

The Direct Transmit Packet Available (DTPA)[3:0] provides per-port indication of the fill status of each corresponding FIFO. When working in single PTA pin mode, the Polled Transmit Packet Available (PTPA) and Selected Transmit Packet Available (STPA) pins give an indication of FIFO availability to the link layer. The PTPA polls the non-selected Tx-FIFO port. The STPA obtains the status of the currently selected Tx-FIFO port (FIFO to which the data is currently being sent).

NOTE: The PTPA pin is physically the same pin as the DTPA[0], which functions according to the POS interface configuration.

By programming the Tx FHL (FIFO High Limit) and Tx FLL (FIFO Low Limit), the user can designate the number of double (four-byte) words in the Tx FIFO on which the available Transmit Packet Available (TPA) indications are given. TPA indications (STPA, PTPA, DTPA) are determined by the selected mode of operation. When the number of (double) words in the Tx-FIFO is less than the Tx FLL, one of the TPA pins is asserted depending on the selected mode of operation. When the number of (double) words in the Tx FIFO is greater than the Tx FHL, one of the TPA pins is deasserted.

4.5.2 Receive

The Direct Receive Packet Available (DRPA)[3:0] provides per-port indication of the fill status of each corresponding Rx FIFO. The Received Polled Packet Available (PRPA) pin is used to poll the Rx port selected by the address-bus of the interface, and indicates that data is valid in the polled Rx FIFO. The Receive Signal Validity (RVAL) indicates the validity of the receive signal pins. For each Rx FIFO, low and high limit values are programmable.

For each Rx FIFO, a Rx FHL register allows the user to program the number of (double) words on which one of the RPA signals is asserted. The RPA signal asserted depends upon the selected mode of operation. When the number of (double) words in the Rx FIFO is greater than the value held in the Rx FIFO High Limit (FHL) (in (double) word granularity), one of the RPA pins is asserted depending on the selected mode of operation. An RPA pin is also asserted whenever there is at least one EOP in the Rx FIFO. It is deasserted when the number of (double) words is less than the value held by the Rx FLL register.

For proper operation of the FIFO, the definition of the FHL value must be greater than the FLL value. Although the values held in the FHL and FLL registers are in word boundaries, this does not limit the packet itself to word boundaries. It can also be in byte boundaries.

4.5.3 Signals/Pins

The POS/SDH interface includes the following pins:

- RxSOP/TxSOP—Rx/Tx Start of Packet indicates the first word of the a packet.
- RxEOP/TxEOP—Rx/Tx End of Packet indicates the last word of a packet.
- RxMOD/TxMOD—Rx/Tx Modulo indicates the length of the last data word in a packet (8/16 bits).
- RxERR/TxERR—Rx/Tx error indicates an error was detected during the transfer of the packet and the packet should be discarded due to abort sequence, FCS error, etc. (RERR/TERR is asserted only during the transfer of the last word of a packet).
- PTPA—Tx Packet Available indicates that a predefined minimum number of words (two bytes) is available in the polled Tx FIFO. Logic 1 indicates that the FIFO is not full. The number of words in the FIFO is less than the value held by the Tx FLL. Logic 0 indicates that the Tx FIFO is full or almost full (user programmable by the Tx FHL) and data may not be transmitted. The PTPA is driven by the chip when the address on the TADR bus matches the address of one of its ports. When using the PTPA pin (polling the FIFO's status through a single pin), the DTPA[0] pin is used. This means that the same physical pin is used for both DTPA[0] and PTPA functions, depending on the port configuration. The use of the PTPA pin (for multiplexed status polling) is not available in the Hot Selection mode of the interface.
- STPA—Tx Selected Packet Available. Logic 1 indicates that a minimum (predefined) number of words are available in the selected FIFO (FIFO to which data is currently being sent). This means that the number of words in the FIFO is less than the value held by the Tx FLL. Logic 0 indicates that the FIFO is full or almost full (user programmable by the Tx FHL).

- DTPA[3:0]—Direct Transmit Packet Available indicates the FIFO associated with each bit of this bus. Logic 1 indicates that the corresponding FIFO is not full (holds less than minimum predefined words held in the Tx FLL). The POS processor will not initiate transmission until the number of words in the FIFO reaches the predefined number (i.e., DTPA [x] equals zero). Logic 0 indicates that the FIFO is full or nearly full (determined by the value held in the Tx FHL register).
- PRPA—Received Polled Packet Available indicates that data is available in the polled Rx FIFO. Logic 1 indicates that the polled FIFO has at least one EOP or holds a predefined number of double words (held in the Rx FHL) to be read. Logic 0 indicates that the Rx FIFO holds less than the predefined number of words and no EOP is held. The PRPA is driven by the chip when the address on the RADR bus matches the address of one of its ports. When using the PRPA (polling the status of the four ports through a single pin), the DRPA[0] pin is used. This means that the PRPA and DRPA[0] are physically the same pin with functionality according to the programming of the POS interface port.
- RVAL—Receive Data Valid. Logic 1 indicates that receive signals are valid (RxDAT, RxSOP, RxEOP, RxMOD, RxPRTY, RxERR). RVAL is asserted when data transfer is initiated (conditional on DRPA also being asserted). RVAL changes to logic 0 on FIFO empty condition (no valid data in the FIFO) or on EOP Read condition from the FIFO. No data is read from the FIFO while RVAL is deasserted. RVAL is reasserted after the current FIFO is deselected. RVAL allows monitoring of the selected FIFO. Other FIFOs are polled by the DRPA bus.
- DRPA[3:0]—Direct Receive Packet Available indicates the FIFO status associated with each bit of this bus. Logic 1 indicates that the corresponding FIFO holds at least one EOP or a predefined number of words to be read. Logic 0 indicates that the FIFO holds no EOP and less than the predefined number of words.
- TxDAT/RxDAT[15:0]—Tx/Rx data bus. Valid only when TxENB/RxENB are asserted.
- TxADR/RxADR[4:0]—Tx/Rx address bus. Used to select which port data is being written or read and which port is being polled.
- TxPRTY/RxPRTY—Tx/Rx data bus parity information indicates that a parity error should be reported but that data transfer should not be interrupted.
- TxENB/RxENB—Enables the Write/Read transfer operation. In Normal Selection mode, while TxENB/RxENB are asserted, TxADR/RxADR are used to poll other FIFOs (using the PRPA and PTPA pins) while data is transferred from/to the selected port. In Hot Selection mode, when TxENB/RxENB are asserted, data is being transferred; however, polling is not available.
- TxClk/RxClk—UTOPIA/POS Tx/Rx clock, is used to write/read data to/from the FIFOs. These clocks should cycle at no higher than 50 MHz, but not less than the rate that would cause overflows in the FIFOs.

4.6 Microprocessor Interface

4.6.1 Interface Signals

A microprocessor port is provided for management and status purposes. This port allows the system to read or write to the different registers, and to obtain status information, i.e., an event causing an interrupt or a port error status. It is also used for programming the device mode of operation and to define the data to be transmitted (loading the registers with data of the overhead words, other than the default defined by the standards).

The CX29704 supports a general microprocessor (µP) interface.

The following signals are supported:

- 9-bit address bus
- 16-bit bidirectional data bus
- *CS (Chip Select)
- *DSTB (Output Enable)
- W/*R (Defines transaction direction)
- *READY (Synchronizes between processor and chip frequencies and indicates when valid data is present on the bus)
- *INTR (Signals the µP that an Interrupt event has occurred)

For details about wave forms and timing, see AC characteristics in Chapter 10.0.

4.6.2 Programming Model

The CX29704 registers are divided into two groups:

- 16-bit registers
- 32-bit registers

Accessing a 16-bit register is accomplished using a single µP access (read or write). Accessing a 32-bit register is accomplished using 2 µP accesses. The first access is addressed to the LSW (bits 15:0) of the register. The second access is addressed to the MSW (bits 31:16) of the registers. Accesses must be consecutive; otherwise, the value of the MSW is unknown. Registers that receive a reset value during read are reset when the LSW is read.

For details about register addresses, see Chapter 6.0.

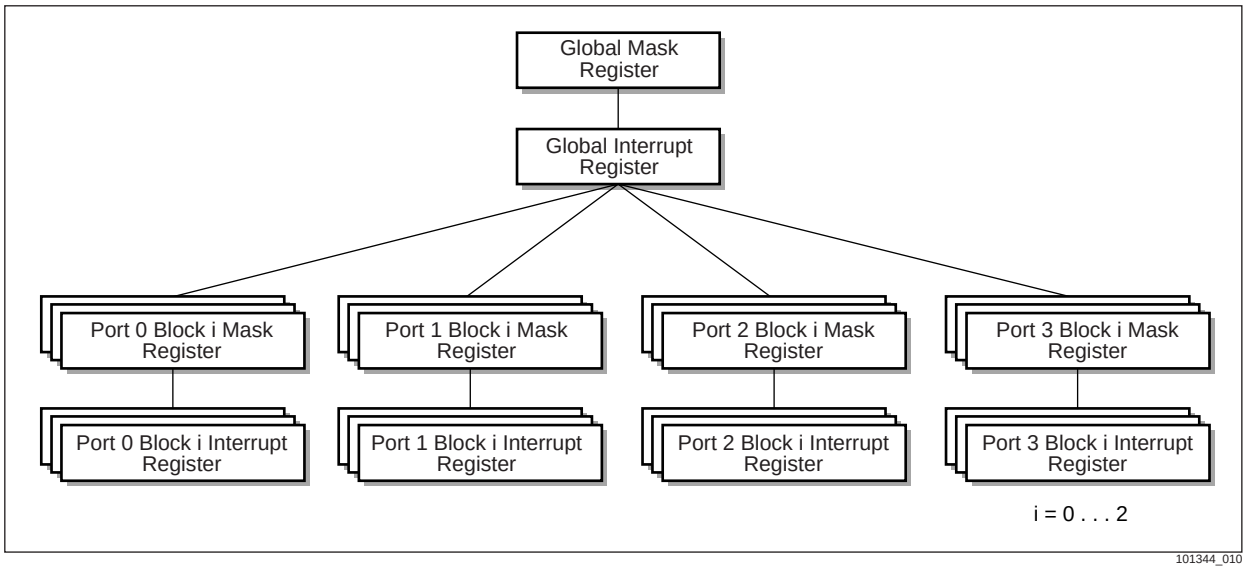
Unused bit values are read 0. For compatibility with future generations of the CX29704, these bits should be written as 0.

4.7 Interrupt Mechanism

The CX29704 supports interrupt generation upon the occurrence of various events. Every port can generate an interrupt according to its individual event. It is the user's responsibility to define the events that are the source of the interrupts. These events can be masked individually to disable interrupt generation. Interrupt registers continue to be updated by new events, even if the associated interrupt is disabled. Upon reading these registers, all bits are cleared. To reset pending interrupts by software, a dedicated bit is assigned in the Global Reset and Revision Number register (Table 6-2). For additional details about mask and status registers, please see the register descriptions in Chapter 6.0.

When unmasking interrupt events, the appropriate interrupt registers should be read to clear these registers and avoid interrupt generation based on older events. Upon receiving an interrupt, the Global Interrupt register should be read to determine the source block of the interrupt. On each port there are four interrupt source options: Framer Block, Overhead Byte Processor Block (A & B), and FIFO/UTOPIA Block. Based upon the source block indicated by the Global Interrupt register, the specific block features a register indicating which event caused the interrupt.

Figure 4-5. CX29704 Interrupt Mechanism Structure



Following is a list of events that generate interrupts:

- Framer Block
  - Change in LOS defect status
  - Change in SEF defect status
  - Change in LOF defect status
  - Rx Frame counter is half-full
  - Tx Frame counter is half-full

- Overhead Byte Processor Block
  - BIP8-S error was detected
  - Change in AIS-L defect status
  - Change in RDI-L defect status
  - BIP24-L error was detected
  - REI-L was detected
  - New value of K1, K2 overhead bytes was captured
  - APS state machine enters or exits the inconsistent state
  - New value of S1 overhead byte was captured
  - New value of C2 overhead byte was captured
  - New value of the Path Trace 64-byte (SONET) or 16-byte (SDH) identifier was captured
  - Change in LOP-P defect status
  - Change in AIS-P defect status
  - Change in ERDI-P bit values
  - BIP8-P error was detected
  - Change in REI-P defect status
  - Line BER (B2) exceeded threshold

- Cell/Packet Processor, FIFO and UTOPIA/POS Interface Blocks:
  - Change in OCD defect status
  - Change in LCD defect status
  - Correctable Bad Header (CBH) was detected
  - Uncorrectable Bad Header (UBH) was detected
  - Rx FIFO Overrun (RFO) was detected (in POS mode only)
  - Rx FIFO Underrun (RFU) was detected
  - Tx FIFO Overrun (TFO) was detected
  - Tx FIFO Underrun (TFU) was detected
  - Parity Error (PE) was detected
  - Start Of Cell Error (SOCE) was detected
  - Correctable bad header counter is half-full
  - Uncorrectable bad header counter is half-full
  - Bad FCS packet was detected
  - Abort sequence was transmitted
  - Abort sequence was received
  - Longer than maximum allowed packet was detected
  - Smaller than minimum allowed packet was detected
  - Rx cell/packet counter is half-full

NOTE: Tx Cell/Packet Counter Is Half-Full Interrupt and Performance Monitor registers are reset upon read.

4.8 Alarms Status Serial Interface (ASSI)

The ASSI provides important permanent status alarm signals for external use. It is most suitable for driving LEDs (with minimum external logic).

This interface consists of the following three pins:

1. ASCLK: interface clock
2. ASDO: drives the data serially
3. *ASSTB: data strobe

The information stream is constructed from the following status errors:

- LCD, LOP, AIS-P, AIS-L, LOF, TxC/P, RxC/P, LOS

Tx Cells/Packets (TxC/P) and Rx Cells/Packets (RxC/P) are status bits that indicate whether valid cells are being transmitted or received (excluding idle cells). This information is useful for obtaining permanent traffic indications. Each indication is driven for four clock cycles, one clock cycle for each port, starting from port 0. The *ASSTB marks the end of the information stream, which marks the LOS status of Port three.

The external application can be implemented by using shift registers and latches, or by using PLDs. A maximum application (accessing all signals) requires only four 8-bit shift registers and latches.

In general, the interface clock (ASCLK) shifts the serial data (ASDO) through the shift registers. The data strobe (*ASSTB) latches the data (to the appropriate location) using the latches whose inputs are connected in parallel to the shift registers' outputs.

For functional timing, see the Alarms Status Serial Interface Functional Timing in Chapter 8.0. For an application example, see Appendix C.

4.9 Diagnostics/Testing

The following section describes testing support, including:

- Loopback operations
- Error insertion
- Direct access to on-chip counters
- Disabling Scrambler/Descrambler
- Boundary Scan (JTAG) for PCB testing
- Full scan for chip production testing
- Block Bypass

4.9.1 Loopback Operation

The CX29704 provides the following three loopback modes of operation:

1. Line loopback—Exercises the block containing the clock and data recovery mechanism (see Figure 4-6)
2. SONET loopback—Exercises the block and the SONET/SDH logic core without the UTOPIA/POS interface (see Figure 4-7)
3. ATM loopback—Exercises the logic core of the CX29704 (see Figure 4-8)

Figure 4-6. Line Loopback

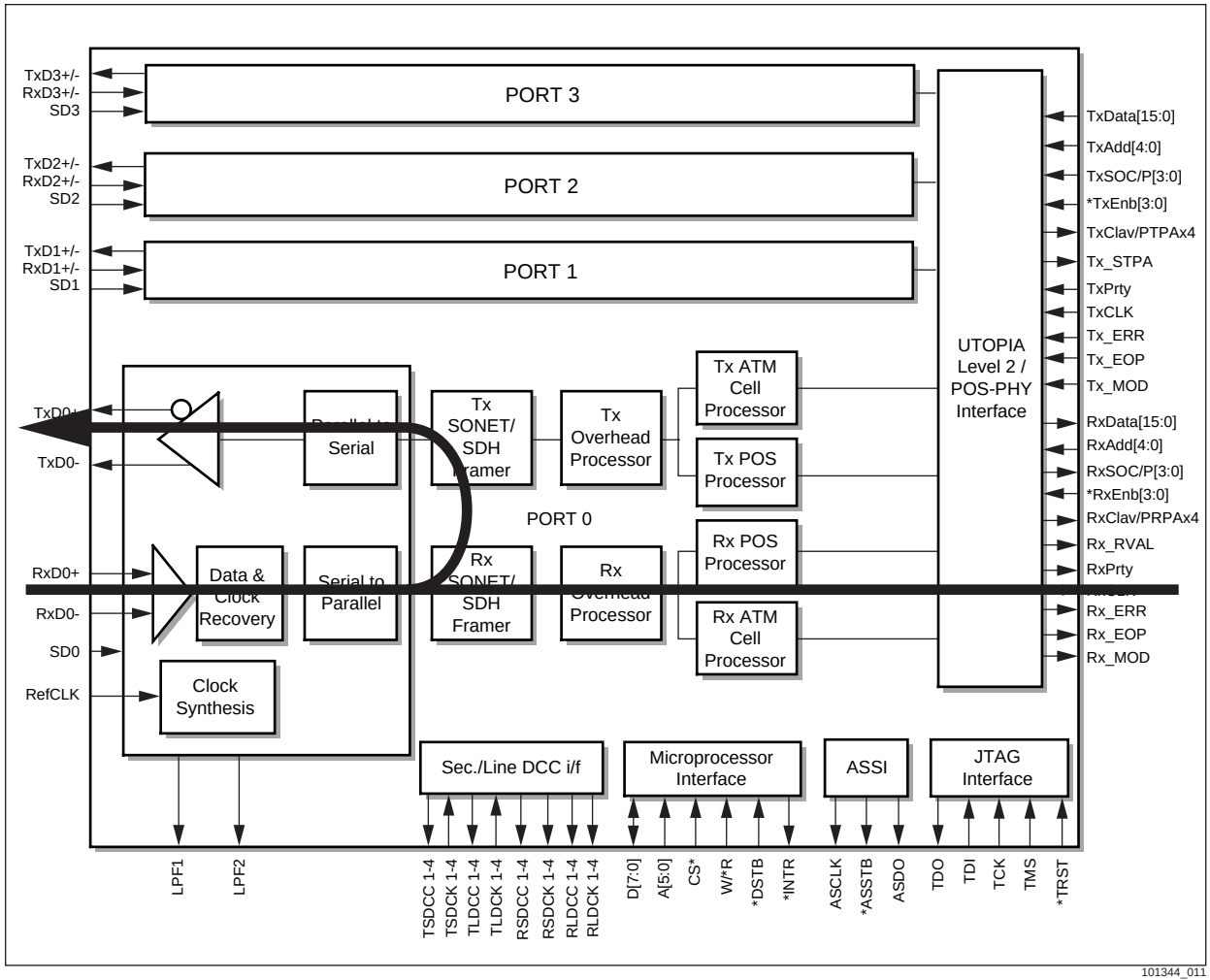


Figure 4-7. SONET Loopback

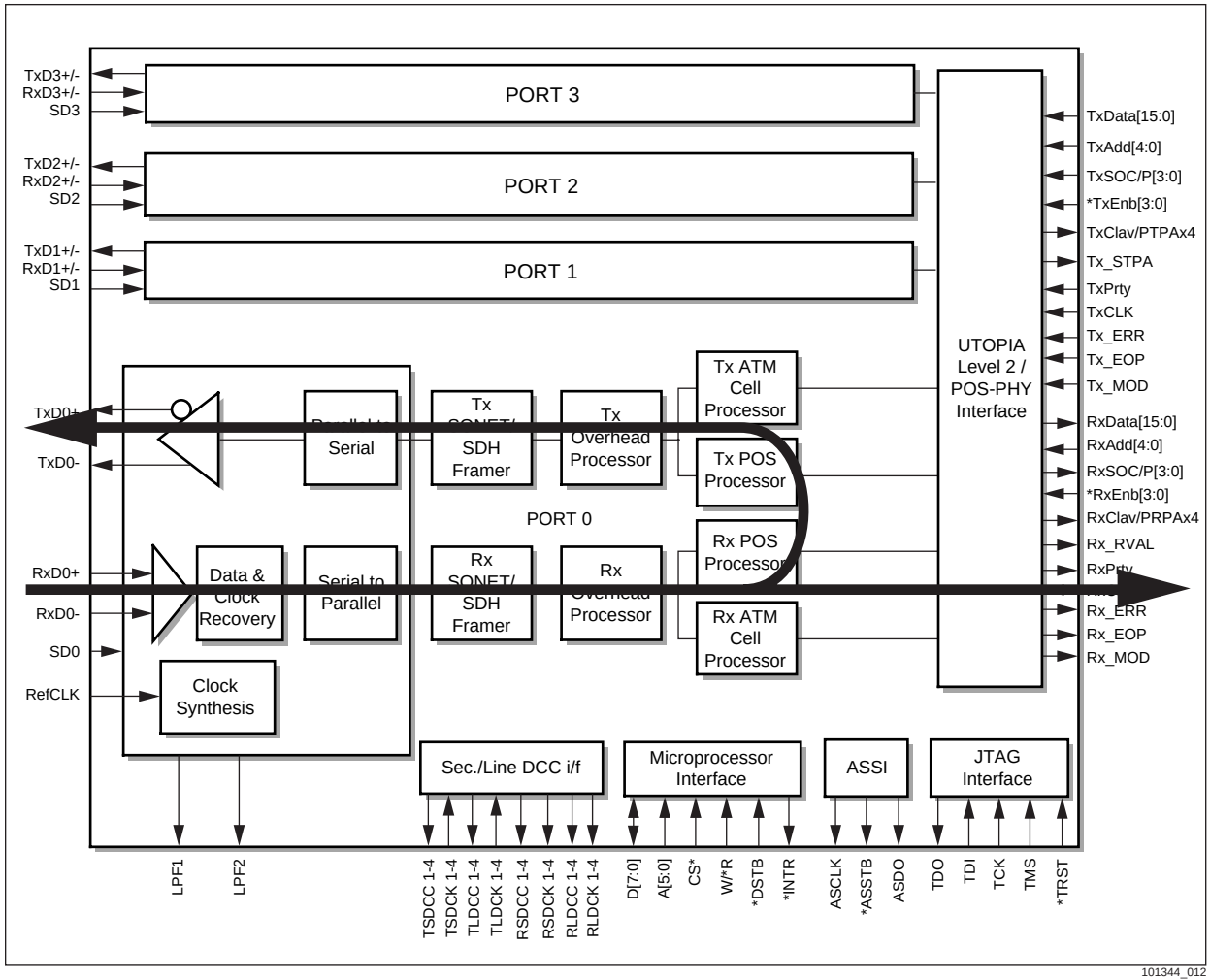
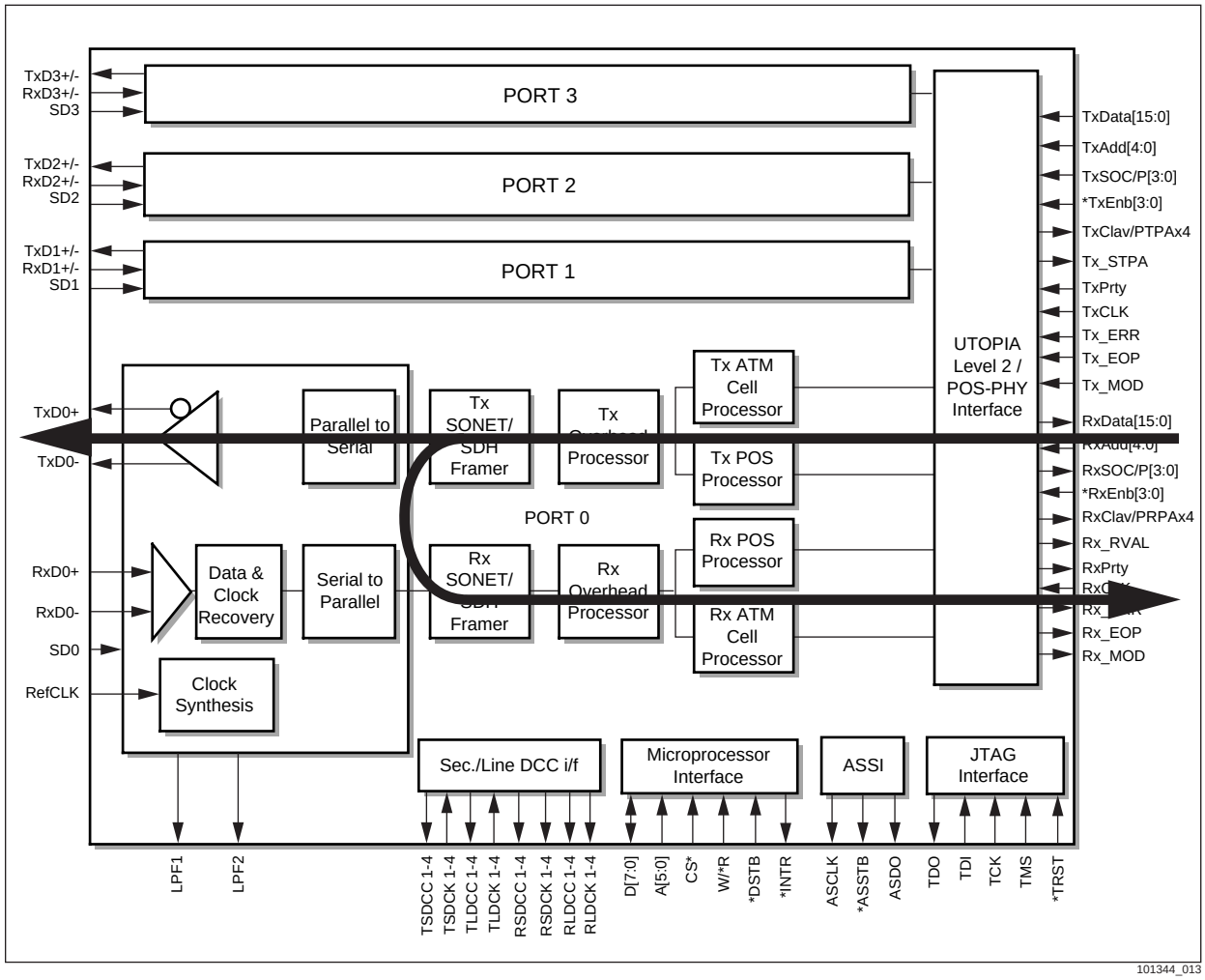


Figure 4-8. ATM Loopback



4.9.2 Error Insertion

4.9.2.1 Overhead Bytes

An error insertion mechanism is provided for diagnostic purposes. Errors can be inserted for the following events:

- Incorrect header on transmitted cells. This mode enables one-bit header error insertion by inverting the LSBit of header byte number one, and multi-bit header error insertion by inverting the two LSBits of header byte number one.
- Incorrect FCS on transmitted packet. This mode allows the transmission of inverted FCS code of the packet (bit-wise).
- Incorrect B3 byte (path BIP-8 overhead byte) on transmitted frame. The B3 byte is transmitted inverted.
- Incorrect B2 bytes (line BIP-24 overhead byte) on transmitted frame. B2 bytes are transmitted inverted.
- Incorrect B1 byte (section BIP-8 overhead byte) on transmitted frame. The B1 is transmitted inverted.
- Incorrect A1, A2 on transmitted frame for emulating an LOF condition. The third A1 byte and the first A2 byte are transmitted inverted.

4.9.2.2 Loss Of Signal (LOS) Condition

For emulating an LOS condition, the transmitter can be forced to transmit an all-0s pattern.

4.9.2.3 Disabling Scramblers/ Descramblers

Frame/Cell/Payload Scramblers (on the transmit path) and Frame/Cell/Payload Descramblers (on the receive path) can be disabled for diagnostic purposes.

4.10 JTAG

The CX29704 supports boundary scan according to IEEE Standard 1149.1. Support includes the following five pins:

1. TDO
2. TDI
3. TCK (Up to 5 MHz)
4. TMs
5. *TRST

Mandatory function support includes the following:

- Extent
- Bypass
- Sample
- JTAG ID number

The JTAG chain connects all except the following pins: RxD[0,1,2,3]+, RxD[0,1,2,3]–, TxD[0,1,2,3]+, TxD[0,1,2,3], SD[0,1,2,3], PCAP[0,1,2,3], NCAP[0,1,2,3], REXT[0,1], TMS, TCK, TDI, TDO, TRTS, RefCLK

4.11 Full Scan

The CX29704 supports full scan. Logic is connected in 50 scan chains.

4.12 Block Bypass

This mode enables bypass of the block by connecting the line interface pins directly to the Serial-to-Parallel/Parallel-to-Serial blocks.

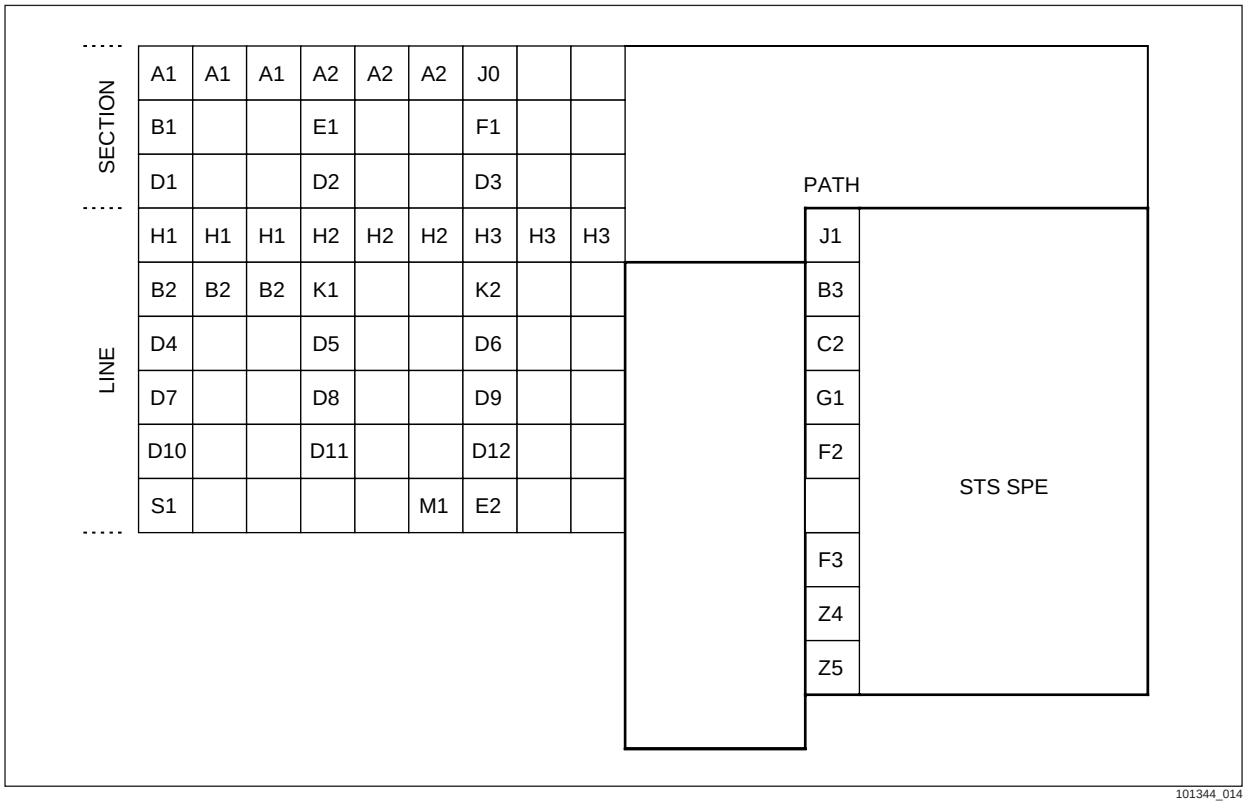
This mode is for manufacturing testing only.

5.0 Overhead Byte Support

5.1 Overhead Byte Support

Figure 5-1 illustrates the SONET/SDH overhead bytes that are being processed by the CX29704 or are available for receive and transmit through the microprocessor interface.

Figure 5-1. STS-3c/STM-1 Overhead Byte Support



Following is a description of the overhead bytes being processed by the CX29704.

Section Overhead

- A1, A2: Framing—Used to identify the SONET/SDH frame boundaries within the serial stream.
- B1: Section BIP-8—BIP-8 is used for section error monitoring. The Section BIP-8 error code is calculated over the entire frame. A 16-bit saturating counter is provided for accumulation of these errors and an interrupt is generated whenever an error is captured.
- D1–D3: Data Communication Channel—The three-section Data Communication Channel overhead bytes are captured and serially transmitted out using a serial clock. On the transmit path, the D1–D3 bytes are inserted using a serial input port and transmitted on the line.
- Section Trace/Growth (J0/Z0)—As a default, the Section Trace/Growth overhead bytes are ignored on the receive path and a default value is transmitted (01, 02, 03). These bytes can be optionally captured into a register on the receive path and read for transmit from a register on the transmit path.
- Order Wire Byte (E1)—The Order Wire byte formerly used to facilitate a voice channel is ignored on the receive path and a default value is used on the transmit path. It can be optionally captured and read via the microprocessor port on the receive path and transmitted with a register value, preloaded via the microprocessor port.
- Section User Channel (F1)—The Section User Channel byte is ignored on the receive path and a default value is used on the transmit path. It can be optionally captured and read via the microprocessor port on the receive path, and transmitted with a register value, preloaded via the microprocessor port.

Line Overhead

- H1, H2: STS Payload Pointer—These bytes contain the pointer that indicates the offset in bytes between the last H2 byte and the first byte of the STS SPE.
- H3: Pointer Action Byte—The Pointer Action Byte contains the SPE extra byte in the event of negative pointer adjustment.
- B2: Line BIP-24—BIP-24 is used for line error monitoring. The Line BIP-24 error code is calculated over the entire frame excluding the section overhead bytes. A 32-bit saturating counter is provided for accumulation of these errors and an interrupt is generated whenever an error is captured.
- K1, K2: Automatic Protection Switching Channel—Used when Automatic Protection Switching is supported. The K2 overhead byte is also used to detect Alarm Indication Signal-Line (AIS-L) and Remote Defect Indication-Line (RDI-L). These bytes are available both for transmit and receive through the microprocessor interface. On receive, these bytes are captured only when, in three consecutive frames, the same new value is received. Interrupt is generated upon capture.
- S1: Synchronization Status—Bits 4–7 (of the BellCore standard) are used for Synchronization Status messages. Bits 0–3 are currently undefined. These bits are available both for transmit and receive through the microprocessor interface.
- M1: Remote Error Indication-Line (REI-L)—A 32-bit saturating counter is provided for accumulation of these indications and an interrupt is generated whenever an indication is captured.

- Line Data Communication Channel Extraction (D4–D12)—The 9 Line DCC overhead bytes (D4–D12) are captured and optionally serially transmitted out of the chip using a 648 kHz clock with 50% duty cycle (which is active part of the time to produce a 576 kHz nominal clock rate). This 576 kHz clock is derived from the recovered clock. On the transmit path, these 9 bytes are inserted from a serial port using a 576 kHz clock and transmitted to the line as part of the SONET/SDH overhead bytes.
- Order Wire Byte (E2)—The Order Wire byte, formerly used to facilitate a voice channel, is ignored on the receive path and a default value is used on the transmit path. It can be optionally captured and read via the microprocessor port on the receive path and transmitted with a register value, preloaded via the microprocessor port.

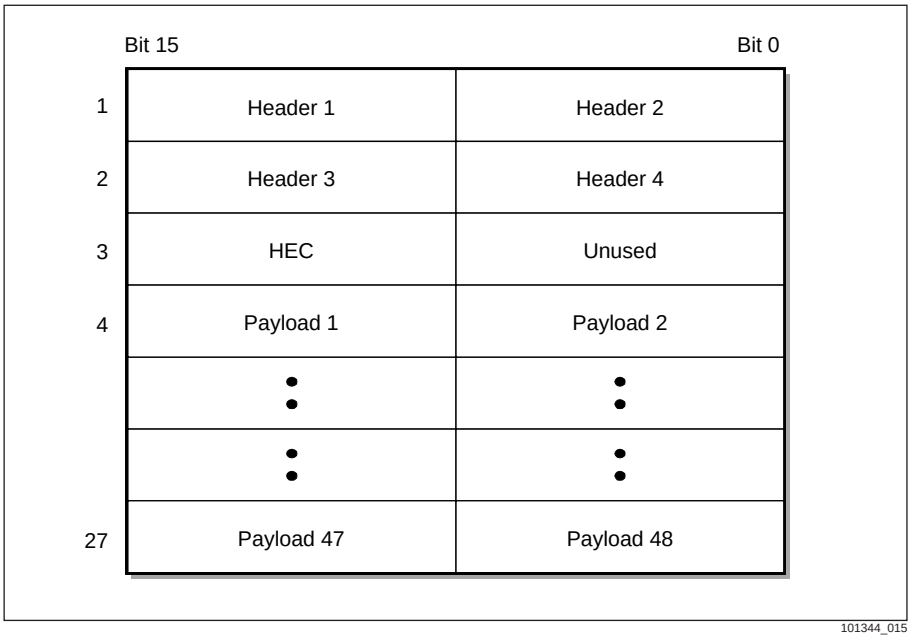
Path Overhead

- J1: Path Trace—Transmits an identifier to the path termination equipment so that the path layer receiving the frame can verify its connection. In SONET, it is used as a 64-byte string and, in SDH, it is used as a 16-byte identifier according to the *E.164* format. A 64-byte (for SONET) or a 16-byte (for SDH) Path Trace buffer is provided for both the receive stream and the transmit stream. On the transmit stream, there is a possibility to transmit a desired identifier. On the receive stream, an Interrupt is generated when two consecutive, identical, new identifiers are received. The identifier is then available through the receive buffer. When not used, J1 should contain the value 0x0.
- B3: Path BIP-8—BIP-8 is used for path error monitoring. The Path BIP-8 error code is calculated over the entire STS SPE. A 16-bit saturating counter is provided for accumulation of these errors and an interrupt is generated whenever an error is captured.
- C2: Path Signal Label—Used for indicating the content of the SPE. The 0x13 value is transmitted as the default, this value indicates mapping for ATM. This byte is available both for transmit and receive through the microprocessor interface. On receive, this byte is captured only when the same new value is received in five consecutive frames. Interrupt is generated upon capture.
- G1: Path Status—Bits 4–7 are used for Remote Error Indication-Path (REI-P) and bits 1–3 are used for Remote Defect Indication-Path (RDI-P). A 16-bit saturating counter is provided for accumulation of REI-P and an interrupt is generated whenever an indication is captured. An RDI-P status bit is provided and an Interrupt upon generation and termination. Enhanced RDI is supported. Bits 1-3 are available for transmit and receive.
- F2, F3: Path User Channel—These bytes are allocated for user communication purposes between path terminating network equipment and are available for both transmit and receive through the microprocessor interface.
- Path Growth Bytes (Z4–Z5)—The Path Growth Bytes are ignored on the receive path and a default value is used on the transmit path. The Path Growth bytes can be optionally captured and read via the microprocessor port on the receive path and transmitted with a register value, preloaded via the microprocessor port.

5.2 16-Bit Cell Format

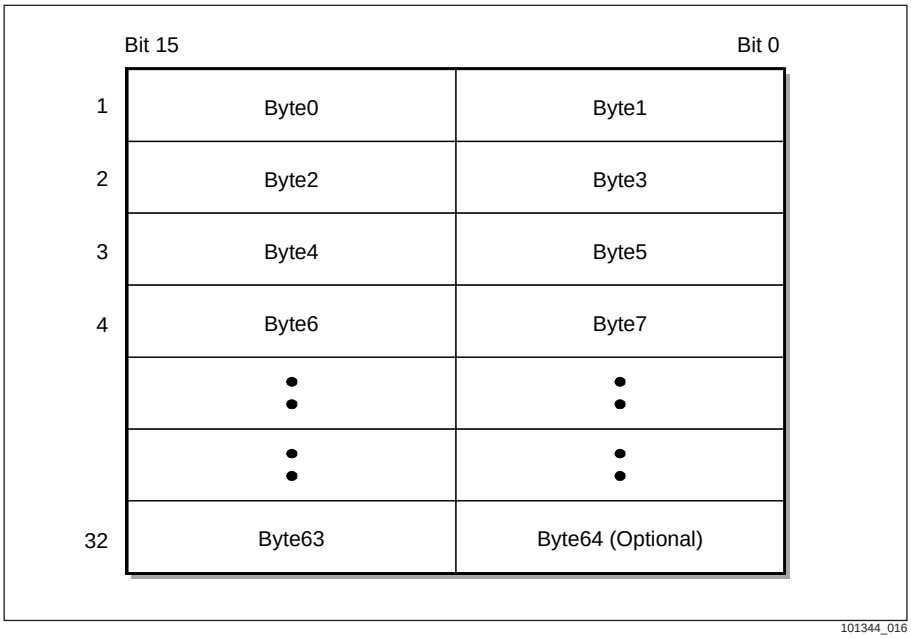
The UTOPIA Level 2 Interface supports a 16-bit cell format mode of operation. Figure 5-2 illustrates the 16-bit cell format.

Figure 5-2. 16-Bit Cell Format



In the 16-bit mode of operation, the cell is constructed from 54 bytes—five header bytes, one unused byte, and 48 payload bytes. The HEC byte is considered to be the fifth byte of the header. The cell bytes are transferred or taken from the ATM layer as words. Each word contains two bytes. The unused byte is transmitted with a value of 0x0 and is ignored in the receive stream.

Figure 5-3. Packet Over SONET/SDH—Data Arrangement (64-byte packet)



In this mode of operation, POS data is transmitted/received on a 16-bit basis. The MSB of the data bus are the bits to be transmitted first. They are also the bits that are received first.

6.0 Register Descriptions

NOTE: The convention used in this section is that bit 0 represents the least significant bit while bit 7 represents the most significant bit. This convention may contradict the order used in the SONET/SDH standards, therefore special attention should be paid.

Table 6-1. Register Address Mapping (1 of 3)

Address				Register
Port 0	**Port 1**	**Port 2**	**Port 3**	
0x000				Global Reset and Revision Number
0x001				Global Configuration
0x002	0x042	0x082	0x0C2	Port Configuration A
0x003	0x043	0x083	0x0C3	Port Configuration B
0x004	0x044	0x084	0x0C4	Port Diagnostic Port FIFOs Control/Status
0x005	0x045	0x085	0x0C5	Port Status
0x006	0x046	0x086	0x0C6	Port Rx—FIFO Control/Status (ATM mode)
0x007	0x047	0x087	0x0C7	Port Tx—FIFOs Control/Status (ATM mode)
0x008	0x048	0x088	0x0C8	Rx Port FIFO Status (POS mode)
0x009	0x049	0x089	0x0C9	Tx Port FIFO Status (POS mode)
0x00A	0x04A	0x08A	0x0CA	Tx FIFO threshold; Tx IFF
0x010	—			Global Interrupt
0x011	—			Global Mask
0x012	0x052	0x092	0x0D2	Framer Interrupt
0x013	0x053	0x093	0x0D3	Framer Mask
0x014	0x054	0x094	0x0D4	Overhead Bytes Processor Interrupt A
0x015	0x055	0x095	0x0D5	Overhead Bytes Processor Mask A
0x016	0x056	0x096	0x0D6	Overhead Bytes Processor Interrupt B
0X017	0x057	0x097	0x0D7	Overhead Bytes Processor Mask B
0x018	0x058	0x098	0x0D8	Cell, FIFO and UTOPIA Interrupt
0x019	0x059	0x099	0x0D9	Cell, FIFO and UTOPIA Mask

Table 6-1. Register Address Mapping (2 of 3)

Address				Register
Port 0	**Port 1**	**Port 2**	**Port 3**	
0x01A	0x05A	0x09A	0X0DA	Minimum Packet Length (Min_Pack_length)
0x01B	0x05B	0x09B	0x0DB	Maximum Packet Length (Max_Pack_Length)
0x01C	0x05C	0x09C	0x0DC	Rx FIFO High Limit (Rx_FHL)
0x01D	0x05D	0x09D	0x0DD	Rx FIFO Low Limit (Rx_FLL)
0x01E	0x05E	0x09E	0x0DE	Tx FIFO High Limit (Tx_FHL)
0x01F	0X05F	0x09F	0x0DF	Tx FIFO Low Limit (Tx_FLL)
0x020	0x060	0x0A0	0x0E0	Section Error Monitor
0x021	0x061	0x0A1	0x0E1	Line Error Monitor (Lower Word)
0x022	0x062	0x0A2	0x0E2	Line Error Monitor (Upper Word)
0x023	0x063	0x0A3	0x0E3	Line Remote Error Indication (Lower Word)
0x024	0x064	0x0A4	0x0E4	Line Remote Error Indication (Upper Word)
0x025	0x065	0x0A5	0x0E5	Path Error Monitor
0x026	0x066	0x0A6	0x0E6	Path Remote Error Indication
0x027	0x067	0x0A7	0x0E7	Uncorrectable Bad Header Counter
0x028	0x068	0x0A8	0x0E8	Correctable Bad Header Counter
0x029	0x069	0x0A9	0x0E9	Rx Cell Counter (Lower Word)
0x02A	0x06A	0x0AA	0x0EA	Rx Cell Counter (Upper Word)
0x02B	0x06B	0x0AB	0x0EB	Tx Cell Counter (Lower Word)
0x02C	0x06C	0x0AC	0x0EC	Tx Cell Counter (Upper Word)
0x02D	0x06D	0x0AD	0x0ED	Rx Frame Counter
0x02E	0x06E	0x0AE	0x0EE	Tx Frame Counter
0x030	0x070	0x0B0	0x0F0	Rx APS Channel (K1, K2)
0x031	0x071	0x0B1	0x0F1	Tx APS Channel (K1, K2)
0x032	0x072	0x0B2	0x0F2	Rx Synchronization Status Message (S1)
0x033	0x073	0x0B3	0x0F3	Tx Synchronization Status Message (S1)
0x034	0x074	0x0B4	0x0F4	Rx Path Signal Label (C2)
0x035	0x075	0x0B5	0x0F5	Tx Path Signal Label (C2)
0x036	0x076	0x0B6	0x0F6	Rx Path User Channel (F2, F3)
0x037	0x077	0x0B7	0x0F7	Tx Path User Channel (F2, F3)
0x038	0x078	0x0B8	0x0F8	Path Trace Address
0x039	0x079	0x0B9	0x0F9	Path Trace Data
0x03A	0x07A	0x0BA	0x0FA	Rx RDI-P Register
0x03B	0x07B	0x0BB	0x0FB	Tx RDI-P Register

Table 6-1. Register Address Mapping (3 of 3)

Address				Register
Port 0	**Port 1**	**Port 2**	**Port 3**	
0x101	0x141	0x181	0x1C1	Rx Order Wire Byte (E1, E2)
0x102	0x142	0x182	0x1C2	Tx Order Wire Byte (E1, E2)
0x103	0x143	0x183	0x1C3	Rx Section User Channel (F1)
0x104	0x144	0x184	0x1C4	Tx Section User Channel (F1)
0x105	0x145	0x185	0x1C5	Rx Growth Bytes (Z4, Z5)
0x106	0x146	0x186	0x1C6	Tx Growth Bytes (Z4, Z5)
0x107	0x147	0x187	0x1C7	FCS Error Found (POS Mode)
0x108	0x148	0x188	0x1C8	Maximum Length Violating Packets Found (POS)
0x109	0x149	0x189	0x1C9	Minimum Length Violating Packets Found (POS)
0x10A	0x14A	0x18A	0x1CA	Error Free Packet Received (POS) (Lower Word)
0x10B	0x14B	0x18B	0x1CA	Error Free Packet Received (POS) (Higher Word)
0x10C	0x14C	0x18C	0x1CB	Received Aborted packets
0x10D	0x14D	0x18D	0x1CD	Transmitted Aborted packets
0x10E	0x14E	0x18E	0x1CE	Number of Transmitted Packets (POS) (Lower Word)
0x10F	0x14F	0x18F	0x1CF	Number of Transmitted Packets (POS) (Higher Word)
0x110	0x150	0x190	0x1D0	B2 BER Error Counter
0x111	0x151	0x191	0x1D1	B2 BER Threshold
0x112	0x152	0x192	0x1D2	B2 BER Period (Lower Word)
0x113	0x153	0x193	0x1D3	B2 BER Period (Upper Word)

Table 6-2. Global Reset and Revision Number Register (add:0x00)

Bit	Type	Name	Default	Description
0	R	Rev0	1	This three-bit value represents the CX29704 revision number.
1	R	Rev1	0	—
2	R	Rev2	0	—
3	W	Soft Reset	0	Soft reset is performed when writing 1 to this bit. The reset state is entered on the positive edge of the data-strobe pin (of the access writing the 1 into this bit). This reset state ends after 20 clock cycles.
4	W	Intr Reset	0	Interrupt registers are cleared when writing 1 to this bit.
15:5	R	Unused	0	Reserved for future functionality.

Table 6-3. Global Configuration Register (Add: 0x01)

Bit	Type	Name	Default	Description
1:0	R/W	UTOPIA mode	00	00 = One Rx/Tx CLAV (ATM mode), Single TPA/RPA (POS mode) 01 = Direct Status Indication (4 CLAV (ATM mode), 4 TPA/RPA (POS mode) 10 = Multiplexed Status Indication (refers to ATM ports only)
2	R/W	POS interface mode	0	(POS mode only) 0 = Normal selection 1 = Hot selection (in Hot Selection mode, the ENB pin cannot be deasserted while changing the address value)
3	R/W	Port 0 Power-down	0	0 = Port 0 is enabled 1 = Port 0 is in Power-down mode (disabled) ***NOTE:*** The Power-down mode can only be entered after the FIFO port is disabled (in the FIFO Status and Control register)
4	R/W	Port 1 Power-down	0	0 = Port 1 is enabled 1 = Port 1 is in Power-down mode (disabled) ***NOTE:*** The Power-down mode can only be entered after the FIFO port is disabled (in the FIFO Status and Control register)
5	R/W	Port 2 Power-down	0	0 = Port 2 is enabled 1 = Port 2 is in power-down mode (disabled) ***NOTE:*** The Power-down mode can only be entered after the FIFO port is disabled (in the FIFO status and control register)
6	R/W	Port 3 Power-down	0	0 = Port 3 is enabled 1 = Port 3 is in Power-down mode (disabled)
15:7	R	Reserved	0	Reserved for future functionality

Table 6-4. Port Configuration Register A, Ports 0–3 (Add: 0x02, 0x42, 0x82, 0xC2)

Bit	Type	Name	Default	Description
0	R/W	SDH/SONET	0	0 = SDH mode 1 = SONET mode
1	R/W	Tx Timing	0	0 = The reference clock is the timing source of the transmit path 1 = The recovered clock (divided by 8) is the timing source of the transmit path
2	R/W	SBIP Individual /Frame	0	0 = Each Section BIP-8 error is accumulated in the SBIP register 1 = One or more Section BIP-8 errors are detected in a frame and result in an accumulated error in the SBIP register
3	R/W	LBIP Individual /Frame	0	0 = Each Line BIP-24 error is accumulated in the LBIP register 1 = One or more Line BIP-24 errors are detected in a frame and result in an accumulated error in the LBIP register
4	R/W	REI-L Individual /Frame	0	0 = Each Line REI is accumulated in the REI-L register 1 = One or more Line REIs were received in the same frame and result in an accumulated error in the REI-L register
5	R/W	PBIP Individual /Frame	0	0 = Each Path BIP-8 error is accumulated in the PBIP register 1 = One or more Path BIP-8 errors are detected in a frame and result in an accumulated error in the PBIP register
6	R/W	REI-P Individual /Frame	0	0 = Each Path REI is accumulated in the REI-P register 1 = One or more Path REIs are received in the same frame and result in an accumulated error in the REI-P register
7	R/W	CHEDC	0	Cell Header Error Detection or Correction mode of operation 0 = Header error detection mode of operation 1 = Header error correction mode of operation
12:8	R/W	Port Add [4:0]	0 = Port 0 1 = Port 1 2 = Port 2 3 = Port 3	The address assigned to a port to read, write, or poll the FIFO by the higher link layer through the UTOPIA/POS interface port
13	R/W	ATM/POS	0	Selects the mode of operation of the port 0 = ATM 1 = POS
14	R/W	19M/8K	1	0 = The RCLK pin toggles with the 19.44 MHz recovered clock (divided by 8) 1 = The RCLK pin toggles with the 8 kHz frame sync
15	R	Tx Clock Switch	0	Selects Tx clock switch in case of LOS or SD pin is low 0 = No auto-switch to synthesized clock 1 = Auto-switch to synthesized clock

Table 6-5. Port Configuration Register B, Ports 0–3 (Add: 0x03, 0x43, 0x83, 0xC3)

Bit	Type	Name	Default	Description
0	R/W	Rx SDCC	0	Controlling the Receive Section DCC port 0 = The port is disabled and no clock or data pins are active 1 = The port and the 192 kHz clock are enabled; Received Section DCC bytes are serially available on the pin
1	R/W	Tx SDCC	0	Controlling the Transmit Section DCC port 0 = The port is disabled and no clock or data pins are active 1 = The port is enabled; data on the TSDCD pin is sampled using the 192 kHz clock pin (RSDCC) and transmitted as part of the SONET/SDH section overhead bytes
2	R/W	Rx LDCC	0	Controlling the Receive Line DCC port 0 = Port is disabled, no clock or data pins are active 1 = Port is enabled; the 576 kHz clock is enabled, and received line DCC bytes are serially available on the RLDCD pin
3	R/W	Tx LDCC	0	Controlling the Transmit Line DCC port 0 = The port is disabled and no clock or data pins are active. 1 = The port is enabled; data on the TLDCD pin is sampled using the 576 kHz clock pin (TLDCC) and transmitted as part of the SONET/SDH line overhead bytes
5:4	R/W	Tx FCS mode	01	Controlling the FCS Transmit mode while in POS mode (FCS is calculated before scrambling and byte stuffing) 00 = CRC-CCITT (16-bit) is calculated 01 = CRC-32 (32-bit) is calculated 10 = Reserved for future functionality 11 = Reserved for future functionality
7:6	R/W	Rx FCS mode	01	Controlling the FCS Receive mode while in POS mode (FCS is calculated after descrambling and byte destuffing) 00 = CRC-CCITT (16-bit) is calculated 01 = CRC-32 (32-bit) is calculated 10 = FCS detection is disabled (16 bits are stripped from Information) 11 = FCS detection is disabled (32 bits are stripped from Information)
8	R/W	Line BER enable	0	0 = The section BER mechanism is disabled 1 = The Line (B2) BER mechanism is enabled; this bit can only be set to 1 after the Threshold and Period are loaded with the appropriate values
9	R/W	RDI enable	0	0 = RDI-P is disabled on the transmit side 1 = RDI-P is enabled
10	R/W	Enhanced RDI	0	0 = Enhanced RDI is disabled on the transmit side 1 = Enhanced RDI-P is enabled on the transmit side ***NOTE:*** Both bits (9,10) of this register should be set to logic 1 to enable ERDI-P
15:11	R	Reserved	0	Reserved for future functionality

Table 6-6. Port Diagnostic Register, Ports 0–3 (Add: 0x04, 0x44, 0x84, 0xC4)

Bit	Type	Name	Default	Description
2:0	R/W	Loopback Control [2:0]	0	000 = Loopbacks are disabled 001 = Line Loopback is enabled 010 = SONET Loopback is enabled 011 = ATM/POS Loopback is enabled 101 = Digital Clock Halt—In this mode, all digital clocks will be disabled (global clock from PLL and RxClk/TxClk of each port). This mode can only be changed by hardware reset. Disabling the clock of Port 3 also disables the global clock (global PLL clock divided by 8). 100 = Jitter test mode (Engineering only)
3	R/W	LOS insertion	0	1 = Insertion of all-0s pattern in the transmit stream to simulate LOS defect for diagnostic purposes
4	R/W	LOF insertion	0	1 = Inversion of the third A1 and the first A2 framing bytes to simulate LOF defect for diagnostic purposes
5	R/W	B1 inversion	0	1 = Inverted insertion of the B1 byte for diagnostic purposes
6	R/W	B2 inversion	0	1 = Inverted insertion of the B2 bytes for diagnostic purposes
7	R/W	B3 inversion	0	1 = Inverted insertion of the B3 overhead byte for diagnostic purposes
8	R/W	FDD	0	0 = Frame descrambling enabled 1 = Frame descrambling disabled
9	R/W	FSD	0	0 = Frame scrambling enabled 1 = Frame scrambling disabled
10	R/W	CDD	0	0 = Cell descrambling enabled or Payload descrambling in POS mode 1 = Cell descrambling disabled or Payload descrambling in POS mode
11	R/W	CSD	0	0 = Cell scrambling enabled or Payload scrambling enabled in POS mode 1 = Cell scrambling disabled or Payload scrambling disabled in POS mode
13:12	R/W	CHEI[1:0]	0	Cell Header Error Insertion 00 = No error insertion 01 = One-bit error insertion (second bit of a cell) 11 = Multi-bit error insertion (first 2 bits of a cell)
14	R/W	FCS inversion	0	1 = Inverted insertion of the FCS error code of the packet (bit-wise of the FCS bits)
15	R/W	Reserved	0	Reserved for future functionality

Table 6-7. Port Status Register, Ports 0–3 (Add: 0x05, 0x45, 0x85, 0xC5)

Bit	Type	Name	Default	Description
0	R	LOS status	*	1 = LOS defect is present
1	R	SEF status	*	1 = SEF defect is present
2	R	LOF status	*	1 = LOF defect is present
3	R	AIS-L status	*	1 = AIS-L defect is present
4	R	RDI-L status	*	1 = RDI-L defect is present
5	R	LOP-P status	*	1 = LOP-P defect is present
6	R	AIS-P status	*	1 = AIS-P defect is present
7	R	RDI-P status	*	1 = RDI-P defect is present
8	R	OCD status	*	1 = OCD defect is present
9	R	LCD status	*	1 = LCD defect is present
10	R	APS Mismatch status	*	1 = APS State Machine is in the Inconsistent state
11	R	PLM status	*	1 = PLM defect is present
12	R	UNEQipped	*	1 = Unequipped defect is present
15:13	—	Unused	—	—
NOTE(S): * = Upon reset, it is assumed that the receive path is defective. Status bits reflecting the defects are cleared only after valid data (for the appropriate number of frames) is detected.				

Table 6-8. Rx FIFO Control/Status Register (ATM mode); Ports 0–3 (Add: 0x06, 0x46, 0x86, 0xC6)

Bit	Type	Name	Default	Description
2:0	R	RFS[0:2] (Engineering Only)	X	Rx FIFO Status 000 = Rx FIFO does not contain a complete cell 001 = Rx FIFO contains a complete cell 010 = Rx FIFO contains two complete cells 011 = Rx FIFO contains three complete cells 100 = Rx FIFO contains four complete cells
3	R/W	Rx FIFO reset	0	1 = Rx FIFO is in Reset mode
4	R/W	Rx UTOPIA reset	0	1 = Rx UTOPIA reset This mode is provided for quick recovery on a link fault. By resetting the FIFO (bit 3) and the UTOPIA (bit 4), the user can configure the port and disable the data writing to the FIFOs. In this case, the CLAV/Packet-Available pin is not driven with a value when the port is selected (because it is usually mapped to another port's address to act as the hot back-up). As soon as a fault is detected and cleared, the Rx FIFO can be enabled to begin receiving/transmitting data.
15:5	R	Reserved	0	Reserved for future functionality.

Table 6-9. Tx FIFO Control/Status Register (ATM mode), Ports 0–3 (Add: 0x07, 0x47, 0x87, 0xC7)

Bit	Type	Name	Default	Description
2:0	R	TFS[0:2] (Engineering Only)	X	Tx FIFO Status 000 = Tx FIFO does not contain a complete cell 001 = Tx FIFO contains a complete cell 010 = Tx FIFO contains two complete cells 011 = Tx FIFO contains three complete cells 100 = Tx FIFO contains four complete cells
15:3	R	Reserved	0	Reserved for future functionality

Table 6-10. FIFO Status Register (POS mode), Ports 0–3 (Add: 0x08, 0x48, 0x88, 0xC8)

Bit	Type	Name	Default	Description
5:0	R	Rx BAV	0x00	Number of bytes in the Rx FIFO (POS mode); the count is in double words
15:6	R	Reserved	0	Reserved for future functionality

Table 6-11. FIFO Status Register (POS mode), Ports 0–3 (Add: 0x09, 0x49, 0x89, 0xC9)

Bit	Type	Name	Default	Description
7:0	R	Tx BAV	0x00	Number of bytes in the Tx FIFO (POS mode); the count is in double words
15:8	R	Reserved	0	Reserved for future functionality

Table 6-12. Tx FIFO Threshold; Tx-Inter-Frame-Fill, Ports 0–3 (Add: 0x0A, 0x4A, 0x8A, 0xCA)

Bit	Type	Name	Default	Description
5:0	R/W	Tx FIFO Thres	0x06	The number of words in the FIFO (POS mode) above which packets' transmission begins. This value should be chosen based on the system requirements to avoid underrun of the FIFOs.
7:6	R	Reserved	—	Reserved
14:8	R/W	Tx IFF	0x01	The number of flags inserted between two packets. The End-Of-Packet is marked with a flag. To achieve maximum performance, only one flag is required; however, the system may try to process the End-Of-Packet. The user may choose to add additional IFF flags. Choosing value 1 adds one flag to the necessary one. Choosing value 0 does not add any frame fill.
15	R	Reserved	—	Reserved

Table 6-13. Global Interrupt Register (Add: 0x10)

Bit	Type	Name	Default	Description
0	R	Port 0 Framer	X	1 = Port 0 Framer block is the interrupt source
1	R	Port 0 Overhead A	X	1 = Port 0 Overhead A Byte Processor block is the interrupt source
2	R	Port 0 Overhead B	X	1= Port 0 Overhead B Byte Processor block is the interrupt source
3	R	Port 0 Cell, FIFO and UTOPIA	X	1 = Port 0 Cell/Packet Processor, FIFO, or UTOPIA block is the interrupt source
4	R	Port 1 Framer	X	1 = Port 1 Framer block is the interrupt source
5	R	Port 1 Overhead A	X	1 = Port 1 Overhead A Byte Processor block is the interrupt source
6	R	Port 1 Overhead B	X	1 = Port 1 Overhead B Byte Processor block is the interrupt source
7	R	Port 1 Cell, FIFO and UTOPIA	X	1 = Port 1 Cell/Packet Processor, FIFO, or UTOPIA block is the interrupt source
8	R	Port 2 Framer	X	1 = Port 2 Framer block is the interrupt source
9	R	Port 2 Overhead A	X	1 = Port 2 Overhead A Byte Processor block is the interrupt source
10	R	Port 2 Overhead B	X	1 = Port 2 Overhead B Byte Processor block is the interrupt source
11	R	Port 2 Cell, FIFO and UTOPIA	X	1 = Port 2 Cell/Packet Processor, FIFO, or UTOPIA block is the interrupt source
12	R	Port 3 Framer	X	1 = Port 3 Framer block is the interrupt source
13	R	Port 3 Overhead A	X	1 = Port 3 Overhead A Byte Processor block is the interrupt source
14	R	Port 3 Overhead B	X	1 = Port 3 Overhead B Byte Processor block is the interrupt source
15	R	Port 3 Cell, FIFO and UTOPIA	X	1 = Port 3 Cell/Packet Processor, FIFO, or UTOPIA block is the interrupt source
NOTE(S): Interrupt registers are reset upon read.				

Table 6-14. Global Mask Register (Add: 0x11)

Bit	Type	Name	Default	Description
0	R/W	Port 0 Framer	1	1 = Mask Port 0 Framer block interrupts
1	R/W	Port 0 Overhead A	1	1 = Mask Port 0 Overhead Bytes Processor interrupts
2	R/W	Port 0 Overhead B	1	1 = Mask Port 0 Overhead Bytes Processor
3	R/W	Port 0 Cell, FIFO and UTOPIA	1	1 = Mask Port 0 Cell/Packet Processor, FIFO, and UTOPIA/POS Interface Block interrupts
4	R/W	Port 1 Framer	1	1 = Mask Port 1 Framer Block interrupts
5	R/W	Port 1 Overhead A	1	1 = Mask Port 1 Overhead A Byte Processor Block interrupts
6	R/W	Port 1 Overhead B	1	1 = Mask Port 1 Overhead B Byte Processor Block interrupts
7	R/W	Port 1 Cell, FIFO and UTOPIA	1	1 = Mask Port 1 Cell/Packet Processor, FIFO, and UTOPIA/POS Interface Block interrupts
8	R/W	Port 2 Framer	1	1 = Mask Port 2 Framer Block interrupts
9	R/W	Port 2 Overhead	1	1 = Mask Port 2 Overhead A Byte Processor Block interrupts
10	R/W	Port 2 Overhead B	1	1 = Mask Port 2 Overhead B Byte Processor Block interrupts
11	R/W	Port 2 Cell, FIFO and UTOPIA	1	1 = Mask Port 2 Cell/Packet Processor, FIFO, and UTOPIA/POS Interface Block interrupts
12	R/W	Port 3 Framer	1	1 = Mask Port 3 Framer Block interrupts
13	R/W	Port 3 Overhead	1	1 = Mask Port 3 Overhead A Byte Processor Block interrupts
14	R/W	Port 3 Overhead B	1	1 = Mask Port 3 Overhead B Byte Processor Block interrupts
15	R/W	Port 3 Cell, FIFO and UTOPIA	1	1 = Mask Port 3 Cell/Packet Processor, FIFO, and UTOPIA/POS Interface Block interrupts

Table 6-15. Framer Interrupt Register (Add: 0x12, 0x52, 0x92, 0xD2)

Bit	Type	Name	Default	Description
0	R/W	LOS intr	X	1 = LOS defect was generated or terminated
1	R/W	SEF intr	X	1 = SEF defect was generated or terminated
2	R/W	LOF intr	X	1 = LOF defect was generated or terminated
3	R/W	RFCHF intr	X	1 = Rx Frame Counter is half-full
4	R/W	TFCHF intr	X	1 = Tx Frame Counter is half-full
15:5	—	Unused	—	—

Table 6-16. Framer Mask Register (Add: 0x13, 0x53, 0x93, 0xD3)

Bit	Type	Name	Default	Description
0	R/W	LOS mask	1	1 = LOS intr mask
1	R/W	SEF mask	1	1 = SEF intr mask
2	R/W	LOF mask	1	1 = LOF intr mask
3	R/W	RFCHF mask	1	1 = RFCHF intr mask
4	R/W	TFCHF mask	1	1 = TFCHF intr mask
15:5	—	Unused	—	—

Table 6-17. Overhead Byte Processor Interrupt Register A (Add: 0x14, 0x54, 0x94, 0xD4)

Bit	Type	Name	Default	Description
0	R/W	SBIP intr	*	1 = Section BIP-8 error was detected
1	R/W	AIS-L intr	*	1 = AIS-L defect was detected or terminated
2	R/W	RDI-L intr	*	1 = RDI-L defect was detected or terminated
3	R/W	LBIP intr	*	1 = Line BIP-8/24 error was detected
4	R/W	REI-L intr	*	1 = REI-L error was detected
5	R/W	K1/K2 capture intr	*	1 = New value for the K1 or K2 Overhead bytes was captured. Value is captured when three consecutive identical frames are received.
6	R/W	K1/K2 state intr	*	1 = APS state machine changed state. This machine changes to the Inconsistent State if within a 12-frame period; no three consecutive K1 bytes are received with the same value. This machine exits the Inconsistent State when three consecutive, equal K1 values are received.
7	R/W	S1 intr	*	1 = New value for bits 4–7 of the S1 overhead byte was captured
8	R/W	LOP-P intr	*	1 = LOP-P defect was detected or terminated
9	R/W	AIS-P intr	*	1 = AIS-P defect was detected or terminated
10	R/W	RDI-P intr	*	1 = RDI-P defect was detected or terminated
11	R/W	PBIP intr	*	1 = Path BIP-8 error was detected
12	R/W	REI-P intr	*	1 = REI-P error was detected
13	R/W	PSL intr	*	1 = New value for the C2 Overhead byte was captured. A new value is captured when five consecutive identical values are received.
14	R/W	PTMIS intr	*	1 = Path Trace Mismatch occurred
15	R/W	PLM intr	*	1 = PLM defect was detected or terminated
NOTE(S): Upon reset, it is assumed that the receive path is defective. Status bits reflecting the defects are cleared only after valid data (for the appropriate number of frames) is detected.				

Table 6-18. Overhead Byte Processor Mask Register A (Add: 0x15, 0x55, 0x95, 0xD5)

Bit	Type	Name	Default	Description
0	R/W	SBIP mask	1	1 = SBIP intr mask
1	R/W	AIS-L mask	1	1 = AIS-L intr mask
2	R/W	RDI-L mask	1	1 = RDI-L intr mask
3	R/W	LBIP mask	1	1 = LBIP intr mask
4	R/W	REI-L mask	1	1 = REI-L intr mask
5	R/W	K1/K2 capture mask	1	1 = K1/K2 capture intr mask
6	R/W	K1/K2 state intr mask	1	1 = K1/K2 state intr mask
7	R/W	S1 mask	1	1 = S1 intr mask
8	R/W	LOP-P mask	1	1 = LOP-P intr mask
9	R/W	AIS-P mask	1	1 = AIS-P intr mask
10	R/W	RDI-P mask	1	1 = RDI-P intr mask
11	R/W	PBIP mask	1	1 = PBIP8 intr mask
12	R/W	REI-P mask	1	1 = REI-P intr mask
13	R/W	PSL mask	1	1 = PSL intr mask
14	R/W	PTMIS mask	1	1 = PTMIS intr mask
15	R/W	PLM mask	1	1 = PLM intr mask

Table 6-19. Overhead Byte Processor Interrupt Register B (Add: 0x16, 0x56, 0x96, 0xD6)

Bit	Type	Name	Default	Description
0	R/W	Unequipped intr	*	1 = Unequipped error was detected
1	R/W	Tx Abort	*	1 = An abort sequence was transmitted due to an error (POS mode)
2	R/W	Rx Abort	*	1 = An abort sequence was received (POS mode)
3	R/W	Line BER intr	*	1 = Line BER exceeded the threshold. An interrupt is generated when the number of pre-programmed B2 errors (threshold) occurs during the programmed period.
4	R/W	Rx FCS error	*	1 = FCS error was found on the receive path (POS mode)
5	R/W	Rx Runt Packet error	*	1 = An illegal (less than one byte of information) packet was found on the receive path (POS mode)
15:6	R	Reserved	0	Reserved for future functionality
NOTE(S): * = Upon reset, it is assumed that the receive path is defective. Status bits reflecting the defects are cleared only after valid data (for the appropriate number of frames) is detected.				

Table 6-20. Overhead Byte Processor Mask Register (Add: 0x17, 0x57, 0x97, 0xD7)

Bit	Type	Name	Default	Description
0	R/W	Unquipped mask	1	1 = Unequipped error mask
1	R/W	Tx Abort mask	1	1 = Tx abort intr mask
2	R/W	Rx Abort mask	1	1 = Rx abort intr mask
3	R/W	Line BER mask	1	1 = Line BER intr mask
4	R/W	FCS Error mask	*	1 = FCS error intr mask
5	R/W	Runt Packet mask	*	1 = Runt (less than one byte of information) packet intr mask
15:6	R	Reserved	0	Reserved for future functionality

Table 6-21. Cell, FIFO, and UTOPIA/POS Interrupt Register (Add: 0x18, 0x58, 0x98, 0xD8)

Bit	Type	Name	Default	Description
0	R/W	OCD intr	*	1 = OCD defect was detected or terminated (ATM mode)
1	R/W	LCD intr	*	1 = LCD defect was detected or terminated (ATM mode)
2	R/W	CBH intr	*	1 = Correctable Bad Header (CBH) was detected (ATM mode)
3	R/W	UBH intr	*	1 = Uncorrectable Bad Header (UBH) was detected (ATM mode)
4	R/W	RFO intr	*	1 = Rx FIFO overrun
5	R/W	TFO intr	*	1 = Tx FIFO overrun
6	R/W	RFU intr	*	1 = Rx FIFO underrun
7	R/W	TFU intr	*	1 = Tx FIFO underrun
8	R/W	PE intr	*	1 = Tx Parity Error
9	R/W	SOCE intr	*	1 = Start Of Cell Error Generated when TxSOC is sampled high and a cell is already being transmitted
10	R/W	CBHCHF intr	*	1 = Correctable Bad Header Counter is half-full
11	R/W	UBHCHF intr	*	1 = Uncorrectable Bad Header Counter is half-full
12	R/W	RCCHF intr	*	1 = Rx Cell/Packet Counter is half-full
13	R/W	TCCHF intr	*	1 = Tx Cell/Packet Counter is half-full
14	R/W	PEMIL intr	*	1 = Packet exceeded minimum length limit
15	R/W	PEMAL intr	*	1 = Packet exceeded maximum length limit

NOTE(S): * = Upon reset, it is assumed that the receive path is defective. Status bits reflecting the defects are cleared only after valid data (for the appropriate number of frames) is detected.

Table 6-22. Cell, FIFO, and UTOPIA Mask Register (Add: 0x19, 0x59, 0x99, 0xD9)

Bit	Type	Name	Default	Description
0	R/W	OCD mask	1	1 = OCD intr mask
1	R/W	LCD mask	1	1 = LCD intr mask
2	R/W	CBH mask	1	1 = CBH intr mask
3	R/W	UBH mask	1	1 = UBH intr mask
4	R/W	RFO mask	1	1 = RFO intr mask
5	R/W	TFO mask	1	1 = TFO intr mask
6	R/W	RFU mask	1	1 = RFU intr mask
7	R/W	TFU mask	1	1 = TFU intr mask
8	R/W	PE mask	1	1 = PE intr mask
9	R/W	SOCE mask	1	1 = SOCE intr mask
10	R/W	CBHCHF mask	1	1 = CBHCHF intr mask
11	R/W	UBHCHF mask	1	1 = UBHCHF intr mask
12	R/W	RCCHF mask	1	1 = RCCHF intr mask
13	R/W	TCCHF mask	1	1 = TCCHF intr mask
14	R/W	PEMIL mask	1	1 = PEMIL intr mask
15	R/W	PEMAL mask	1	1 = PEMAL mask

Table 6-23. Rx Minimum Packet Length Register (Add: 0x1A, 0x5A, 0x9A, 0xDA)

Bit	Type	Name	Default	Description
7:0	R/W	Min_Pack_Length	0x02	Determines the minimum length of a packet (POS mode). Packets violating this limit are marked as error packets. An interrupt upon detection of an error is optional.
15:8	R	Reserved	0	Reserved for future functionality.

Table 6-24. Rx Maximum Packet Length Register (Add: 0x1B, 0x5B, 0x9B, 0xDB)

Bit	Type	Name	Default	Description
15:0	R/W	Max_Pack_Length	0x0600	Determines the maximum length of a packet (POS mode). Packets violating this limit are marked as error packets. An interrupt upon detection of an error is optional.

Table 6-25. Rx FIFO High-Limit (Rx FHL) Register (Add: 0x1C, 0x5C, 0x9C, 0xDC)

Bit	Type	Name	Default	Description
5:0	R/W	Rx FIFO High Limit	0x2F	Determines the number of double words (32-bit) that is the limit for Rx FIFO full condition. When the number of double words in the Rx FIFO exceeds the [predefined] value, the DRPA and PRPA pins are asserted. When at least one End-Of-Packet resides in the Rx FIFO, the RPA signals will be asserted regardless of the quantity of words in the FIFO. The RPA pins are not deasserted when the number of double words is less than the predefined value. Although the value specified in this register allows setting boundaries to the FIFO in words (two bytes), the POS packet can end within byte boundaries, as described in the POS interface.
15:6	R	Reserved	0	Reserved for future functionality.

Table 6-26. Rx FIFO Low-Limit (Rx FLL) Register (Add: 0x1D, 0x5D, 0x9D, 0xDD)

Bit	Type	Name	Default	Description
5:0	R/W	Rx FIFO Low Limit	0x08	Determines the number of double words (32-bit) that is the limit for Rx FIFO empty condition. When the number of double words in the Rx FIFO is less than the [predefined] value, the DRPA and PRPA pins are deasserted. Although the value specified in this register sets FIFO boundaries in double words (four bytes), the POS packet can end within byte boundaries, as described in the POS interface.
15:6	R	Reserved	0	Reserved for future functionality.

Table 6-27. Tx FIFO High-Limit (Tx FHL) Register (Add: 0x1E, 0x5E, 0x9E, 0xDE)

Bit	Type	Name	Default	Description
5:0	R/W	Tx FIFO High Limit	0x2F	Determines the number of double words (32-bit) in the Tx FIFO on which the DTPA and PTPA pins are deasserted. When the number of double words in the Tx FIFO exceeds this [predefined] value, the TPA signals are negated (according to the POS interface functionality) to reflect a Tx FIFO full condition. When the number of double words is less than this value, the DTPA and PTPA pins are not asserted. Although the number specified in this register sets FIFO boundaries in words (two bytes), the POS packet can end within byte boundaries as described in the POS interface.
15:6	R	Reserved	0	Reserved for future functionality.

Table 6-28. Tx FIFO Low Limit (Tx-FLL) Register (Add: 0x1F, 0x5F, 0x9F, 0xDF)

Bit	Type	Name	Default	Description
5:0	R/W	Tx FIFO Low Limit	0x08	Determines the number of double words (32-bit), which is the limit for Tx FIFO empty condition. When Tx FIFO contain less double words than the [predefined] value, the DRPA and PRPA pins are asserted. Although the number specified in this register sets FIFO boundaries in double words (four bytes), the POS packet can end within byte boundaries as described in the POS interface.
15:6	R	Reserved	0	Reserved for future functionality.

Table 6-29. Section Error Monitor Register (Add: 0x20, 0x60, 0xA0, 0xE0)

Bit	Type	Name	Default	Description
15:0	R	SBIP[15:0]	0	Section BIP-8 error 16-bit saturating counter. This counter reflects the number of Section BIP-8 errors (Individual or Frame mode) detected since the last time this counter was read. The counter should be polled at least once per second to avoid saturation. Counter is reset upon read.
NOTE(S): * Performance Monitor Registers are reset upon read.				

Table 6-30. Line Error Monitor Register, Lower Word (Add: 0x21, 0x61, 0xA1, 0xE1)

Bit	Type	Name	Default	Description
15:0	R	LBIP[15:0]	0	Line BIP-24 Error, 32-bit saturating counter. This counter reflects the number of line BIP-8 errors (Individual or Frame mode) detected since the last time this counter was read. This is the lower word of the counter and should be read first. The counter is reset upon read.

Table 6-31. Line Error Monitor Register, Upper Word (Add: 0x22, 0x62, 0xA2, 0xE2)

Bit	Type	Name	Default	Description
15:0	R	LBIP[31:16]	0	Line BIP-24 Error, 32-bit saturating counter. This is the upper word of the counter and should be read immediately after the lower word to avoid loss of information.

Table 6-32. Line Remote Error Indication Register, Lower Word (Add: 0x23, 0x63, 0xA3, 0xE3)

Bit	Type	Name	Default	Description
15:0	R	REI-L[15:0]	0	REI-L 32-bit saturating counter. This counter reflects the number of REI-Ls (Individual or Frame mode) detected since the last time this counter was read. This is the lower word of the counter and should be read first. The counter is reset upon read.

Table 6-33. Line Remote Error Indication Register, Upper Word (Add: 0x24, 0x64, 0xA4, 0xE4)

Bit	Type	Name	Default	Description
15:0	R	REI-L[31:16]	0	REI-L 32-bit saturating counter. This is the upper word of the counter and should be read immediately after the lower word to avoid loss of information.

Table 6-34. Path Error Monitor Register (Add: 0x25, 0x65, 0xA5, 0xE5)

Bit	Type	Name	Default	Description
15:0	R	PBIP[15:0]	0	Path BIP-8 error 16-bit saturating counter. This counter reflects the number of Path BIP-8 errors (Individual or Frame mode) detected since the last time this counter was read. The counter should be polled at least once per second to avoid saturation. The counter is reset upon read.

Table 6-35. Path Remote Error Indication Register (Add: 0x26, 0x66, 0xA6, 0xE6)

Bit	Type	Name	Default	Description
15:0	R	REI-P[15:0]	0	Path BIP-8 16-bit saturating counter. This counter reflects the number of REI-Ps (Individual or Frame mode) detected since the last time this counter was read. The counter should be polled at least once per second to avoid saturation. The counter is reset upon read.

Table 6-36. Uncorrectable Bad Header Counter Register (Add: 0x27, 0x67, 0xA7, 0xE7)

Bit	Type	Name	Default	Description
15:0	R	UBH[15:0]	0	Uncorrectable Bad Header Cell 16-bit saturating counter. This counter reflects the number of uncorrectable bad header cells received since the last time this counter was read. The counter is reset upon read (ATM mode).

Table 6-37. Correctable Bad Header Counter Register (Add: 0x28, 0x68, 0xA8, 0xE8)

Bit	Type	Name	Default	Description
15:0	R	CBH[15:0]	0	Correctable Bad Header Cell 16-bit saturating counter. This counter reflects the number of correctable bad header cells received since the last time this counter was read. The counter is reset upon read (ATM mode).

Table 6-38. Rx Cell Counter Register, Lower Word (Add: 0x29, 0x69, 0xA9, 0xE9)

Bit	Type	Name	Default	Description
15:0	R	RxCell[15:0]	0	Receive cell 32-bit saturating counter. This counter reflects the number of cells/s received and transferred into the Rx FIFO since the last time this counter was read. This number does not include idle/unassigned cells/packets and uncorrectable bad header cells. This is the lower word of the counter and should be read first. The counter is reset upon read. When counting packets, each EOP is counted when entering the FIFO.

Table 6-39. Rx Cell Counter Register, Upper Word (Add: 0x2A, 0x6A, 0xAA, 0xEA)

Bit	Type	Name	Default	Description
15:0	R	RxCell[31:16]	0	Receive cell 32-bit saturating counter. This is the upper word of the counter and should be read immediately after the lower word to avoid loss of information.

Table 6-40. Tx Cell Counter Register, Lower Word (Add: 0x2B, 0x6B, 0xAB, 0xEB)

Bit	Type	Name	Default	Description
15:0	R	TxCell[15:0]	0	Transmit cell 32-bit saturating counter. This counter reflects the number of cells that were drawn from the Tx FIFO and transmitted into the line since the last time this counter was read. This number does not include generated idle/unassigned cells. This is the lower word of the counter and should be read first. The counter is reset upon read. Each EOP is counted when read from the FIFO.

Table 6-41. Tx Cell Counter Register, Upper Word (Add: 0x2C, 0x6C, 0xAC, 0xEC)

Bit	Type	Name	Default	Description
31:16	R	TxCell[31:16]	0	Transmit cell 32-bit saturating counter. This is the upper word of the counter and should be read immediately after the lower word to avoid loss of information.

Table 6-42. Rx Frame Counter Register (Add: 0x2D, 0x6D, 0xAD, 0xED)

Bit	Type	Name	Default	Description
15:0	R	RxFrame[15:0]	0	Receive frame 16-bit saturating counter. This counter reflects the number of frames received since the last time this counter was read. The counter is reset upon read.

Table 6-43. Tx Frame Counter Register (Add: 0x2E, 0x6E, 0xAE, 0xEE)

Bit	Type	Name	Default	Description
15:0	R	TxFrame[15:0]	0	Transmit frame 16-bit saturating counter. This counter reflects the number of frames transmitted since the last time this counter was read. Counter is reset upon read.

Table 6-44. Rx APS Channel Register (K1, K2) (Add: 0x30, 0x70, 0xB0, 0xF0)

Bit	Type	Name	Default	Description
7:0	R	K2[7:0]	X	These bytes are the received K1 and K2 overhead bytes, which are used for automatic protection switching purposes. A new value is captured if new K1 value is received for three consecutive frames. An Interrupt is generated upon capture. ***NOTE:*** Bits [2:0] of K2 are reserved for AIS-L and RDI-L.
15:8	R	K1[7:0]	X	—

Table 6-45. Tx APS Channel Register (K1, K2) (Add: 0x31, 0x71, 0xB1, 0xF1)

Bit	Type	Name	Default	Description
7:0	R/W	K2[7:0]	0	These bytes are the transmitted K1 and K2 overhead bytes. ***NOTE:*** Bits 0:2 of K2 are controlled by the hardware and may not be modified.
15:8	R/W	K1[7:0]	0	—

Table 6-46. Rx Synchronization Status Message Register (S1) (Add: 0x32, 0x72, 0xB2, 0xF2)

Bit	Type	Name	Default	Description
3:0	R	S1[0:3]	X	Bits 0–3 of the received S1 overhead byte. These bits are assigned for synchronization status messages. An Interrupt is generated upon capture of a new S1 value. These bits correspond to BellCore's standard bits 4–7.
15:4	—	Unused	—	—

Table 6-47. Tx Synchronization Status Message Register (S1) (Add: 0x33, 0x73, 0xB3, 0xF3)

Bit	Type	Name	Default	Description
3:0	R/W	S1[0:3]	0	Bits 0–3 of the transmitted S1 overhead byte. These bits are assigned for synchronization status messages.
15:4	—	Unused	—	—

Table 6-48. Rx Path Signal Label Register (C2) (Add: 0x34, 0x74, 0xB4, 0xF4)

Bit	Type	Name	Default	Description
7:0	R	C2[7:0]	X	Receive Path Signal Label overhead byte. A value is captured each time the same new value is received for five consecutive frames. An Interrupt is generated upon capture.
15:8	—	Unused	—	—

Table 6-49. Tx Path Signal Label Register (C2) (Add: 0x35, 0x75, 0xB5, 0xF5)

Bit	Type	Name	Default	Description
7:0	R/W	C2[7:0]	0x13	Transmit Path Signal Label overhead byte. Transmitted with Default Value 0x13, which designates ATM mapping.
15:8	—	Unused	—	—

Table 6-50. Rx Path User Channel Register (F2, F3) (Add: 0x36, 0x76, 0xB6, 0xF6)

Bit	Type	Name	Default	Description
7:0	R/W	F2[7:0]	X	Receive Path User Channel overhead bytes
15:8	R/W	F3[7:0]	X	—

Table 6-51. Tx Path User Channel Register (F2, F3) (Add: 0x37, 0x77, 0xB7, 0xF7)

Bit	Type	Name	Default	Description
7:0	R/W	F2[7:0]	0	Transmit Path User Channel overhead bytes
15:8	R/W	F3[7:0]	0	—

Table 6-52. Path Trace Address Register (Add: 0x38, 0x78, 0xB8, 0xF8)

Bit	Type	Name	Default	Description
4:0	R/W	Address	0	Address of word in Path Trace Buffer (0x0–0x1F). This value will be incremented automatically after every access (read or write) to the Path Trace buffer.
5	R/W	Tx/Rx	0	0 = Access to Transmit buffer 1 = Access to Receive buffer
6	R/W	W/R	0	0 = Write value to Path Trace register 1 = Read value from Path Trace register
7	Enb	Enable/ Disable	0	0 = Path Trace Transmission disabled 1 = Path Trace Transmission enabled
15:8	—	Unused	—	—

Table 6-53. Path Trace Data Register (Add: 0x39, 0x79, 0xB9, 0xF9)

Bit	Type	Name	Default	Description
15:0	R/W	Data	0	Data written/read to/from the Path Trace buffer. This register should be written/read only after writing the appropriate address to the Path Trace Address register.

Table 6-54. Rx RDI-P Register (Add: 0x3A, 0x7A, 0xBA, 0xFA)

Bit	Type	Name	Default	Description
2:0	R	RDI[2:0]	101	Bits 0–2 of the received G1 byte.
15:3	—	Unused	—	—

Table 6-55. Tx RDI-P Register (Add: 0x3B, 0x7B, 0xBB, 0xFB)

Bit	Type	Name	Default	Description
2:0	R/W	RDI[2:0]	0	Bits 0–2 of the transmitted G1 byte.
15:3	—	Unused	—	—

Table 6-56. Rx Order Wire Byte Register (E1, E2) (Add: 0x101, 0x141, 0x181, 0x1C1)

Bit	Type	Name	Default	Description
7:0	R/W	E1[7:0]	0	Receive Order Wire overhead bytes
15:8	R/W	E2[7:0]	0	Receive Order Wire overhead bytes

Table 6-57. Tx Order Wire Byte Register (E1, E2) (Add: 0x102, 0x142, 0x182, 0x1C2)

Bit	Type	Name	Default	Description
7:0	R/W	E1[7:0]	0	Transmit Order Wire overhead bytes
15:8	R/W	E2[7:0]	0	Transmit Order Wire overhead bytes

Table 6-58. Rx Section User Channel Register (F1) and Rx Section Trace Path (Add: 0x103, 0x143, 0x183, 0x1C3)

Bit	Type	Name	Default	Description
7:0	R/W	F1[7:0]	0	Received Order Wire overhead bytes.
15:8	R	J0[7:0]	0	Received Section Trace byte. This byte is not in the message format like J1, but rather a single, general-purpose byte.

Table 6-59. Tx Section User Channel Register (F1) and Tx Section Trace Path (J0) (Add: 0x104, 0x144, 0x184, 0x1C4)

Bit	Type	Name	Default	Description
7:0	R/W	F1[7:0]	0	Transmit Order Wire overhead bytes.
15:8	R/W	J0[7:0]	1	Transmit Section Trace byte. This byte is not in the message format like J1, but rather a single, general-purpose byte.

Table 6-60. Rx Path Growth Byte Register (Z4, Z5) (Add: 0x105, 0x145, 0x185, 0x1C5)

Bit	Type	Name	Default	Description
7:0	R/W	Z4[7:0]	0	Receive Path Growth overhead bytes
15:8	R/W	Z5[7:0]	0	Receive Path Growth overhead bytes

Table 6-61. Tx Path Growth Byte Register (Z4, Z5) (Add: 0x106, 0x146, 0x186, 0x1C6)

Bit	Type	Name	Default	Description
7:0	R/W	Z4[7:0]	0	Transmit Path Growth overhead bytes
15:8	R/W	Z5[7:0]	0	Transmit Path Growth overhead bytes

Table 6-62. Rx Bad FCS Counter Register (Add: 0x107, 0x147, 0x187, 0x1C7)

Bit	Type	Name	Default	Description
15:0	R	BFC[15:0]	0	Number of packets received with a bad FCS code (POS mode)

Table 6-63. Rx Maximum Length Violating Packet Counter Register (Add: 0x108, 0x148, 0x188, 0x1C8)

Bit	Type	Name	Default	Description
15:0	R	MXV[15:0]	0	Number of packets which violated the maximum packet limit (POS mode)

Table 6-64. Rx Minimum Length Violating Packet Counter Register (Add: 0x109, 0x149, 0x189, 0x1C9)

Bit	Type	Name	Default	Description
15:0	R	MNV[15:0]	0	Number of packets which violated the minimum packet limit (POS mode)

Table 6-65. Rx Packet Counter Register, Lower Word (Add: 0x10A, 0x14A, 0x18A, 0x1Ca)

Bit	Type	Name	Default	Description
15:0	R	Rx Pack[15:0]	0	Receive Packet 32-bit saturating counter. This counter reflects the number of packets received and transferred into the Rx FIFO since the last time the counter was read. This is the lower word of the counter and should be read first. The counter is reset upon read. Each EOP is counted when entering the FIFO.

Table 6-66. Rx Packet Counter Register, Upper Word (Add: 0x10B, 0x14B, 0x18B, 0x1CB)

Bit	Type	Name	Default	Description
15:0	R	Rx Pack[31:16]	0	Receive Packet 32-bit saturating counter. This is the upper word of the counter and should be read immediately after the lower word to avoid loss of information.

Table 6-67. Rx Aborted Packet Counter Register (Add: 0x10C, 0x14C, 0x18C, 0x1CC)

Bit	Type	Name	Default	Description
15:0	R	Rx Ab_Packet [15:0]	0	This counter holds the number of received aborted packets. This register is reset to its default value upon reading.

Table 6-68. Tx Aborted Packet Counter Register (Add: 0x10D, 0x14D, 0x18D,0x1CD

Bit	Type	Name	Default	Description
15:0	R	Tx Ab_Packet[15:0]	0	This counter holds the number of transmitted packets that were aborted. This register is reset to its default value upon reading.

Table 6-69. Tx Packet Counter Register, Lower Word (Add: 0x10E, 0x14E, 0x18E, 0x1CE)

Bit	Type	Name	Default	Description
15:0	R	TxPack[15:0]	0	Transmit Packet 32-bit saturating counter. This counter reflects the number of packets drawn from the Tx FIFO and transmitted into the line since the last time this counter was read. This is the lower word of the counter and should be read first. The counter is reset upon read. Each EOP is counted when read from the FIFO.

Table 6-70. Tx Packet Counter Register, Upper Word (Add: 0x10F, 0x14F, 0x18F, 0x1CF)

Bit	Type	Name	Default	Description
31:16	R	TxPack[31:16]	0	Transmit Packet 32-bit saturating counter. This is the upper word of the counter and should be read immediately after the lower word to avoid loss of information.

Table 6-71. B2 BER Error Counter Register (Add: 0x110, 0x150, 0x190, 0x1D0)

Bit	Type	Name	Default	Description
15:0	R	B2-ber-err	0	This 16-bit register holds the number of line errors (B2) detected since the counter was last reset. This counter is working in conjunction with the Threshold and Period register to provide error counting within a predefined period of time. When the period counter reaches the value of zero (EOP), the error counter is reset to zero and the counting starts over.

Table 6-72. B2 Error Threshold Register (Add: 0x111, 0x151, 0x191, 0x1D1)

Bit	Type	Name	Default	Description
15:0	R	B2-err-thrs	0	This 16-bit register holds the threshold of B2 errors above which an interrupt is generated. When the number of errors is more than the value held in the register within the specified period, the interrupt is generated.

Table 6-73. Line Error Period Register, Lower Word (Add: 0x112, 0x152, 0x192, 0x1D2)

Bit	Type	Name	Default	Description
15:0	R	Line-err-per	0	The period counter is a 32-bit counter which counts the 19.44 MHz clock. To define a specific period of time in which the error counting is accomplished, the user should load this register with the appropriate value which reflects the required period of time.

Table 6-74. Line Error Period Register, Upper Word (Add: 0x113, 0x153, 0x193, 0x1D3)

Bit	Type	Name	Default	Description
15:0	R	Line-err-per	0	The period counter is a 32-bit counter which counts the 19.44 MHz clock. To define a specific period of time in which the error counting is accomplished, the user should load this register with the appropriate value which reflects the required period of time.

7.0 Functional Timing and Electrical Specification

7.1 ATM Layer Interface

7.1.1 One Rx/Tx CLAV

7.1.1.1 Receive

RxClav indicates whether the PHY port, whose address was on RxAdd in the previous clock cycle, has a complete cell available. The ATM layer selects a PHY port from which to receive the next cell by placing its address on RxAdd when *RxEnb is not asserted and asserting *RxEnb on the next cycle.

Figure 7-1. Receive One Rx/Tx CLAV Functional Timing

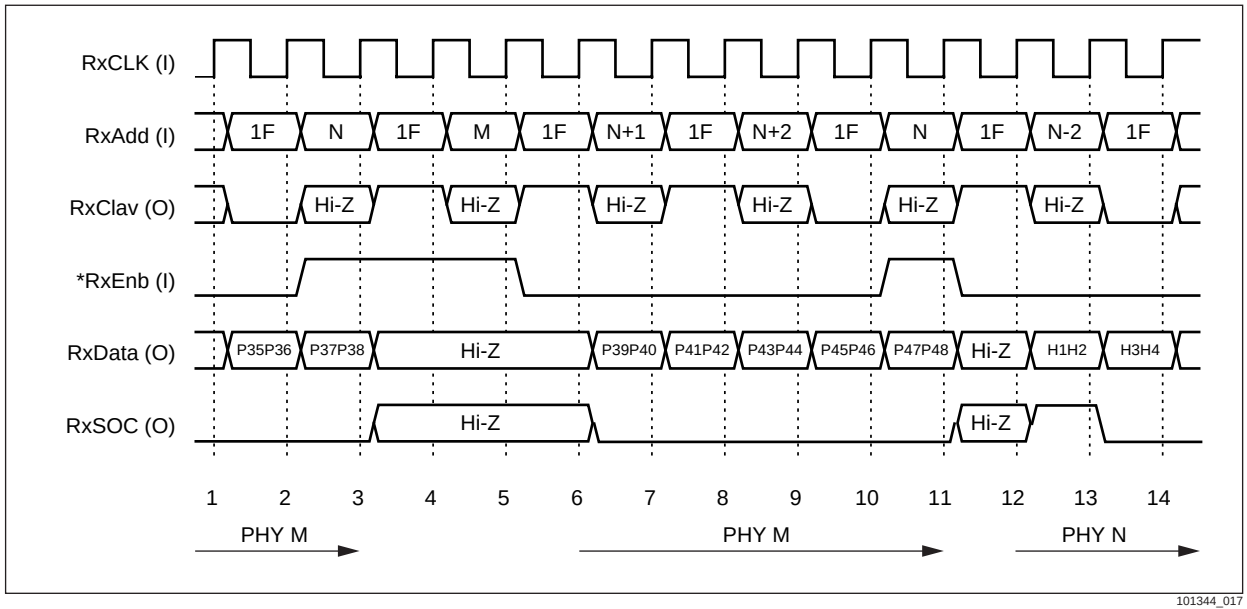
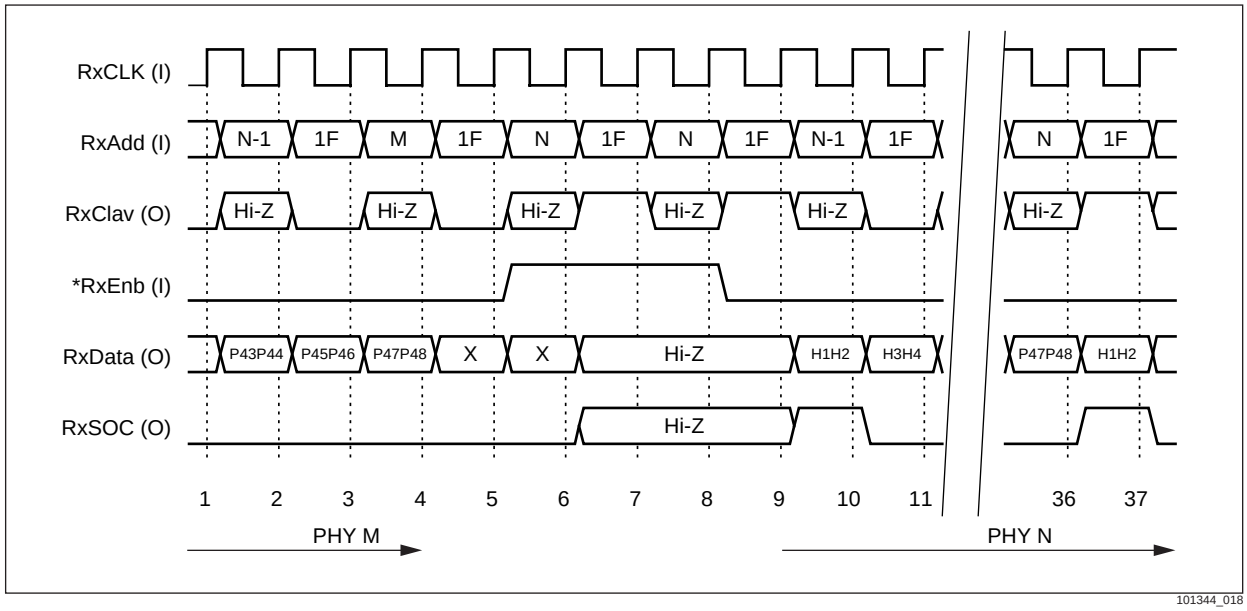


Figure 7-2. Receive One Rx/Tx CLAV Functional Timing

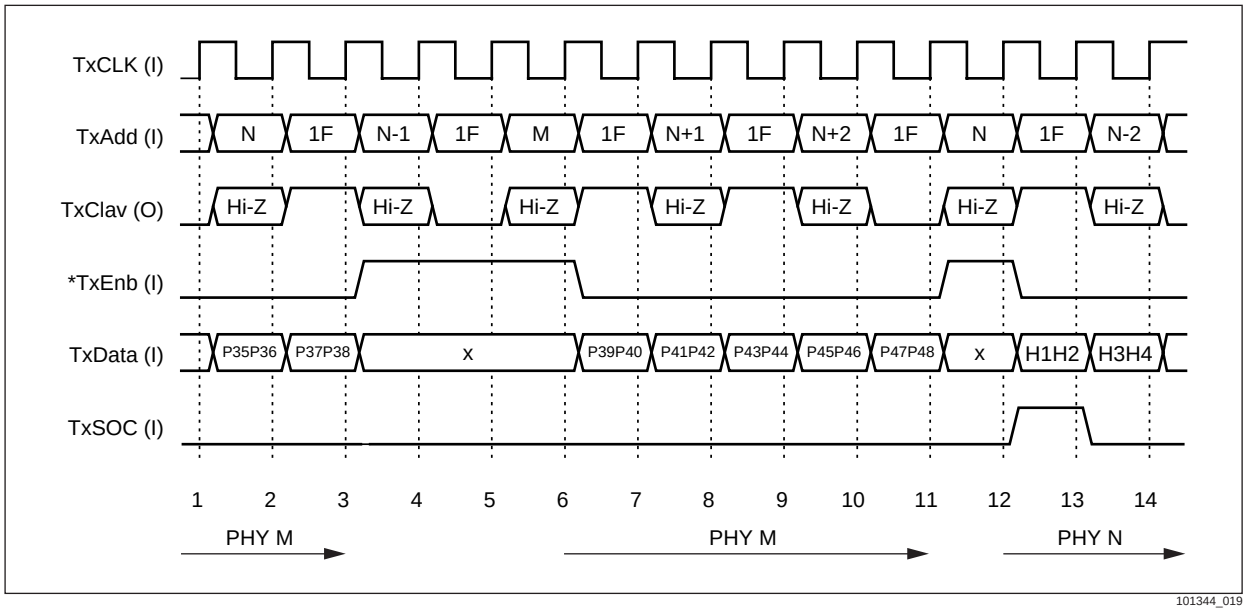


7.1.1.2 Transmit

Figure 7-3 illustrates the functional timing of one TxClav mode of operation.

TxClav indicates whether the PHY port, whose address was on TxAdd in the previous clock cycle, can accept a complete cell. The ATM layer selects a PHY port which receives the next cell by placing its address on RxAdd when *TxEnb is not asserted and asserting *TxEnb on the next cycle.

Figure 7-3. Transmit One Rx/Tx CLAV Functional Timing



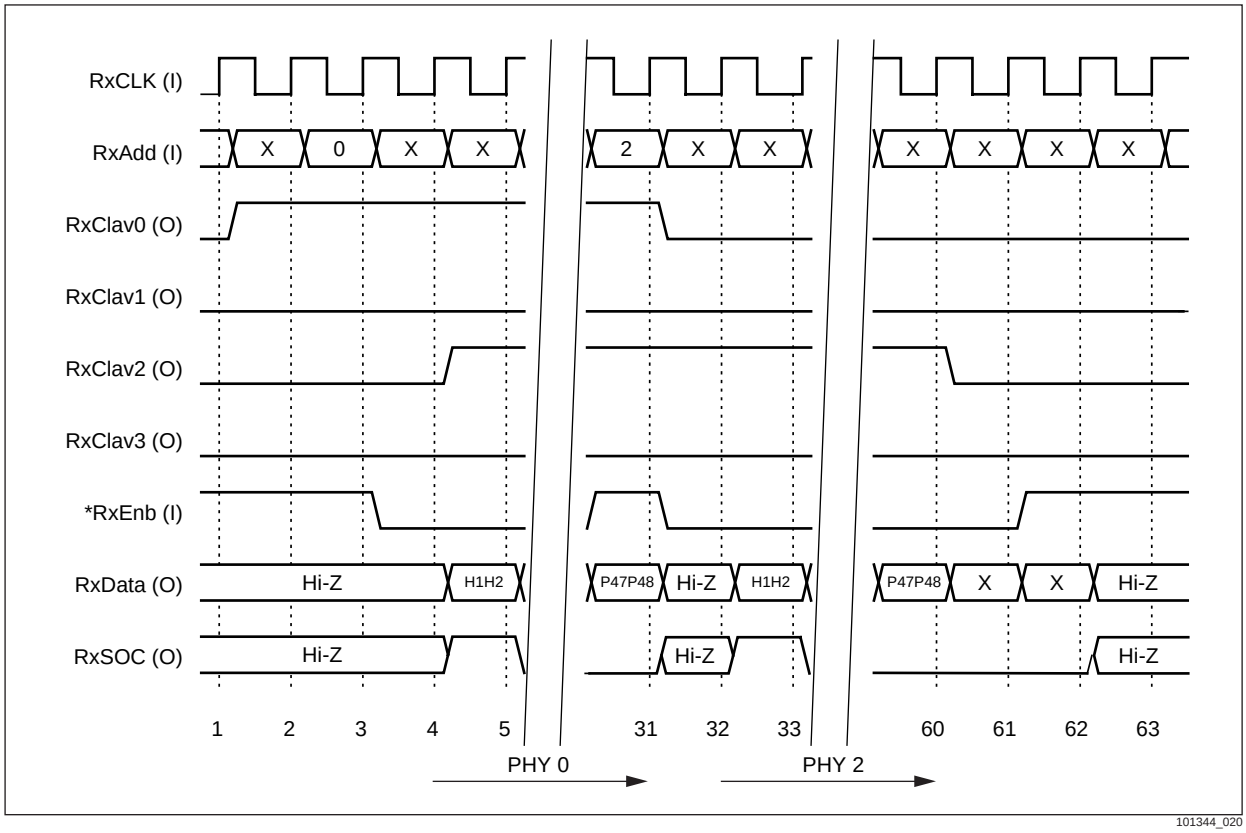
7.1.2 Direct Status Indication

7.1.2.1 Receive

Figure 7-4 illustrates the functional timing of the Direct Status Indication mode of operation.

RxClav0–RxClav3 indicate continuously whether the PHY ports have a complete cell available. The ATM layer selects a PHY port from which to receive the next cell by placing its address on RxAdd when *RxEnb is not asserted and asserting *RxEnb on the next cycle.

Figure 7-4. Receive Direct Status Indication Functional Timing

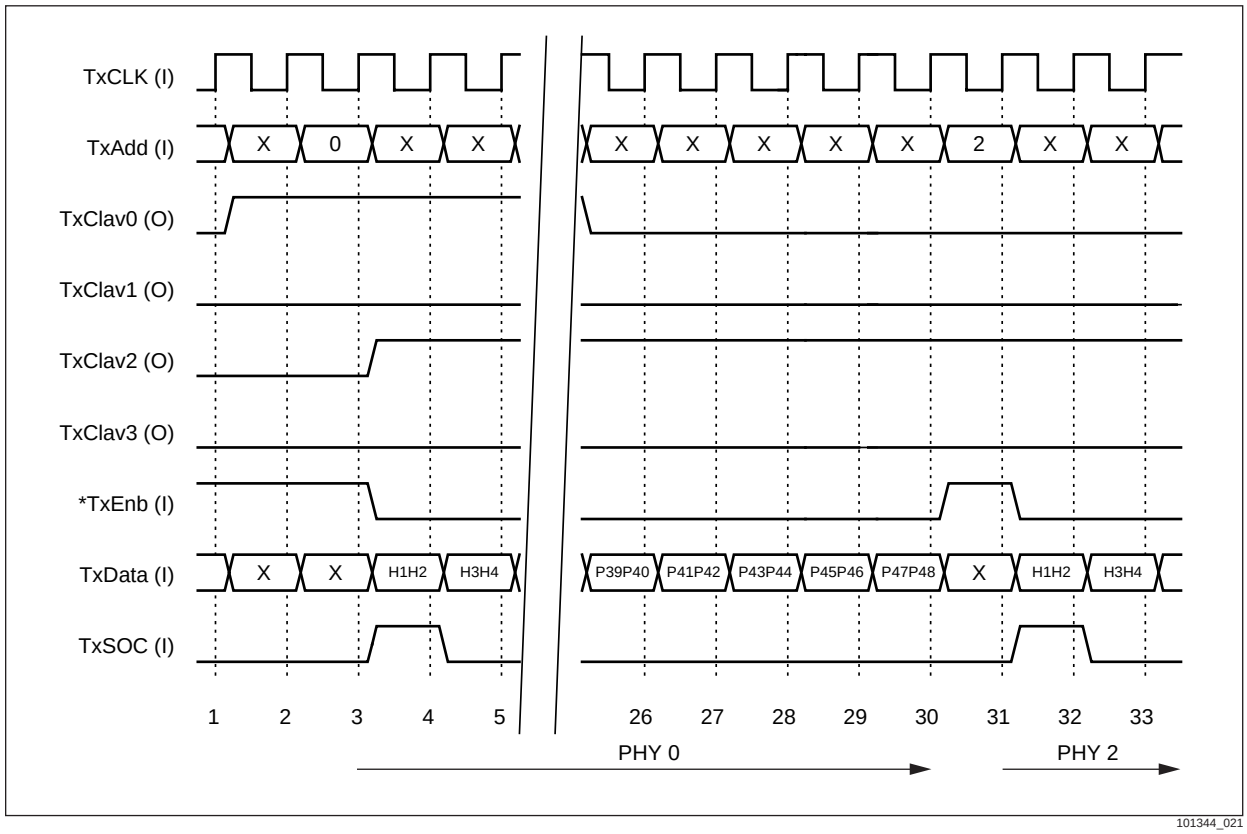


7.1.2.2 Transmit

Figure 7-5 illustrates functional timing of Direct Status Indication mode of operation.

TxClav0–TxClav3 indicates continuously whether the PHY ports can accept a complete cell. The ATM layer selects a PHY port which will get the next cell by placing its address on RxAdd when *TxEnb is not asserted and asserting *TxEnb on the next cycle.

Figure 7-5. Transmit Direct Status Indication Functional Timing



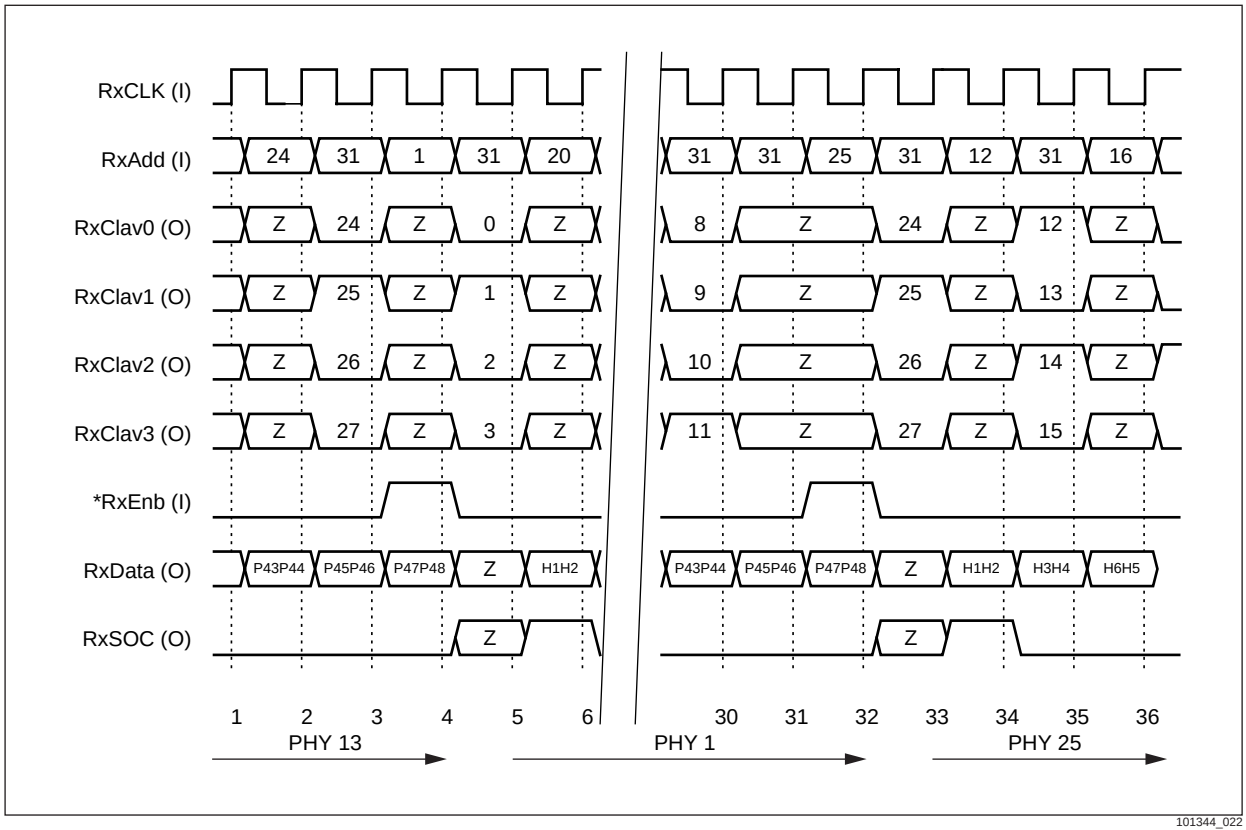
7.1.3 Multiplexed Status Polling

7.1.3.1 Receive

Figure 7-6 illustrates functional timing of Multiplexed Status Polling mode.

RxClav0–RxClav3 indicate whether the PHY ports, which belong to the address group of the address that was on RxAdd in the previous clock cycle, have a complete cell available. The ATM layer selects a PHY port from which to receive the next cell by placing its address on RxAdd when *RxEnb is not asserted, and by asserting *RxEnb on the next cycle.

Figure 7-6. Receive Multiplexed Status Polling Functional Timing

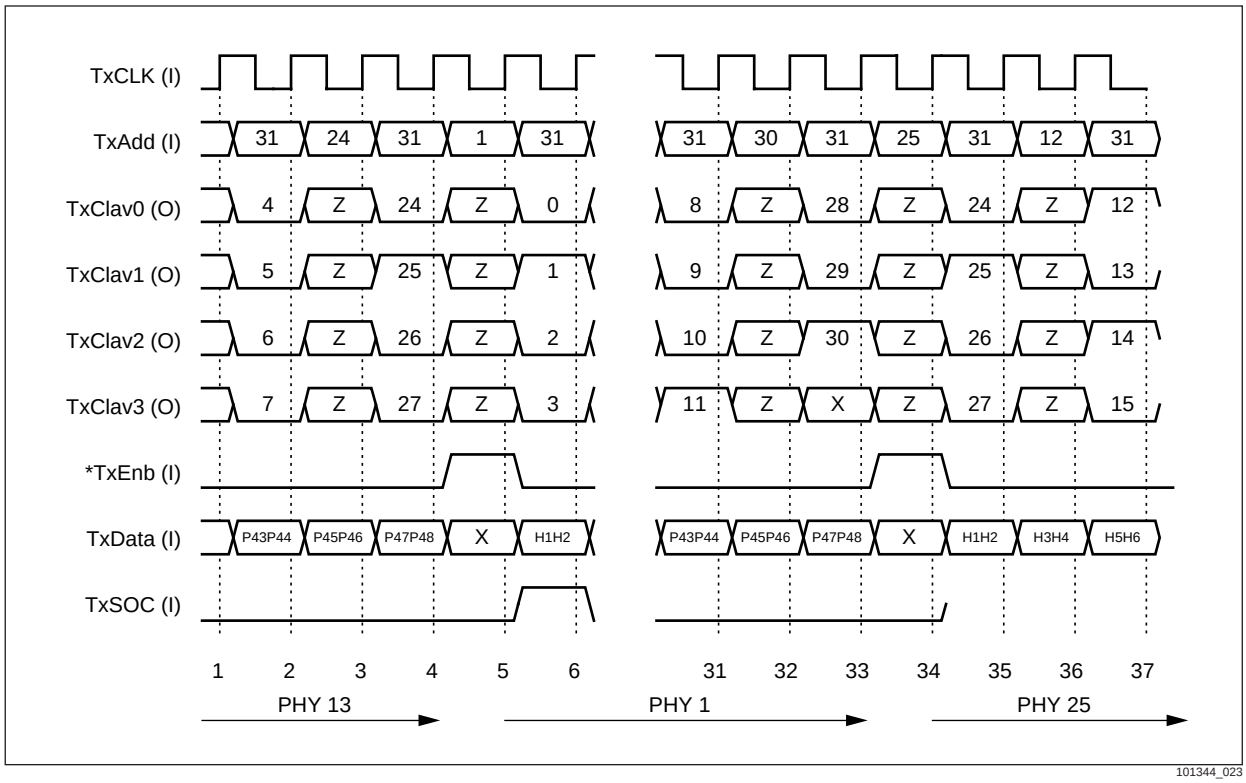


7.1.3.2 Transmit

Figure 7-7 illustrates functional timing of Multiplexed Status Polling Mode.

RxClav0–RxClav3 indicate whether the PHY ports, which belong to the address group of the address that was on RxAdd in the previous clock cycle, can accept a complete cell. The ATM layer selects the PHY port which will get the next cell by placing its address on RxAdd when *TxEnb is not asserted and asserting *TxEnb on the next cycle.

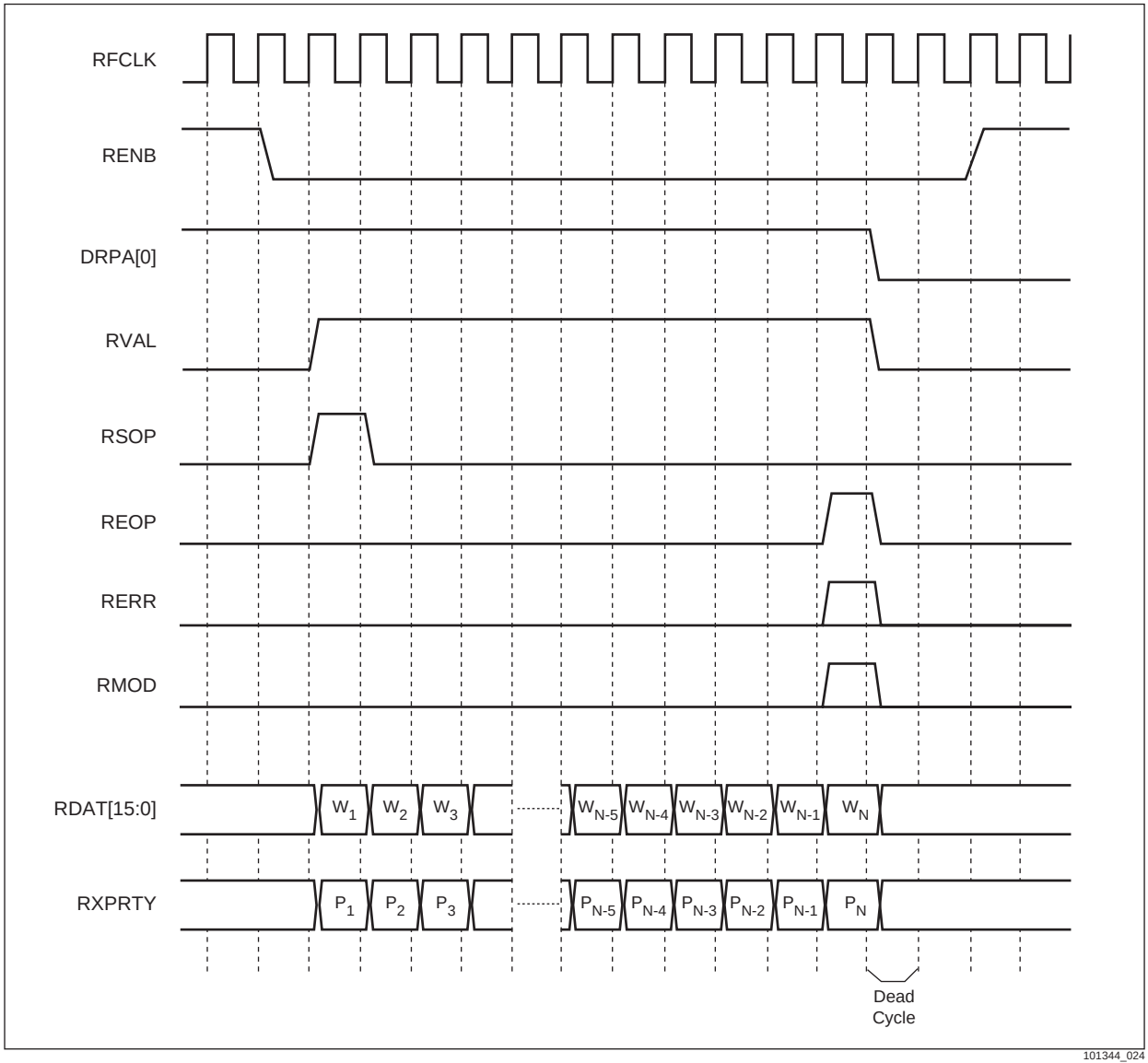
Figure 7-7. Transmit Multiplexed Status Polling Functional Timing



7.1.4 Receive Link Layer Interface (POS Mode)

Figure 7-8 illustrates the functional timing of receive cycles from a single PHY. The DRPA pin provides the indication of the last word of a valid packet on the Rx data bus.

Figure 7-8. Rx Single PHY Functional Timing



The RMOD, RSOP, REOP, and RERR are valid during the period when RVAL is high (and *RxENB is active (low) prior to the rising of RVAL). The PHY ignores any additional reads while the RVAL is deasserted. A dead cycle occurs after the RVAL pin is deasserted. When a read cycle is attempted while the RVAL is low, the data on the data bus is not valid (dead cycle) and the link layer should deassert the RENB pin after that dead cycle.

7.1.5 Multiport, Hot Selection Mode

Figure 7-9. Multiport, Hot Selection Mode, Functional Timing

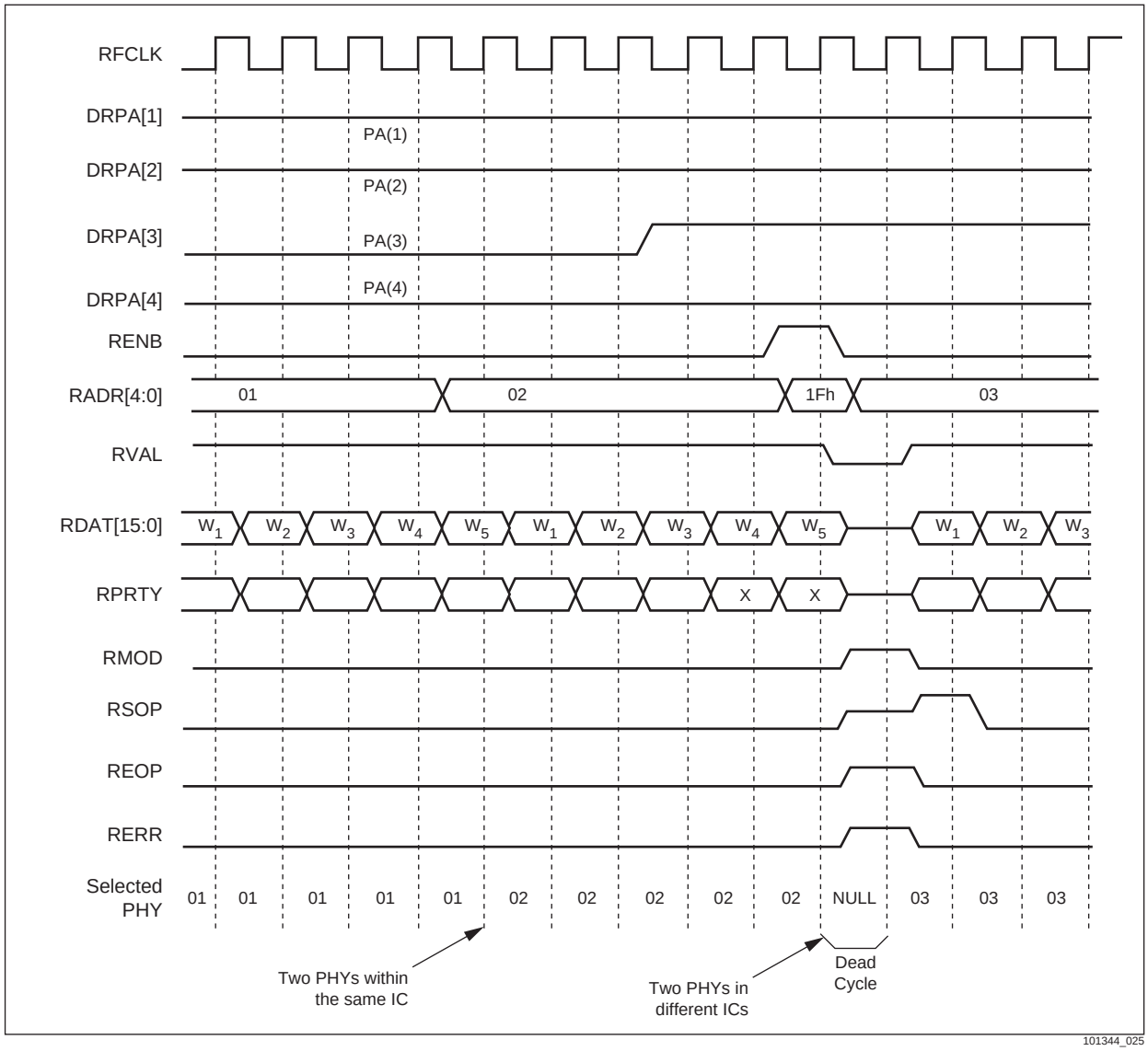


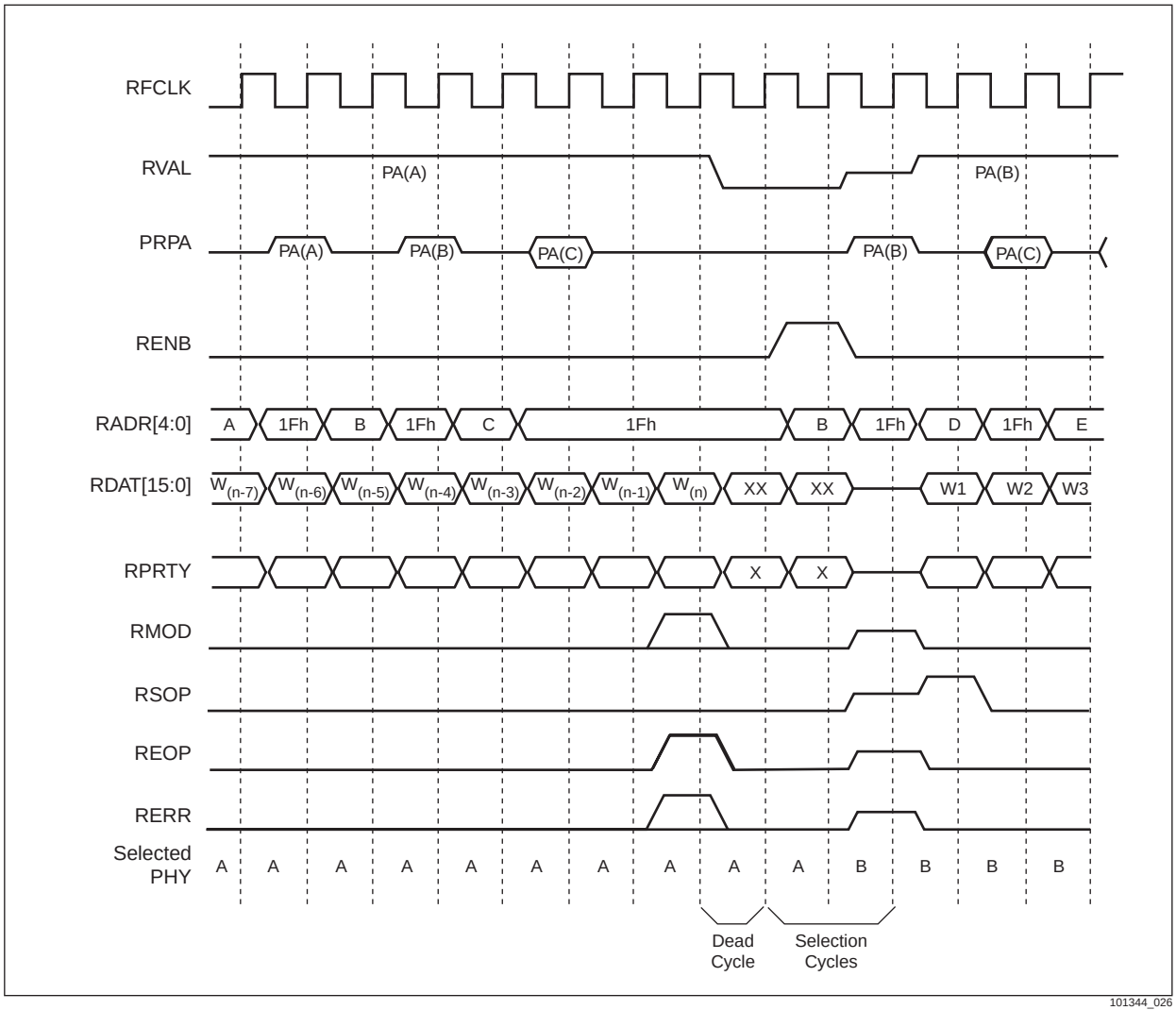
Figure 7-9 illustrates the hot selection of a multiport device. Direct Status indication is obtained by the DRPA pins. This example presents four ports with each pair packed in the same IC device (Ports 1 and 2 in the same IC and Ports 3 and 4 in the same IC).

NOTE: The transition between the selection of Port 1 and Port 2 is done without a dead cycle (no deassertion of the RENB pin is required). A transition between two ports of different devices, however, requires the deassertion of the RENB pin and thus causes a dead cycle.

7.1.6 Rx Multiport, Normal Selection Mode

Figure 7-10 illustrates an example of the polling and selection procedures.

Figure 7-10. Rx Multiport, Normal Selection Mode, Functional Timing

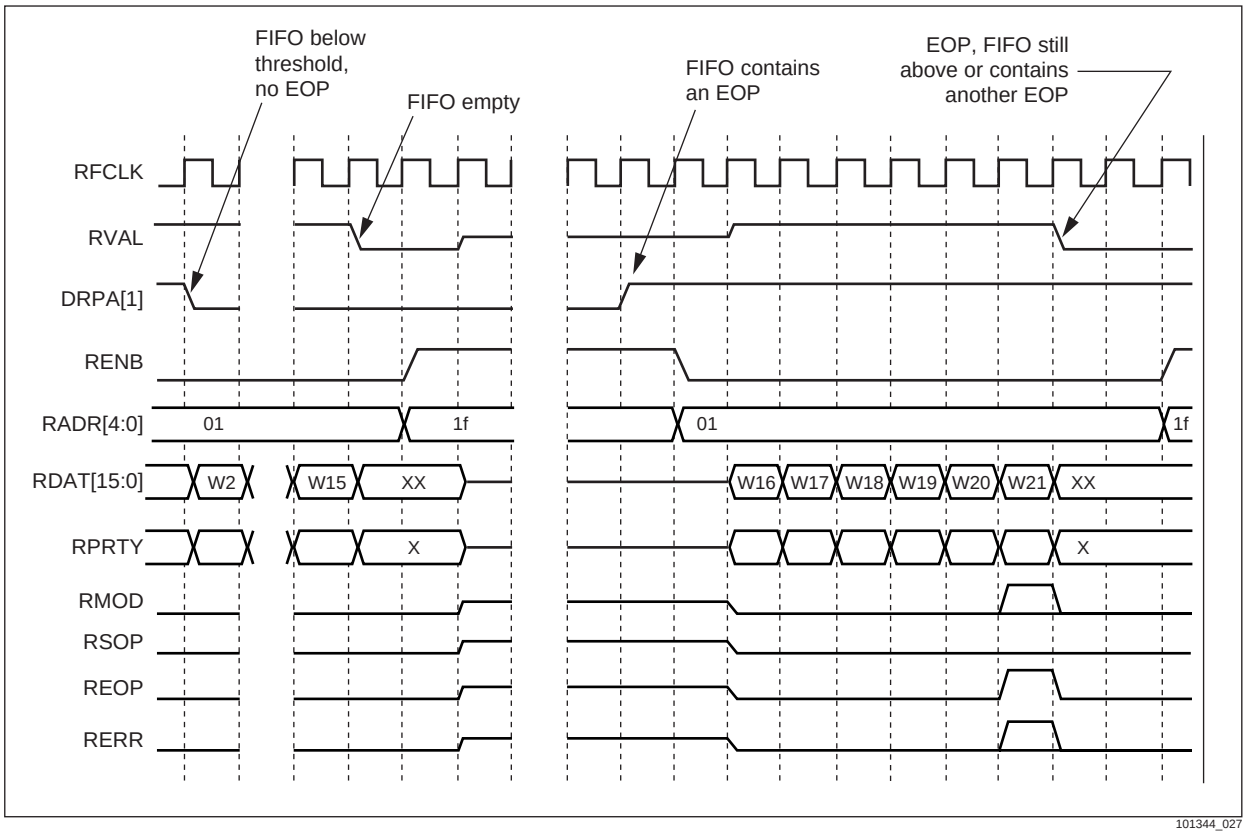


The ports that are mapped to addresses A and B flag that a packet is available in the FIFOs. Then Port B is selected (the RENB pin is asserted). When data is transferred from one port, other ports may be polled for available packets.

7.1.7 RVAL and RPA Functionality

Figure 7-11 illustrates RPA and RVAL functionality while functioning in Hot Selection mode.

Figure 7-11. RVAL and RPA Functionality in Hot Selection Mode



In the first transfer, the DRPA[1] pin is deasserted to reflect the fact that the amount of data in the Rx FIFO is below the threshold. The RVAL pin remains asserted, indicating that valid data still exists and is being transferred. When the RVAL is deasserted, the FIFO is empty. The link layer should then deassert the RENB pin.

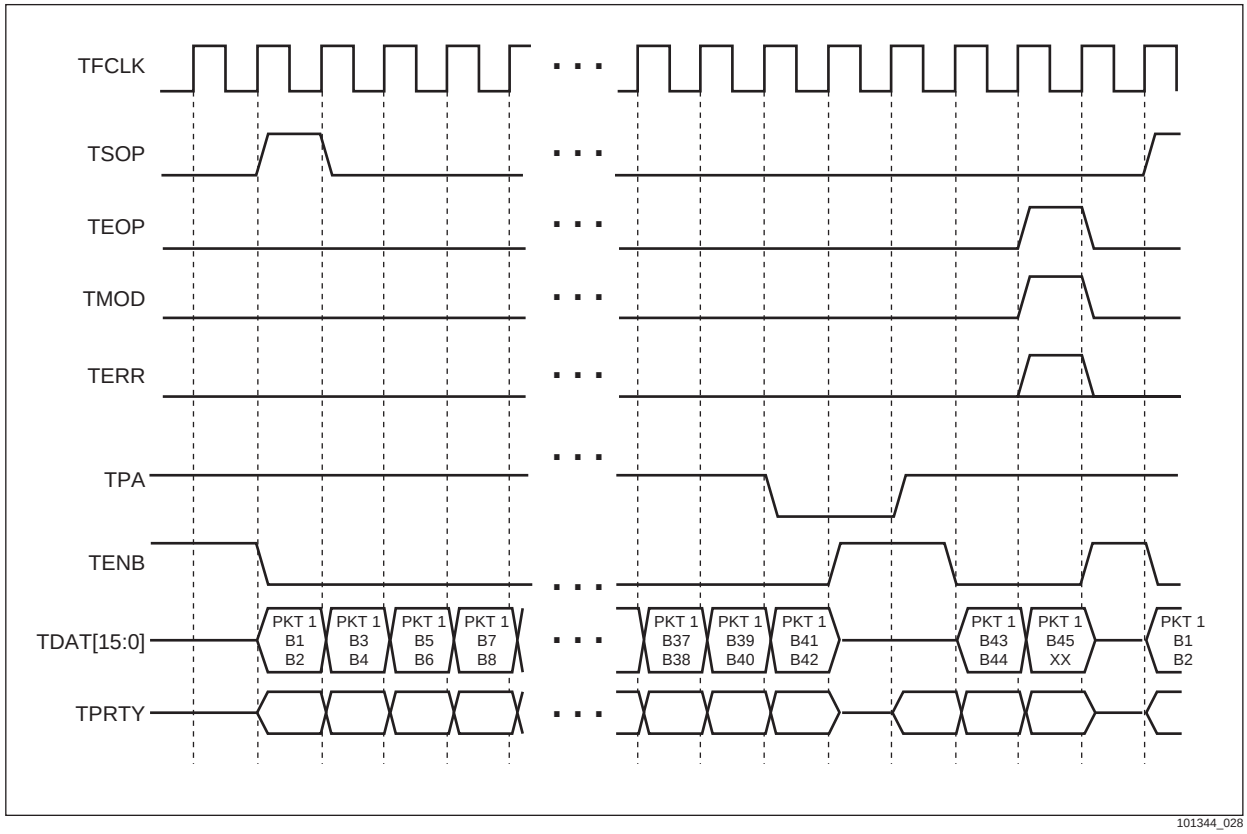
In the lower part of Figure 7-11, another read process starts (DRPA[1] is asserted due the existence of [EOP] in the FIFO). In this case, the FIFO continues to be filled the data of the next packet after the EOP of the current packet enters the FIFO.

When reading the FIFO at the EOP, the RVAL pin is deasserted. When this occurs, no data is transferred from the port. At that point, the link layer may deselect and reselect the same port, and reinitiate the transfer of a new packet.

7.1.8 Transmit

The previous timing diagrams refer to the receive side of the POS interface; however, the same timing diagram (with the exception of the RVAL signal) is valid for the transmit side. The assertion and deassertion of the available free bytes in the FIFO act in the same manner as the available bytes to be read in the receive side.

Figure 7-12. Tx Single Port, Functional Timing

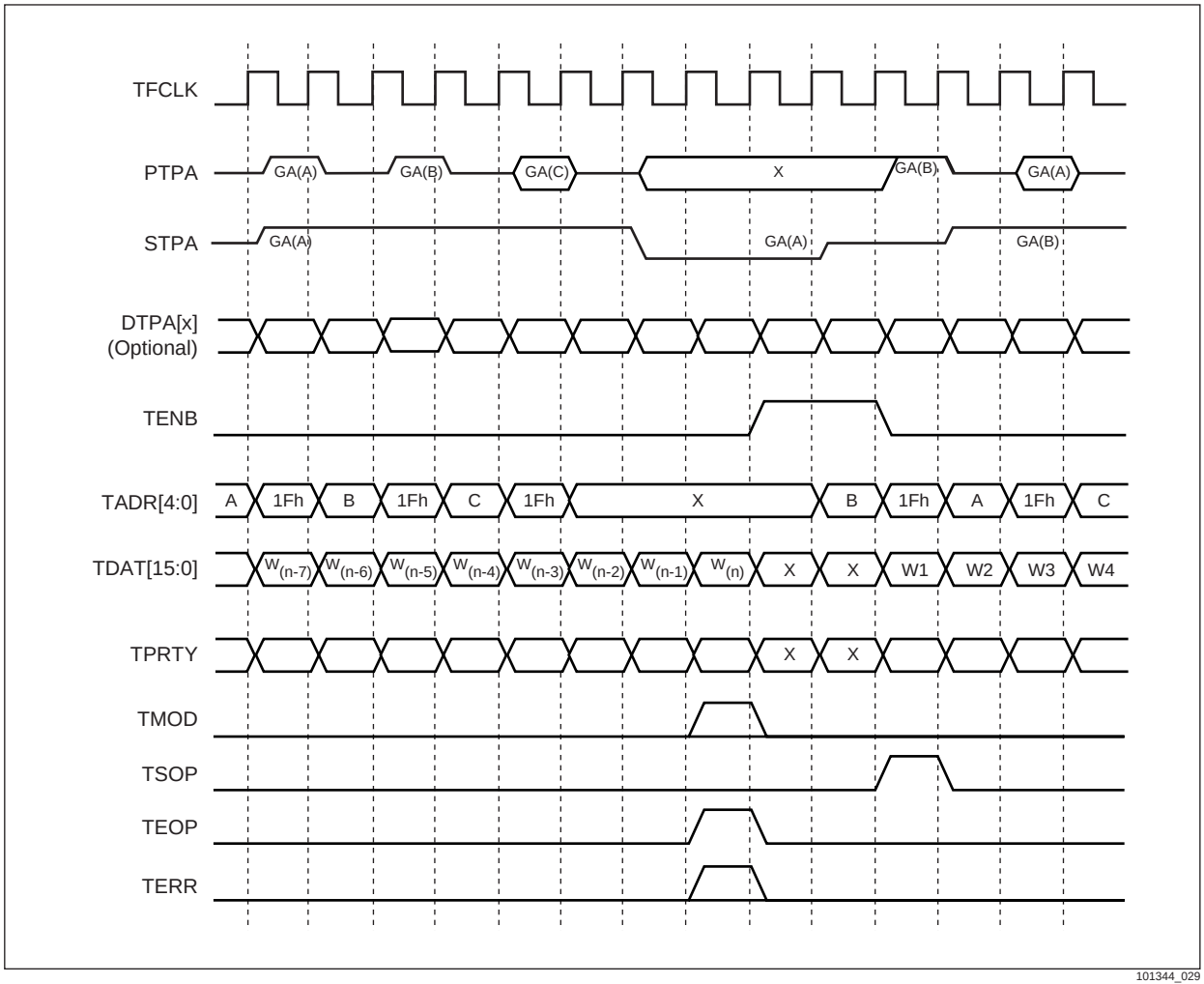


The TPA assertion indicates that the FIFO is ready to have data written to it. When the number of bytes in the FIFO exceeds the predefined number (by the register Tx FHL in 32-bit granularity), the TPA pin is deasserted. Then the TENB pin should be asserted. During the transfer of the first word of the packet, the TSOP must be asserted. The TEOP must be asserted during the writing to the FIFO of the last word of a packet. When an SOP is encountered without the assertion of EOP at the previous transfer, the new packet is handled and the previous one is marked with an error and aborted.

7.1.9 Tx Multiport, Normal Mode Operation

Figure 7-13 illustrates the functional timing of the transmit side when operating with a multiport device.

Figure 7-13. Tx Multiport, Normal Mode Functional Timing



In this example, the port which is mapped to Address A (its status is obtained by the DTPA[0] pin) is busy and cannot accept any additional data. The port that is mapped to Address B is free to accept data. Port B is then selected and the data is transferred to it. The STPA pin can be used to obtain the selected port status to halt the data transfer when the FIFO is filled up.

8.0 Alarms Status Serial Interface (ASSI)

Figure 8-1 illustrates the ASSI functional timing.

Figure 8-1. ASSI Functional Timing

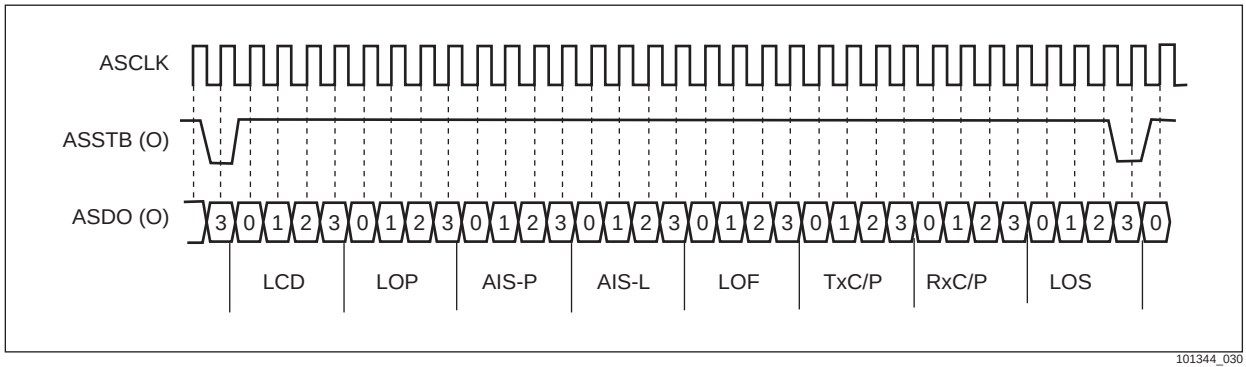


Table 8-1. ASSI AC Parameters

Symbol	Parameter	Min	Max	Units
ASClk	Frequency	—	20	MHz

9.0 Data Communication Channel Port (DCC)

Figures 9-1, 9-2, 9-3, and 9-4 illustrate the timing diagrams of the DCC. The Section DCC port is functioning with a 216 kHz clock (50% duty cycle), which is active to part of the frame, to generate a nominal clock of 192 kHz. The Line DCC port is functioning with a 648 kHz clock (50% duty cycle), which is active to part of the frame, to generate a nominal clock of 576 kHz clock.

Figure 9-1. Rx Section Data Communication Channel

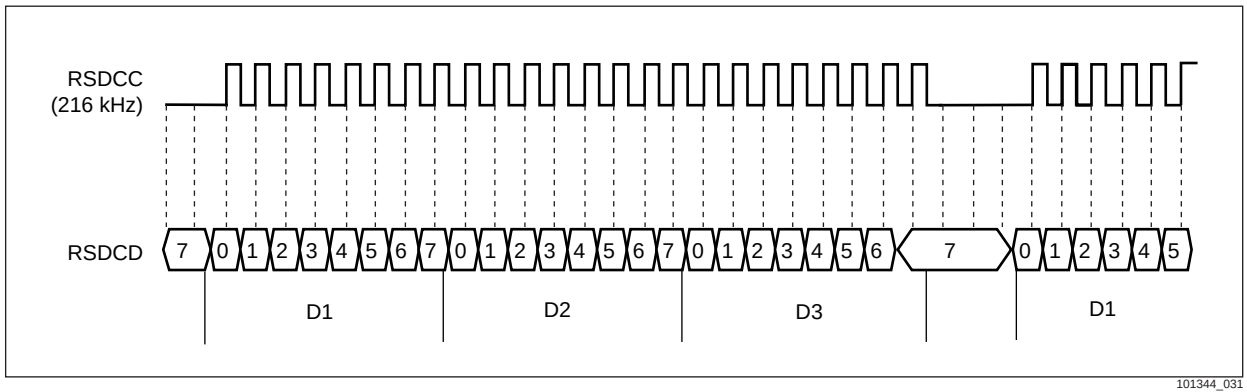


Figure 9-2. Tx Section Data Communication Channel

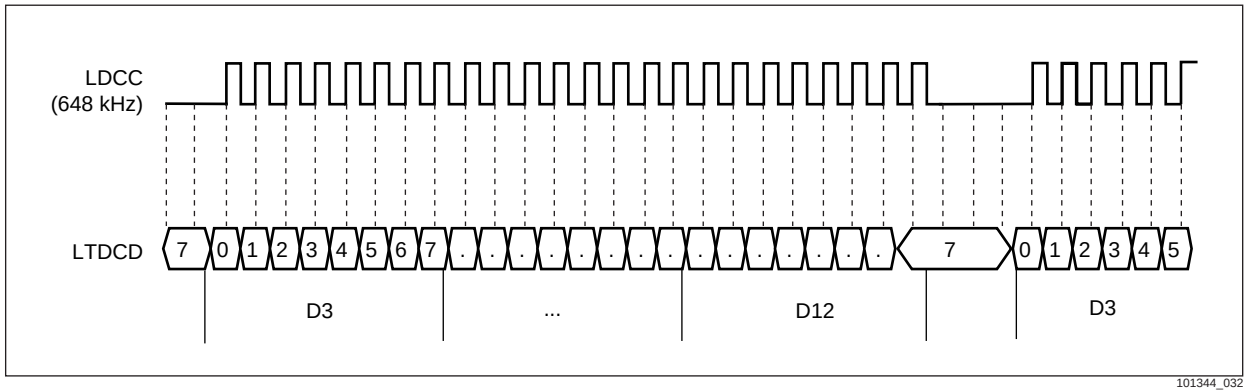


Figure 9-3. Rx Line Data Communication Channel

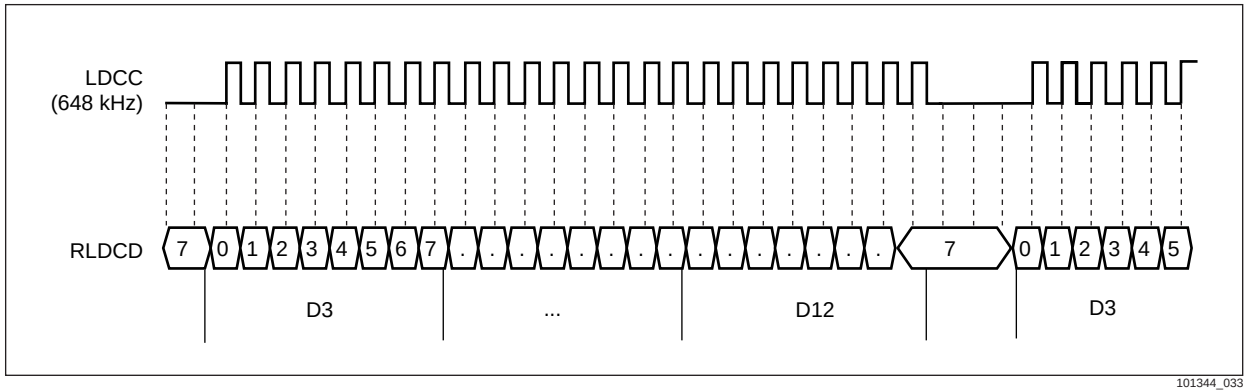
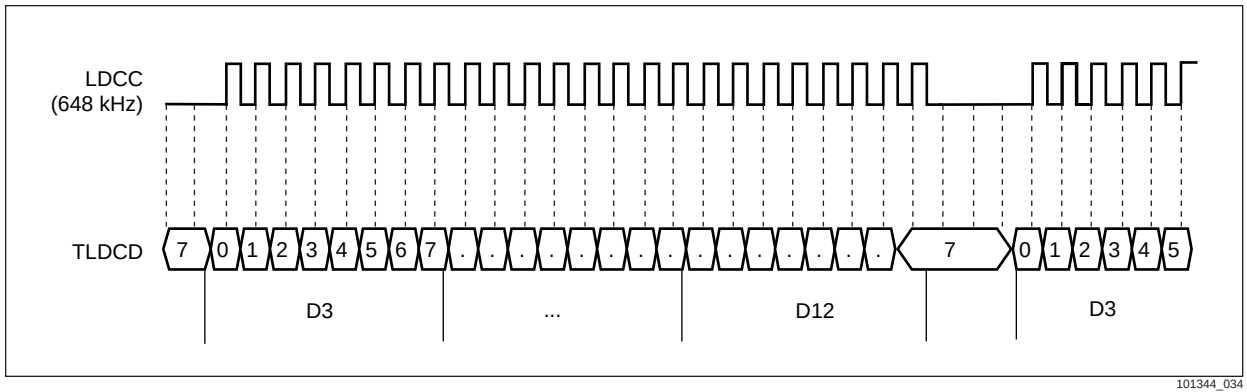


Figure 9-4. Tx Line Data Communication Channel



10.0 AC Characteristics

10.1 Microprocessor Interface

Figure 10-1. Microprocessor Write Cycle AC Timing

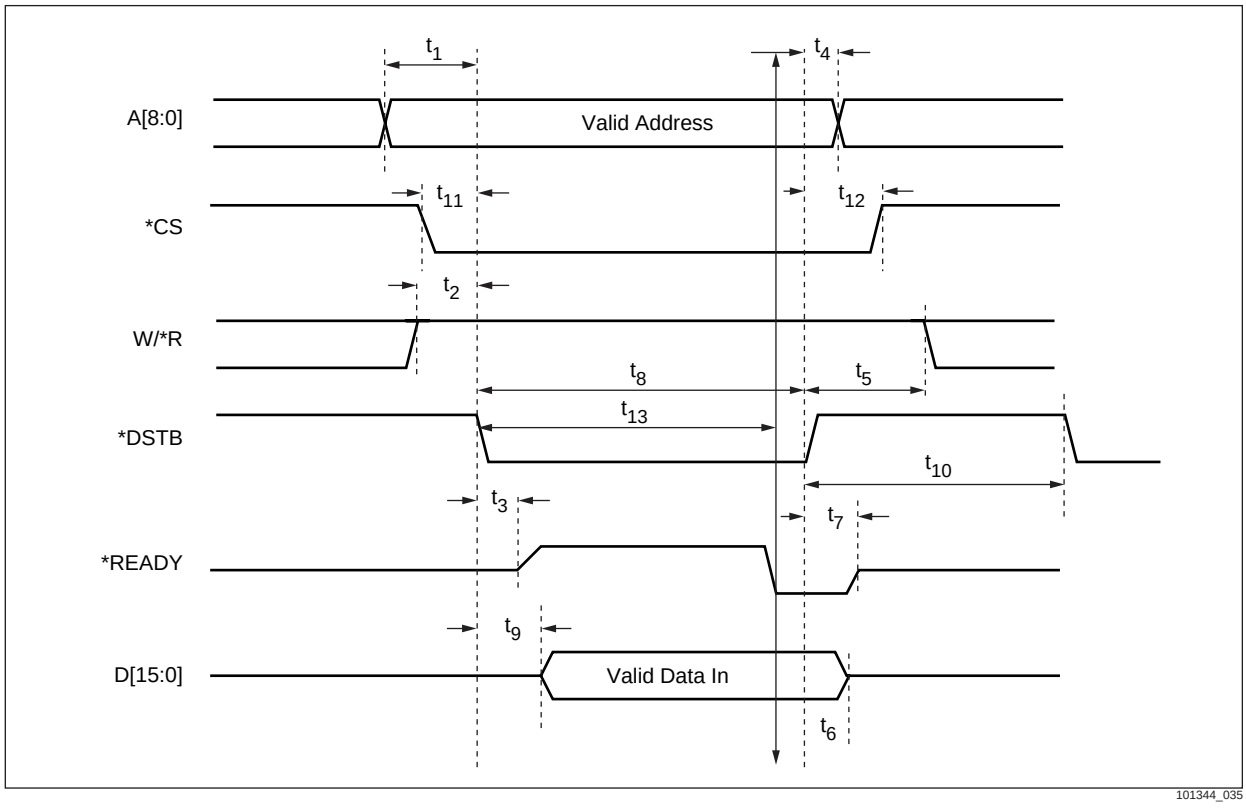


Figure 10-2. Microprocessor Read Cycle AC Timing

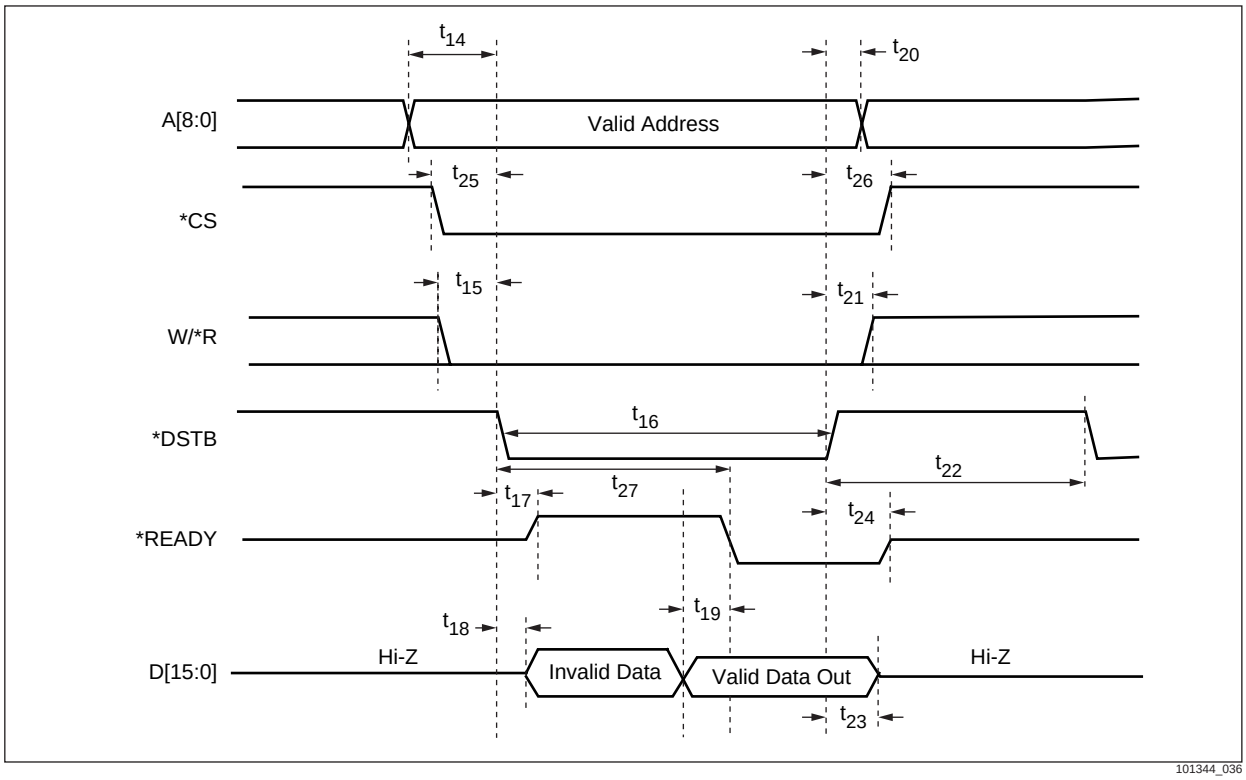


Table 10-1. Microprocessor Write/Read Cycle AC Parameters (1 of 2)

Subject	Symbol	Parameter	Min.	Max.	Units
WRITE CYCLE	t1	Address bus setup time before *DSTB active	10	—	ns
—	t2	W/*R changes to 1 before *DSTB active	5	—	ns
—	t3	*READY valid after *DSTB active	—	15	ns
—	t4	Address bus hold time after *DSTB inactive	0	—	ns
—	t5	W/*R changes to 0 before *DSTB inactive	0	—	ns
—	t6	Data bus hold time after *DSTB inactive	0	—	ns
—	t7	*READY high-Z to after DSTB inactive	—	10	ns
—	t8	*DSTB minimum negative pulse width	TBD	—	ns
—	t9	Data bus valid after *DSTB active	—	15	ns
—	t10	*DSTB recovery time	TBD	—	ns
—	t11	*CS changes to 0 before *DSTB active	0	—	ns
—	t12	*CS changes to 1 after *DSTB inactive	0	—	ns
—	t13	*READY active after *DSTB active	—	310	ns
READ CYCLE	t14	Address bus setup time before *DSTB active	10	—	ns

Table 10-1. Microprocessor Write/Read Cycle AC Parameters (2 of 2)

Subject	Symbol	Parameter	Min.	Max.	Units
—	t15	W/*R changes to 0 before *DSTB active	5	—	ns
—	t16	*DSTRB minimum negative pulse width	TBD	—	ns
—	t17	*READY valid after *DSTB active	—	15	ns
—	t18	Data bus delay from Hi-Z until invalid data out	0	—	ns
—	t19	Valid data out delay from *READY active	0	—	ns
—	t20	Address bus hold time after *DSTB inactive	0	—	ns
—	t21	W/*R changes to 1 before *DSTB inactive	0	—	ns
—	t22	*DSTB recovery time	TBD	—	ns
—	t23	Data bus hold time after *DSTB inactive	0	15	ns
—	t24	*READY high-Z after DSTB inactive	0	—	ns
—	t25	*CS changes to 0 before *DSTB active	0	—	ns
—	t26	*CS changes to 1 after *DSTB inactive	0	—	ns
—	t27	*READY active after *DSTRB active	—	TBD	ns

10.2 UTOPIA Interface

Figure 10-3. UTOPIA Transmit Direction AC Timing

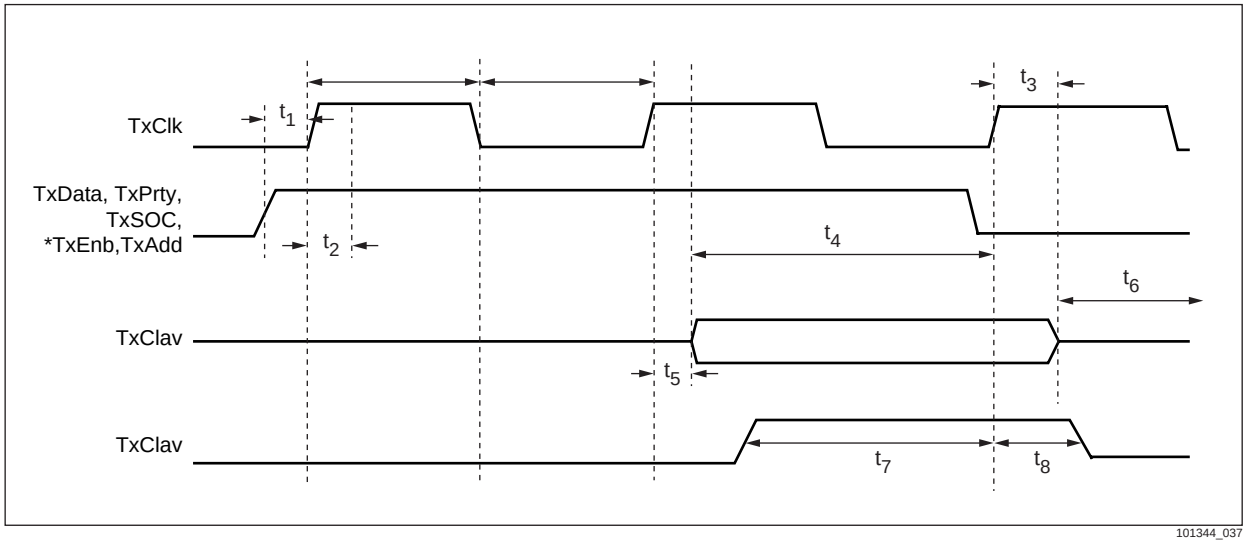


Figure 10-4. UTOPIA Receive Direction AC Timing

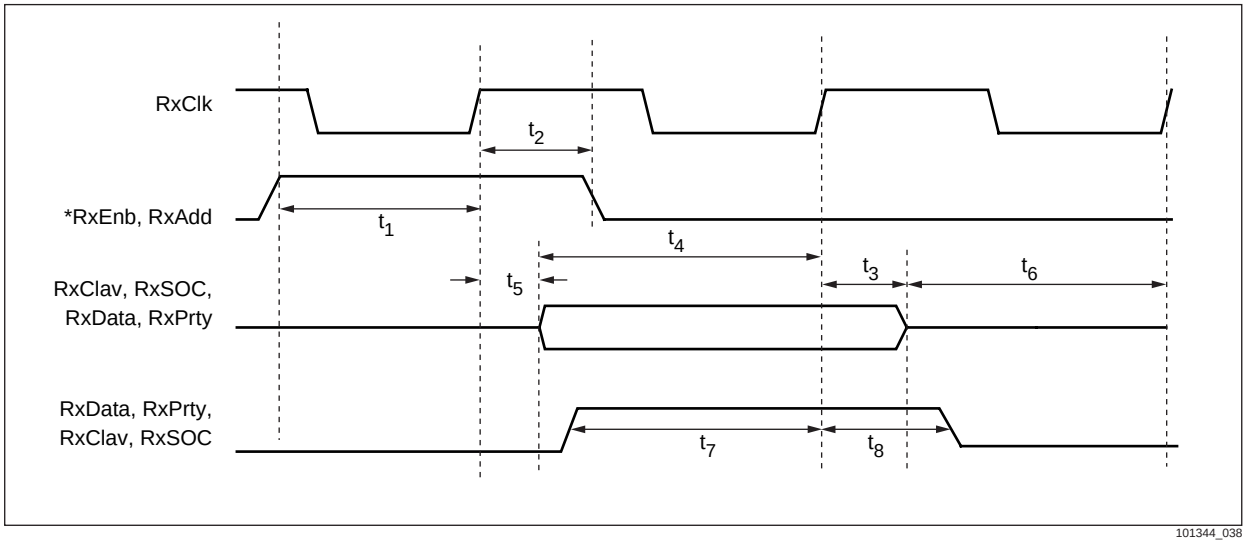


Table 10-2. UTOPIA Transmit/Receive AC Parameters

Subject	Symbol	Parameter	Min.	Max.	Units
Transmit Direction	TxClk	Frequency	20	50	MHz
—	—	Duty cycle	40	60	%
—	—	TxClk rise/fall time	—	2	ns
—	—	Peak-to-peak jitter	—	3	%
—	t1	Input setup to TxClk	4	—	ns
—	t2	Input hold from TxClk	1	—	ns
—	t3	Signal going high impedance from TxClk	1	—	ns
—	t4	Signal going low impedance to TxClk	4	—	ns
—	t5	Signal going low impedance from TxClk	1	—	ns
—	t6	Signal going high impedance to TxClk	0	—	ns
—	t7	Output setup to TxClk	4	—	ns
—	t8	Output hold from TxClk	1	—	ns
Receive Direction	RxClk	Frequency	0	50	MHz
—	—	Duty cycle	40	60	%
—	—	RxClk rise/fall time	—	2	ns
—	—	Peak-to-peak jitter	—	3	%
—	t1	Input setup to RxClk	4	—	ns
—	t2	Input hold from RxClk	1	—	ns
—	t3	Signal going high impedance from RxClk	1	—	ns
—	t4	Signal going low impedance to RxClk	4	—	ns
—	t5	Signal going low impedance from RxClk	1	—	ns
—	t6	Signal going high impedance to RxClk	0	—	ns
—	t7	Output setup to TxClk	4	—	ns
—	t8	Output hold from TxClk	1	—	ns

10.3 POS Interface

10.3.1 Rx AC Timing

Figure 10-5 illustrates the AC timing of the Receive POS interface and its characteristics.

Figure 10-5. POS Interface, AC Characteristics (Receive Path)

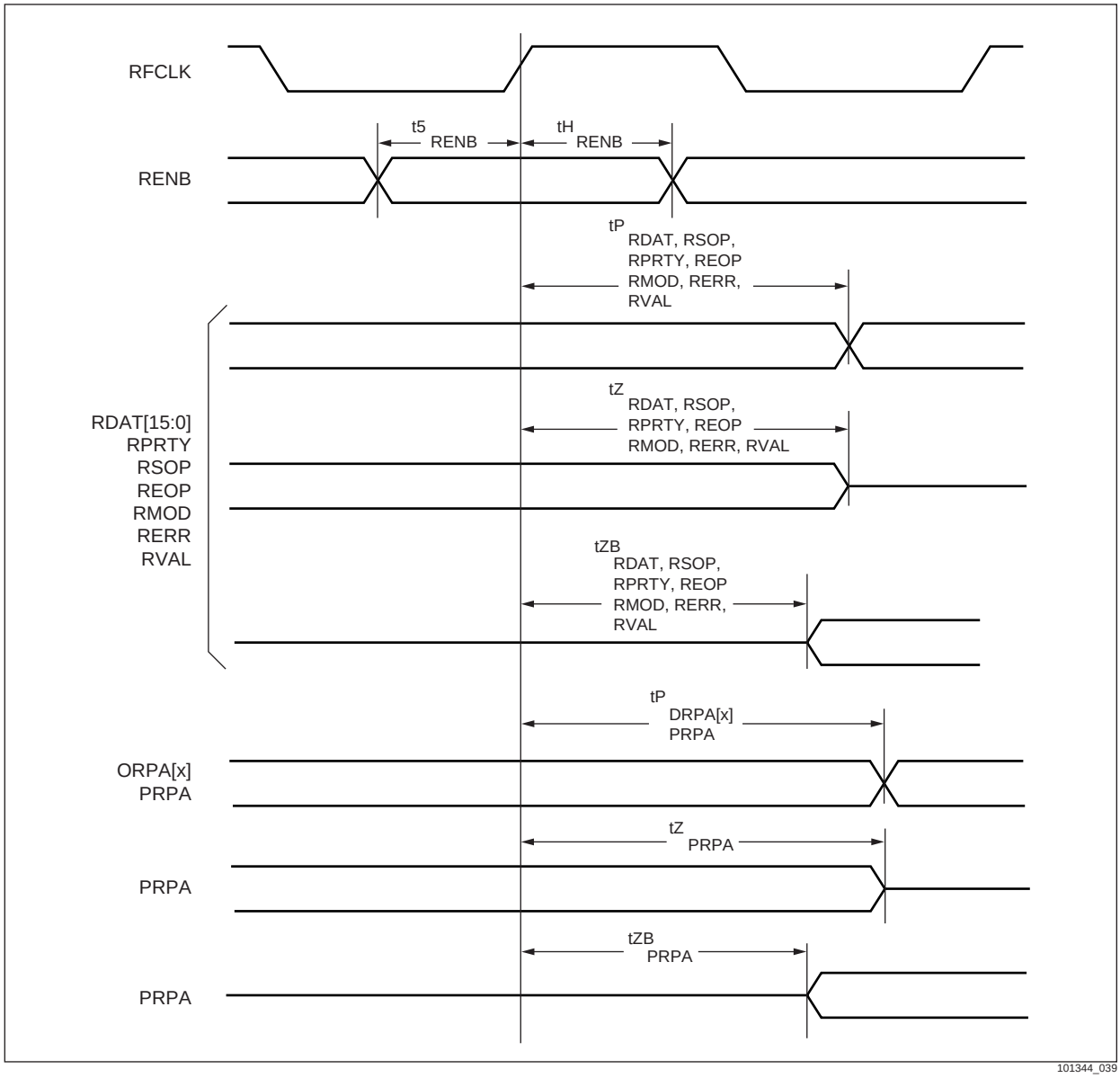


Table 10-3. POS Interface Receive AC Parameters

Symbol	Description	Min	Max	Units
—	RxClk Frequency	25	50	MHz
—	RxClk Duty Cycle	40	60	%
tS_{RxEnb}	RxEnb Set-up time to RxClk	4	—	ns
tH_{RxEnb}	RxEnb Hold Time to RxClk	0	—	ns
tS_{RxAdd}	RxAdd[4:0] Set-up Time to RxClk	4	—	ns
tH_{RxAdd}	RxAdd[4:0] Hold Time to RxClk	0	—	ns
tP_{RxData}	RxClk High to RxData Valid	1	12	ns
tZ_{RxData}	RxClk High to RxData High-Z	1	12	ns
tZB_{RxData}	RxClk High to RxData Driven	0	—	ns
tP_{RxPrty}	RxClk High to RxPrty Valid	1	12	ns
tZ_{RxPrty}	RxClk High to RxPrty High-Z	1	12	ns
tZB_{RxPrty}	RxClk High to RxPrty Driven	0	—	ns
tP_{RxSOP}	RxClk High to RxSOP Valid	1	12	ns
tZ_{RxSOP}	RxClk High to RxSOP High-Z	1	12	ns
tZB_{RxSOP}	RxClk High to RxSOP Driven	0	—	ns
tP_{RxEOP}	RxClk High to RxEOP Valid	1	12	ns
tZ_{RxEOP}	RxClk High to RxEOP High-Z	1	12	ns
tZB_{RxEOP}	RxClk High to RxEOP Driven	0	—	ns
tP_{RxMOD}	RxClk High to RxMOD Valid	1	12	ns
tZ_{RxMOD}	RxClk High to RxMOD High-Z	1	12	ns
tZB_{RxMOD}	RxClk High to RxMOD Driven	0	—	ns
tP_{RxERR}	RxClk High to RxERR Valid	1	12	ns
tZ_{RxERR}	RxClk High to RxERR High-Z	1	12	ns
tZB_{RxERR}	RxClk High to RxERR Driven	0	—	ns
tP_{RVAL}	RxClk High to RVAL Valid	1	12	ns
tZ_{RVAL}	RxClk High to RVAL High-Z	1	12	ns
tZB_{RVAL}	RxClk High to RVAL Driven	0	—	ns
tP_{PRPA}	RxClk High to PRPA Valid	1	12	ns
tZ_{PRPA}	RxClk High to PRPA High-Z	1	12	ns
tzb_{PRPA}	RxClk High to PRPA Driven	0	—	ns
tP_{DRPA}	RxClk High to DRPA[3:0] Valid	1	12	ns

10.3.2 Tx AC Timing

Figure 10-6 illustrates the AC timing and characteristics of the Transmit POS interface.

Figure 10-6. POS Interface, AC Characteristics (Transmit Path)

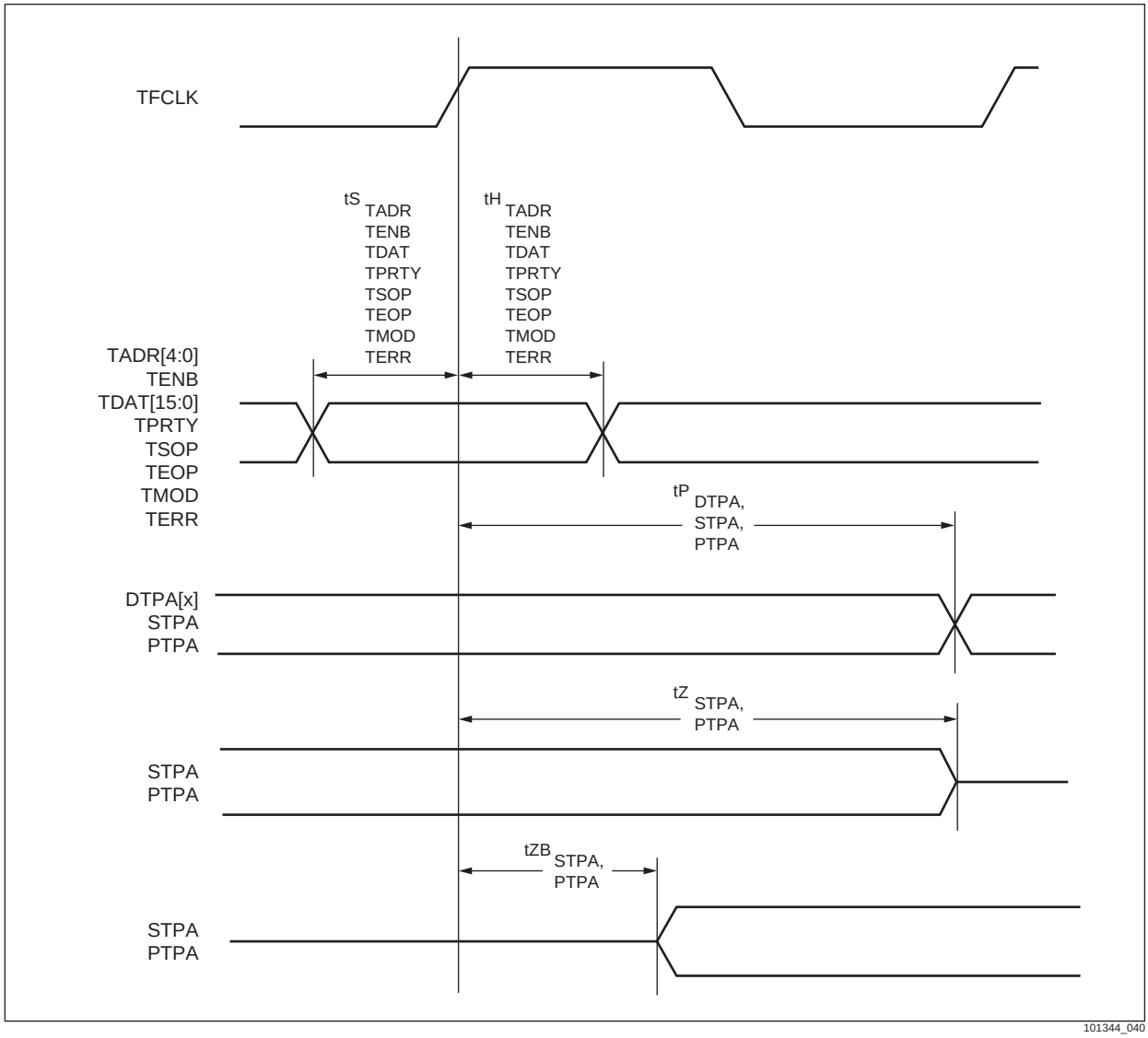


Table 10-4. POS Interface Transmit AC Parameters

Symbol	Description	Min	Max	Units
—	TxClk Frequency	25	50	MHz
—	TxClk Duty Cycle	40	60	%
tS_{TxEnb}	TxEnb Set-up time to TxClk	4	—	ns
tH_{TxEnb}	TxEnb Hold Time to TxClk	0	—	ns
tS_{TxData}	TxData[15:0] Set-up Time to TxClk	4	—	ns
tH_{TxData}	TxData[15:0] Hold Time to TxClk	0	—	ns
tS_{TxPrty}	TxPrty Set-up Time to TxClk	4	—	ns
tH_{TxPrty}	TxPrty Hold Time to TxClk	0	—	ns
tS_{TxSOP}	TxSOP Set-up Time to TxClk	4	—	ns
tH_{TxSOP}	TxSOP Hold Time to TxClk	0	—	ns
tS_{TxEOP}	TxEOP Set-up Time to TxClk	4	—	ns
tH_{TxEOP}	TxEOP Hold Time to TxClk	0	—	ns
tS_{TxMOD}	TxMOD Set-up Time to TxClk	4	—	ns
tH_{TxMOD}	TxMOD Hold Time to TxClk	0	—	ns
tS_{TxERR}	TxERR Set-up Time to TxClk	4	—	ns
tH_{TxERR}	TxERR Hold Time to TxClk	0	—	ns
tS_{TxAdd}	TxAdd[4:0] Set-up Time to TxClk	4	—	ns
tH_{TxAdd}	TxAdd[4:0] Hold Time to TxClk	0	—	ns
tP_{STPA}	TxClk High to STPA Valid	1	12	ns
tZ_{STPA}	TxClk High to STPA High-Z	1	10	ns
tZB_{STPA}	TxClk High to STPA Driven	0	—	ns
tZ_{PTPA}	TxClk High to PTPA High-Z	1	10	ns
tZP_{PTPA}	TxClk High to PTPA Driven	0	—	ns
tP_{DTPA}	TxClk High to DTPA[3:0] Valid	1	12	ns

10.4 DCC Interface

Table 10-5. Section DCC Timing

Parameter	Min.	Max.	Units
RSDCD set-up time to RSDCC	25	—	ns
RSDCD hold time to RSDCC	25	—	ns
RSDCC low to RSDCD valid	–12	5	ns

Table 10-6. Line DCC Timing

Parameter	Min.	Max.	Units
RLDCD set-up time to RLDCC	25	—	ns
RLDCD hold time to RLDCC	25	—	ns
RLDCC low to RLDCD valid	–12	5	ns

10.5 JTAG Interface

Figure 10-7. JTAG AC Timing

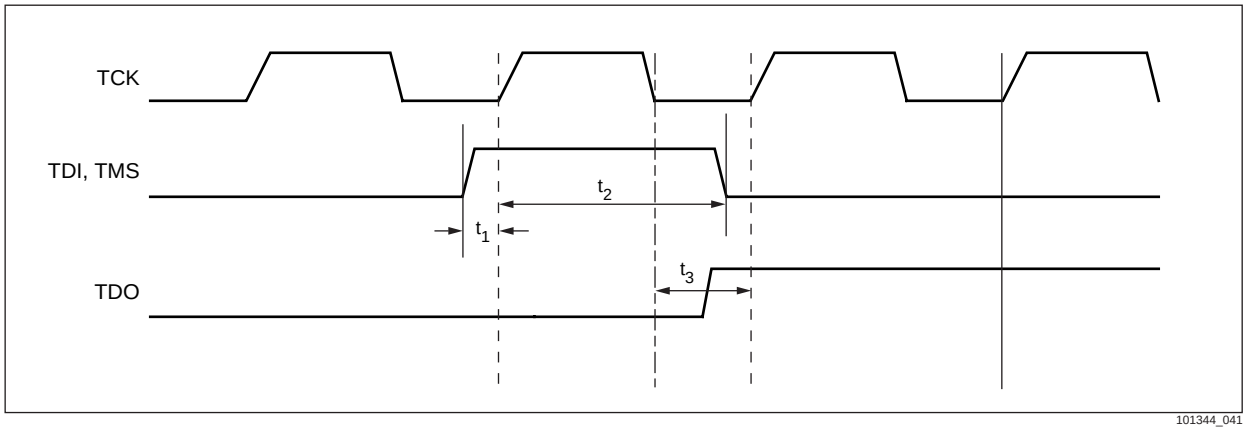


Table 10-7. JTAG AC Parameters

Symbol	Parameter	Min.	Max.	Units
TCK	Frequency	—	1	MHz
	Duty cycle	40	60	%
	TMS set-up time to TCK	50	—	ns
	TMS hold time to TCK	50	—	ns
	TDI set-up time to TCK	50	—	ns
	TDI hold time to TCK	50	—	ns

10.6 Power-Up Reset

Figure 10-8. Power-Up Reset Timing

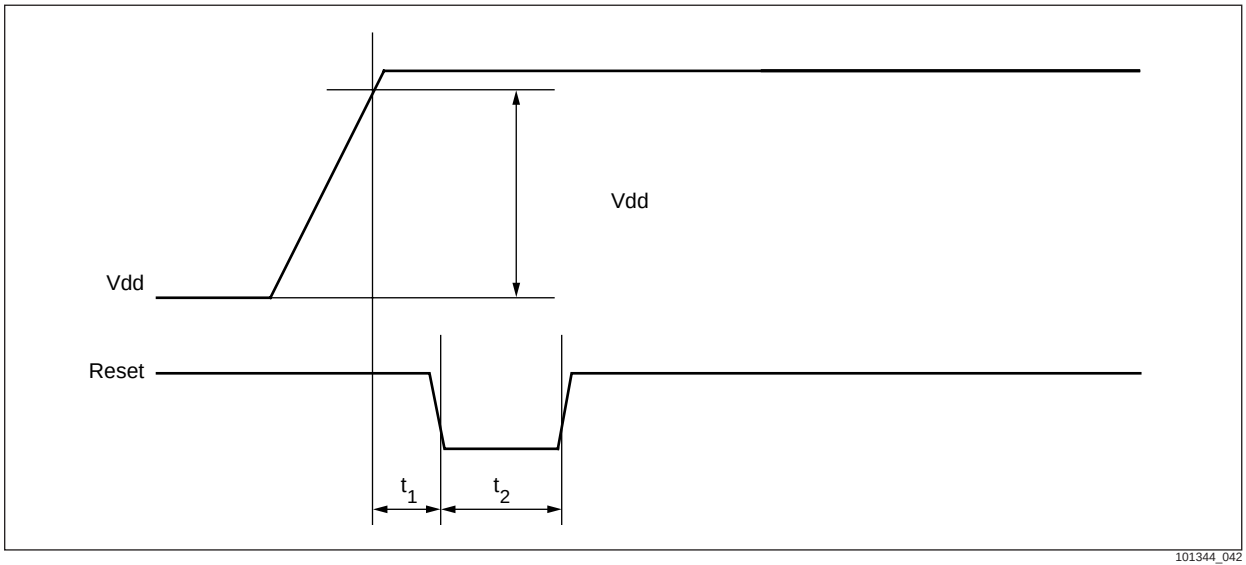


Table 10-8. Power-Up Reset Parameters

Symbol	Description	Min	Max	Units
t_1	Reset wait time	0	—	ms
t_2	Reset pulse width	50	—	ms

Table 10-9. Soft Reset Parameters

Symbol	Description	Min	Max	Units
t_2	Reset pulse width	1	—	ms

10.7 Line Interface

10.7.1 Transmit Line Interface

The CX29704 has a true PECL line interface. The PECL receiver is designed as a self-biased, wide-swing, high-gain amplifier. The input stage can withstand a wide common mode range at its inputs while maintaining high gain and wide bandwidth.

The technique used to extend the input common mode range of the PECL comparator is to use two complementary differential amplifier stages in parallel.

Table 10-10. Transmit Line Interface Parameters

Description	Value	Note
Type	PECL Transmitter	—
Data Rate	155 Mb/s	—
Max (worst case p-p) differential amplitude	2,000 mV	4
Min (opening) differential amplitude	1,100 mV	4
Max (off) differential amplitude	170 mV	1
Maximum Rise/Fall time (20–80%)	327 ps	3
Minimum Rise/Fall time (20–80%)	85 ps	3
Differential skew (max)	25 ps	—
Deterministic jitter	10% UI	—
Random jitter	12% UI	—
Output current—Ioh (typ)	TBD mA	2
Output current—Iol (typ)	TBD mA	—
Output current—Ioz (leakage)	TBD mA	—

NOTE(S):
1. An example of an Off Transmitter is no power supplied to the PMD and PMA transmit output being driven to a static state during loopback
2. At Vtt = Vdd – 1.32 V for 50 Ω pad
3. Cl ~ 2 pf
4. Differential p-p amplitude represents a 2x voltage swing measured at each output pad (Tx + Tx)

10.7.2 Receive Line Interface

The PECL receiver is designed as a self-biased, wide-swing, high-gain amplifier. The input stage can withstand a wide common mode range at its inputs while maintaining high gain and wide bandwidth.

The technique used to extend the input common mode range of the PECL comparator is to use two complementary differential amplifiers stages in parallel.

Table 10-11. Receive Line Interface Parameters

Description	Value
Type	PECL Receiver
Data rate	155 Mb/s
Minimum differential sensitivity (p-p)(1)	200 mV
Maximum differential sensitivity (p-p)(2)	2,000 mV
Input impedance	1 MΩ
Differential skew (max)	175 ps
Differential skew (max)	25 ps

NOTE(S):
(1) D21.5 idle pattern
(2) AC coupling input

11.0 DC Characteristics

11.1 Absolute Maximum Ratings

The absolute maximum ratings listed below are the maximum stresses that the device can tolerate without risking permanent damage.These ratings are not typical of normal device operation. Exposure to absolute maximum rating conditions for extended time periods may affect the device's reliability. This device should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

Table 11-1. Absolute Maximum Ratings

Parameter	Value
Supply Voltage	3.3 ±5% V
Operating Temperature—No Air Flow	40 °C/W
Operating Temperature—200 Linear Feet (1 Meter) per Minute	33 °C/W
Storage Temperature	–40 to 125 °C
θ_{JA}	11 °C/W
Ambient Temperature under Bias	–40 to 85 °C
Junction Temperature	+150 °C
Static Discharge Voltage	±2,000 V
Latchup Current	±300 mA

11.2 DC Characteristics

Table 11-2. DC Characteristics of the CX20704 UTOPIA/POS_Phy Pins

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VIL	Input low voltage	–0.3	—	0.8	V	—
VIH	Input high voltage	2.0	—	VDD + 0.3	V	—
VOL	Output low voltage	—	—	0.5	V	IOL $\geq$ 8 mA
VOH	Output high voltage	2.4	—	—	V	IOH $\geq$ |–8 mA|
IOL	Output current at low voltage	–8	—	—	mA	VOH $\geq$ 2.4 V
IOH	Output current at high voltage	—	—	8	mA	VOL $\leq$ 0.5V
—	Input and Output Timing reference level	—	1.4	—	V	—
—	Input Leakage current	–10	—	10	µA	V_{in} = 3.3 V or GND
—	Input Leakage current	–50	—	50	µA	V_{in} = 5 V
—	Three-State Output Leakage current	–10	—	10	µA	V_{out} = 3.3 V or GND
—	Input capacitance of Input/Output	—	10	—	pF	—
—	Output load	—	100	—	pF	—

Table 11-3. DC Characteristics of the CX29704 Pins

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VIL	Input low voltage	–0.3	—	0.8	V	—
VIH	Input high voltage	2.0	—	VDD + 0.3	V	—
VOL	Output low voltage	—	—	0.4	V	IOL ≥ 4 mA
VOH	Output high voltage	2.4	—	—	V	IOH ≥ |–4 mA|
IOL	Output current at low voltage	–4	—	—	mA	VOH ≥ 2.4 V
IOH	Output current at high voltage	—	—	4	mA	VOL ≤ 0.5V
VIL_p	SD input low voltage	—	—	0.3 VDD	V	—
VIH_p	SD input high voltage	0.7 VDD	—	—	V	—
—	Input and Output Timing reference level	—	1.4	—	V	—
—	Input Leakage current	–10	—	10	µA	V_{in} = 3.3 V or GND
—	Input Leakage current	–50	—	50	µA	V_{in} = 5 V
—	Three-State Output Leakage current	–10	—	10	µA	V_{out} = 3.3 V or GND
—	Input capacitance of Input/Output	—	2.5	—	pF	—
—	Output load	—	—	—	pF	—

12.0 Package Specifications

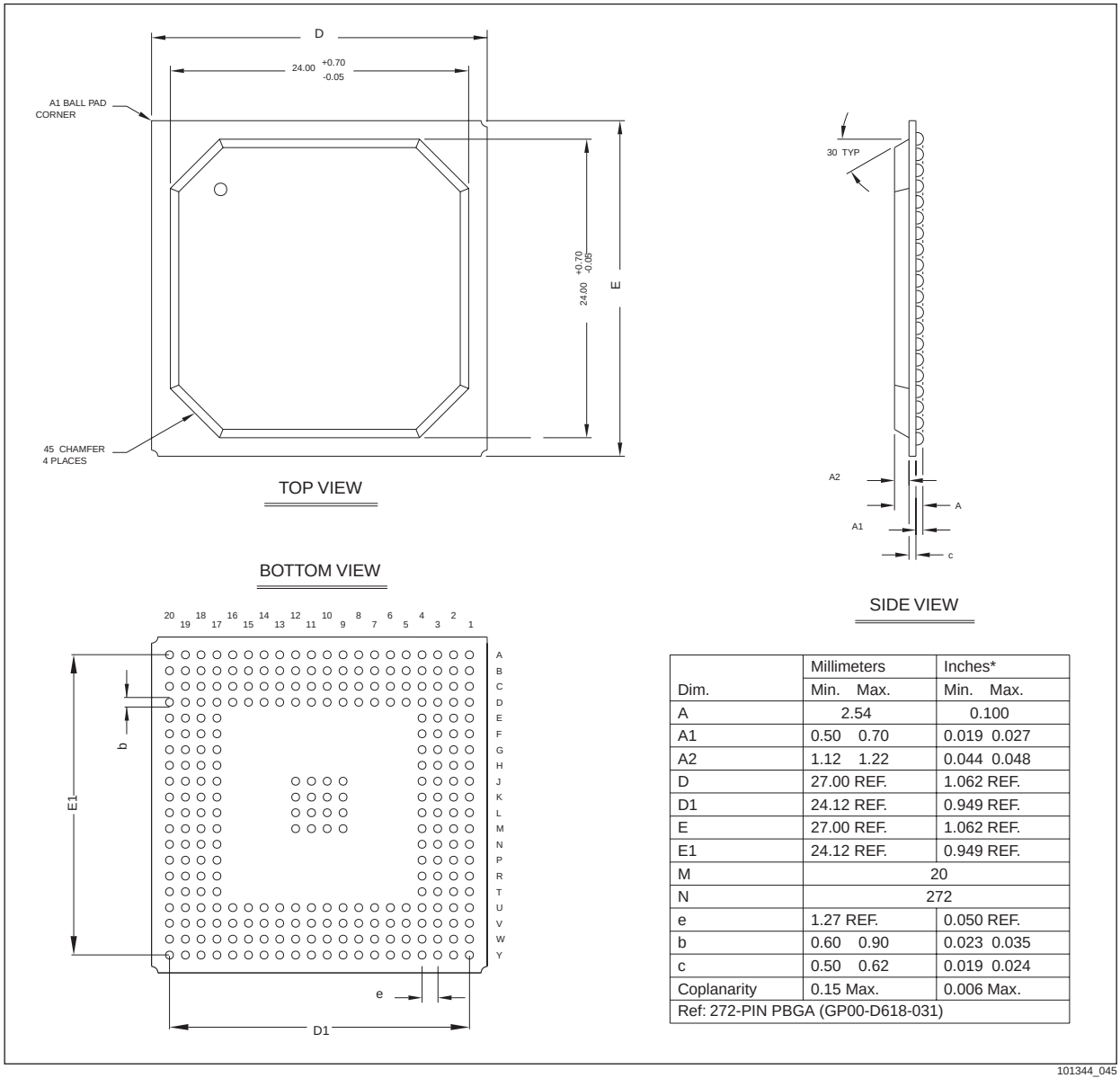
The CX29704 is packed in a 272-PBGA package with a body size of 27 × 27 mm and a ball pitch of 1.27 mm.

Figure 12-1. CX29704 Package Layout (Bottom View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
1	VSS	NC	TXMOD	RLDCC [1]	TXCLAV [2]	TXSOC	TSDCC [0]	TLDCC [0]	VDD	TLDCD [0]	TXDATA [15]	RLDCD [0]	TXDATA [8]	TXDATA [6]	TXDATA [4]	TXDATA [2]	BPSSG	RECCLKO	VSSA	RXDO-
2	TDI	RLDCD [1]	VDD	VSS	TXCLAV [3]	TSDCD [0]	TXENB	TXADD [1]	TXADD [4]	TXCLK	TXDATA [14]	TXDATA [11]	RLDCC [0]	TXDATA [5]	TXDATA [3]	RSDCD [0]	SD1	VSSD	VDDA	PCAPO+
3	TRST	RXADD [0]	TDO	RXERR	STPA	TXCLAV [1]	TXPRTY	TXADD [0]	TXADD [3]	VSS	TXDATA [13]	TXDATA [10]	TXDATA [7]	RSDCC [0]	TXDATA [0]	SDO	VSSD	RXDO+	VSSA	VDDD
4	RSDCC [1]	TCK	RXADD [1]	VSS	TXEOP	VDD	TXCLAV [0]	VSS	TXADD [2]	VDD	TXDATA [12]	TXDATA [9]	VSS	TXDATA [1]	VDD	RECCLK1	VSS	VDDA	PCAPO-	TXDO+
5	RXDATA [0]	RXADD [2]	TMS	RSDCD [1]													VDDD	VSSA	TXDO-	VSSD
6	RXDATA [2]	RXDATA [1]	RXADD [3]	VDD													VDD	VSSD	RXD1+	VDDA
7	RXDATA [4]	RXDATA [3]	TSDCD [1]	RXADD [4]													VSSA	RXD1-	VSSA	PCAP1+
8	RXDATA [6]	RXDATA [5]	TLDCD [1]	VSS													VSS	PCAP1-	VDDA	VDDD
9	RXDATA [9]	TLDCC [1]	RXDATA [8]	RXDATA [7]					VSS	VSS	VSS	VSS					VDDD	TXD1+	VSSA	TXD1-
10	VSS	TSDCC [1]	RXDATA [11]	RXDATA [10]					VSS	VSS	VSS	VSS					VDD	VDDA	VDDA	REXT1
11	VDD	RXDATA [11]	RXDATA [12]	VDD					VSS	VSS	VSS	VSS					VSSD	VSSA	VSSA	REXT2
12	SCANEN	TM	RXCLK	RLDCD [2]					VSS	VSS	VSS	VSS					VDDA	VDDA	REFCLK	VSSD
13	RXDATA [14]	TLDCD [2]	RXDATA [15]	VSS													VSS	VSSA	VSSD	VSSD
14	RXCLAV [0]	RXCLAV [1	RXCLAV [2	RXCLAV [3					Bottom View								VDDA	VSSA	VDDA	RXD2+
15	RSDCC [2]	RXPRTY	RSDCD [2]	VDD													VDD	VDDD	PCAP2+	RXD2-
16	RXSOC	RXEOP	RVAL	RXMOD													VSSD	VSSA	VDDD	PCAP2-
17	RLDCC [2]	TLDCC [2]	RXENB	VSS	UPADDR[1]	VDD	UPADDR[7]	VSS	UPDATA [3]	UPDATA [6]	VDD	UPDATA [14]	VSS	TSDCD [3]	VDD	TXD3+	VSS	VSSA	TXD2-	TXD2+
18	RXERR	RESET	TSDCC [2]	TSDCD [2]	UPADDR[4]	UPADDR[6]	CS	UPDATA [1]	UPDATA [4]	UPDATA [7]	UPDATA [10]	UPDATA [13]	TSDCC [3]	ASENB	SD3	RECCLK2	VDDD	RXD3-	RXD3+	VSSD
19	INTR	VDD	UPADDR[0]	UPADDR[3]	UPADDR[5]	RLDCC [3]	WRNRD	RSDCC [3]	UPDATA [5]	UPDATA [8]	UPDATA [11]	TLDCC [3]	ASDO	ASCLK	VDD	RECCLK3	VDDD	VDDA	VSSA	VDDA

13.0 Mechanical Specifications

Figure 13-1. 272-Pin PBGA



Dim.	Millimeters Min.	Max.	Inches* Min.	Max.
A	2.54		0.100	
A1	0.50	0.70	0.019	0.027
A2	1.12	1.22	0.044	0.048
D	27.00 REF.		1.062 REF.	
D1	24.12 REF.		0.949 REF.	
E	27.00 REF.		1.062 REF.	
E1	24.12 REF.		0.949 REF.	
M	20			
N	272			
e	1.27 REF.		0.050 REF.	
b	0.60	0.90	0.023	0.035
c	0.50	0.62	0.019	0.024
Coplanarity	0.15 Max.		0.006 Max.	
Ref: 272-PIN PBGA (GP00-D618-031)				

101344_045

Appendix A. Acronyms

AIS-L	Alarm Indication Signal—Line
AIS-P	Alarm Indication Signal—Path
ASSI	Alarms Status Serial Interface
ATM	Asynchronous Transfer Mode
BIP	Bit Interleaved Parity
B-ISDN	Broadband—Integrated Services Digital Network
DCD	Duty Cycle Distortion
HEC	Header Error Check
LCD	Loss of Cell Delineation
LOF	Loss Of Frame
LOP-P	Loss Of Pointer—Path
LOS	Loss Of Signal
NDF	New Data Flag
NRZ	Non-Return to Zero
OCD	Out-of-Cell Delineation
PHY	Physical
PLL	Phase Locked Loop
PMD	Physical Medium Dependent
RDI-L	Remote Defect Indication—Line
RDI-P	Remote Defect Indication—Path
REI-L	Remote Error Indication—Line
REI-P	Remote Error Indication—Path
SEF	Severe Error Framing
SOC	Start Of Cell
SPE	Synchronous Payload Envelope
STM	Synchronous Transport Module
STP	Shielded Twisted Pair
STS	Synchronous Transport Signal
TC	Transmission Convergence
UNI	User Network Interface
UTOPIA	Universal Test and Operations PHY Interface for ATM
UTP	Unshielded Twisted Pair
VC	Virtual Container
VCO	Voltage-Controlled Oscillator

Appendix B. References

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3. *ATM Forum*—"UTOPIA Level 1, v2.01," March 1994.
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6. Bell Communications Research—*GR-253-CORE*, Issue 2, Rev 1, "SONET Transport Systems, Common Generic Criteria," December 1997.
7. American National Standard Institute—*T1.646*, "Broadband ISDN–Physical Layer Specification for User Network Interfaces," 1995.
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11. Bell Communications Research—*GR-436-CORE*, "Digital Network Synchronization Plan," Issue 1 Revision 1, June 1996.
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13. *ITU-T Recommendation G.704*—"General Aspects of Digital Transmission".
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17. *ITU Recommendation G.783*—"Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks," 1996.
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19. IETF Network Working Group—*RFC-1662*, "PPP in HDLC Like Framing," July 1994.

Appendix C. ASSI Application Example

Figure C-1. ASSI Application Example

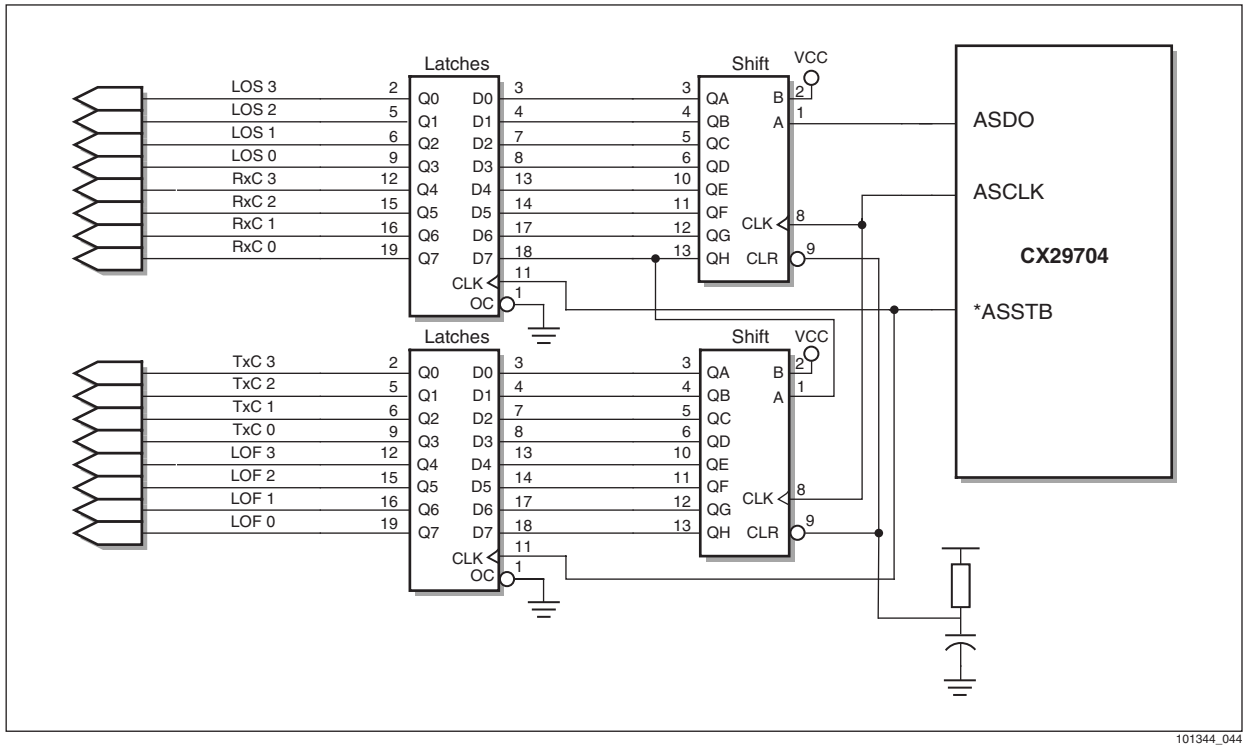

Figure C-1 illustrates a sample application for the ASSI. This application provides permanent status of LOS, RxC, TxC, and LOF for each one of the ports. In a similar manner, all other indications that the ASSI provides may be exploited. An application using less indications is also an option.

The interface clock (ASCLK) is used to shift the serial data (ASDO) through the shift registers. The data strobe (*ASSTB) is used to latch the data at the appropriate location.

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