

Data Sheet

CX60077 2.5 Gbps Long Haul Laser Driver

Key Features

- Single supply : -5.2 Volts
- CML interface (with capability of receiving ECL level)
- Low power consumption ≤ 400 mW
- Input impedance of 50Ω
- Loss of input data detection
- Pulse and bias current monitors
- 1 to 80 mA laser diode bias current
- 5 to 80 mA pulse current range

Applications

- Fiber-optic communication systems (OC-48)
- SONET/SDH test equipment

Product Description

The CX60077 is a high-speed laser driver designed for use in a transmitter module for fiber-optic communications, such as Synchronous Optical Network (SONET), Synchronous Digital Hierarchy (SDH), Asynchronous Transfer Mode (ATM), and Dense Wavelength Division Multiplexer (DWDM). This device can achieve a maximum output drive current of 80 mA into a 25Ω load. Figure 1 illustrates the functional block diagram, and Table 1 lists terminal descriptions. The CX60077 is available in a 32-pin flat pack, which is illustrated in Figures 10 and 11.

Figure 1. CX60077 Functional Block Diagram

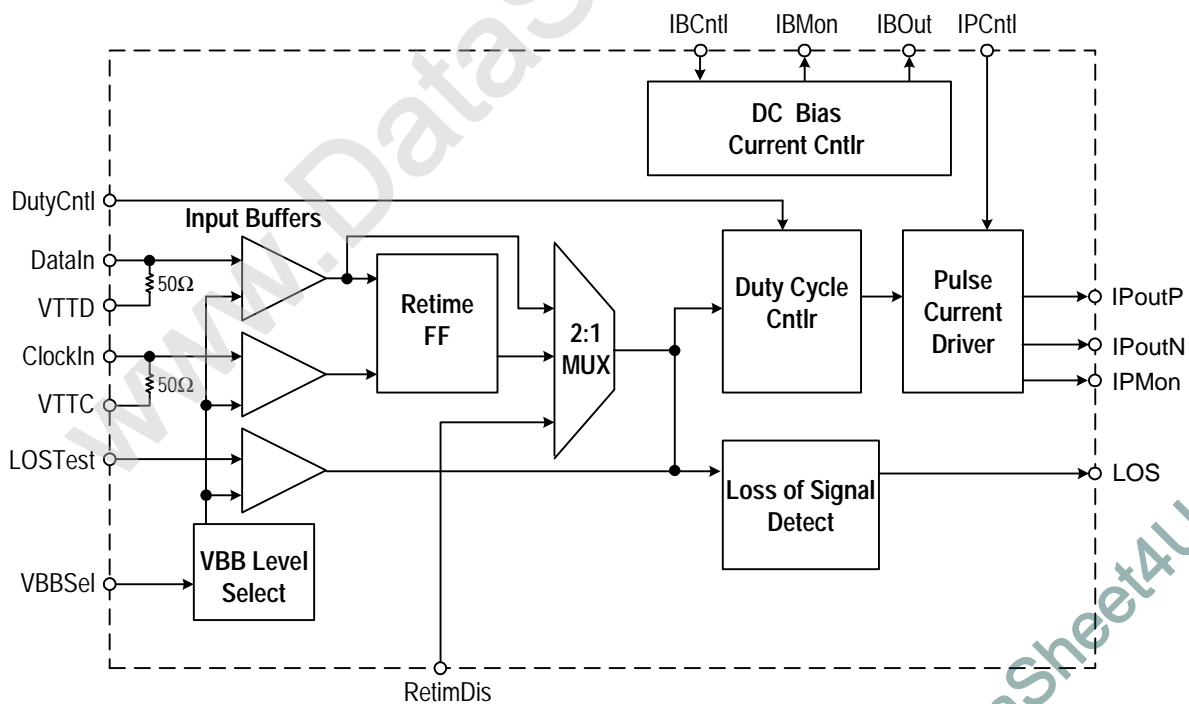


Table 1. CX60077 Terminal Descriptions

Number	Terminal Name	Description	Type	I/O	Rate/DC
27	IBOut	Laser diode, DC bias current output	Current Sink	O	DC
21	IBCntl	DC bias current, control signal input	Analog	I	DC
22	IBMon	DC bias current monitor	Current Sink	O	DC
19	LOS	Loss of input or clock signal indicator output	Current Sink		DC
15	VBBSel	VBB (threshold) Voltage Select between CML and ECL	(1)		DC
11	DataIn	Data input	CML	I	2.5 Ghz*
17	RetimDis	Input for disabling data and clock retiming	(2)	I	DC
24	IBMon2	Additional independent IBMon output	Current Sink	O	DC
13	ClkIn	Clock input	CML	I	2.5 Gbps*
16	LOSTest	Loss of Signal test Input (3)	Analog	I	DC
18	DutyCntl	Output current, duty cycle control signal input	Analog	I	DC
3, 4, 5, 6, 25	Vee	Supply voltage	-	-	DC
20	IPCntl	Output current, control signal input	Analog	I	DC
23	IPMon	Output pulse current monitor	Current Sink	O	AC
1, 2, 7, 8, 9, 10, 26, 30	Gnd	Ground	-		DC
31, 32	IPOutN	Inverted output	Current Sink	O	2.5 Gbps
28, 29	IPOutP	Non-inverted output	Current Sink	O	2.5 Gbps
14	V TTC	50Ω input clock termination reference	AC Ground	I	DC
12	V TTD	50Ω input data termination reference	AC Ground	I	DC

* High Speed Terminal

Note 1: See Table 2.

Note 2: To select retimed data this terminal can be connected to -2 V or it can float. Connecting the RetimDis terminal to ground selects non-retimed data.

Note 3: This is an input to allow testing of the LOS function. When it is grounded: Assert LOS output signal continuously. When it is connected to -2.0 V: Enable LOS function.

Functional Description

The CX60077 2.5 GHz Long Haul Laser Driver translates input data on DataIn from a digital voltage signal to a digital current signal on pins IpoutP and IpoutN to drive a laser diode. The Input Buffers accept data, clock, and test signals and transfer the buffered signals to their respective circuits. When the input data and clock are direct coupled, the input threshold level is set by means of the VBBSel terminal. See Table 2 for the relationship between VBBSel and the input threshold level.

Retimed data is selected with the RetimDis terminal, and the duty cycle of the output signal is controlled with the DutyCntl pin.

The data output pulse current driver IPOut (P/N) is adjusted using the IPCntl pin and monitored using the IPMon pin. A current driver supplying DC bias for the laser is provided on pin IBOut. The output bias current is monitored using the IBMon and/or IBMon2 pins and adjusted using the IBCntl pin.

The Loss of Signal (LOS) Detect circuit detects the loss of transitions on the data signal. When a LOS is detected, the output of this circuit can be used to shut down both the output pulse (IP) current and DC bias current (IB). The LOSTest pin provides a means to simulate a LOS condition for testing.

High Speed Inputs and VBB Level Select

The DataIn and ClkIn pins are high-speed CML data inputs each having a 50 Ω on-chip termination resistor to VTTC and VTTC respectively (see Figure 1) and are capable of operating at CML and ECL logic levels, as described in Table 2.

The VBBSel pin controls the threshold voltage for the LOSTest, DataIn, and ClkIn Input Buffers, as described in Table 2. The VTTC and VTTC pins should be connected to ground when the DataIn and ClkIn pins are direct coupled to a CML output. When the DataIn and ClkIn pins are direct coupled to an ECL output, the VTTC and VTTC pins should be connected to -2 V. When DataIn and ClkIn are AC coupled, VTTC and VTTC should be connected to -0.45 V.

The CML threshold is -0.45 V and the ECL threshold is -1.32 V. It is necessary for the clock and data inputs to have an edge through these thresholds. For low input clock and/or data levels, it might be necessary to either AC couple and connect VTTC and/or VTTC to a negative voltage source to ensure there is an edge through the appropriate threshold.

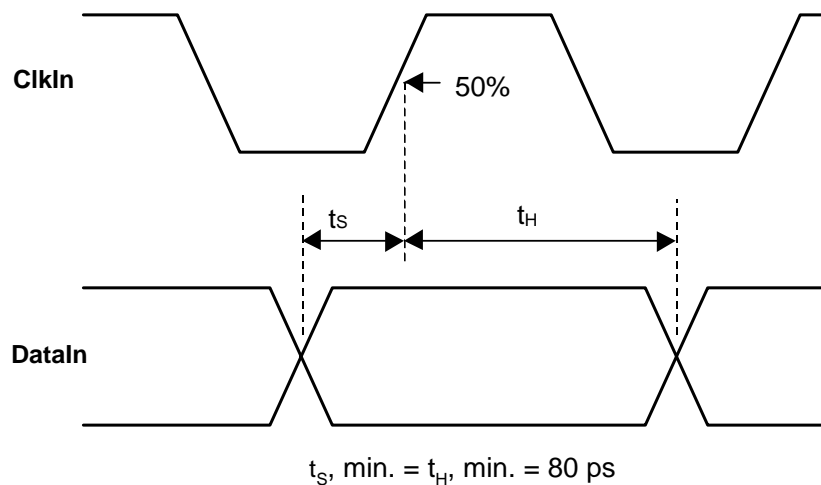
Table 2. Required Connections

DataIn/ClkIn Input Type	V Threshold	VTTC/VTTC Connection	VBBSel Connection
CML Direct Coupled	-0.45	Ground	Open
ECL Direct Coupled	-1.32	-2.0 V	Ground
AC Coupled	-0.45	-0.45 V	Open

Input Data Retiming

Input data from the DataIn pin is retimed in the Retime Flip-Flop by a clock signal from the ClkIn pin. Figure 2 illustrates the DataIn and ClkIn relationship.

Figure 2. Falling Edge of ClkIn Synchronized to Data Transitions



Retiming Terminal

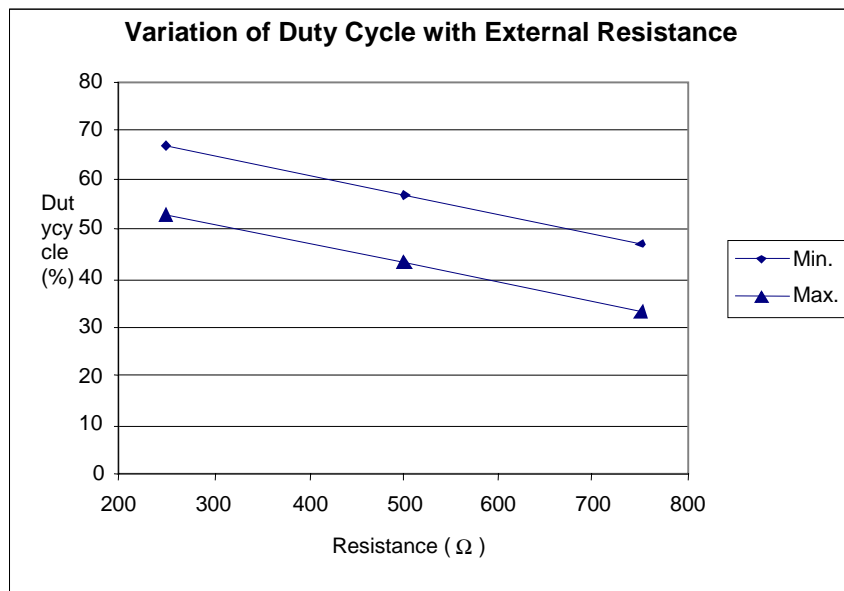
A high-isolation 2:1-multiplexer (2:1 MUX) selects retimed data from the Retime Flip Flop when the RetimDis pin is connected to an ECL logic high level (-2.0 V) or left open. The RetimDis input is compatible with ECL logic levels, and has an on-chip 250 μ A current sink. Setting RetimDis to Ground enables the 2:1 MUX to select non-retimed data directly from the DataIn Input Buffer.

Duty Cycle Control

The analog input voltage on the DutyCntl pin controls the duty cycle of the data output (IPOut). This input incorporates a 250 μ A current sink.

The DutyCntl pin should be connected to ground through an external resistor or controlled with a voltage source (i.e. a DAC). By varying the resistor value, thus the input voltage, the CX60077 duty cycle can be modified. Figure 3 illustrates the duty cycle as controlled by the resistor value.

Figure 3. Duty Cycle and DutyCntl Voltage versus Resistor Value

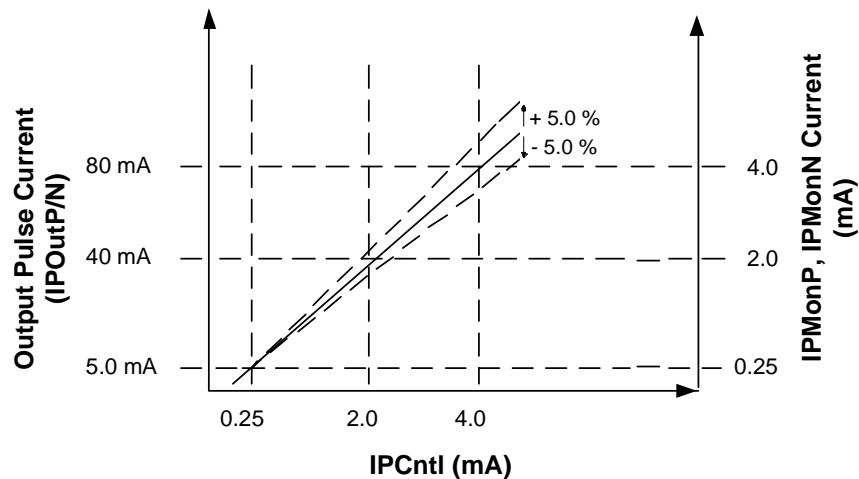


Pulse Current Driver, Control and Monitoring

The dual IOutP and IOutN pins (signal complements) are the CX60077 data output signals. Each of the two IOutP/N pins must be terminated into 50Ω, or alternatively, two of the same phase pins can be connected together to drive a 25Ω load. The IPCntl pin, using an externally supplied current, controls the amplitude of the IOutP/IOutN pulse modulation current, which is approximately twenty times the IPCntl input current.

The IPMon pin monitors the IOut modulation current. The IPMon pin sinks one-twentieth of the IOut modulation current in the high state and will be equal to IPCntl. Figure 4 illustrates the IP control characteristics.

Figure 4. IP Control Characteristics

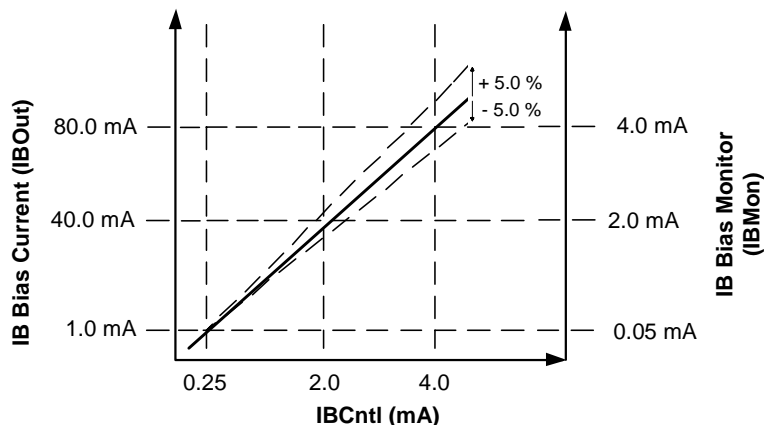


DC Bias Current Driver, Control and Monitoring

The IBOut pin provides an adjustable DC bias current for use with the laser diode. The IBCntl pin, using an externally supplied current, controls the DC bias current on IBOut.

The DC bias current on IBOut will be approximately twenty times the IBCntl input current. The IBMon and IBMon2 pins are separate but identical outputs, which monitor the IBOut current and are capable of sinking one-twentieth of the IBOut current. Figure 5 illustrates the IB control characteristics.

Figure 5. IB Control Characteristics

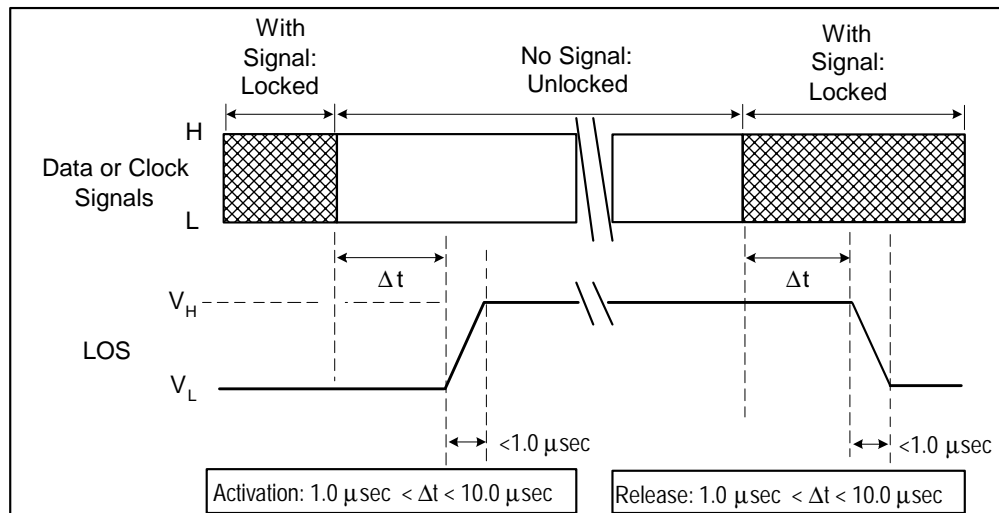


Loss of Signal Detection

The Loss of Signal (LOS) Detect circuit detects the loss of transitions in the data path out of the 2:1 MUX. Under normal operating conditions when data is toggling LOS remains high (Gnd). When data is lost (no signal transitions) the LOS output pin goes low (-2.0 V). Figure 6 illustrates the LOS detect circuit timing waveforms. LOS can be used by an external control circuit to shut down both the output pulse current and DC bias current drivers. LOS can be made CML logic compatible by termination with a 2 K Ω resistor to Ground for a LOS condition.

The LOSTest input pin can be used to force LOS to assert (-2.0 V). This function is used for board test purposes. The LOSTest input is similar to the DataIn and ClkIn pins in that it is capable of handling either CML or ECL logic levels. However, LOSTest does not have an on-chip termination resistor. Under normal operating conditions, whether using CML or ECL input levels, LOSTest should be held in the low (inactive) level (-2.0 V), or if LOSTest will not be used in board level tests, it should be terminated with a 2 K Ω resistor into -2 V.

Figure 6. Timing Waveforms for the Loss of Data Detect Circuit



Electrical Specifications

Table 3 lists the CX60077 electrical specifications.

Table 3. CX60077 Electrical Specifications

Ts = 0 °C to +85 °C, Vee = -5.2 V ±10%, RL = 25 Ω

Description	Parameter	Min	Typical	Max	Unit
Input Data Level (DataIn) ⁽¹⁾⁽²⁾	VDAT p-p	200	–	1200	mV
Input Clock Level (ClkIn) ⁽¹⁾⁽²⁾	VCLK p-p	200	–	1200	mV
DataIn DC Offset Range					mV
ClkIn DC Offset Range					mV
Input Data Duty Cycle	tDATdc	90	100	110	%
Input CLK Duty Cycle	tCLKdc	45	50	55	%
Input Data Rise/Fall Time ⁽³⁾	tDATr, tDATf	–	110	140	psec
Input CLK Rise/Fall Time ⁽³⁾	tCLKr, tCLKf	–	75	90	psec
Bias Current	IB	1	–	80	mA
Peak Current	IP	5	–	80	mA
Output Swing (peak-to-peak)	V p-p	–	–	2.8	V
Output Duty Cycle ⁽⁴⁾	tIPdc	84	100	116	%
Output Rise/Fall Time	tIPr, tIPf	–	90	130	ps
Power Consumption ⁽⁵⁾	P	–	370	400	mW
IPCntl versus IPOut, IPMon					
IPCntl vs. IPOut [(IPOut) ÷ (IPCntl × 20)]		0.9	1.00	1.10	–
IPCntl vs. IPMon [(IPMon) ÷ (IPCntl)]		0.95	1.00	1.05	–
IPOut vs. IPMon [(IPOut) ÷ (IPMon × 20)]		0.987	1.00	1.012	–
IBCntl versus IBOut, IBMon					
IBCntl vs. IBOut [(IBOut) ÷ (IBCntl × 20)]		0.95	1.00	1.05	–
IBCntl vs. IBMon [(IBMon) ÷ (IBCntl)]		0.95	1.00	1.05	–
IBOut vs. IBMon [(IBOut) ÷ (IBMon × 20)]		0.987	1.00	1.012	–
Loss of Signal Detection Characteristics (Conditions) (See Figure 6)					
LOS VL (LOS output low level) (No Transitions on DataIn/ClkIn)	V _{L-LOS}	-1.15	–	-0.85	V
LOS VH (LOS output high level) (DataIn/ClkIn Transitioning)	V _{H-LOS}	-0.1	–	+0.1	V
LOS Activation Time (No Transitions on DataIn/ClkIn)	T _{Activation}	1.0	–	10	μs
LOS Deactivation Time (DataIn / ClkIn Transitioning)	T _{Release}	1.0	–	10	μs

Notes:

(1) Input value: 0.900 V p-p.

(2) It is necessary to have a data and clock edge through the input threshold established by VBBSel: VBBSel = 0, input threshold = ECL = -1.32 V; VBBSel = open, input threshold = CML = -0.45 V.

(3) Based on 20%/80% levels. (4) Duty Cycle Ratio = “Duty”/Average Data (NRZ) bit period” (see Figure 8). (5) Outputs open.

Table 4 lists the absolute maximum ratings.

Table 4. CX60077 Absolute Maximum Ratings

Exceeding the CX60077 absolute maximum ratings listed in Table 4 will damage the unit.

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V _{ee}	-7.0	+0.5	V
Input Voltage	V _{in}	V _{ee} -0.5	+0.5	V
Input Current (DataIn, ClkIn)	I _{in}	–	50	mA
Input Current (except DataIn, ClkIn)	I _{in}	–	8	mA
IB, IB Maximum Current	I _{max}	–	120	mA
Case Operating Temperature	T _c	-65	+150	°C
Storage Temperature	T _{st}	-65	+150	°C
Electrostatic Discharge (Human Body Model)	ESD	–	>2000	V
High-speed Terminals		–	≥100	V

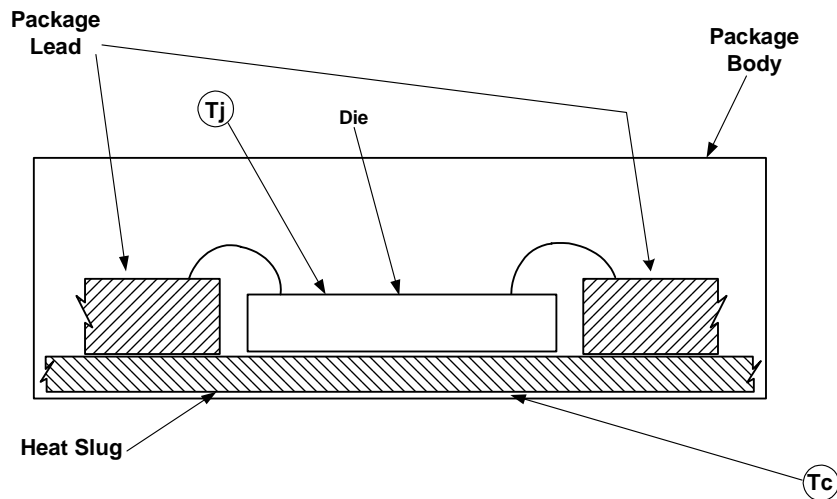
Table 5 lists the recommended operating conditions.

Table 5. CX60077 Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V _{ee}	-4.68	-5.20	-5.72	V
Operating Temperature	T _c ⁽¹⁾	0	+25	+85	°C
Junction Temperature	T _j ⁽¹⁾	0	–	+150	°C

Note 1: See Figure 7 for locations for temperature measurement locations.

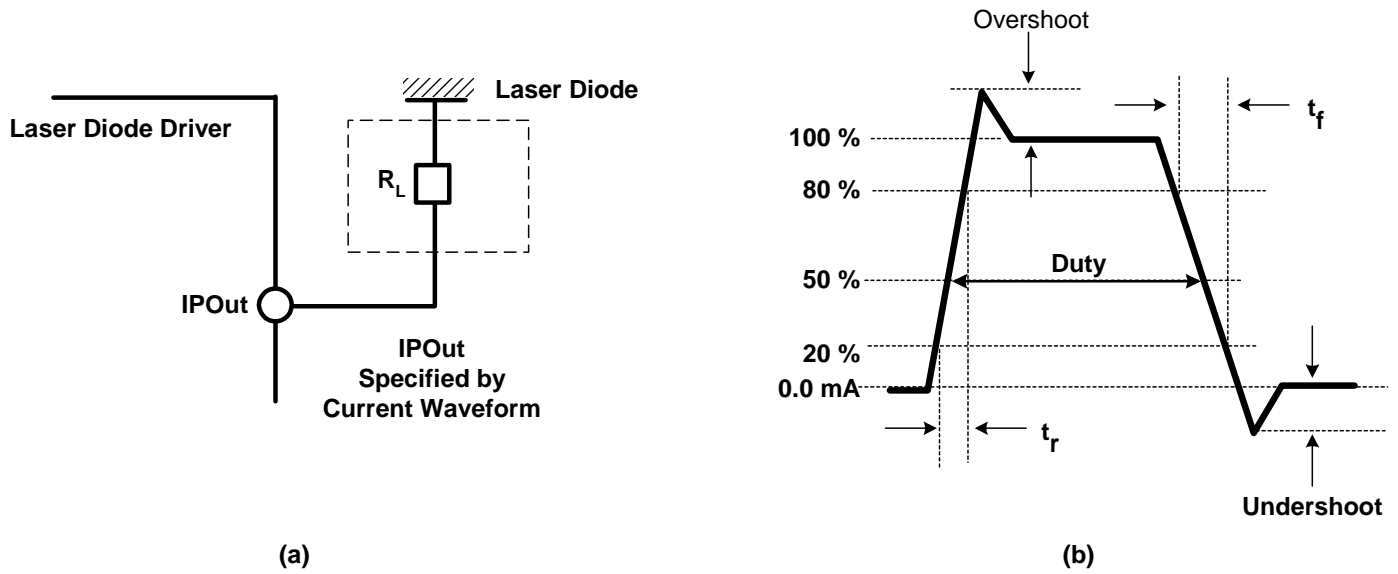
Figure 7. Temperature Measurement Locations



Waveform Evaluation

Figure 8 illustrates the evaluation equivalent load circuit and waveform specifications.

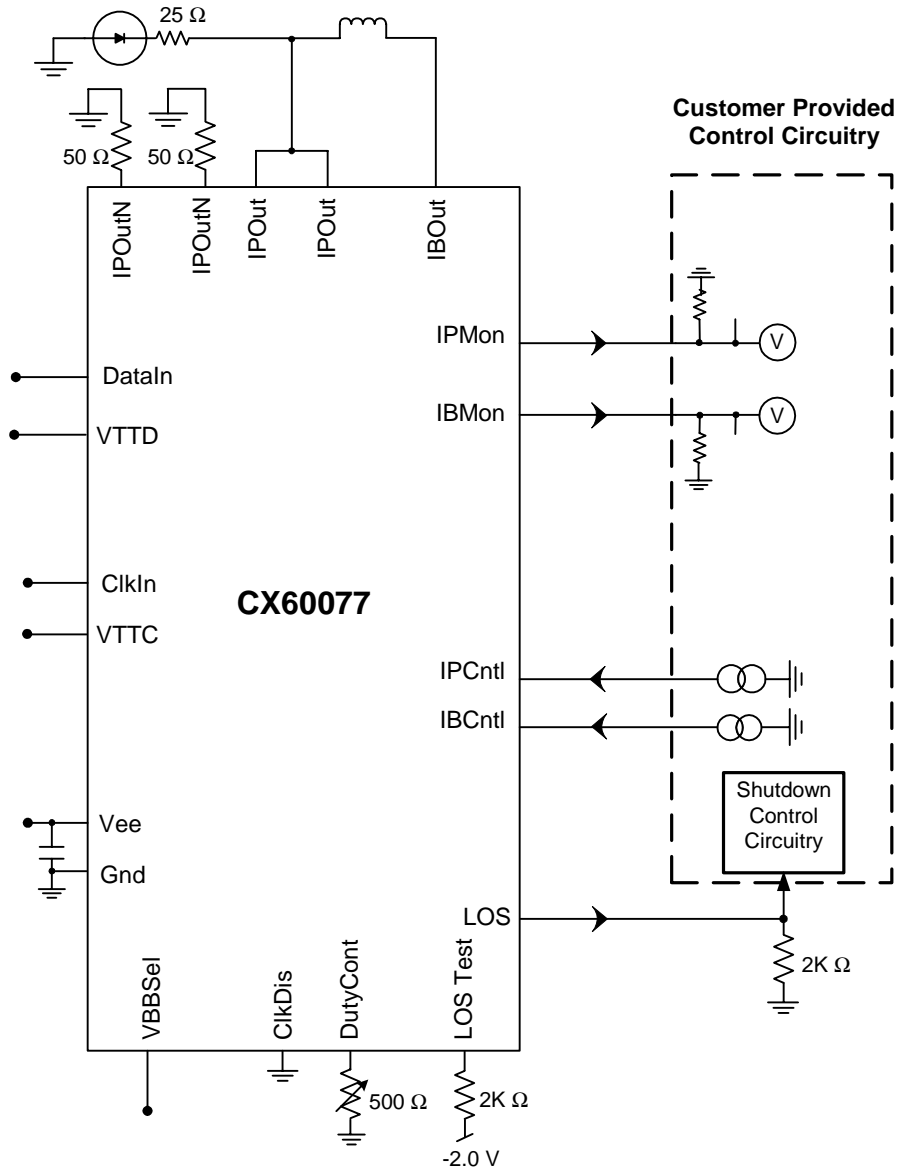
Figure 8. Equivalent Load Circuit for Waveform Evaluation (a) and Waveform Specifications (b)



Typical Application

Figure 9 is a block diagram of the CX60077 in a typical application.

Figure 9. CX60077 Typical Application Block Diagram



Package Pin Configuration and Assignments

The CX60077 package pin configuration is illustrated in Figure 10 and package pin assignments are listed in Table 6.

Figure 10. Package Pin Configuration

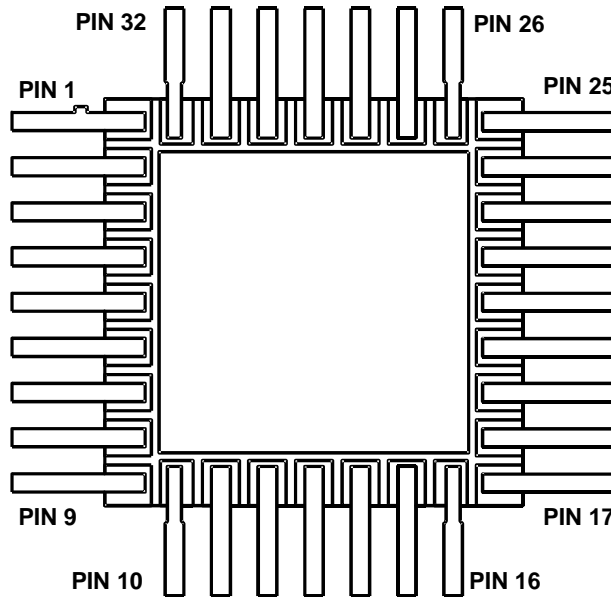


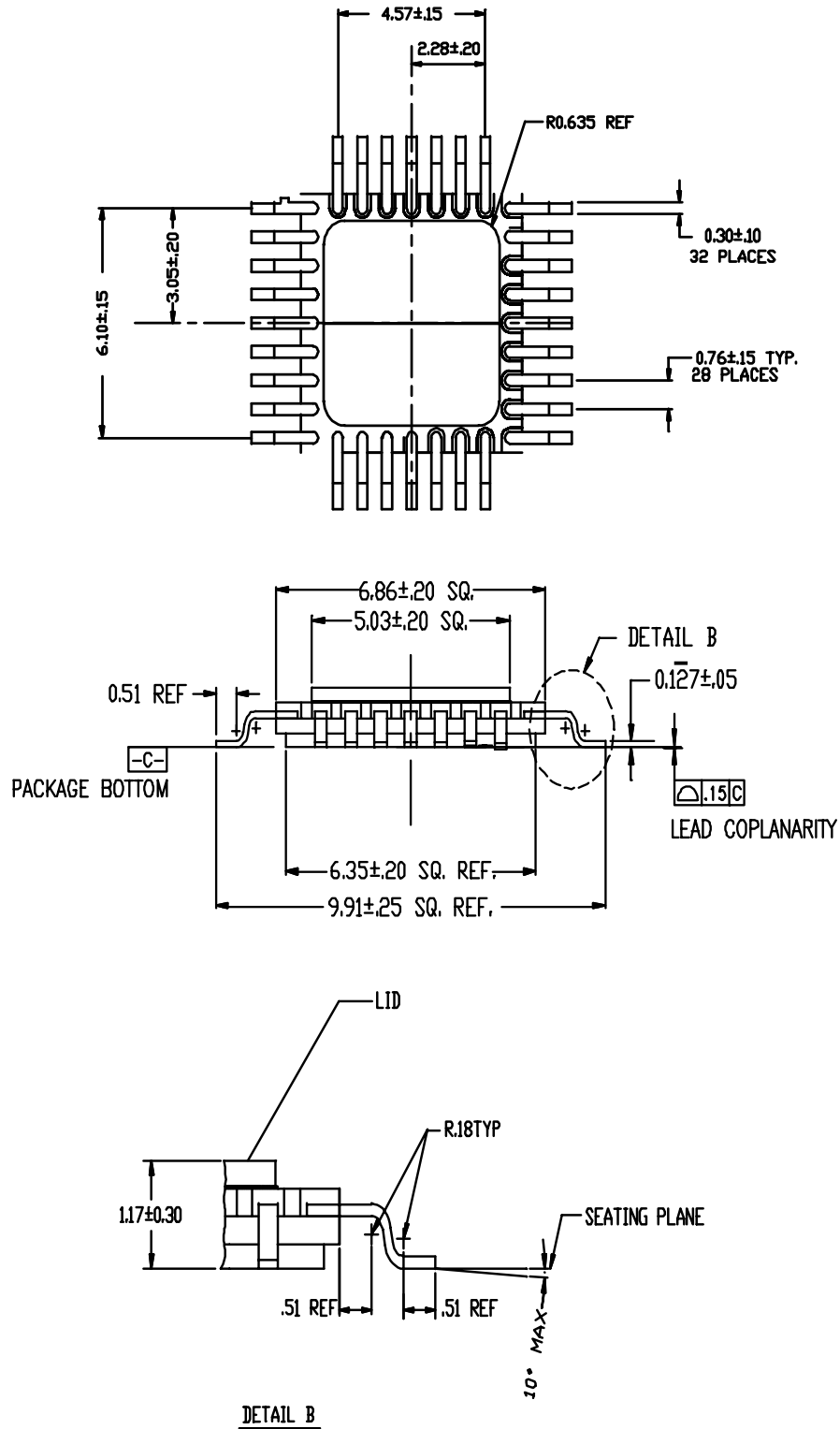
Table 6. Package Pin Assignments

Pin Number	Signal on Pin
11	DataIn
12	VTTD
13	ClkIn
14	VTTC
15	VBBSel
16	LOSTest
17	RetimDis
18	DutyCont
19	LOS
20	IPCntl
21	IBCntl
22	IBMon
23	IPMon
24	IBMon2
27	IBOut
28,29	IPOutP
31,32	IPOutN
1,2,7,8,9,10,26,30	Gnd
3,4,5,6,25	Vee

Package Dimensions

Figure 11 illustrates the CX60077 package dimensions in millimeters.

Figure 11. Package Pin Configuration



Ordering Information

Name	Number	Package Data
2.5 Gbps Long Haul Laser Driver	CX60077	30 Pin flat pack

Revision History

Revision	Date	Comments
CX60077 Rev 2c	5/10/00	Added review material.
CX60077 Rev 2d	10/26/00	Adding engineering design changes. Revised Figure 2 and Table 2.

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