

CX74036

IS-136 Receive RF IC for TDMA and AMPS Applications

Conexant's CX74036 receive RF IC is an advanced, highly integrated and high performance, triple-mode, dual-band IC for IS-136 compliant cellular radio applications and is designed in an advanced 28 GHz Ft BiCMOS process. In the 800 MHz cellular band, the CX74036 is designed to operate in both the Time Division Multiple Access (TDMA) mode and Advanced Mobile Phone System (AMPS) mode. In the 1900 MHz Personal Communications System (PCS) band, the device operates in the TDMA mode.

The CX74036 embodies all the necessary functions for a radio receiver system except for the RF and Intermediate Frequency (IF) filters and RF Local Oscillator (LO) sources. The device front-end section has two Low Noise Amplifier (LNA) and mixer pairs, one for the 800 MHz band and the other for the 1900 MHz band. A common path is taken from the first IF mixer output to the demodulator output.

The CX74036 48-pin, 7x7 Land Grid Array (LGA) package pin configuration is shown in Figure 1. A block diagram of the CX74036 is shown in Figure 2.

Features

- Front-end to baseband in one IC
- Inphase and Quadrature (I/Q) demodulator
- 3 V supply operation
- Low current consumption
- LNA gain switch with current reduction
- IF LO synthesizer with Voltage Controlled Oscillator (VCO) (requires external tank)
- 70 dB Variable Gain Amplifier (VGA) dynamic range
- Low Noise Figure (NF) and high 3rd order Input Intercept Point (IIP3) mixers

Applications

- Cellular and/or PCS band phones
- TDMA and/or AMPS mode phones
- Portable battery powered radio equipment

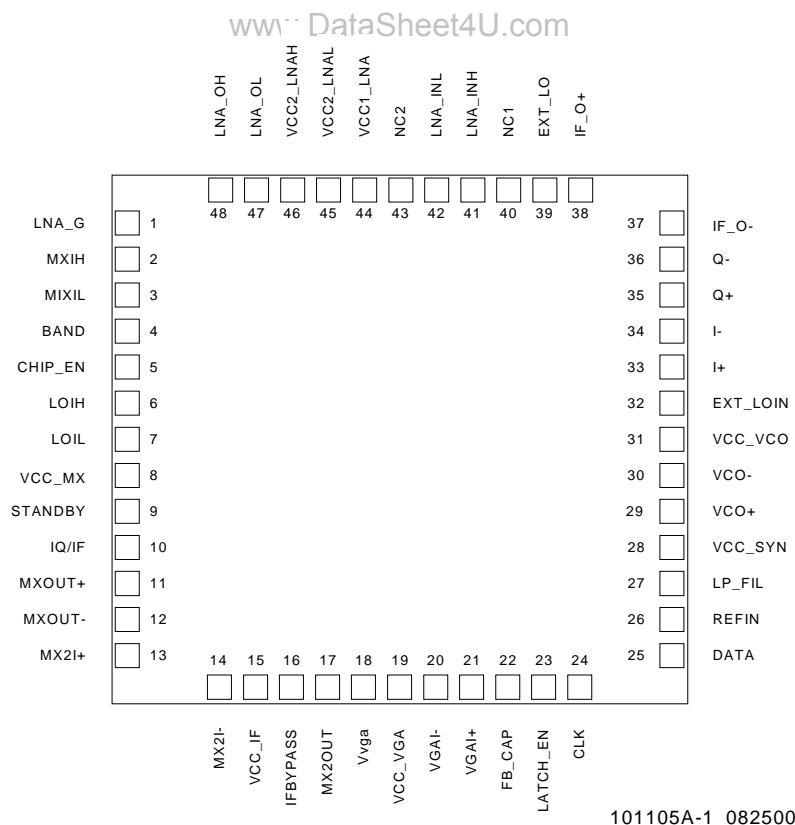


Figure 1. CX74036 48-Pin, 7x7 LGA Package Pin Configuration

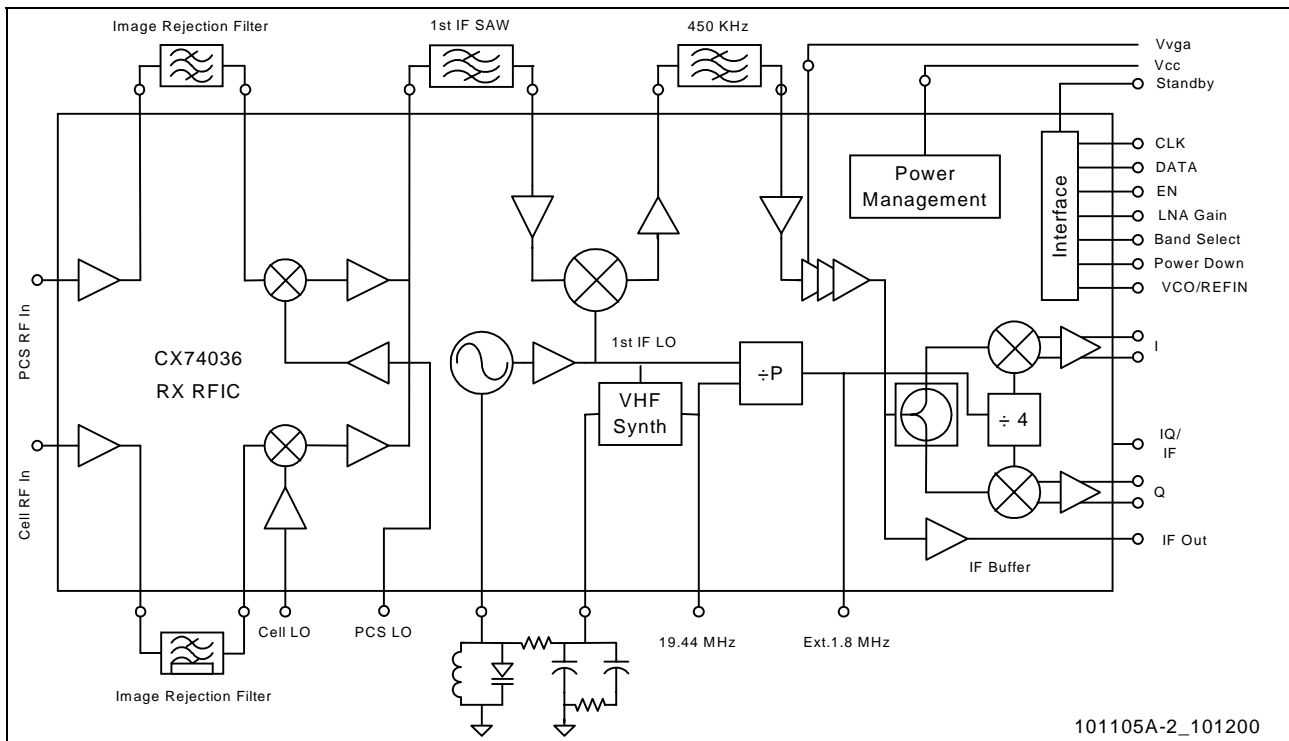


Figure 2. CX74036 Functional Block Diagram

Technical Description

Low Noise Amplifiers: The CX74036 contains two independent LNAs for the cellular and PCS bands. The gain of both LNAs can be switched off to a loss mode via one command line interface. Only one LNA is powered at any given time. Control is done by an external band-select control signal. The input and output matches are external to the chip. The LNAs' parameters, Noise Figure (NF), and gain are chosen to provide an excellent balance between system sensitivity and IIP3 requirements to achieve maximum dynamic range. Both LNA outputs are ported off-chip to allow for image filtering before being fed to the RF mixer inputs.

RF Mixers: The mixers are designed to operate with a low LO input power level of -10 dBm. This eliminates the requirement of buffer amplifiers for the external VCO. Cellular band mixer high gain and low NF performance allow for the cellular LNA gain to be lower, which saves current consumption. Both mixers are designed to provide high suppression of one-half IF response. The outputs of both mixers share a common interface path to the external IF Surface Acoustic Wave (SAW) filter, which reduces complexity and cost. The RF mixer load configuration is shown in Figure 3. Inductors can be Surface Mount Multilayer Chip (SMMC) components.

First IF Mixer: This mixer begins the common signal path for both cellular and PCS band modes. Input and output impedance are set to values that are close to the most commonly available SAW and ceramic filters.

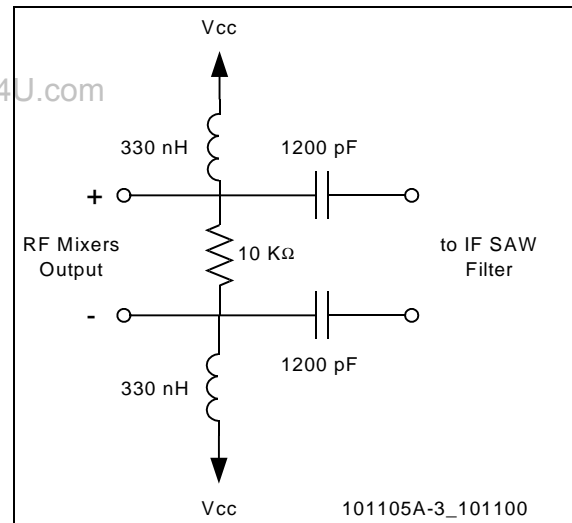


Figure 3. RF Mixer Load Configuration

Variable Gain Amplifier: The VGA itself provides 70 dB of dynamic range to satisfy the high system dynamic range requirement. With the inclusion of the LNA gain switch, the system dynamic range is extended to more than 95 dB.

I/Q Demodulator: Using digital circuitry generates a stable quadrature LO signal, on-chip direct connection to the VGA output, on-chip LO source, and lowpass filtering for each channel. This, in turn, provides a high performance I/Q demodulator with very low amplitude and phase offsets. The output signal quality is compatible with many baseband interface requirements.

VHF Synthesizer and Oscillator: The on-chip VHF synthesizer and an oscillator with an added external tank circuit generate the required second IF LO signal for conversion down to the standard second IF signal. A programmable divide circuit is also included to generate the LO for the I/Q demodulator. Depending on the frequency plan used, an option is provided to inject an external LO source for the I/Q demodulator.

Control Logic Truth Table. The Control Logic Truth Table is shown in Table 1.

3-Wire Bus Programming. The 3-wire bus programming data is included in Table 2. The 3-wire programming data pattern diagram is shown in Figure 4.

Electrical and Mechanical Specifications

The signal pin assignments, names, and descriptions are found in Table 3. Absolute maximum ratings are provided in Table 4, the recommended operating conditions are specified in Table 5. Electrical characteristics are shown in Table 6.

Figure 6 provides the 48-Pin, 7x7 LGA package dimensions.

ESD Sensitivity

The CX74036 is a static-sensitive electronic device. Do not operate or store near strong electrostatic fields. Take proper ESD precautions.

Table 1. Control Logic Truth Table

Mode	LNA_G	BAND	CHIP_EN	STANDBY	IQ/IF	LO_EXT
Active, Low Band, LNA High Gain, IQ	1	0	1	1	0	1
Active, High Band, LNA High Gain, IQ	1	1	1	1	0	1
Active, Low Band, LNA Low Gain, IQ	0	0	1	1	0	1
Active, High Band, LNA Low Gain, IQ	0	1	1	1	0	1
Active, Low Band, LNA High Gain, IF	1	0	1	1	1	1
Active, High Band, LNA High Gain, IF	1	1	1	1	1	1
Active, Low Band, LNA Low Gain, IF	0	0	1	1	1	1
Active, High Band, LNA Low Gain, IF	0	1	1	1	1	1
Standby	---	---	0	1	---	1
External LO Mode	---	---	---	---	---	0
Sleep	---	---	0	0	---	0

Note. Synthesizer prescaler and charge pump can be turned off via programming from the 3-wire bus. This mode can be used when driving the IF Mixer with an external synthesizer.

Table 2. 3-Wire Bus Programming Data

Bit Number	Function	Programming
00	Select VCO or Reference Input to Programming Counter	"0" = Reference Input "1" = VCO Input
01 – 08	Synthesizer M Counter Programming, MB0 – MB7	
09 – 12	Synthesizer A Counter Programming, AB0 – AB3	
13 – 23	Synthesizer Reference Counter Programming, RB0 – RB10	
24	Charge Pump Polarity	"0" = Ground Referenced Varactor "1" = VCC Referenced Varactor
25 – 32	Programmable M Counter Programming, M2B0 – M2B1	
33 – 34	Programmable A Counter Programming, A2B0 – A2B1	
35	Synthesizer Power down (For External Synthesizer Mode)	"0" = Internal Synthesizer "1" = External Synthesizer

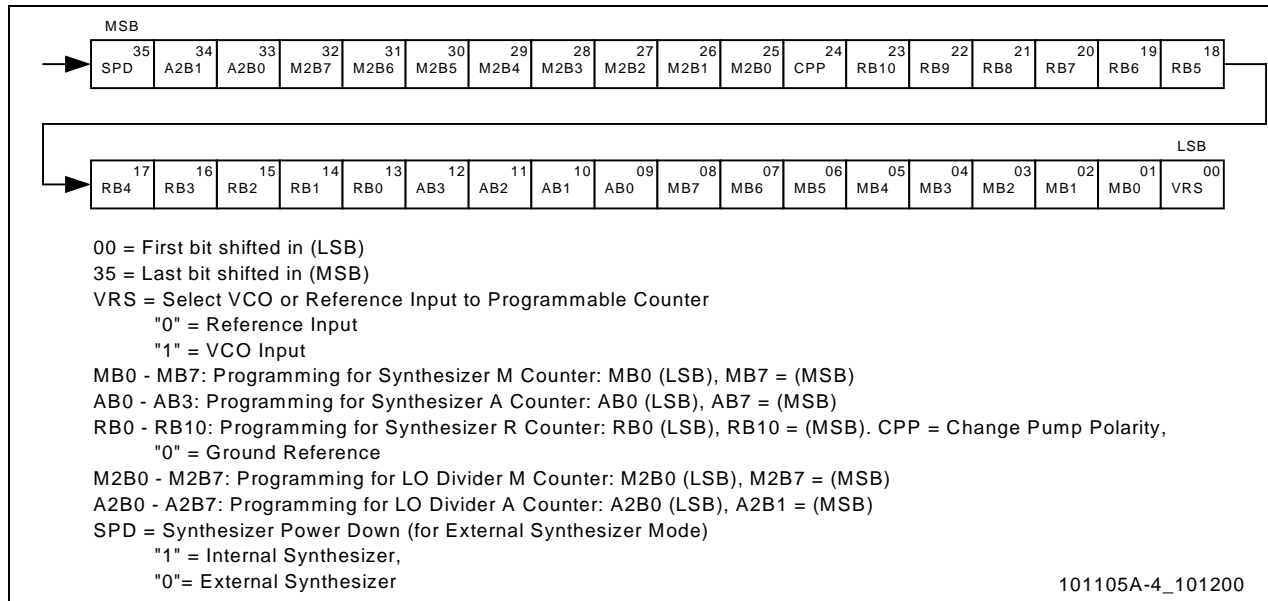


Figure 4. 3-Wire Programming Data Pattern

Table 3. Signal Pin Names and Definitions (1 of 2)

Pin No.	Signal Name	Description
1	LNA_G	LNAs gain control command
2	MXIH	1900 MHz band mixer Input
3	MIXIL	800 MHz band mixer Input
4	BAND	800 MHz/1900 MHz band select command
5	CHIP_EN	Chip power down select command
6	LOIH	1900 MHz RF mixer LO input
7	LOIL	800 MHz RF mixer LO input
8	VCC_MX	RF mixer VCC
9	STANDBY	Control signal to enable RF LO buffers and VHF synthesizer
10	IQ/IF	I/Q or IF output select command
11	MXOUT+	RF mixer output. Open Collector.
12	MXOUT-	RF mixer output. Open Collector.
13	MX2I+	IF mixer input
14	MX2I-	IF mixer input
15	VCC_IF	IF section VCC
16	IFBYPASS	IF mixer bias decoupling
17	MX2OUT	IF mixer output
18	Vvga	Analog voltage input for VGA gain control
19	VCC_VGA	VGA section VCC
20	VGAI-	VGA input
21	VGAI+	VGA input
22	FB_CAP	VGA DC feedback filter capacitor connection
23	LATCH_EN	Enable input line for internal synthesizer programming
24	CLK	Serial clock input line for internal synthesizer programming
25	DATA	Serial data input line for internal synthesizer programming
26	REFIN	19.44 MHz reference oscillator input. Requires VCC/2 DC bias.

Table 3. Signal Pin Names and Definitions (2 of 2)

Pin No.	Signal Name	Description
27	LP_FIL	IF PLL external loop filter connection
28	VCC_SYN	Synthesizer section VCC
29	VCO+	IF VCO external tank circuit connection
30	VCO-	IF VCO external tank circuit connection
31	VCC_VCO	VCO section VCC
32	EXT_LOIN	External LO input for quadrature detector. Requires VCC/2 DC bias.
33	I+	I Channel data output
34	I-	I Channel data output
35	Q+	Q Channel data output
36	Q-	Q Channel data output
37	IF_O-	Buffered IF output
38	IF_O+	Buffered IF output
39	EXT_LO	Programmable counter ON/OFF control signal for choosing between Internal and External demodulator LO.
40	NC1	No connect
41	LNA_INH	1900 MHz band LNA input
42	LNA_INL	800 MHz band LNA input
43	NC2	No connect
44	VCC1_LNA	Bias VCC for LNAs
45	VCC2_LNAL	VCC for cellular band LNA.
46	VCC2_LNAH	VCC for PCS band LNA.
47	LNA_OL	800 MHz band LNA output. Requires external matching and AC coupling.
48	LNA_OH	1900 MHz band LNA output. Requires external matching and AC coupling.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	VCC	-0.3		+3.6	V
Input voltage range		-0.3		VCC	V
LNA input power				+5	dBm
Power dissipation				600	mW
Ambient operating temperature		-40		+85	°C
Storage temperature		-40		+125	°C

Table 5. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage		2.7	3.0	3.6	V
Logic level high		1.9			V
Logic level low				0.8	V
Supply current in cellular TDMA/AMPS, high gain			30		mA
Supply current in cellular TDMA/AMPS, low gain			28		mA
Supply current in PCS TDMA, high gain			33		mA
Supply current in PCS TDMA, low gain			30		mA
Supply current in cellular IF, high gain			29		mA
Supply current in PCS IF, high gain			32		
Supply current in sleep mode			TBD		μA

Table 6. Electrical Characteristics (1 of 5)

VCC = 3.0 V, TA = 25 °C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
LNA 800						
Input frequency band			869		894	MHz
Noise figure, high gain		15 to 50 °C		2	2.3	dB
Noise figure, low gain		-40 to +85 °C			2.75 20	
High gain		-40 to +85 °C	15	16	17	dB
Low gain				-15		
Output P1dB		At high/low gain		≥ 0 / ≥ -25		dBm
Output IP3, high gain		15 to 50 °C	9	10		dBm
Output IP3, low gain		-40 to +85 °C	8 -15			
Input impedance		External match and AC coupled		TBD		Ω
Output impedance		Internal match and internal AC coupled		50		Ω
Output return loss			-14			dB
Reverse isolation		At high/low gain		≥ 30 / ≥ -15		dB
Input damage threshold				10		dBm
Switched gain, current reduction				1.5		mA
MIX 800						
Input frequency band			869		894	MHz
Output frequency band			120		180	MHz
LO frequency band			989		1074	MHz
Power gain		Differential gain to 400 Ω load. -40 to +85 °C	9	10	11	dB
Noise figure		15 to 50 °C -40 to +85 °C		8.5	9.0 10	dB
Output IP3		15 to 50 °C -40 to +85 °C	14 13	15		dBm
Output P1dB				5		dBm
Input impedance		External match to 50 Ω and AC coupled.		450		Ω

Table 6. Electrical Characteristics (2 of 5)

VCC = 3.0 V, T_A = 25 °C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
MIX 800 (continued)						
Mixer spurious performance: 2x(LO – RF); (LO – RF)/2 3x(LO – RF); (LO – RF)/3		LO = –10 dBm RF = –50 dBm	–59	–60 –60		dBc dBc
Output impedance		Set externally using defined circuit topology.		400		Ω
LO input port impedance		Internal match. External AC coupled		50		Ω
LO input port load isolation		Active/standby transition	–20			dB
Required LO level			–13	–10	–5	dBm
LO to RF port isolation		Referenced to LO input pin		30		dB
LO to IF port isolation		Referenced to LO input pin		20		dB
LNA 1900						
Input frequency band			1930		1990	MHz
Noise figure, high gain		15 to 50 °C –40 to +85 °C		2.5	2.8 3.3	dB
Noise figure, low gain					18	
High gain Low gain		–40 to +85 °C	15	16 –15	17	dB
Output P1dB				≥ 0 / ≥ –25		dBm
Output IP3, high gain		15 to 50 °C –40 to +85 °C	9 8	10		dBm
Output IP3, low gain			–15			
Input impedance		External match and AC coupled.		TBD		Ω
Output impedance		Internal match and internal AC coupled.		50		Ω
Output return loss			–14			dB
Reverse isolation		At high/low gain		≥ 30 / ≥ –15		dB
Input damage threshold				10		dBm
Switched gain, current reduction				2.5		mA
MIX 1900						
Input frequency band			1930		1990	MHz
Output frequency band			120		180	MHz
LO frequency band			2050		2170	MHz
Power gain		–40 to +85 °C	9	10	11	dB
Noise figure		15 to 50 °C –40 to +85 °C		9.0	10.3 11	dB
Output IP3		15 to 50 °C –40 to +85 °C	14 13	15		dBm
Output P1dB				5		dBm
Input impedance		External match to 50 Ω and AC coupled.		200		Ω
Mixer spurious performance: 2x(LO – RF); (LO – RF)/2 3x(LO – RF); (LO – RF)/3		LO = –10 dBm RF = –50 dBm	–59	–60 –60		dBc dBc

Table 6. Electrical Characteristics (3 of 5)

VCC = 3.0 V, TA = 25 °C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
MIX 1900 (continued)						
Output impedance		Set externally using defined circuit topology.		400		Ω
LO input port impedance		Internal match. External AC coupled		50		Ω
LO input port load isolation		Active/standby transition	-20			dB
Required LO level			-13	-10	-5	dBm
LO to RF port isolation		Referenced to LO input pin		30		dB
LO to IF port isolation		Referenced to LO input pin		20		dB
MIX-2						
Input frequency range			120		180	MHz
Output frequency				450		kHz
Power gain		-40 to +85 °C 15 dB of power gain = 22 dB of Volt gain	14	15	16	dB
Noise figure		15 to 50 °C -40 to +85 °C		12	13 14	dB
Input impedance		Differential, possible to use single-ended also		400		Ω
Output P1dB				-8		dBm
Output IP3		15 to 50 °C -40 to +85 °C	1 0	2		dBm
Required LO level for external source		High input impedance. In place of the internal VCO		300		mVp-p
LO leakage at RF port		Assuming 50 Ω calculation or match			-40	dBm
LO leakage at IF port		Assuming 50 Ω calculation or match			-30	dBm
Output impedance		Single-ended	1.8k	2k	2.2k	Ω
VGA 450						
Frequency range			300	450	500	kHz
Dynamic range				70		dB
Maximum voltage gain Maximum power gain				54 70		dB dB
Input noise figure, maximum gain Input noise figure, minimum gain				43	15	dB
Input P1dB @ Gain = 0 dB				-20		dBm
Output IP3 @ Gain = 0 dB		IP3 will remain constant over the entire gain range		-10		dBm
Input impedance		Differential		2k		Ω
Gain slope				45		dB/V
VGA control		Analog control voltage	0.25		2.5	V

Table 6. Electrical Characteristics (4 of 5)

VCC = 3.0 V, TA = 25 °C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
I/Q Demod + LFAMP						
Voltage gain				30		dB
Noise figure				25		dB
Filter response				2 poles @ 200 kHz		
Input P1dB				-20		dBm
Output load termination				10 k Ω // 5 pF		
Output signal level		Differential. 2.0 Vp-p represents 1 dB compression point.		0.5	2.0	Vp-p
Output IP3 calculated using 50 Ω		15 to 50 °C - 40 to + 85 °C	18 16	20		dBm
I/Q gain imbalance					\pm 0.25	dB
I/Q phase imbalance					2	degrees
DC offset: I to I and Q to I/Q I channel to Q channel I and Q to DC bias					20 30 8	mV mV mV
IF Buffered Output						
Voltage gain				20		dB
Output signal level		Differential		0.16		Vp-p
Frequency				450		kHz
PLL Synthesizer						
Input reference frequency			14.40	19.44		MHz
Reference divider ratio		Steps of unity	18		2047	
Feedback divider input frequency			90		250	MHz
Feedback divider ratio		16/17 prescaler, steps of unity	256		2667	
Phase detector noise floor					-154	dBc/Hz
Phase detector gain				0.32		mA/rad
IF VCO						
Frequency			90	150	250	MHz
Tuning sensitivity				10		MHz/V
Harmonic levels				TBD		dBc
Phase noise @ 60 kHz		External tank circuitry, uses 0603 size multilayer resonator inductor. -40 to 85 °C		-113	-110	dBc/Hz
Programmable Divider (Div-P)						
Input frequency		From internal VCO or reference oscillator input (REFIN)		150 or 19.44 input		MHz
Output frequency				1.8		MHz
Counter ratio			8		255	
External input level		Internal divider disabled		250		mVp-p

Table 6. Electrical Characteristics (5 of 5)

VCC = 3.0 V, TA = 25 °C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
3-Wire Bus						
Data to clock setup time (See Figure 5)	T _{CS}		50			nsec
Data to clock hold time (See Figure 5)	T _{CH}		100			nsec
Clock pulse width high (See Figure 5)	T _{CWH}		50			nsec
Clock pulse width low (See Figure 5)	T _{CWL}		50			nsec
Clock to load enable setup time (See Figure 5)	T _{ES}		50			nsec
Load enable pulse width (See Figure 5)	T _{EW}		50			nsec

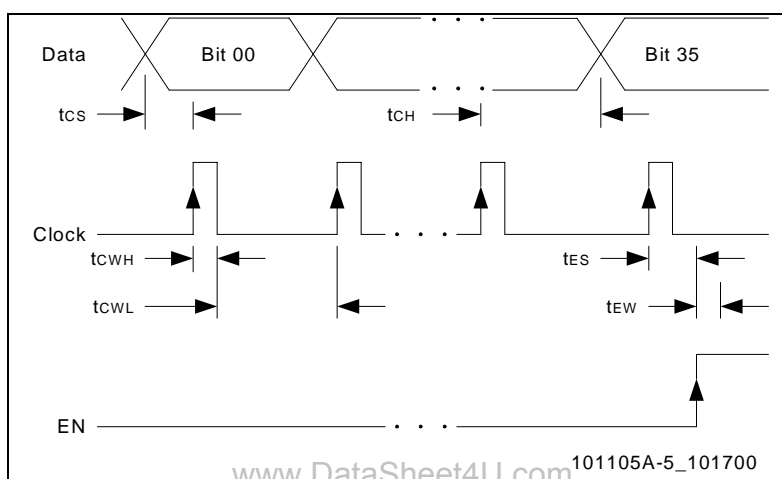


Figure 5. 3-Wire Bus Timing Diagram

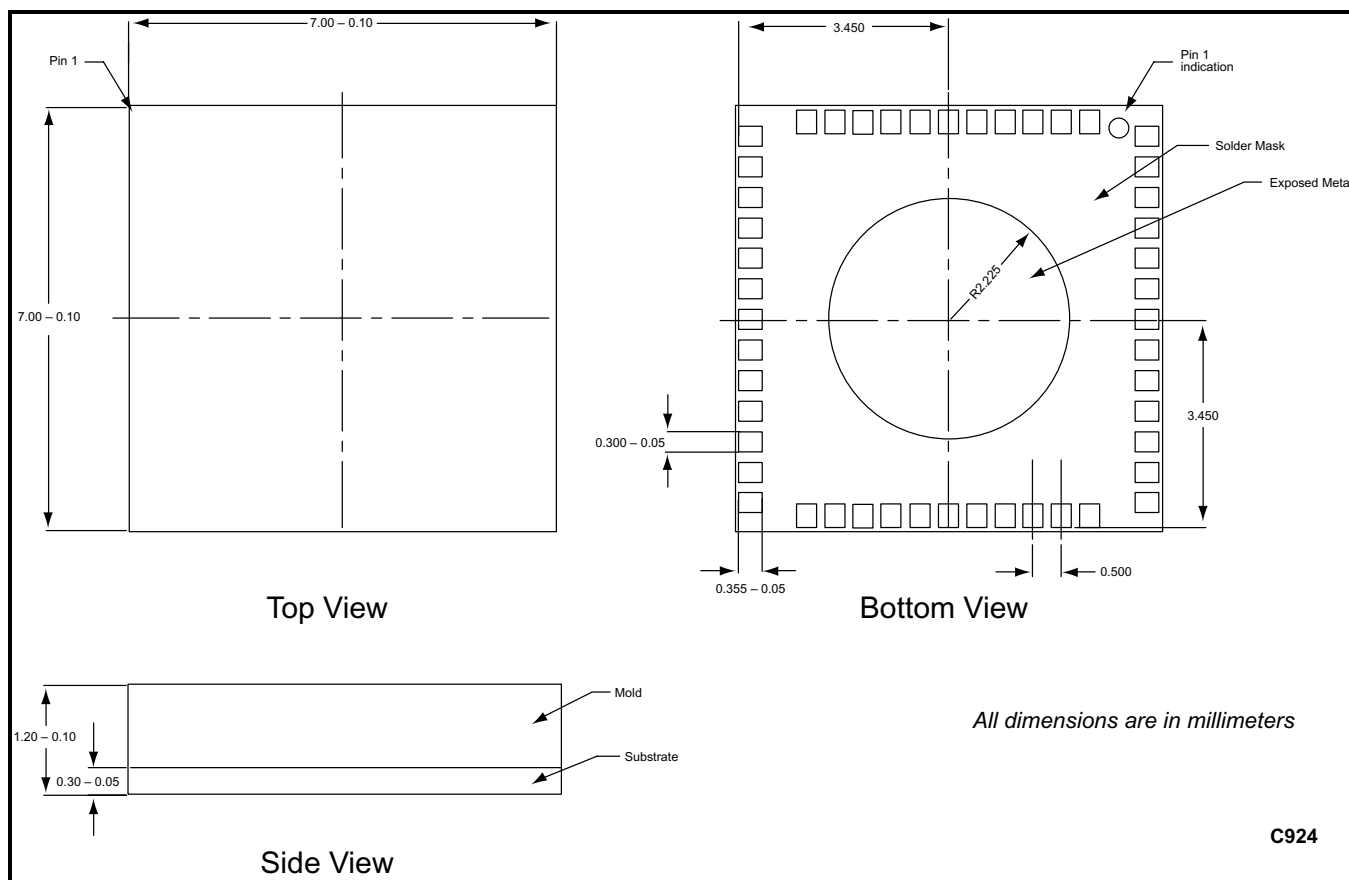


Figure 6. 48-Pin, 7x7 LGA Package Dimensions

Ordering Information

Table 7. Ordering Information

Model Name	Manufacturing Part Number
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