Advance Information

This document contains information on a product under development. The parametric information contains target parameters that are subject to change.

CONEXANT™

CX77314

PA Module for Quad-band GSM850/900 DCS1800 PCS1900 / GPRS Applications

The CX77314 Power Amplifier Module (PAM) is designed in a compact form factor for quad-band cellular handsets comprising GSM850/900, DCS1800, and PCS1900 operation. The PAM also supports Class 10 General Packet Radio Service (GPRS) multi-slot operation.

The module consists of a GSM850/900 PA block and a DCS1800/PCS1900 PA block, impedance-matching circuitry for 50 Ω input and output impedances, and interface circuitry. The two separate Heterojunction Bipolar Transistor (HBT) PA blocks are fabricated onto a single Gallium Arsenide (GaAs) die. One PA block supports the GSM850/900 bands and the other PA block supports the DCS1800 and PCS1900 bands. Both PA blocks share common power supply pins to distribute current. A custom CMOS integrated circuit provides the internal interface circuitry, including a current amplifier that minimizes the required power control current (I_{APC}) to 10 μA, typical. The GaAs die, the Silicon (Si) die, and the passive components are mounted on a multi-layer laminate substrate. The assembly is encapsulated with plastic overmold.

The RF input and output ports are internally matched to 50 Ω to reduce the number of external components for a quad-band design. Extremely low leakage current (10 μA, typical) of the dual PA module maximizes handset standby time. The CX77314 also contains band select switching circuitry to select GSM (logic 0) and DCS/PCS (logic 1) as determined from the Band Select (BS) signal. In the functional block diagram shown below, the BS pin selects the PA output (DCS/PCS OUT or GSM850/900 OUT) while the Analog Power Control (APC) controls the level of output power.

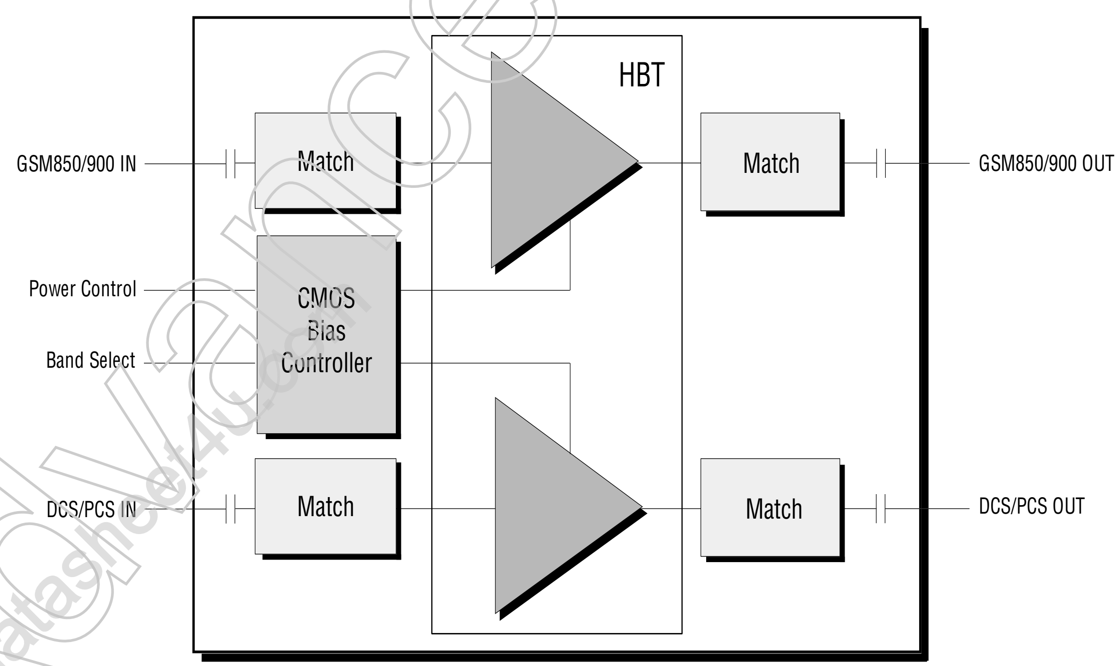
Distinguishing Features

- High efficiency
  - GSM850 55%
  - GSM900 55%
  - DCS 45%;
  - PCS 45%
- Input/output matching
  - 50 Ω internal
- Small outline
  - 8 mm × 10 mm
- Low profile
  - 1.5 mm maximum
- Low APC current
  - 10 μA, typical
- Gold plated, lead-free contacts

Applications

- Quad-band cellular handsets encompassing
  - GSM850/900 (Class 4)
  - DCS1800
  - PCS1900, and
  - GPRS (Class 10) multi-slot operation

Functional Block Diagram



Electrical Specifications

The following tables list the electrical characteristics of the CX77314 Power Amplifier Module. Table 1 lists the absolute maximum ratings and Table 2 shows the recommended operating conditions. Table 3 lists the electrical characteristics of the CX77314 for modes GSM850, GSM900, DCS1800 and PCS1900. Figure 1 is a diagram of a typical CX77314 application.

The CX77314 is a static-sensitive electronic device and should not be stored or operated near strong electrostatic fields. Detailed information on device dimensions, pin descriptions, packaging and handling can be found in later sections of this data sheet.

Table 1. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Input Power (P_{IN})	—	15	dBm
Supply Voltage (V_{CC}), Standby, $V_{APC} \leq 0.3$ V	—	7	V
Control Voltage (V_{APC})	–0.5	$V_{CC_{MAX}} - 0.2$ (See Table 3)	V
Storage Temperature	–55	+100	°C

Table 2. Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Unit
Supply Voltage (V_{CC})	2.9	3.5	4.8V(1)	V
Supply Current (I_{CC})	0		2.5(1)	A
Operating Case Temperature (T_{CASE})				°C
1-Slot (12.5% duty cycle)	–20		100	
2-Slot (25% duty cycle)	–20		90	
3-Slot (37.5% duty cycle)	–20		75	
4-Slot (50% duty cycle)	–20		60	

NOTE(S):
(1) For charging conditions with $V_{CC} > 4.8$ V, derate I_{CC} linearly down to 0.5 A max at $V_{CC} = 5.5$ V.

Table 3. CX77314 Electrical Specifications[1] *(1 of 8)*

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
General						
Supply voltage	V_{CC}	—	2.9	3.5	4.8	V
Power control current	I_{APC}	—	—	10	100	µA
Standby Mode Leakage current	I_q	$V_{CC} \leq 4.5$ V $V_{APC} \leq 0.3$ V $T_{CASE} = +25$ °C $P_{IN} \leq -60$ dBm	—	—	10	µA
APC Enable Threshold	$V_{APC_{TH}}$	—	200	—	500	mV
APC Enable Switching Delay	t_{SW}	Time from $V_{APC} \geq V_{APC_{TH}}$ until $P_{OUT} \leq (P_{OUT\_FINAL} - 3$ dB)	1		3	µs
GSM850 Mode (f = 824 to 849 MHz and P_{IN} = 6 to 12 dBm)						
Frequency range	f	—	824	—	849	MHz
Input power	P_{IN}	—	6	—	12	dBm
Analog power control voltage	V_{APC}	$P_{OUT} \leq 35$ dBm	0.1	—	2.1	V
Power Added Efficiency	PAE	$V_{CC} = 3.5$ V $P_{OUT} \geq 34.5$ dBm $V_{APC} \approx 2.0$ V, pulse width 577 µs, duty cycle 1:8 $T_{CASE} = +25$ °C	50	55	—	%
2nd to 13th harmonics	$2f_0$ to $13f_0$	BW = 3 MHz 5 dBm $\leq P_{OUT} \leq$ 35 dBm	—	–20	–10	dBm
Output power	P_{OUT}	$V_{CC} = 3.5$ V $V_{APC} \approx 2.0$ V $T_{CASE} = +25$ °C	34.5	35.0	—	dBm
	$P_{OUT_{MAX\ LOW\ VOLTAGE}}$	$V_{CC} = 2.9$ V $V_{APC} \leq 2.6$ V $T_{CASE} = -20$ °C to +100 °C (See Table 2 for multislot.) $P_{IN} = 7$ dBm	32.5	33	—	dBm
	$P_{OUT_{MAX\ HIGH\ VOLTAGE}}$	$V_{CC} = 4.8$ V $V_{APC} \leq 2.6$ V $T_{CASE} = -20$ °C to +100 °C (See Table 2 for multislot.) $P_{IN} = 7$ dBm	32.5	33	—	dBm
Input VSWR	Γ_{IN}	P_{OUT} = 5 to 35 dBm, controlled by V_{APC}	—	1.5:1	2.2:1	
Forward isolation	$P_{OUT_{STANDBY}}$	$P_{IN} = 12$ dBm $V_{APC} = 0.3$ V	—	–30	–25	dBm

Table 3. CX77314 Electrical Specifications[1] *(2 of 8)*

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Switching time	τ_{RISE}, τ_{FALL}	Time from P_{OUT} = –10 dBm to P_{OUT} = +5 dBm, $\tau \approx$ 90%	—	2.5	3.0	µs
		Time from P_{OUT} = –10 dBm to P_{OUT} = +20 dBm, $\tau \approx$ 90%	—	2.0	3.0	µs
		Time from P_{OUT} = –10 dBm to P_{OUT} = +34.5 dBm, $\tau \approx$ 90%	—	2.0	2.5	µs
Spurious	Spur	All combinations of the following parameters: V_{APC} = controlled[2] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > –36 dBm			
Load mismatch	Load	All combinations of the following parameters: V_{APC} = controlled[2] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise power	P_{NOISE}	At f_0 + 20 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 34.5 dBm T_{CASE} = +25 °C	—	—	–82	dBm
		At f_0 + 10 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 34.5 dBm T_{CASE} = +25 °C	—	—	–76	dBm
		At 1805 to 1880 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 34.5 dBm T_{CASE} = +25 °C	—	—	–84	dBm
Coupling of Fundamental, 2nd, and 3rd harmonic from the GSM band into the DCS/PCS band	f_0	Measured at the DCS/PCS output, –15 dBm ≤ P_{OUT} ≤ 34.5 dBm	—	6	9	dBm
	$2f_0$	Measured at the DCS/PCS output, –15 dBm ≤ P_{OUT} ≤ 34.5 dBm	—	–25	–20	dBm
	$3f_0$	Measured at the DCS/PCS output, –15 dBm ≤ P_{OUT} ≤ 34.5 dBm	—	–18	–15	dBm

Table 3. CX77314 Electrical Specifications[1] *(3 of 8)*

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
GSM900 Mode (f = 880 to 915 MHz and P_{IN} = 6 to 12 dBm)						
Frequency range	f	—	880	—	915	MHz
Input power	P_{IN}	—	6	—	12	dBm
Analog power control voltage	V_{APC}	$P_{OUT} \leq 35$ dBm	0.1	—	2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V $P_{OUT} \geq 34.5$ dBm $V_{APC} \approx 2.0$ V, pulse width 577 µs, duty cycle 1:8 T_{CASE} = +25 °C	50	55	—	%
2^{nd} to 13^{th} harmonics	$2f_0$ to $13f_0$	BW = 3 MHz 5 dBm $\leq P_{OUT} \leq$ 35 dBm	—	–20	–10	dBm
Output power	P_{OUT}	V_{CC} = 3.5 V $V_{APC} \approx 2.0$ V T_{CASE} = +25 °C	34.5	35.0	—	dBm
	$P_{OUT_{MAX\ LOW\ VOLTAGE}}$	V_{CC} = 2.9 V $V_{APC} \leq 2.6$ V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 7 dBm	32.5	33	—	dBm
	$P_{OUT_{MAX\ HIGH\ VOLTAGE}}$	V_{CC} = 4.8 V $V_{APC} \leq 2.6$ V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 7 dBm	32.5	33	—	dBm
Input VSWR	Γ_{IN}	P_{OUT} = 5 to 35 dBm, controlled by V_{APC}	—	1.5:1	2.0:1	
Forward isolation	$P_{OUT_{STANDBY}}$	P_{IN} = 12 dBm V_{APC} = 0.3 V	—	–30	–25	dBm
Switching time	τ_{RISE}, τ_{FALL}	Time from P_{OUT} = –10 dBm to P_{OUT} = +5 dBm, $\tau \approx 90\%$	—	2.5	3.0	µs
		Time from P_{OUT} = –10 dBm to P_{OUT} = +20 dBm, $\tau \approx 90\%$	—	2.5	3.0	µs
		Time from P_{OUT} = –10 dBm to P_{OUT} = +34.5 dBm, $\tau \approx 90\%$	—	2.0	2.5	µs
Spurious	Spur	All combinations of the following parameters: V_{APC} = controlled[2] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > –36 dBm			

Table 3. CX77314 Electrical Specifications[1] *(4 of 8)*

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Load mismatch	Load	All combinations of the following parameters: V_{APC} = controlled[2] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise power	P_{NOISE}	At f_0 + 20 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 34.5 dBm T_{CASE} = +25 °C	—	—	–82	dBm
		At f_0 + 10 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 34.5 dBm T_{CASE} = +25 °C	—	—	–76	dBm
		At 1805 to 1880 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 34.5 dBm T_{CASE} = +25 °C	—	—	–84	dBm
Coupling of Fundamental, 2nd, and 3rd harmonic from the GSM band into the DCS/PCS band	f_0	Measured at the DCS/PCS output, –15 dBm ≤ P_{OUT} ≤ 34.5 dBm	—	6	9	dBm
	$2f_0$	Measured at the DCS/PCS output, –15 dBm ≤ P_{OUT} ≤ 34.5 dBm	—	–25	–20	dBm
	$3f_0$	Measured at the DCS/PCS output, –15 dBm ≤ P_{OUT} ≤ 34.5 dBm	—	—	–20	dBm

Table 3. CX77314 Electrical Specifications[1] (5 of 8)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
DCS1800 Mode (f = 1710 to 1785 MHz and P_{IN} = 6 to 11 dBm)						
Frequency range	f	—	1710	—	1785	MHz
Input power	P_{IN}	—	6	—	11	dBm
Analog power control voltage	V_{APC}	$P_{OUT} \leq 32.5$ dBm	0.1	—	2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V $P_{OUT} \geq 32$ dBm $V_{APC} \approx 2.0$ V, pulse width 577 µs, duty cycle 1:8 T_{CASE} = +25 °C	43	46	—	%
	$PAE_{LOW\ INPUT}$	V_{CC} = 3.5 V $P_{OUT} \geq 32$ dBm $V_{APC} \approx 2.0$ V pulse width 577 µs, duty cycle 1:8 T_{CASE} = +25 °C P_{IN} = 4 dBm	—	45	—	%
2nd to 7th harmonics	$2f_0$	BW = 3 MHz, 0 dBm ≤ P_{OUT} ≤ 32 dBm	—	—	–7	dBm
	$3f_0$	BW = 3 MHz, 0 dBm ≤ P_{OUT} ≤ 32 dBm	—	—	–7	dBm
	$4f_0$ to $7f_0$	BW = 3 MHz, 0 dBm ≤ P_{OUT} ≤ 32 dBm	—	–20	–10	dBm
Output power	P_{OUT}	V_{CC} = 3.5 V $V_{APC} \approx 2.0$ V T_{CASE} = +25 °C	32	32.5	—	dBm
	$P_{OUT\ MAX\ LOW\ INPUT}$	V_{CC} = 3.5 V $V_{APC} \approx 2.0$ V T_{CASE} = +25 °C P_{IN} = 4 dBm	—	32.1	—	dBm
	$P_{OUT\ MAX\ LOW\ VOLTAGE}$	V_{CC} = 2.9 V $V_{APC} \leq 2.6$ V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 6 dBm	29.0	30.5	—	dBm
	$P_{OUT\ MAX\ HIGH\ VOLTAGE}$	V_{CC} = 4.8 V $V_{APC} \leq 2.6$ V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 6 dBm	29.0	30.5	—	dBm
Input VSWR	Γ_{IN}	P_{OUT} = 0 to 32 dBm, controlled by V_{APC}	—	—	2:1	—
Forward isolation	$P_{OUT\ STANDBY}$	P_{IN} = 11 dBm V_{APC} = 0.3 V	—	–40	–35	dBm

Table 3. CX77314 Electrical Specifications[1] *(6 of 8)*

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Switching time	τ_{RISE}, τ_{FALL}	Time from P_{OUT} = –10 dBm to P_{OUT} = 0 dBm, $\tau \approx$ 90%	—	—	2	µs
		Time from P_{OUT} = –10 dBm to P_{OUT} = +20 dBm, $\tau \approx$ 90%	—	—	2	µs
		Time from P_{OUT} = –10 dBm to P_{OUT} = +32 dBm, $\tau \approx$ 90%	—	—	2	µs
Spurious	Spur	All combinations of the following parameters: V_{APC} = controlled[3] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > –36 dBm			
Load mismatch	Load	All combinations of the following parameters: V_{APC} = controlled[3] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise power	P_{NOISE}	At f_0 + 20 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 32 dBm T_{CASE} = +25 °C	—	—	–78	dBm
		At 925 to 960 MHz, RBW = 100 kHz. V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 32 dBm T_{CASE} = +25 °C	—	—	–95	dBm

Table 3. CX77314 Electrical Specifications [1] *(7 of 8)*

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
PCS1900 Mode (f = 1850 to 1910 MHz and P_{IN} = 6 to 11 dBm)						
Frequency range	f	—	1850	—	1910	MHz
Input power	P_{IN}	—	6	—	11	dBm
Analog power control voltage	V_{APC}	$P_{OUT} \le 32.5$ dBm	0.1	—	2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V $P_{OUT} \ge 32$ dBm $V_{APC} \approx 2.0$ V, pulse width 577 µs, duty cycle 1:8 T_{CASE} = +25 °C	43	46		%
	$PAE_{LOW\ INPUT}$	V_{CC} = 3.5 V $P_{OUT} \ge 32$ dBm $V_{APC} \approx 2.0$ V pulse width 577 µs, duty cycle 1:8 T_{CASE} = +25 °C P_{IN} = 4 dBm	—	44.5	—	%
2nd to 7th harmonics	$2f_0$	BW = 3 MHz, 0 dBm ≤ P_{OUT} ≤ 32 dBm	—	—	–7	dBm
	$3f_0$	BW = 3 MHz, 0 dBm ≤ P_{OUT} ≤ 32 dBm	—	—	–7	dBm
	$4f_0$ to $7f_0$	BW = 3 MHz, 0 dBm ≤ P_{OUT} ≤ 32 dBm	—	–20	–10	dBm
Output power	P_{OUT}	V_{CC} = 3.5 V $V_{APC} \approx 2.0$ V T_{CASE} = +25 °C	32	32.5	—	dBm
	$P_{OUT\ MAX\ LOW\ INPUT}$	V_{CC} = 3.5 V $V_{APC} \approx 2.0$ V T_{CASE} = +25 °C P_{IN} = 4 dBm	—	32.3	—	dBm
	$P_{OUT\ MAX\ LOW\ VOLTAGE}$	V_{CC} = 2.9 V $V_{APC} \le 2.6$ V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 6 dBm	29.0	30.5	—	dBm
	$P_{OUT\ MAX\ HIGH\ VOLTAGE}$	V_{CC} = 4.8 V $V_{APC} \le 2.6$ V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 6 dBm	29.0	30.5	—	dBm
Input VSWR	Γ_{IN}	P_{OUT} = 0 to 32 dBm controlled by V_{APC}	—	—	2:1	—
Forward isolation	$P_{OUT\ STANDBY}$	P_{IN} = 11 dBm V_{APC} = 0.3 V	—	–40	–35	dBm

Table 3. CX77314 Electrical Specifications[1] *(8 of 8)*

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Switching time	τ_{RISE}, τ_{FALL}	Time from P_{OUT} = –10 dBm to P_{OUT} = 0 dBm, τ ≈ 90%	—	—	2	µs
		Time from P_{OUT} = –10 dBm to P_{OUT} = +20 dBm, τ ≈ 90%	—	—	2	µs
		Time from P_{OUT} = –10 dBm to P_{OUT} = +32 dBm, τ ≈ 90%	—	—	2	µs
Spurious	Spur	All combinations of the following parameters: V_{APC} = controlled[3] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > –36 dBm			
Load mismatch	Load	All combinations of the following parameters: V_{APC} = controlled[3] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise power	P_{NOISE}	At f_0 + 20 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 32 dBm T_{CASE} = +25 °C	—	—	–77	dBm
		At 869 to 894 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 32 dBm T_{CASE} = +25 °C	—	—	–95	dBm

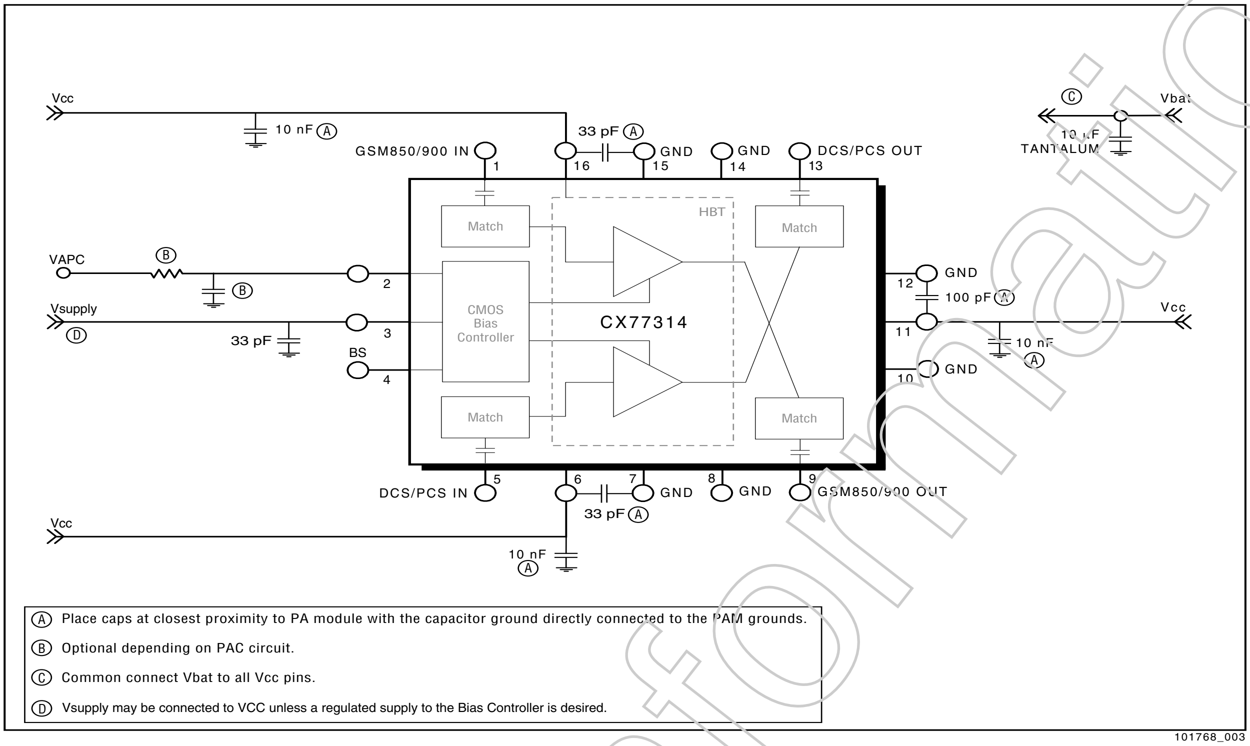
NOTE(S):

(1) Unless specified otherwise: T_{CASE} = –20 to max. operating temperature (see Table 2), RL = 50Ω, pulsed operation with pulse width ≤ 2308 µs and duty cycle ≤ 4:8, V_{CC} = 2.9 V to 4.8 V.

(2) I_{CC} = 0A to xA, where x = current at P_{OUT} = 34.5 dBm, 50 Ω load, and V_{CC} = 3.5 V.

(3) I_{CC} = 0A to xA, where x = current at P_{OUT} = 32.0 dBm, 50 Ω load, and V_{CC} = 3.5 V.

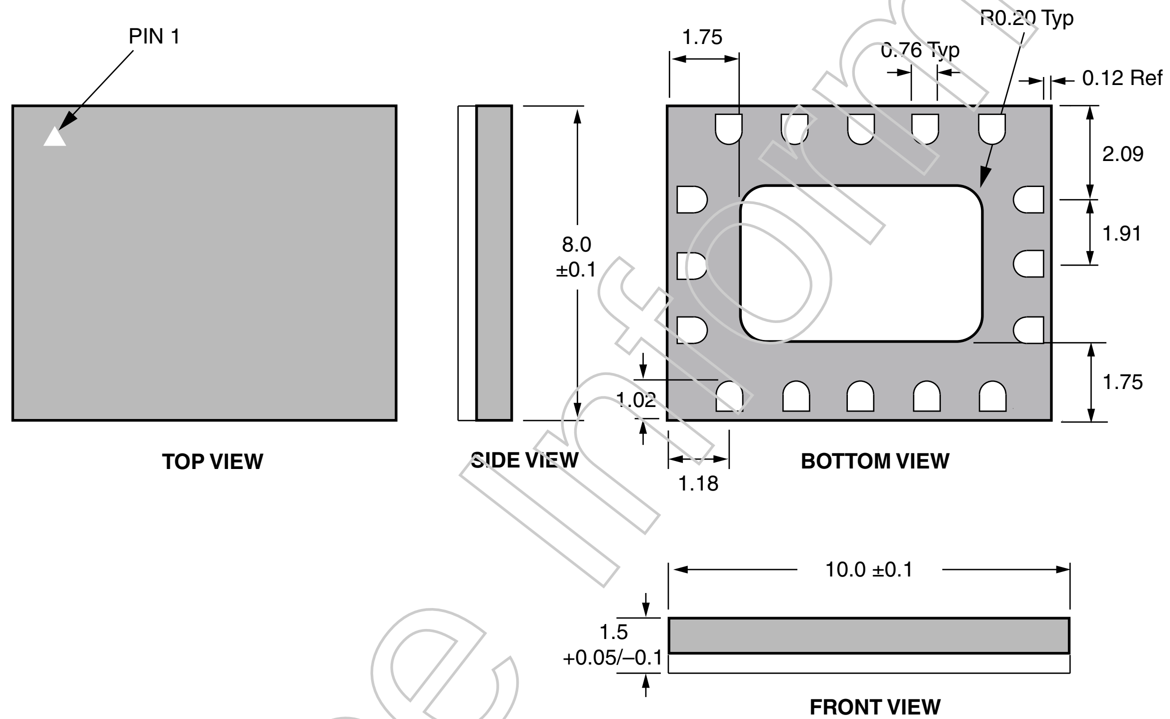
Figure 1. Typical CX77314 PAM Application



Package Dimensions and Pin Descriptions

Figure 2 is a mechanical diagram of the pad layout for the CX77314, a 16-pin leadless quad-band PA module, and Figure 3 shows the pin configuration. The pin numbering convention starts with pin 1 in the upper left, as indicated in Figure 3, and increments counter-clockwise around the package. Table 4 lists the pin names and descriptions.

Figure 2. CX77314 PAM Package Dimensions—16-pin Leadless (All Views)



NOTE(S):
1. All contact points are gold plated, lead free-surfaces.
2. All dimensions are in millimeters.

101788_004

Figure 3. CX77314 PAM Pin Configuration—16-Pin Leadless (Top View)

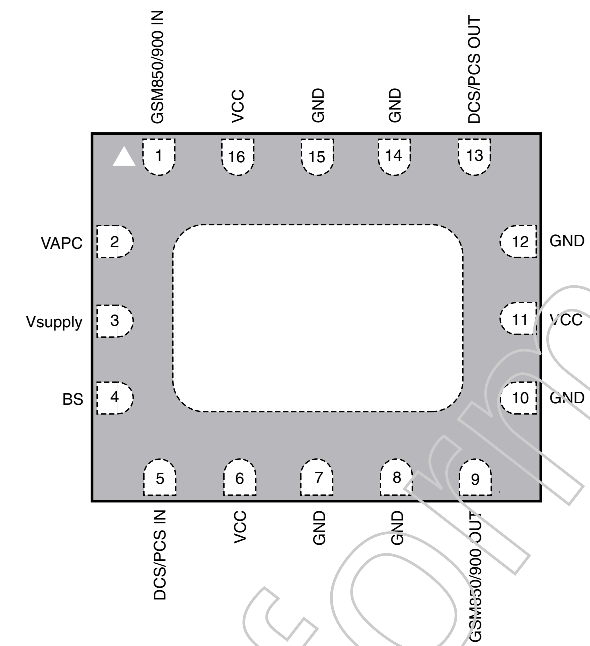


Table 4. CX77314 Signal Description

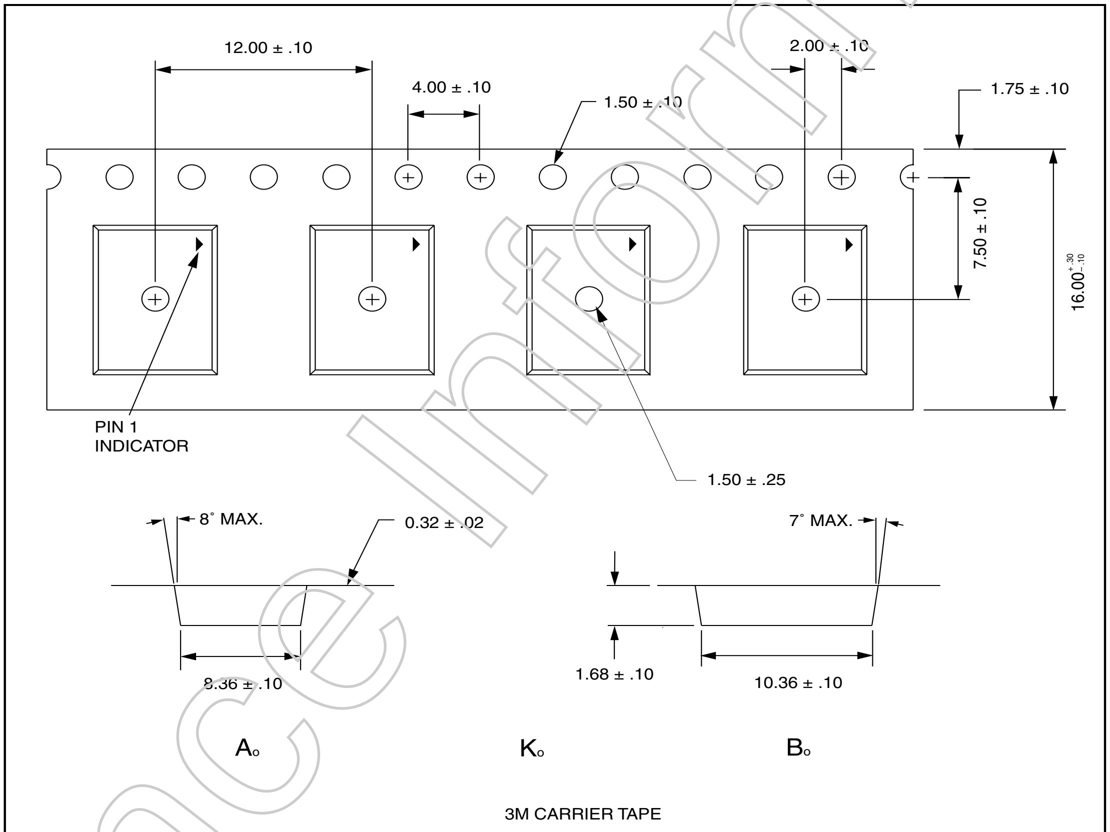
Pin	Name	Description
1	GSM850/900 IN	RF input 824–915 MHz
2	VAPC	Power Control Bias Voltage
3	Vsupply	DC Supply to CMOS Bias Controller
4	BS	Band Select
5	DCS/PCS IN	RF input 1710–1910 MHz
6	VCC	VCC (to GSM 1st stage and DCS 1st stage)
7	GND	RF and DC Ground
8	GND	RF and DC Ground
9	GSM850/900 OUT	RF Output 824–915 MHz
10	GND	RF and DC Ground
11	VCC	VCC (to GSM and DCS Final stages)
12	GND	RF and DC Ground
13	DCS/PCS OUT	RF Output 1710–1910 MHz
14	GND	RF and DC Ground
15	GND	RF and DC Ground
16	VCC	VCC (to DCS 2nd stage)
GND PAD	GND	Ground Pad, bottom

Package and Handling Information

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. For additional details on both attachment techniques, precautions, and handling procedures recommended by Conexant, please refer to *Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752*.

Production quantities of this product are shipped in the standard tape and reel format illustrated in Figure 4 below.

Figure 4. CX77314 Tape and Reel Dimensions



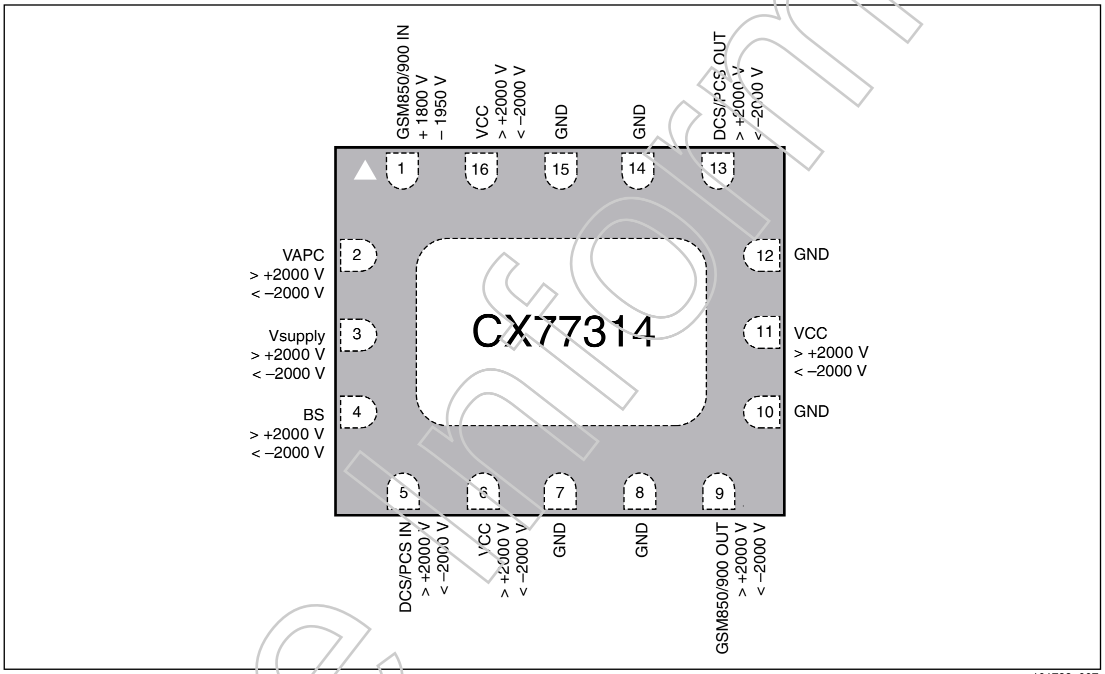
NOTES:
1. Carrier tape material: Black conductive polycarbonate.
2. Carrier tape part No.: 3M068051
3. Cover tape material: Transparent conductive PSA.
4. Cover tape width: 13.3 mm.
5. Number of parts per 13 inch x 24 mm reel: 2000.
6. All diagram dimensions in millimeters.

101788_006

Electrostatic Discharge Sensitivity

The CX77314 is a Class I device. Figure 5 lists the Electrostatic Discharge (ESD) immunity level for each pin of the CX77314 product. The numbers in Figure 5 specify the ESD threshold levels for each pin where the I-V curve between the pin and ground starts to show degradation. The ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model. Since 2000 volts represents the maximum measurement limit of the test equipment used, pins marked > 2000 V pass 2000V ESD stress.

Figure 5. CX77314 ESD Sensitivity Areas (Top View)



Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards which fail devices only after “the pin fails the electrical specification limits” or “the pin becomes completely non-functional”. Conexant employs most stringent criteria, fails devices as soon as the pin begins to show any degradation on a curve tracer.

To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas follow the Class-1 ESD handling precautions listed in Table 5.

Table 5. Precautions: GaAs ICs w/ESD Thresholds Greater Than 200V But Less Than 2000V

Personnel Grounding Wrist Straps Conductive Smocks, Gloves and Finger Cots Antistatic ID Badges	**Facility** Relative Humidity Control and Air Ionizers Dissipative Floors (less than 10^9 Ω to GND)
Protective Workstation Dissipative Table Tops Protective Test Equipment (Properly Grounded) Grounded Tip Soldering Irons Conductive Solder Suckers Static Sensors	**Protective Packaging & Transportation** Bags and Pouches (Faraday Shield) Protective Tote Boxes (Conductive Static Shielding) Protective Trays Grounded Carts Protective Work Order Holders

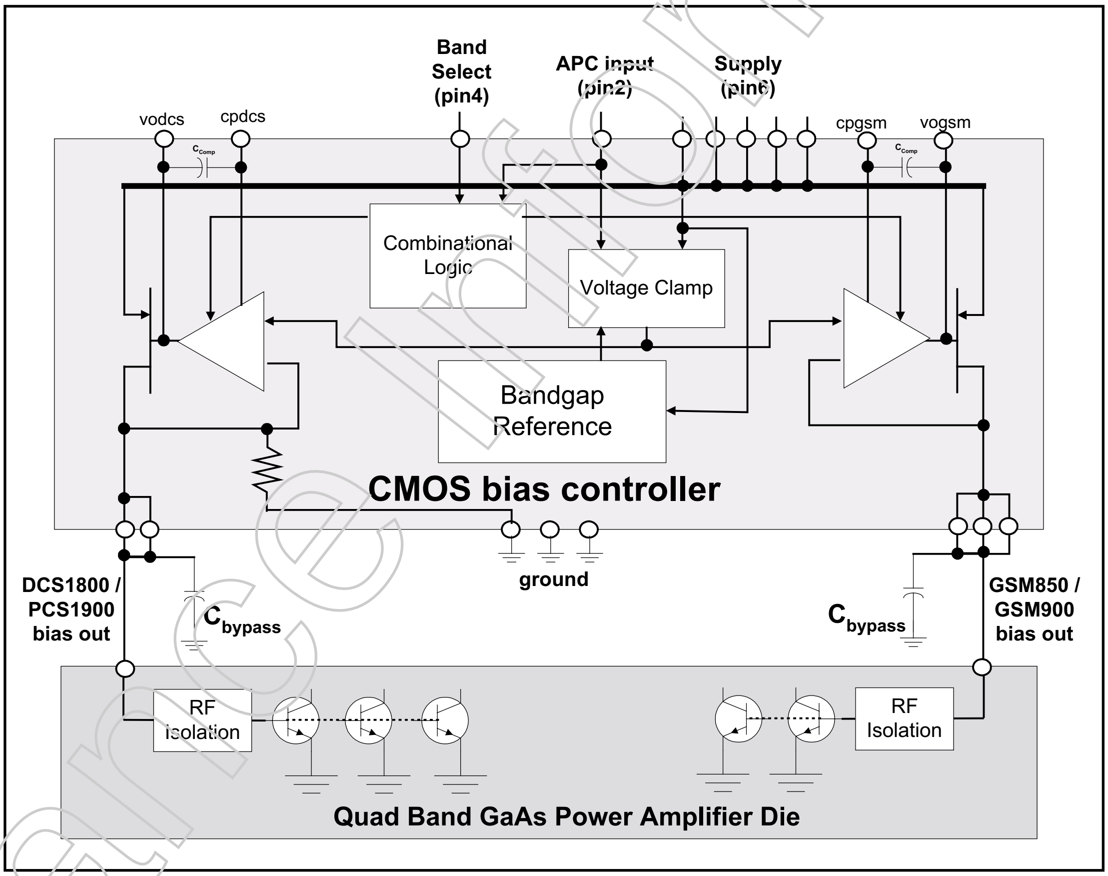
Technical Information

CMOS Bias Controller Characteristics

The CMOS die within the PAM performs several functions that are important to the overall module performance. Some of these functions must be considered for development of the power ramping features in a 3GPP compliant transmitter power control loop[1]. Power ramping considerations will be discussed later in this section.

The four main functions that will be described in this section are Standby Mode Control, Band Select, Voltage Clamp, and Current Buffer. The functional block diagram is shown in Figure 6.

Figure 6. Functional Block Diagram



101788_011

1. Please refer to 3GPP TS 05.05, Digital Cellular Communications System (Phase 2+); Radio Transmission and Reception. All GSM specifications are now the responsibility of 3GPP. The standards are available at http://www.3GPP.org/specs/specs.htm

Standby Mode Control

The Combinational Logic cell includes enable circuitry that monitors the APC ramping voltage from the power amplifier controller (PAC) circuit in the GSM transmitter. Typical handset designs directly connect the PA V_{CC} to the battery at all times, and for some PA manufacturers this requires a control signal to set the device in or out of standby mode. The Conexant PAM does not require a Transmit Enable input because it contains a standby detection circuit that senses the V_{APC} to enable or disable the PA. This feature helps minimize battery discharge when the PA is in standby mode. When V_{APC} is below the enable threshold voltage, the PA goes into a standby mode, which reduces battery current (I_{CC}) to 6 µA, typical, under nominal conditions.

For voltages less than 500 mV at the APC input (pin 4), the PA bias is held at ground. As the APC input exceeds the enable threshold, the bias will activate. After a 3 µs delay, the amplifier internal bias will ramp quickly to match the ramp voltage applied to the APC input. In order for the internal bias to precisely follow the APC ramping voltage, it is critical that a ramp pedestal is set to the APC input at or above the enable threshold level with a timing at least 3 µs prior to ramp-up. This will be discussed in more detail in the following section, “Power Ramping Considerations for 3GPP Compliance”.

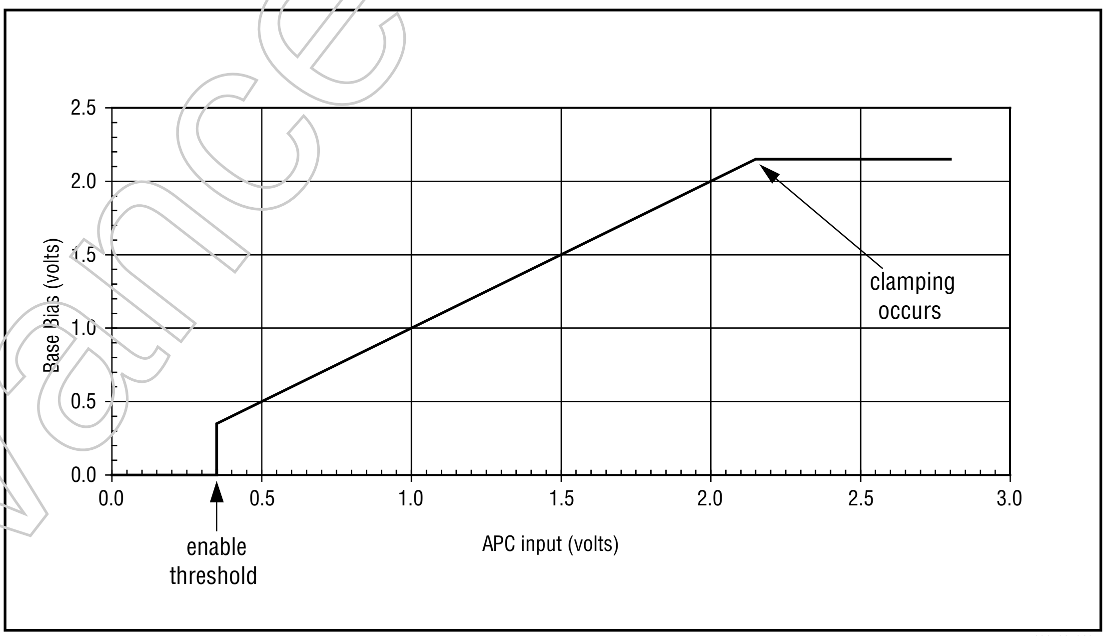
Band Select

The Combinational Logic cell also includes a simple gate arrangement that selects the desired operational band by activating the appropriate current buffer. The voltage threshold level at the Band Select input (pin 5) will determine the active path of the bias output to the GaAs die.

Voltage Clamp

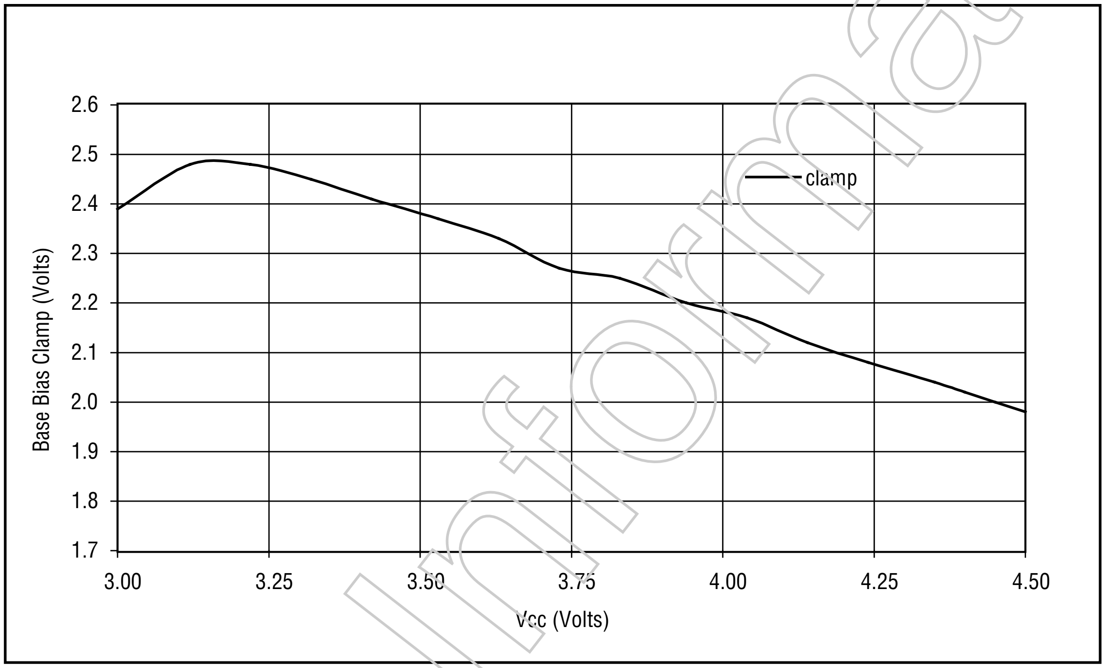
The Voltage Clamp circuit will limit the maximum bias voltage output applied to the bases of the HBT devices on the GaAs die. This provides protection against electrical overstress (EOS) of the active devices during high voltage and/or load mismatch conditions. Figure 7 shows the typical transfer function of the APC input to buffer output under resistively loaded conditions. Notice the enable function near 350 mV, and the clamp acting at 2.15 V, corresponding to a supply voltage of 4.0 V.

Figure 7. Base Bias Voltage vs. APC Input, V_{CC} = 4.0 V



Due to output impedance effects, the bias of the GaAs devices increases as the supply voltage increases. The Voltage Clamp is designed to gradually decrease in level as the battery voltage increases. The performance of the clamp circuit is enhanced by the band gap reference that provides a supply-, process-, and temperature-independent reference voltage. The transfer function relative to V_{BAT} is shown in Figure 8. For battery voltages below 3.4 V, the base bias voltage is limited by the common mode range of the buffer amplifier. For battery voltages above 3.4 V, the clamp limits the base bias.

Figure 8. Base Bias Clamp Voltage vs. Supply Voltage



101768_013b

Current Buffer

The output buffer amplifier performs a vital function in the CMOS device by transferring the APC input voltage ramp to the base of the GaAs power devices. This allows the APC input to be a high impedance port, sinking only 10 µA, typical, assuring no loading effects on the PAC circuit. The buffers are designed to source the high GaAs base currents required, while allowing a settling time of less than 3 µs for a 1.5 V ramp.

Power Ramping Considerations for 3GPP Compliance

These are the primary variables in the power control loop that the system designer must control:

- software control of the DSP / DAC
- software control of the transmitter timing signals
- ramp profile attributes - pedestal, number of steps, duration of steps
- layout of circuit / parasitics
- RC time constants within the PAC circuit design

All of these variables will directly influence the ability of a GSM transmitter power control loop to comply with 3GPP specifications.

Although there is a specific time mask template in which the transmitter power is allowed to ramp up, the method is very critical. The 3GPP system specification for switching transients results in a requirement to limit the edge rate of output power transitions of the mobile. Switching transients are caused by the transition from minimum output power to the desired output power, and vice versa. The spectrum generated by this transition is due to the ramping waveform amplitude modulation imposed on the carrier. Sharper transitions tend to produce more spectral "splatter" than smooth transitions. If the transmit output power is ramped up too slowly, the radio will violate the time mask specification. In this condition, the radio may not successfully initiate or maintain a phone call. If the transmit output power is ramped up too quickly, this will cause RF "splatter" at certain frequency offsets from the carrier as dictated by the 3GPP specification. This splatter, known as Output RF Spectrum (ORFS) due to Switching Transients, will increase the system noise level, which may knock out other users on the system. The main difficulty with TDMA power control is allowing the transmitter to ramp the output power up and down gradually so switching transients are not compromised while meeting the time mask template at all output power levels in all operational bands. The transmitter has 28 µs to ramp up power from an off state to the desired power level.

The GSM transmitter power control loop generally involves feedback around the GaAs PA, which limits the bandwidth of signals that can be applied to the PA bias input. Since the PA is within the feedback loop, its own small-signal frequency response must exhibit a bandwidth 5 to 10 times that of the power control loop. As discussed in the previous section, the PA bias is held at ground for inputs less than the enable threshold voltage (typically 350 mV). As the APC input exceeds the enable threshold, the bias will activate. After a 3 µs delay, the amplifier internal bias will quickly ramp to match the ramp voltage applied to the V_{APC} input. Since the bias must be wide band relative to the power control loop, the ramp will exhibit a fast edge rate. If the APC input increases beyond 1 V before the 3 µs switching delay is allowed to occur after the bias is enabled, the PA will have significant RF output as the internal bias approaches the applied bias. During this ramp, the internal power control is running "open loop" and the edge rates are defined by the frequency response of the PA bias rather than that of the power control loop. This open loop condition will result in switching transients that are directly correlated to the PA bias bandwidth.

Application of an initial APC voltage, which enables the bias at least 3 µs before the V_{APC} voltage is ramped, will ensure that the internal bias of the PAM will directly follow the applied V_{APC}. As a result, the power control loop will define all edge transitions rather than the PA internal bandwidth defining the transition. Figures 9 and 10 show the relationship of the internal bias relative to the applied APC in two cases. One case has ramping starting from ground; the other case has ramping starting with an initial enable pedestal of 500 mV. It is evident that the pedestal level is critical to ensure a predictable and well behaved power control loop.

To enable the CMOS driver in the PAM prior to ramp-up, a PAC output pedestal level to the APC input of the PAM (pin 4) should be set to about 500 mV. This pedestal level should have a duration of at least 3 µs directly prior to the start of ramp up.

Figure 11 shows typical signals and timings measured in a GSM transmitter power control loop. This particular example is at EGSM Power Level 5, Channel 62. The oscilloscope traces are TxVCO_enable, PAC_enable, DAC Ramp, and V_{APC} (pin 4).

NOTE: When the TxVCO is enabled, the pedestal becomes set at the APC input of the PAM, then the PAC is enabled, and finally the DAC ramp begins.

The device specifications for enable threshold level and switching delay are shown in Table 3.

Figure 9. PAM Internal Bias Performance —No Pedestal Applied

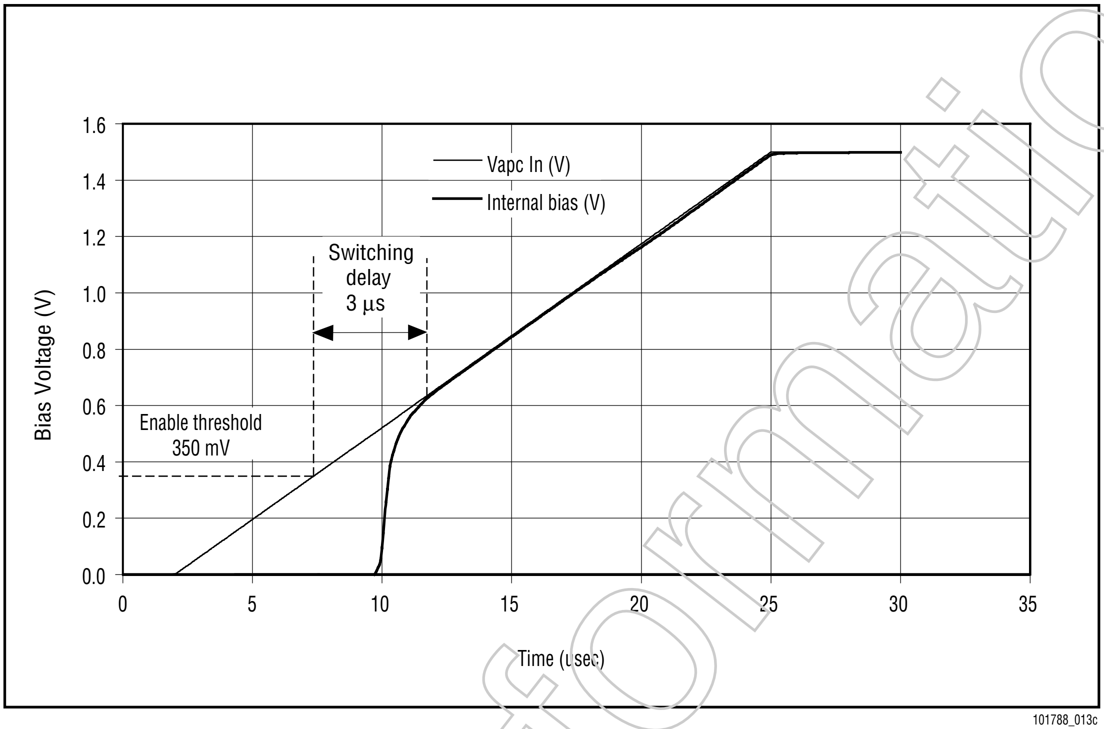


Figure 10. PAM Internal Bias Performance —Pedestal Applied

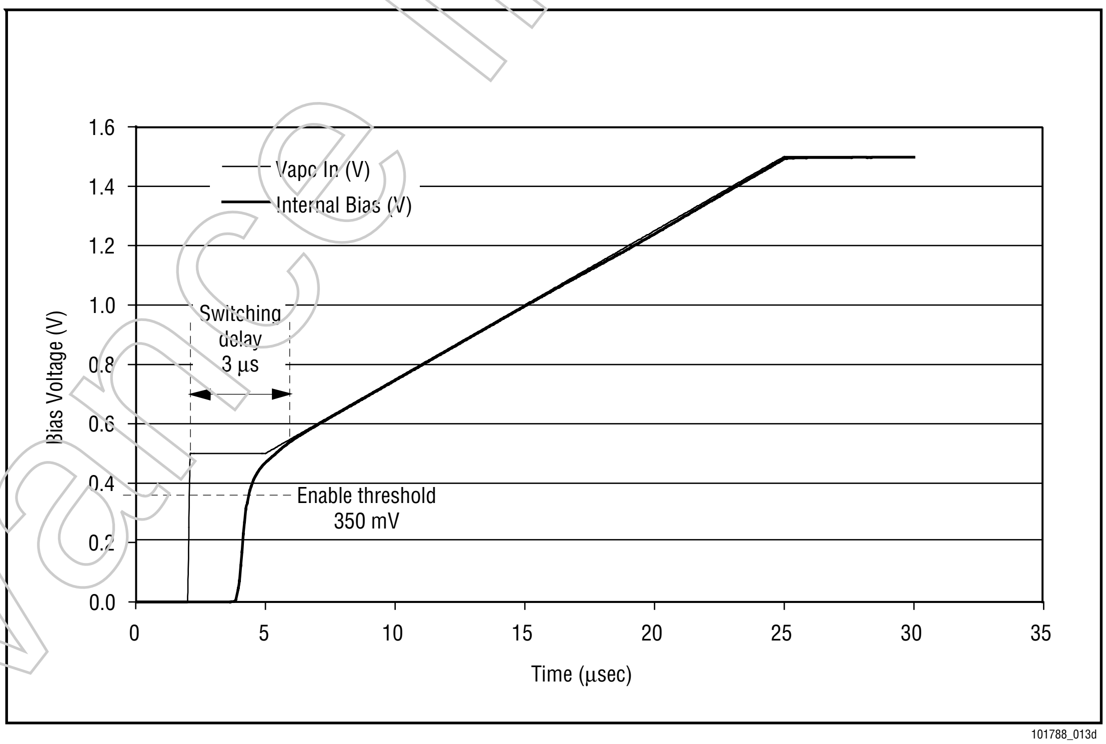
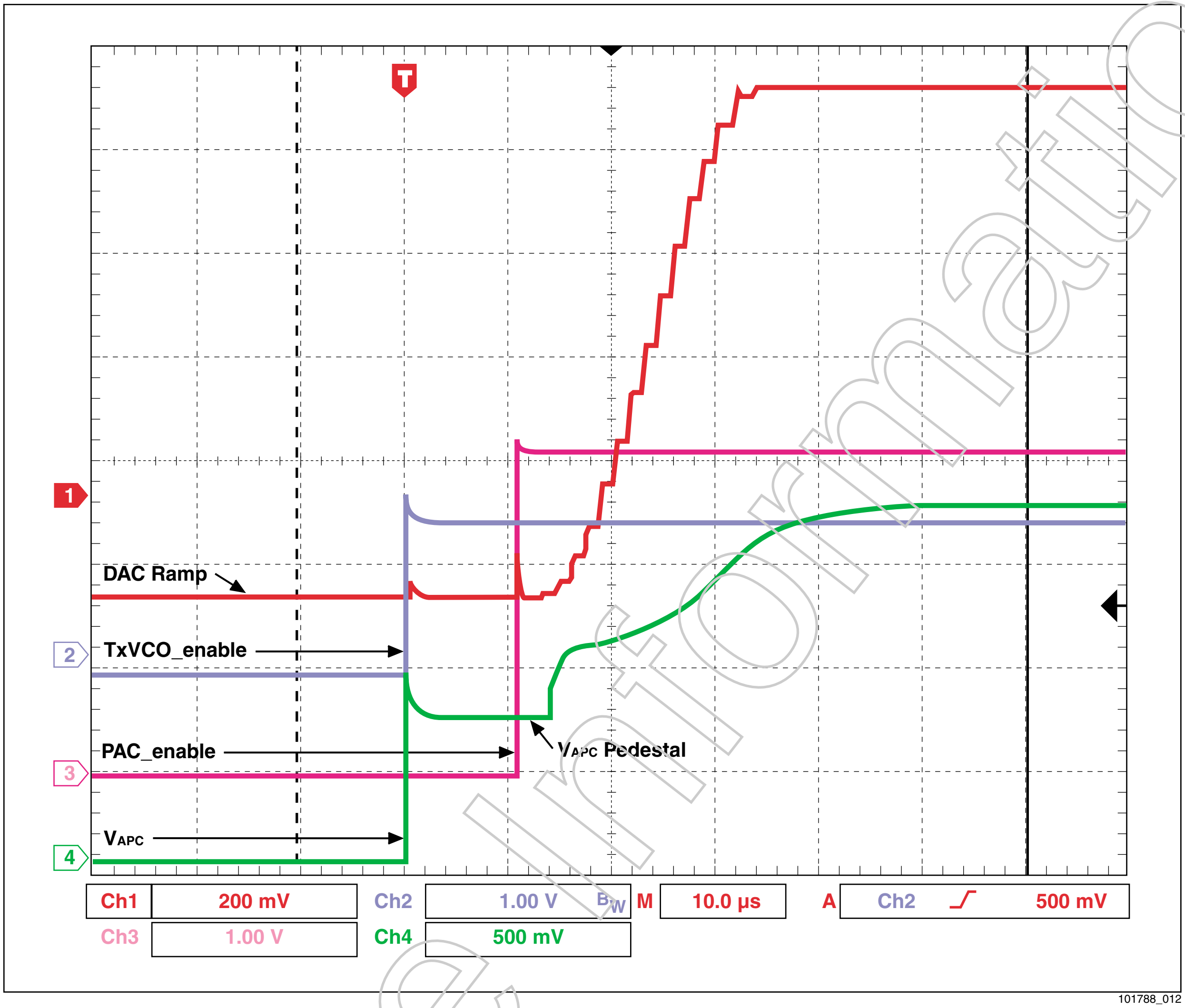


Figure 11. GSM Transmitter—Typical Ramp-up Signals



Ordering Information

Model Number	Manufacturing Part Number	Package	Operating Temperature
CX77314	CX77314	8 x 10 x 1.5 mm	–20 °C to +100 °C

Revision History

Revision	Level	Date	Description
P1		September 2001	Initial Preliminary Information
P2		March 12, 2002	Revise: Functional Block Diag.; Table 3; Figure 1 Add: Technical Information Section
P3		April 15, 2002	Revise: Tables 1, 3, 4; Figures 1, 3, 4, 5, 7, 8, 9 10; Technical Information section

References

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752

Reader Response: Conexant strives to produce quality documentation and welcomes your feedback. Please send comments and suggestions to tech.pubs@conexant.com. For technical questions, contact your local Conexant sales office or field applications engineer.

www.conexant.com
General Information:
U.S. and Canada: (800) 854-8099
International: (949) 483-6996
Headquarters – Newport Beach
4311 Jamboree Rd.
Newport Beach, CA. 92660-3007

CONEXANT™
What's next in communications technologies