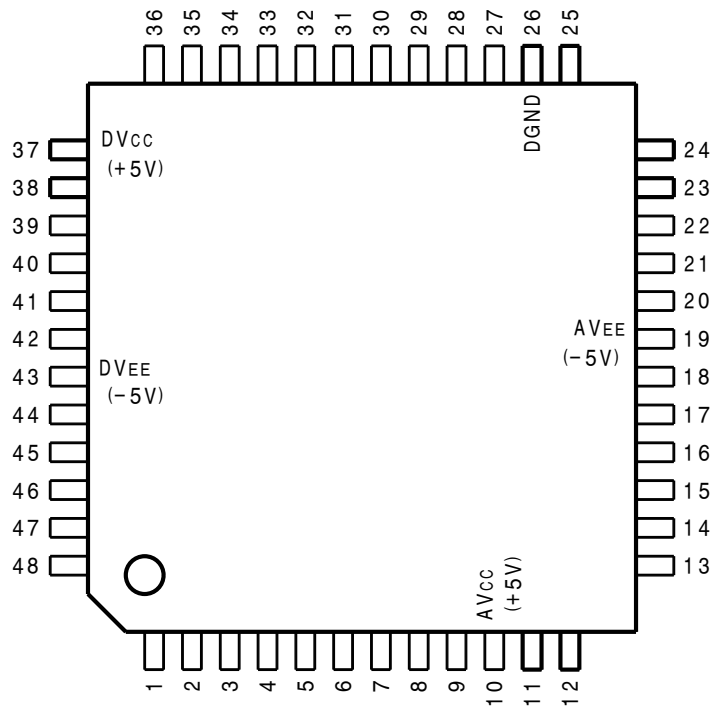


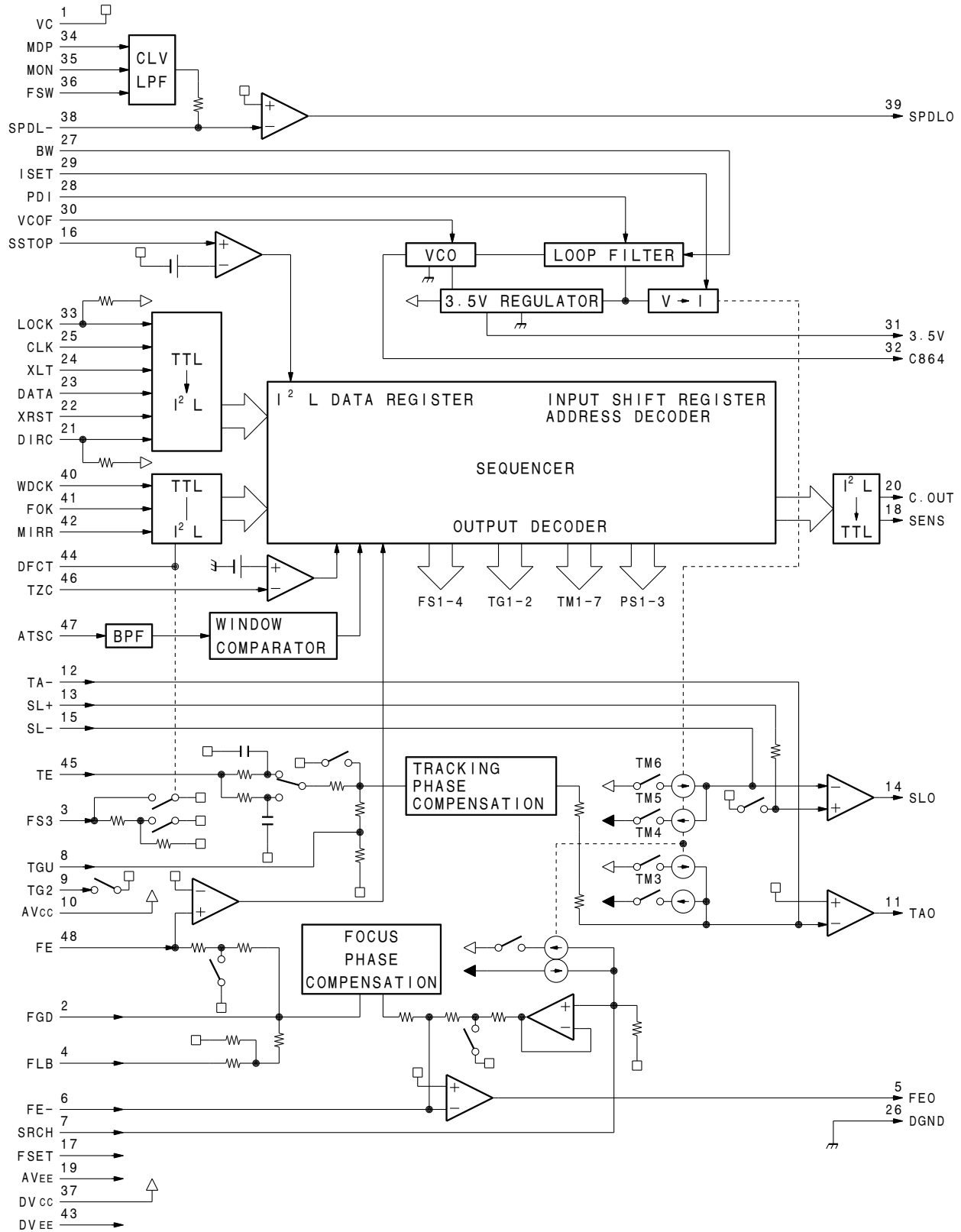
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## SERVO SIGNAL PROCESSOR FOR CD

-TOP VIEW-



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	VC	13	I	SL+	25	I	CLK	37	I	DVcc
2	I	FGD	14	O	SLO	26	-	DGND	38	I	SPDL-
3	I	FS3	15	I	SL-	27	I	BW	39	O	SPDLO
4	I	FLB	16	I	SSTOP	28	I	PDI	40	I	WDCK
5	O	FEO	17	I	FSET	29	I	ISET	41	I	FOK
6	I	FE-	18	O	SENS	30	I	VCOF	42	I	MIRR
7	I	SRCH	19	I	AVEE	31	O	3.5V	43	I	DVEE
8	I	TGU	20	O	C. OUT	32	O	C864	44	I	DFCT
9	I	TG2	21	I	DIRC	33	I	LOCK	45	I	TE
10	-	AVcc	22	I	XRST	34	I	MDP	46	I	TZC
11	O	TA0	23	I	DATA	35	I	MON	47	I	ATSC
12	I	TA-	24	I	XLT	36	I	FSW	48	I	FE



34	MDP	SPDLO	39	
35	MON			
36	FSW			
38	SPDL-			
27	BW	3.5V	31	
29	ISET	C864	32	
28	PDI			
30	VCOF			
33	LOCK	C. OUT	20	
25	CLK	SENS	18	
24	XLT			
23	DATA			
22	XRST			
21	DIRC			
40	WDCK			
41	FOK			
42	MIRR			
44	DFCT			
46	TZC			
47	ATSC			
16	SSTOP			
12	TA-	SLO	14	
13	SL+			
15	SL-			
45	TE	TAO	11	
3	FS3			
8	TGU			
9	TG2			
48	FE	FEO	5	
2	FGD			
4	FLB			
6	FE-			
7	SRCH			
17	FSET			

INPUT

ATSC ; WINDOW COMPARATOR INPUT PIN FOR ATSC DETECTION.  
 BW ; TIME CONSTANT EXTERNAL PIN FOR LOOP FILTER.  
 CLK ; SERIAL DATA TRANSFER CLOCK INPUT FROM CPU.  
 DATA ; SERIAL DATA INPUT FROM CPU.  
 DFCT ; DEFECT SIGNAL INPUT.  
 DIRC ; PIN FOR ONE-TRACK JUMP.  
 FE ; INPUT FOR FOCUS ERROR.  
 FE- ; INVERSE INPUT PIN FOR FOCUS AMPLIFIER.  
 FGD ; CONNECT A CAPACITOR BETWEEN THIS PIN AND  
 PIN 3 TO REDUCE HIGH-FREQUENCY GAIN.  
 FLB ; TIME CONSTANT EXTERNAL PIN TO RAISE THE  
 LOW BANDWIDTH OF THE FOCUS SERVO.  
 FOK ; FOCUS OK SIGNAL INPUT.  
 FS3 ; THE HIGH-FREQUENCY GAIN OF THE FOCUS  
 SERVO IS SWITCHED THROUGH FS3 ON AND OFF.  
 FSET ; PIN TO SET PEAK FREQUENCY OF FOCUS TRACKING  
 PHASE COMPENSATION AND FC OF CLV LPF.  
 FSW ; TIME CONSTANT EXTERNAL PIN FOR CLV SERVO ERROR SIGNAL  
 ISET ; CURRENT IS INPUT TO DETERMINE FOCUS SEARCH,  
 TRACK JUMP, AND SLED KICK HEIGHT.  
 LOCK ; AT"L" SLED RUNAWAY PREVENTION CIRCUIT OPERATES.  
 MDP ; MDP SIGNAL INPUT.  
 MIRR ; MIRR SIGNAL INPUT.  
 MON ; MON SIGNAL INPUT.  
 PDI ; PDO SIGNAL INPUT.  
 SL+ ; NON-INVERSE INPUT PIN FOR SLED AMPLIFIER.  
 SL- ; INVERSE INPUT PIN FOR SLED AMPLIFIER.  
 SPDL- ; INVERSE INPUT FOR SPINDLE DRIVE AMP.  
 SRCH ; TIME CONSTANT EXTERNAL PIN FOR THE  
 FORMATION OF FOCUS SEARCH WAVEFORMS.  
 SSTOP ; LIMIT SW ON/OFF SIGNAL DETECTION PIN FOR  
 DISC INNER PERIPHERY DETECTION.  
 TA- ; INVERSE INPUT PIN FOR TRACKING AMPLIFIER.  
 TE ; TRACKING ERROR SIGNAL INPUT.  
 TG2 ; TIME CONSTANT EXTERNAL PIN FOR  
 THE SELECTION OF TRACKING HIGH BAND GAIN.  
 TGU ; TIME CONSTANT EXTERNAL PIN FOR  
 THE SELECTION OF TRACKING HIGH BAND GAIN.  
 TZC ; INPUT FOR TRACKING ZERO-CROSS COMPARATOR.  
 VCOF ; VCO FREQUENCY CONTROL.  
 WDCK ; CLOCK INPUT FOR AUTO.  
 XLT ; LATCH INPUT FROM CPU.  
 XRST ; RESET INPUT PIN, RESET AT"L"

OUTPUT

C864 ; 8.64MHz VCO OUTPUT  
 C. OUT ; TRACK NUMBER COUNT SIGNAL OUTPUT.  
 FEO ; FOCUS DRIVE OUTPUT.  
 SENS ; OUTPUTS FZC, AS, TZC, SSTOP AND BUSY THROUGH COMMAND FROM CPU.  
 SLO ; SLED DRIVE OUTPUT.  
 SPDLO ; SPINDLE DRIVE OUTPUT.  
 TAO ; TRACKING DRIVE OUTPUT.