SONY

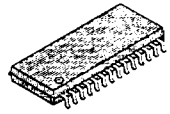
CXA1096M

8-bit 20 MSPS Flash A/D Converter (TTL I/O)

Description

The CXA1096M is an 8-bit 20 MSPS high speed A/D converter IC. This IC is suitable for a wide range of applications where A/D high speed operation is required.

28pin SOP(Plastic)



Features

- Resolution 8-bit ±1/2 LSB
- High speed operation 20MSPS
- Wide band analog input 8MHz (−3dB)
- Low input capacitance 30pF (Typ.)
- Low power consumption 390mW (Typ.)
- I/O level TTL
- Two ways of power supply (Single +5V or dual +5V/−5.2V)
- Sample and Hold amplifier not required
- Binary or Two's complement mode
- Over range output

Structure

Bipolar silicon monolithic IC

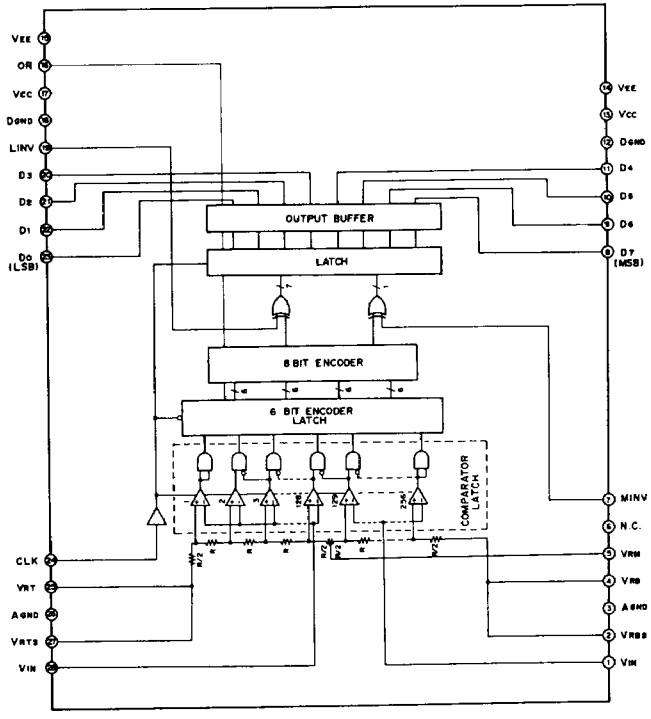
Applications

- Digital TV
- High speed signal processing

Function

8-bit, 20MSPS flash A/D converter

Block Diagram



E89645-HP

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	$V_{CC}-D_{GND}$	0 to +6	V
	$V_{EE}-A_{GND}$	0 to −6	V
	$A_{GND}-D_{GND}$	0 to +6	V
• Input voltage(analog)	V_{IN}	V_{EE} to A_{GND} +0.3	V
• Input voltage (reference)	V_{RT}, V_{RB}, V_{RM}	V_{EE} to A_{GND} +0.3	V
	$\lvert V_{RT} - V_{RB} \rvert$	2.5	V
• Input current (V_{RM})	I_{VRM}	−3 to +3	mA
• Input voltage (digital)	CLK, MINV, LINV	D_{GND}−0.5 to V_{CC}	V
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	0.83	W

Recommended Operating Conditions

• Supply voltage (Single supply)	V_{CC}, A_{GND}	4.75 to 5.25	V
	D_{GND}, V_{EE}	0	V
(Dual supply)	V_{CC}	4.75 to 5.25	V
	V_{EE}	−5.5 to −4.75	V
	D_{GND}, A_{GND}	0	V
• Reference input	V_{RT}	A_{GND} −0.1 to A_{GND} +0.1	V
	V_{RB}	A_{GND} −2.2 to A_{GND} −1.8	V
• Analog input	V_{IN}	V_{RB} to V_{RT}	
• Clock pulse width	T_{PW1}	35 (Min.)	ns
	T_{PW0}	10 (Min.)	ns
• Operating temperature	Topr	−20 to +75	°C

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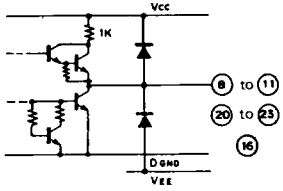
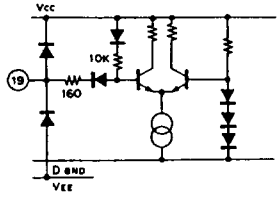
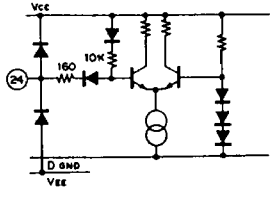
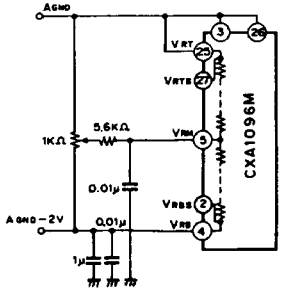
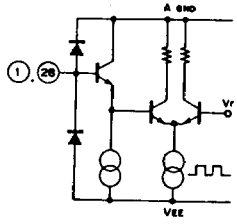
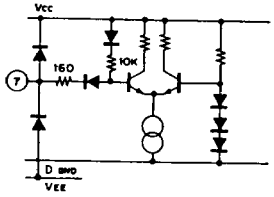
Pin Description and Equivalent Circuit

No.	Symbol	Voltage	Equivalent circuit	Description
8 to 11 20 to 23	D0 to D7	TTL		Digital data output pin D0 (LSB) to D7 (MSB)
16	OR			Over range output pin
12, 18	DGND	GND		Digital GND Separated from AGND
13, 17	Vcc	5V (Typ.)		Digital power supply
14, 15	VEE	GND (Single supply) – 5V (Dual supply)		Analog power supply
19	LINV	TTL		Input pins for output polarity inversion of D0 (LSB) to D6 (See the Input-Output Reference and Output Format) when open "1" is maintained.
24	CLK	TTL		Clock input pin
25	VRT	5V (Typ.) (Single supply)		Reference voltage (Top)
27	VRTS	GND (Dual supply)		Reference voltage sense (Top)
4	VRB	3V (Typ.) (Single supply) – 2V (Typ.) (Dual supply)		Reference voltage (Bottom)
2	VRBS			Reference voltage sense (Bottom)
5	VRM	4V (Typ.) (Single supply) – 1V (Typ.) (Dual supply)		Middle point of reference voltage can be used as the compensation pin for linearity

No.	Symbol	Voltage	Equivalent circuit	Description
3, 26	AGND	5V (Typ.) (Single supply) GND (Dual supply)		Analog power supply
1, 28	VIN	VRT to VRB		Analog input Pin 1 and 28 should be connected together.
7	MINV	TTL		Input pin for output polarity inversion of D7 (MSB) when open "1" is maintained.

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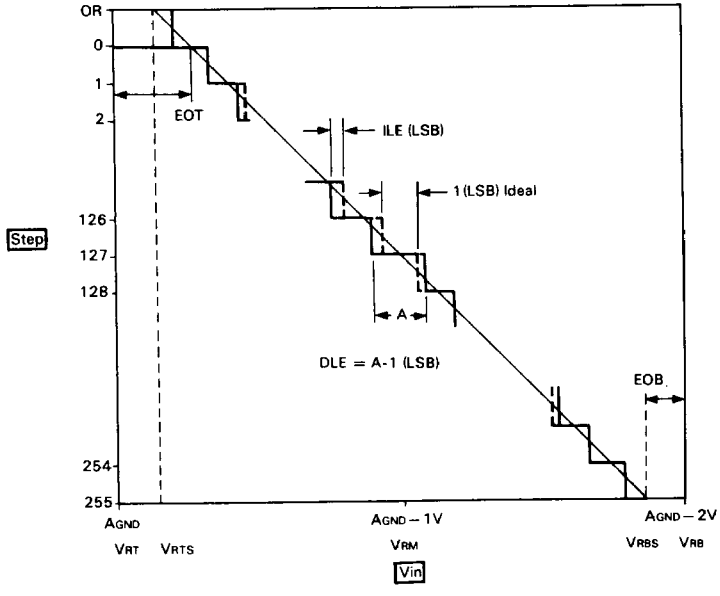
Input-Output Reference and Output Format

Vin	Step	MINV 1 LINV 1 OR MSB LSB	1 0 OR MSB LSB	0 1 OR MSB LSB	0 0 OR MSB LSB
AGND		0 000···00	0 011···11	0 100···00	0 111···11
	0	1 000···00	1 011···11	1 100···00	1 111···11
	1	1 000···01	1 011···10	1 100···01	1 111···10
		.	.	.	.
		.	.	.	.
		.	.	.	.
AGND −1V	127	1 011···11	1 000···00	1 111···11	1 100···00
	128	1 100···00	1 111···11	1 000···00	1 011···11
		.	.	.	.
		.	.	.	.
		.	.	.	.
	254	1 111···10	1 100···01	1 011···10	1 000···01
AGND −2V	255	1 111···11	1 100···00	1 011···11	1 000···00
		1 111···11	1 100···00	1 011···11	1 000···00

1: V_{IH}, V_{OH}
0: V_{IL}, V_{OL}



Electrical Characteristics (Single supply)

V_{CC} = +5V, DGND = 0V, AGND = +5V, V_{EE} = 0V, V_{RT} = +5V, V_{RB} = +3V, Ta = 25°C

Item		Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate		F_C	V_{IN} = 5 to 3V F_{IN} = $F_{C/4}$ − 1 kHz		20			MSPS
Supply current		I_{CC} + I_{EE}			56	71	91	mA
Reference pin current		I_{REF}			11	15	18	mA
Analog input bandwidth		BW			8			MHz
Analog input capacitance		C_{IN}	V_{IN} = 4V + 0.07Vms			30	35	pF
Analog input bias current		I_{IN}	V_{IN} = 4V		15	50	110	μA
Reference resistance (V_{RT} to V_{RB})		R_{REF}				130		Ω
Offset voltage	V_{RT}	E_{OT}			8	13	19	mV
	V_{RB}	E_{OB}			0	5	11	mV
Digital input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Digital input current		I_{IH}	V_{CC} = Max.	V_{IH} = 2.7V	0	−100	−150	μA
		I_{IL}		V_{IL} = 0.5V	−0.1	−0.32	−0.5	mA
Digital output voltage		V_{OH}	V_{CC} = Min.	I_{OH} = −500μA	2.7	3.4		V
		V_{OL}		I_{OL} = 3mA			0.5	V
Output data delay		T_{DLH}	LOAD 1		15	19	22	ns
		T_{DHL}			22	27	31	ns
Non linearity		E_L	F_C = 20 MSPS V_{IN} = 5 to 3V				±1/2	LSB
Differential non linearity		E_D					±1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, F_C = 14.3 MSPS				1.5	%
Differential phase error		DP					0.5	deg.
Aperture jitter		E_{AP}				30		ps
Sampling delay		tds			5	7	9	ns

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Electrical Characteristics (Dual supply)

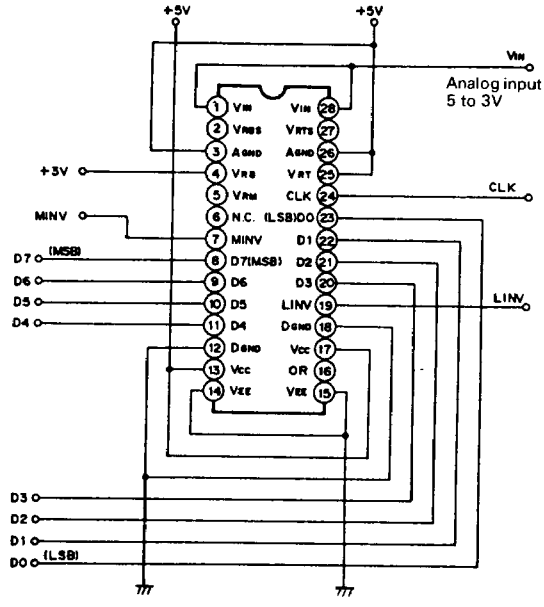
V_{CC} = +5V, DGND = 0V, AGND = 0V, V_{EE} = −5V, V_{RT} = 0V, V_{RB} = −2V, Ta = 25°C

Item		Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate		F_C	V_{IN} = 0 to −2V F_{IN} = F_C/4 − 1 kHz		20			MSPS
Supply current		I_{CC}			7	10	14	mA
		I_{EE}			50	62	78	mA
Reference pin current		I_{REF}			11	15	18	mA
Analog input bandwidth		BW			8			MHz
Analog input capacitance		C_{IN}	V_{IN} = −1V + 0.07Vrms			30	35	pF
Analog input bias current		I_{IN}	V_{IN} = −1V		15	50	110	μA
Reference resistance (V_{RT} to V_{RB})		R_{REF}				130		Ω
Offset voltage	V_{RT}	E_{OT}			8	13	19	mV
	V_{RB}	E_{OB}			0	5	11	mV
Digital input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Digital input current		I_{IH}	V_{CC} = Max.	V_{IH} = 2.7V	0	−100	−150	μA
		I_{IL}		V_{IL} = 0.5V	−0.1	−0.32	−0.5	mA
Digital output voltage		V_{OH}	V_{CC} = Min.	I_{OH} = −500μA	2.7	3.4		V
		V_{OL}		I_{OL} = 3mA			0.5	V
Output data delay		T_{DLH}	LOAD 1		15	19	22	ns
		T_{DHL}			22	27	31	ns
Non linearity		E_L	F_C = 20 MSPS V_{IN} = 0 to −2V				±1/2	LSB
Differential non linearity		E_D					±1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, F_C = 14.3 MSPS				1.5	%
Differential phase error		DP					0.5	deg.
Aperture jitter		E_{AP}				30		ps
Sampling delay		tds			5	7	9	ns

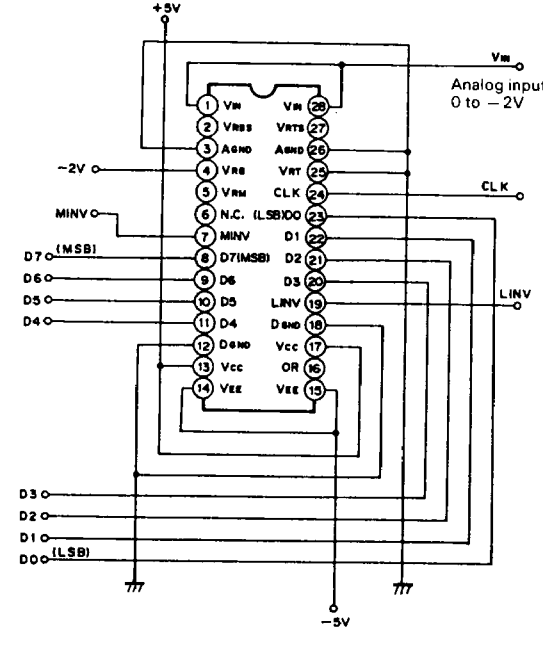
Application Circuit and Electrical Characteristics Test Circuit

1)

Single supply



Dual supply



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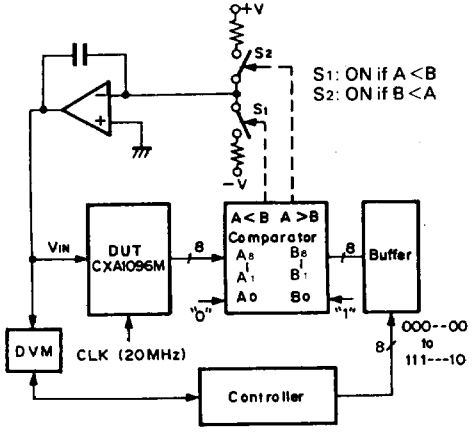
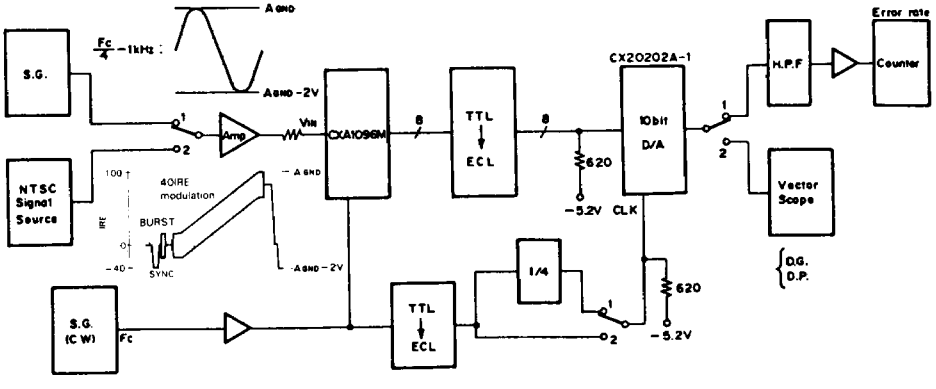


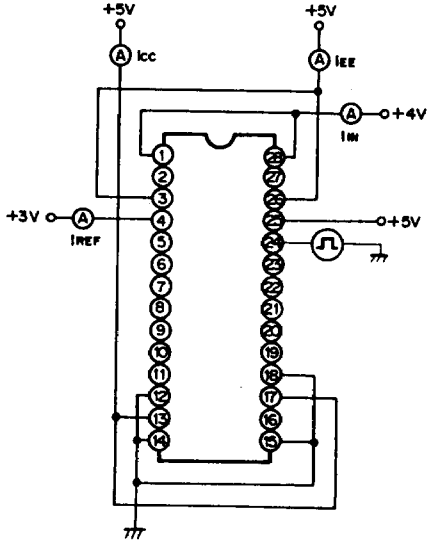
Non linearity
Differential non linearity } Test circuit



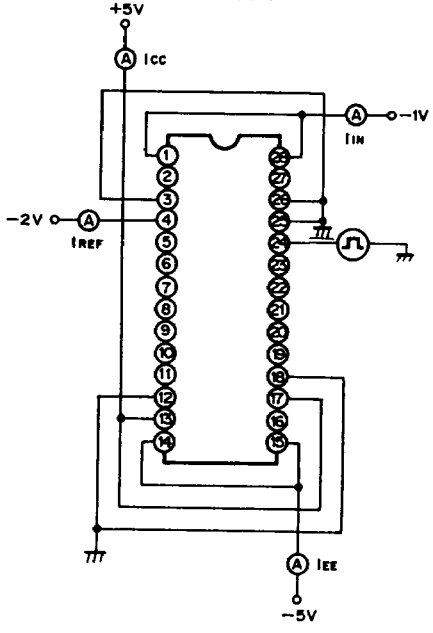
Maximum conversion rate
Differential gain error
Differential phase error } Test circuit

2)

Single supply

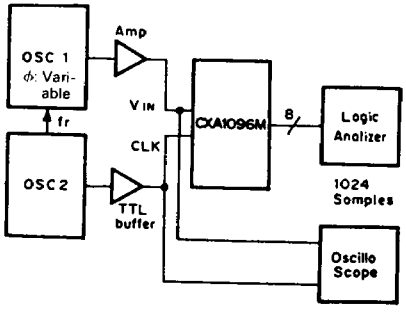


Dual supply

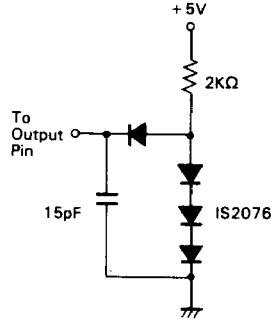


Note) VIN pin is connected to VRT pin for ICC and IEE measurement.

Supply current
Analog input bias current
Reference pin current
} Test circuit

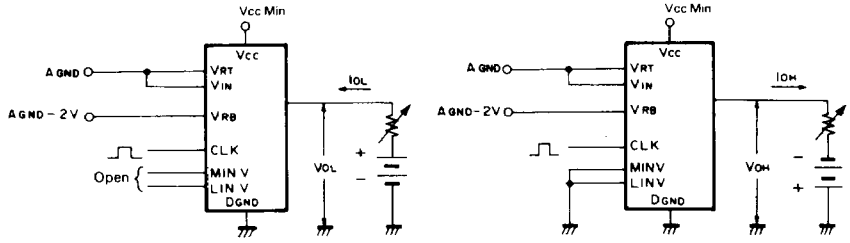


Aperture jitter
Sampling delay
} Test circuit

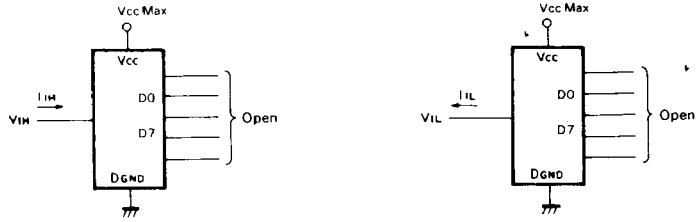


LOAD1 Test Load for Output data delay

3)

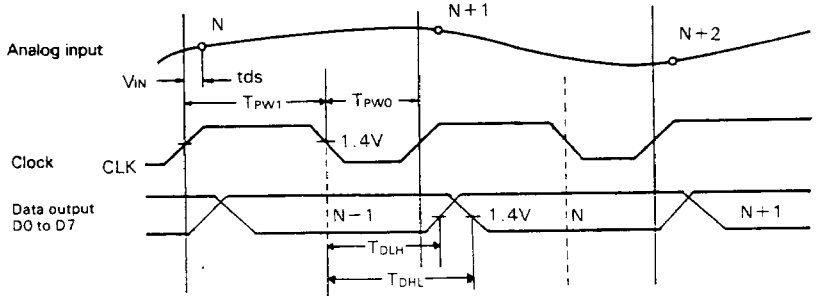


Test circuit of digital output voltage (D0 to D7, OR)

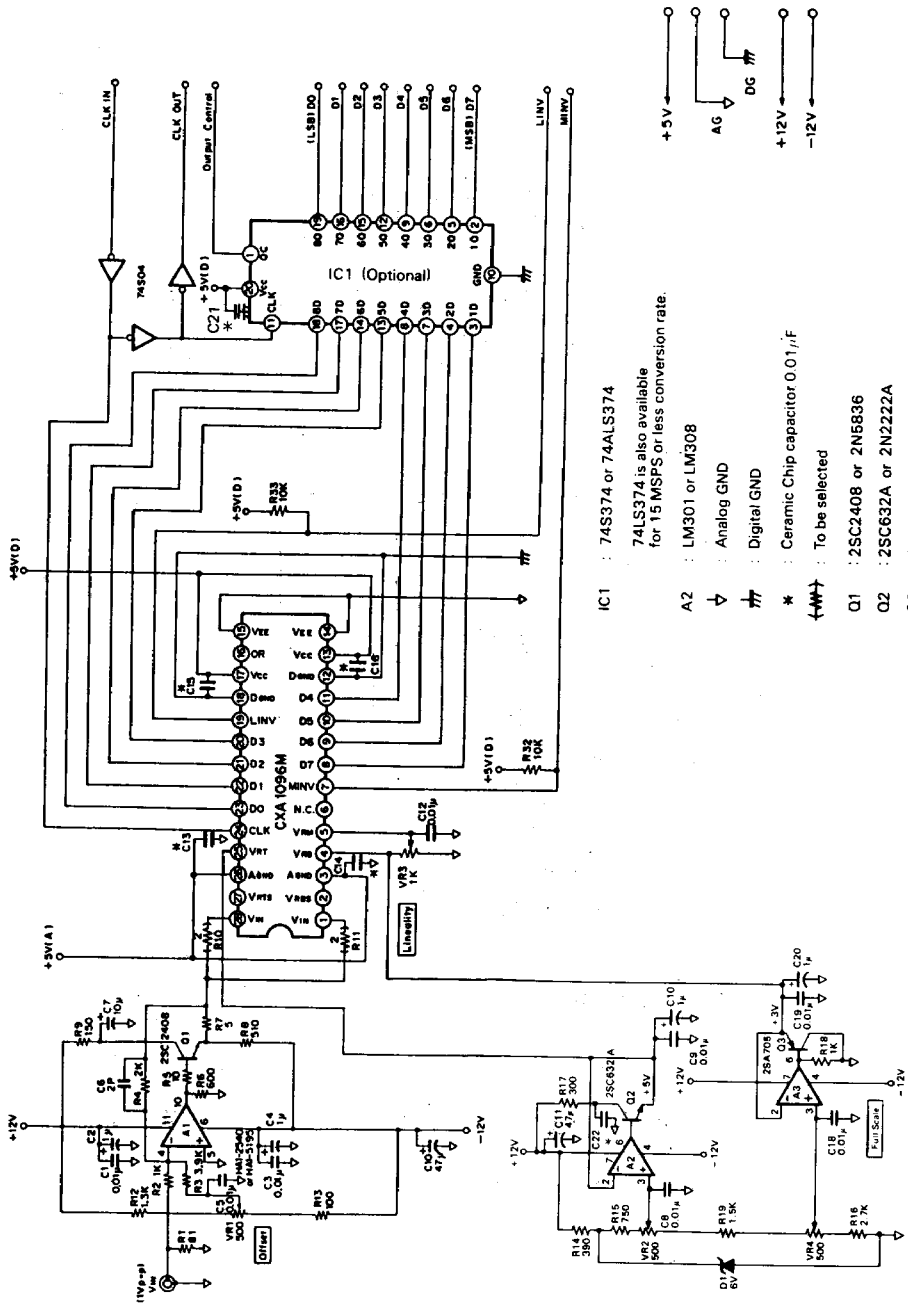


Test circuit of digital input current (CLK, MINV, LINV)

Timing Chart



Application Circuit (Single supply)



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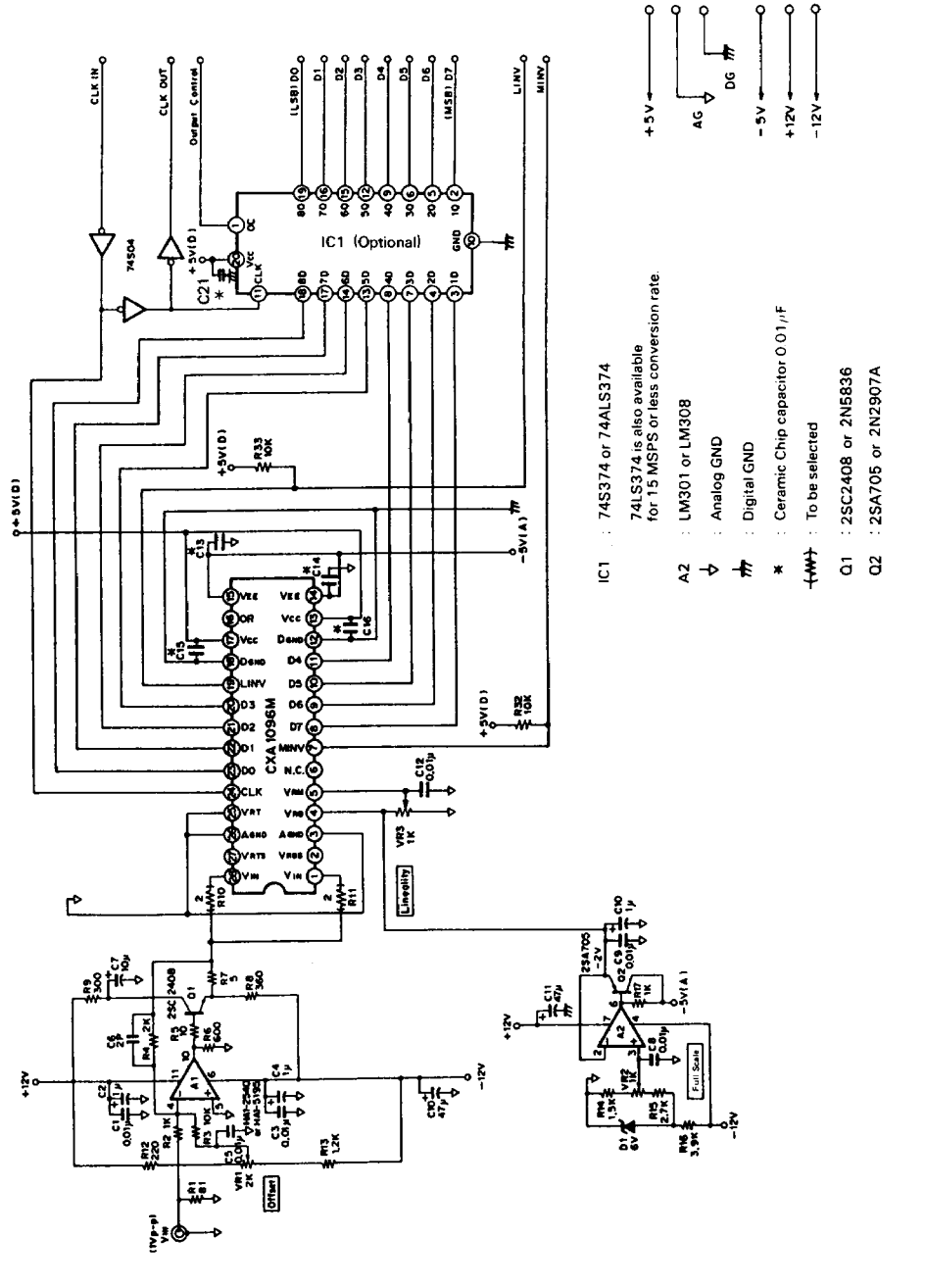
Application Circuit (Dual supply)



Notes on Application

1. Each of DGND pins (12, 18) and each of VCC Pins (13, 17) are divided in internal circuit. All of the pins should be connected to respective PCB patterns.

2. Layout of the analog and digital sections should be separated to reduce noise effect.
   VEE pins to AGND and VCC pins to DGND should be bypassed as closely as possible by means of 1μF and 0.01μF capacitors.
   For the 0.01μF, a ceramic chip capacitor should be used.

3. The input capacitance of the analog input is much smaller than that of the Flash Type A/D converters in use so far. It is necessary to use an amplifier with sufficient band width and driving power.
   Pins VIN (1, 28) are divided in it, so they should be connected together. When driving with a low output impedance amplifier, parasitic oscillation may occur. This can be prevented by introducing between the amplifier output and A/D input a small resistance of 2 to 10Ω with smaller inductance, in series. And, that also each VIN pins are divided with small resistances (shown in the Application Circuit) is effective.
   The amplifier output and A/D input should be connected as closely as possible.

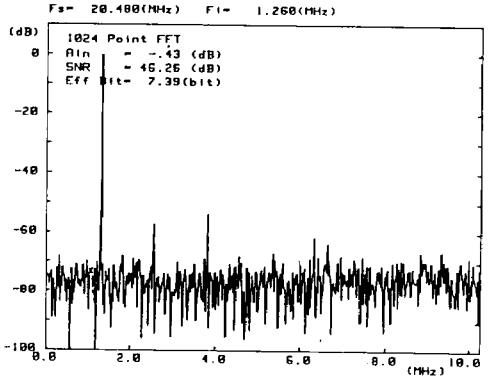
4. Voltage between VRT to VRB is equivalent to the dynamic range of the analog input. VRB pin should be bypassed to AGND by means of 1μF and 0.01μF capacitors.
   Through bypassing VRM pin with a 0.01μF capacitor to AGND, characteristics at high frequency become more balanced. Also, VRM pin can be used as a trimming pin for more precise linearity compensation.

5. CLK line should be wired in short distance and that should be separated from the other section to reduce the inductive.

6. Analog input signal is sampled at the positive going edge of the CLK, and a corresponding digital data appears to the output parts at the negative going edge with a short delay time (TDLH, TDHL).
   If digital data will be latched externally, it should be latched at the negative going edge. (See the Timing Chart)

7. It is recommended to connect free pins to AGND for prevention of noise effect.

FFT data



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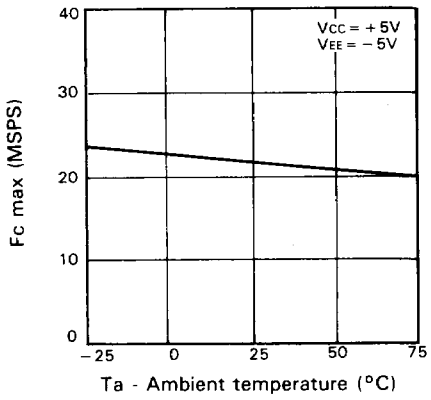
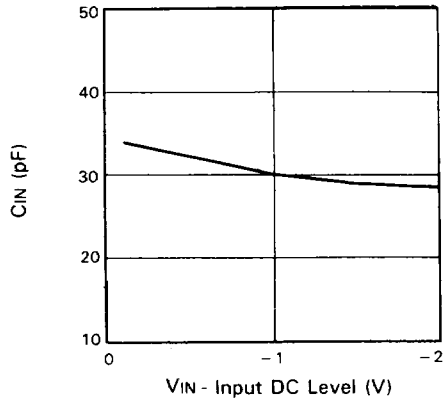
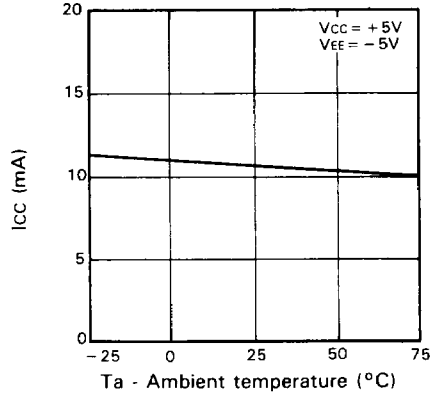
Fc max vs. Ambient temperature



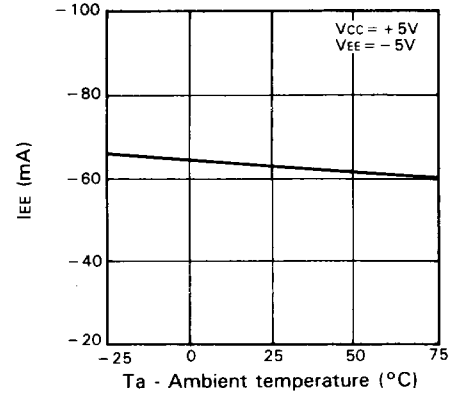
CIN vs. VIN - Input DC level



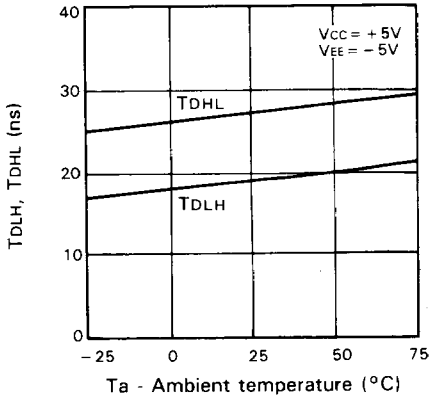
ICC vs. Ambient temperature



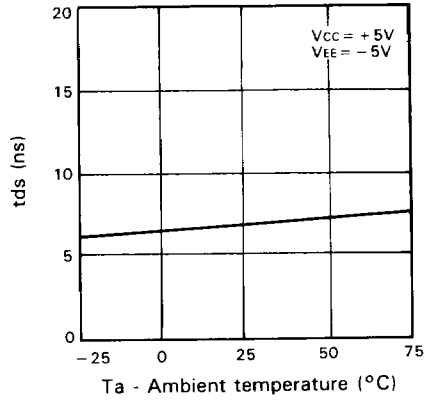
IEE vs. Ambient temperature

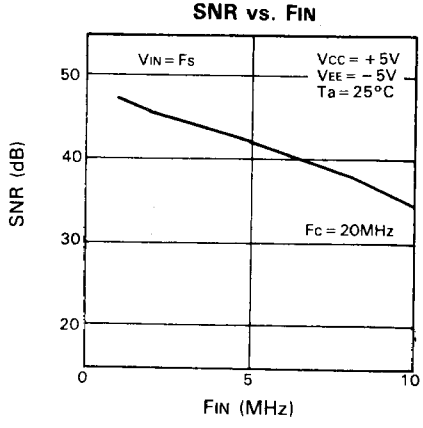


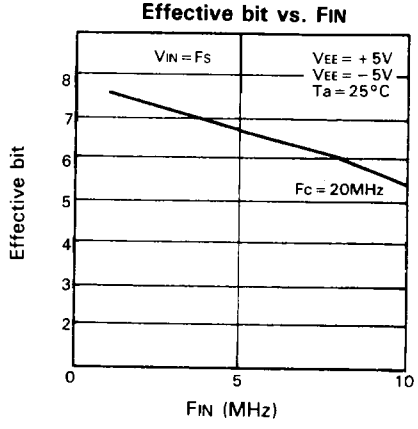
TDLH, TDHL vs. Ambient temperature



tds vs. Ambient temperature







Package Outline Unit : mm

28pin SOP(Plastic) 375mil 0.6g