SONY

CXA1156AQ

8-bit 400MSPS Triple VIDEO D/A Converter

Description

The CXA1156AQ is an 8-bit high-speed D/A converter with input/output of 3 channels for RGB.

This IC achieves maximum conversion rate of 400MSPS, and is suitable for signal processing applications requiring high speed and resolution such as high resolution monitors and high definition video systems.

44 pin QFP (Ceramic)

Features

- High speed: 400MSPS
- High resolution: 8-bit RGB
- Low power consumption: 1.3W (at V_{EE}=–4.5V)
- Video control inputs: Sync, Blank, Overlay
- ECL 100K and 10K compatible inputs
- 25Ω , 37.5Ω load driving capability
- Differential current output
- RS-343A compatible output

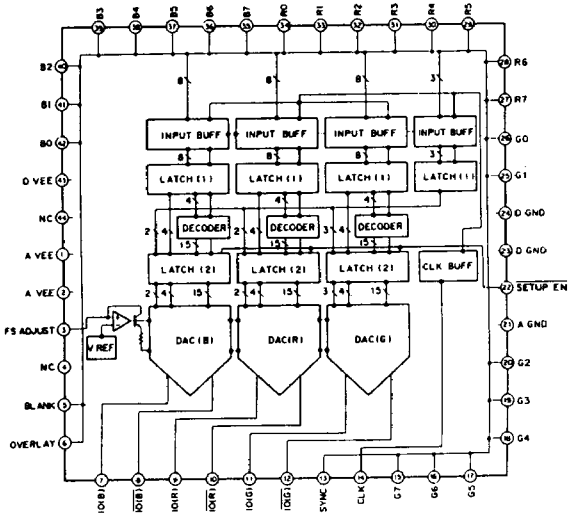
Function

8-bit 400MSPS triple video D/A converter

Structure

Bipolar silicon monolithic IC

Block Diagram/Pin Configuration



Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	AV_{EE}, DV_{EE}	−7 to +0.5	V
• Input voltage (digital)	V_I	DV_{EE} to +0.5	V
(FS. ADJ. pin)	V_{REF}	AV_{EE} to +0.5	V
• Input current (FS. ADJ. pin)	I_{REF}	2.0	mA
• Output voltage	V_O	−2.0 to +2.0	V
• Output current	I_O	50	mA
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	P_D	1.3	W

Operating Conditions

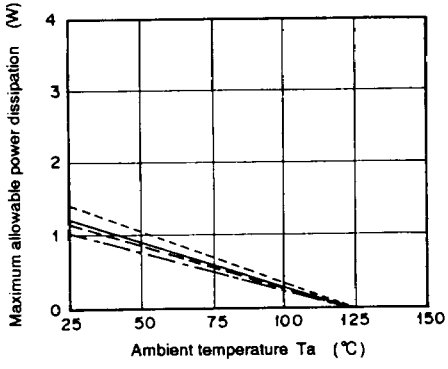
• Supply voltage	AV_{EE}, DV_{EE}	−4.8 to −4.2	V
	AV_{EE}-DV_{EE}	−0.05 to +0.05	V
• Digital input voltage	V_{IH}	−1.05 to −0.7	V
	V_{IL}	−1.9 to −1.49	V
• Reference current	I_{REF}	0.5 to 1.9	mA
• Load resistance	R_L	25 to 37.5	Ω
• Output voltage	V_O (FS.)	0.8 to 1.2	V
• CLK pulse width	tpw_1	1.2 (Min.)	ns
	tpw_0	1.2 (Min.)	ns
• Operating temperature	Tc	−20 to 70	°C

6

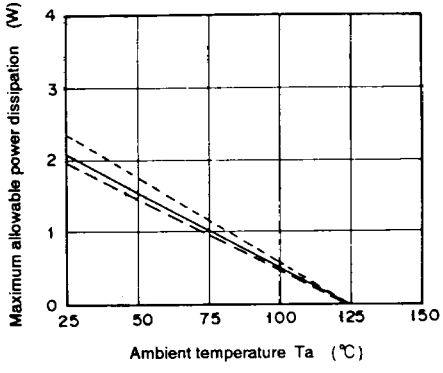
Maximum Allowable Power Dissipation vs. Ambient Temperature

--------- With fin 2290C (*)
——— With fin 2285C (*)
- - - - - - Without fin
—·—·— When not mounted

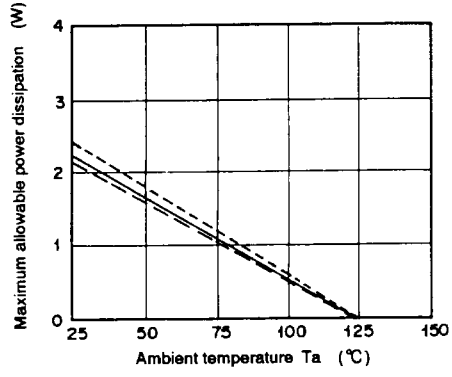
} When mounted on a board (**)



(a) In Still Air



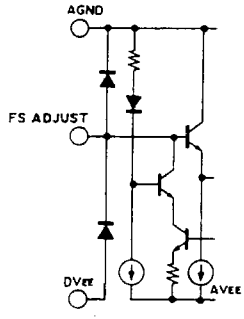
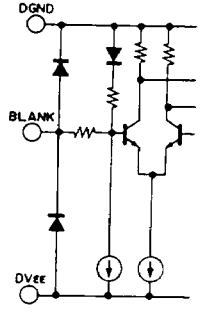
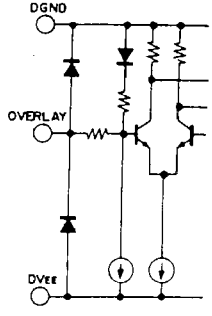
(b) Air Flow Rate 1.5m/sec



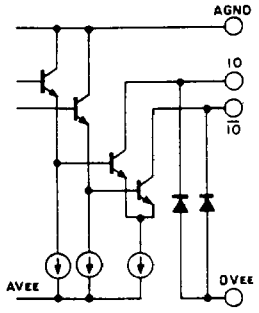
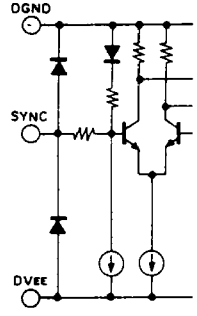
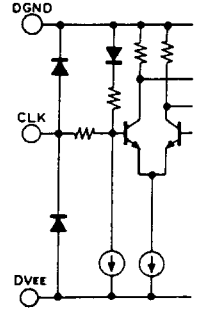
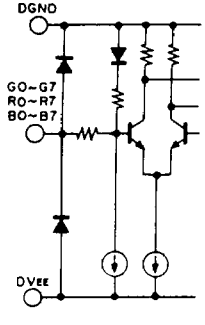
(c) Air Flow Rate 3.0m/sec

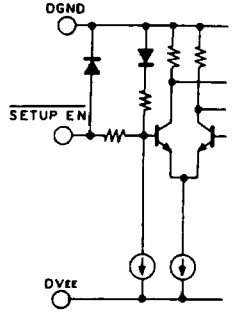
* Manufactured by Thermalloy Inc.
** PCB area 20 × 10 × 1.6mm
1-sided glass fiber epoxy board with 30% copper foil area

Pin Description and Input/Output Equivalent Circuit

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1 2	AVEE	–4.5V (typ.)		Analog power supply.
3	FS ADJUST	–1.3V (typ.)		Controls full-scale level for the D/A converter output. Output current can be adjusted by the resistor value externally connected between this pin and AGND. See the section on Description of Operation for details on how the external resistance should be selected.
4	NC			Unconnected pin. Leave this pin open.
5	BLANK	ECL		Control input for "blank". Setting the input to "1" fixes the D/A output to BLANK level regardless of input data for gray level. When the pin is left open, it functions as when it is set to "0". (See Input / Output Table)
6	OVERLAY	ECL		Control input for "overlay". Setting the input to "1" enhances the D/A output to level of 10% brighter than WHITE level regardless of input data for gray level. When the pin is left open, it functions as when it is set to "0". (See Input / Output Table)

6

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
7, 8 9, 10 11, 12	IO (B), $\overline{\text{IO (B)}}$ IO (R), $\overline{\text{IO (R)}}$ IO (G), $\overline{\text{IO (G)}}$	0 to −1071mV (typ.)		Complementary analog current outputs for red, green and blue (RGB). Output voltages are acquired when they are connected to external pull-up resistors.
13	SYNC	ECL		Control input for "composite sync". This functions only for IO (G), $\overline{\text{IO}}$ (G) output. Setting the input to "1" fixes the D/A output to SYNC level regardless of input data for gray level. When the pin is left open, it functions as when it is set to "0". (See Input / Output Table)
14	CLK	ECL		Clock input. All data and control inputs are latched by the rising edge of CLK. When the pin is left open, it functions as when it is set to "0".
26, 25 20 to 15	G0 to G7	ECL		Digital input for gray level. G0 (LSB) to G7 (MSB) input for GREEN. R0 (LSB) to R7 (MSB) input for RED. B0 (LSB) to B7 (MSB) input for BLUE. When the pin is left open, it functions as when it is set to "0". (See Input / Output Table)
34 to 27	R0 to R7			
42 to 35	B0 to B7			

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
21	AGND	GND		Analog GND. Separated from DGND.
22	$\overline{\text{SETUP EN}}$			Setting this pin to "1" or DGND makes BLANK level equal to BLACK level. Setting this pin to "0" or open makes BLANK level lower than BLACK level by 7.5IRE. (see Fig. 1 to 4)
23, 24	DGND	GND		Digital GND. Separated from AGND.
43	DV_{EE}	–4.5V (typ.)		Digital power supply. Separated from AV_{EE}.
44	NC			Unconnected pin.

6

Electrical Characteristics

(AVEE=DVEE=–4.5V, Ta=25℃)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		8	8	8	bit
Integral linearity error	EL	VFS=661mV			± 1/2	LSB
Differential linearity error	ED				± 1/2	LSB
Digital input current	IIH	VIN=–0.7V	0		180	µA
	IIL	VIN=–1.9V	–100		100	µA
Digital input capacitance	CIN			5		pF
Maximum output current	Io		48			mA
Output compliance voltage	Voc		–1.2		1.5	V
Output resistance	Ro			50		kΩ
Output capacitance	Co			10		pF
Output current						
Full gray scale error	EFS	VFS=661mV	–10	0	10	% of Gray Scale
Full gray scale balance (G, R, B) (Note 1)	EFSB		0	0.5	2.5	% of Gray Scale
Full gray scale temperature coefficient	TCFS			+0.06		% of Gray Scale/℃
Offset current	IOF		0		40	µA
Power supply current	IEE		–430	–310	–200	mA
Maximum conversion rate	FS MAX		400			MSPS
Set-up time (Note 2)	ts	Digital input/clock threshold voltage =–1.3V RL=25Ω	1.0			ns
Hold time (Note 2)	th		0.6			ns
Output rise time	tr			0.5	0.9	ns
Output fall time	tf			0.5	0.9	ns
Output delay	td		2.1	2.8	3.4	ns
Output pipeline delay	tPLD		1	1	1	Clock

Note 1) $E_{FSB}=\mathrm{Max}\{|V_{FS}(G)-V_{FS}(R)|, |V_{FS}(R)-V_{FS}(B)|, |V_{FS}(B)-V_{FS}(G)|\} \div [\{V_{FS}(G)+V_{FS}(R)+V_{FS}(B)\}/3] \times 100$

V_{FS} is full gray scale that is voltage difference between WHITE and BLACK level.

Note 2) Specified at $-20 \leqq T_c \leqq 70$℃

Description of Operation (See Block Diagram / Pin Configuration)

Each of RGB DATA (R0 to R7, G0 to G7, B0 to B7) and CONTROL signals (SYNC, BLANK, OVERLAY) are caught at the rising edge of CLK by LATCH (1).

The upper 4 bits of each DATA, which have been decoded into thermometer code in DECODER section, are transferred to DAC section via LATCH (2), together with the lower 4 bits and CONTROL signals.

DAC section creates analog current output composing of the following portions:

- Weighted lower 4-bit current
- Thermometer-coded upper 4-bit current
- Function output current

The output appears delayed by 1clock after the rising edge of CLK.

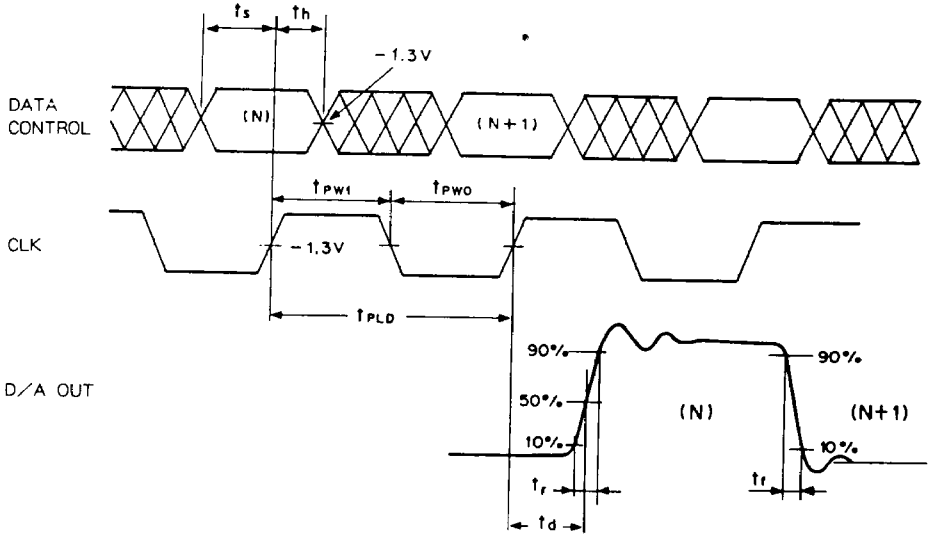
This analog current output is converted to voltage output by load resistor RL that is connected to the output pin.

Output full scale adjustment is possible by setting the value of Rset (shown in the formula below) located between FS ADJUST pin and AGND. The FS ADJUST voltage is produced by an internal band-gap voltage source.

$$Rset = \frac{V_{ADJ}}{\frac{V_{FS}}{R_L} \times \frac{16}{255}} \ [\Omega]$$

Here, V_{FS} represents typical voltage difference between WHITE level and BLACK level. V_{ADJ} is voltage at FS ADJUST pin.

For instance, Rset is approximately 750Ω for V_{FS}=661mV.

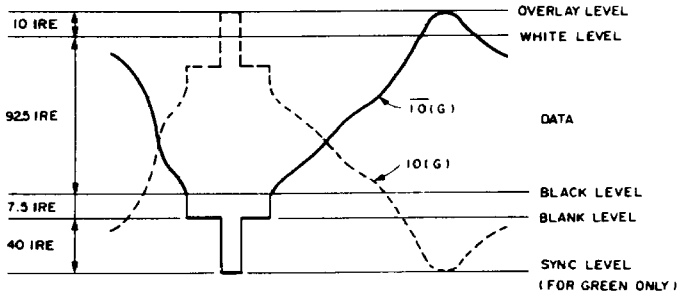


Timing Diagram

6

Output Levels (With SETUP function)

$\overline{IO}$ (G) (mA)	$\overline{VO}$ (G) (V)
0.00	0.000
−2.84	−0.071
−29.28	−0.732
−31.42	−0.785
−42.84	−1.071



* In case of doubly-terminated 50 Ω load.

Fig. 1. Composite Video Output Level (GREEN)

	$\overline{IO}$ (G) (mA)	IO (G) (mA)	$\overline{SETUP\ EN}$	OVERLAY	SYNC	BLANK	D/A Input Data
OVERLAY	0.00	−42.84	0	1	0	0	X X X X X X X X
WHITE	−2.84	−40.00	0	0	0	0	1 1 1 1 1 1 1 1
DATA			0	0	0	0	data
BLACK	−29.28	−13.56	0	0	0	0	0 0 0 0 0 0 0 0
BLANK	−31.42	−11.42	0	X	0	1	X X X X X X X X
SYNC	−42.84	0.00	0	X	1	X	X X X X X X X X

Table 1. Input/Output Table (GREEN)

$\overline{IO\ (R)}$, $\overline{IO\ (B)}$ (mA)	$\overline{VO\ (R)}$, $\overline{VO\ (B)}$ (V)
0.00	0.000
−2.84	−0.071
−29.28	−0.732
−31.42	−0.785

* In case of doubly-terminated 50 Ω load.

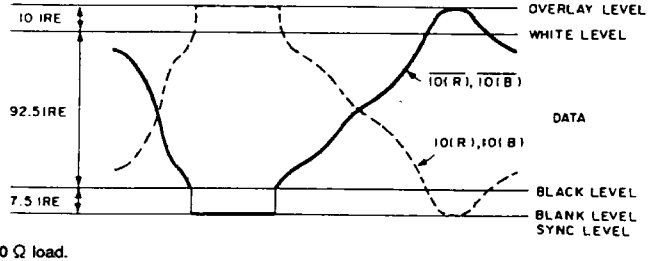


Fig. 2. Composite Video Output Level (RED, BLUE)

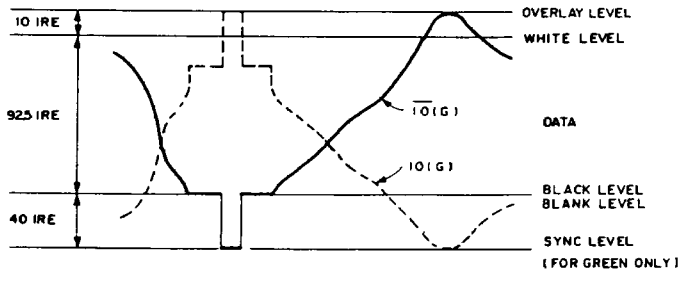
	$\overline{IO\ (R)}$, $\overline{IO\ (B)}$ (mA)	IO (R), IO (B) (mA)	$\overline{SETUP\ EN}$	OVERLAY	SYNC	BLANK	D/A Input Data
OVERLAY	0.00	−31.42	0	1	0	0	X X X X X X X X
WHITE	−2.84	−28.58	0	0	0	0	1 1 1 1 1 1 1 1
DATA			0	0	0	0	data
BLACK	−29.28	−2.14	0	0	0	0	0 0 0 0 0 0 0 0
BLANK	−31.42	0.00	0	×	0	1	X X X X X X X X
SYNC	−31.42	0.00	0	×	1	×	X X X X X X X X

Table 2. Input/Output Table (RED, BLUE)

6

Output Levels (Without SETUP function)

$\overline{IO}$ (G) (mA)	$\overline{VO}$ (G) (V)
0.00	0.000
−2.84	−0.071
−29.28	−0.732
−40.70	−1.018



* In case of doubly-terminated 50 Ω load.

Fig. 3. Composite Video Output Level (GREEN)

	$\overline{IO}$ (G) (mA)	IO (G) (mA)	$\overline{SETUP\ EN}$	OVERLAY	SYNC	BLANK	D/A Input Data
OVERLAY	0.00	−40.70	1	1	0	0	× × × × × × × ×
WHITE	−2.84	−37.86	1	0	0	0	1 1 1 1 1 1 1 1
DATA			1	0	0	0	data
BLACK	−29.28	−11.42	1	0	0	0	0 0 0 0 0 0 0 0
BLANK	−29.28	−11.42	1	×	0	1	× × × × × × × ×
SYNC	−40.70	0.00	1	×	1	×	× × × × × × × ×

Table 3. Input/Output Table (GREEN)

$\overline{IO(R)}$, $\overline{IO(B)}$ (mA)	$\overline{VO(R)}$, $\overline{VO(B)}$ (V)
0.00	0.000
− 2.84	− 0.071
− 29.28	− 0.732

* In case of doubly-terminated 50 Ω load.

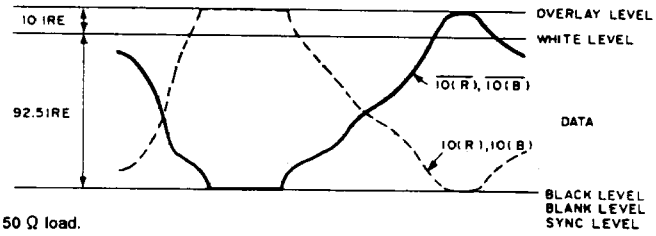


Fig. 4. Composite Video Output Level (RED, BLUE)

	$\overline{IO(R)}$, $\overline{IO(B)}$ (mA)	IO (R), IO (B) (mA)	$\overline{SETUP\ EN}$	OVERLAY	SYNC	BLANK	D/A Input Data
OVERLAY	0.00	−29.28	1	1	0	0	× × × × × × × ×
WHITE	−2.84	−26.44	1	0	0	0	1 1 1 1 1 1 1 1
DATA			1	0	0	0	data
BLACK	−29.28	0.00	1	0	0	0	0 0 0 0 0 0 0 0
BLANK	−29.28	0.00	1	×	0	1	× × × × × × × ×
SYNC	−29.28	0.00	1	×	1	×	× × × × × × × ×

Table 4. Input/Output Table (RED, BLUE)

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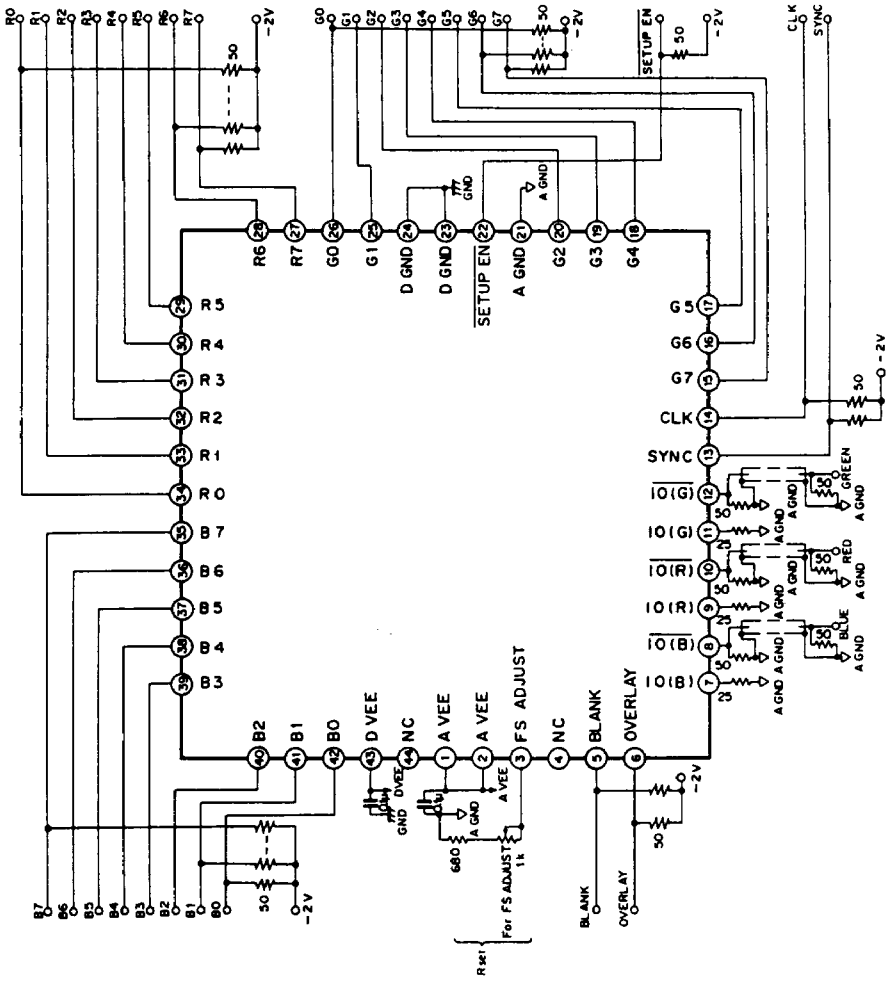
Application Circuit (In case of using 50Ω coaxial cable for output)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

(1) Wiring for Digital Inputs

- All digital inputs are single-ended and ECL compatible. For high-speed operation, it is recommended that line characteristic impedance and termination resistance should be set at 50Ω. The line termination resistors should be placed nearest to the IC input pins.

(2) Noise Reduction Measures

- Use as wide GND plane as possible to reduce parastic inductance and resistance on the board.
- It is advisable to separate AGND and DGND on the board. This also applies for AV_{EE} and DV_{EE}. Also, the connections between AGND and DGND, AV_{EE} and DV_{EE} should respectively be made at the board connector section (entrance/exit of the board).
- AV_{EE} and DV_{EE} pins should be bypassed to AGND/DGND planes of the board as close as possible to the IC, via capacitors of approximately 0.1 µF. Ceramic chip capacitors are recommended.
- V_{TT} (–2V) that is connected with termination resistors should be bypassed to DGND plane via capacitors of approximately 0.1 µF. The capacitors should be located nearest to the termination resistors. Ceramic chip capacitors are recommended.
- An external resistor Rset should be connected as close as possible both to FSADJ pin and AGND. The lead length of the resistor and the pattern length on the board should be as short as possible, in order to minimize noise effect. Also, any capacitors should not be connected with FSADJ pin.

(3) Analog Output Processing

This D/A converter is designed so that it is possible to directly drive 50Ω and 75Ω lines. In order to ensure line matching, it is necessary to terminate both ends of the line with 50Ω (or 75Ω), as indicated in Application Circuit.

In addition, even if some of the following outputs IO (G), $\overline{\text{IO (G)}}$, IO (R), $\overline{\text{IO (R)}}$, IO (B), $\overline{\text{IO (B)}}$ are not used, do not leave the pins open, and be sure to connect them to AGND via 25Ω or directly.

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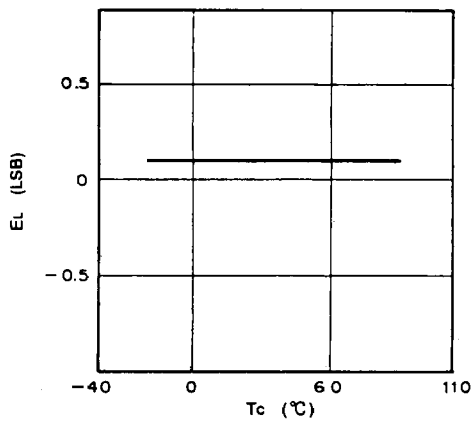
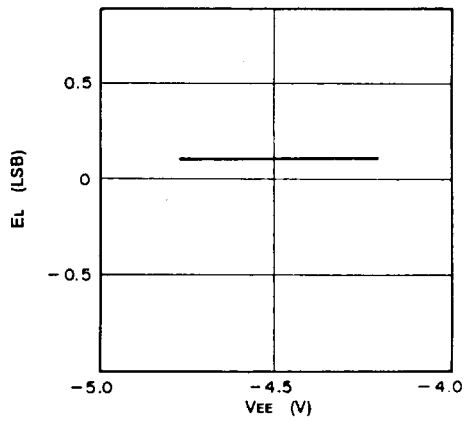
Typical Characteristics

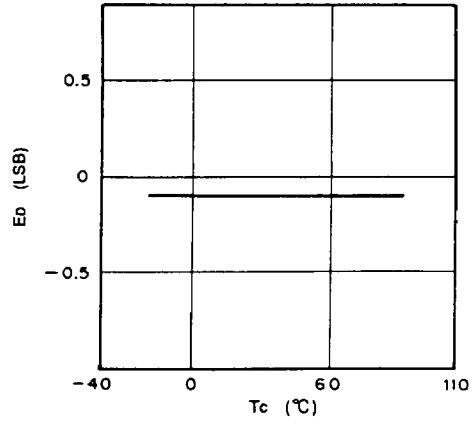
Integral linearity error vs. Tc



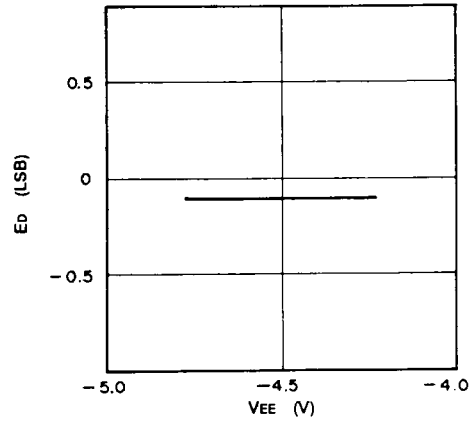
Integral linearity error vs. Supply voltage



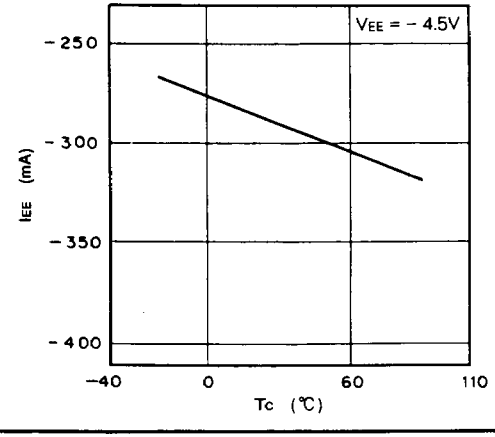
Differential linearity error vs. Tc



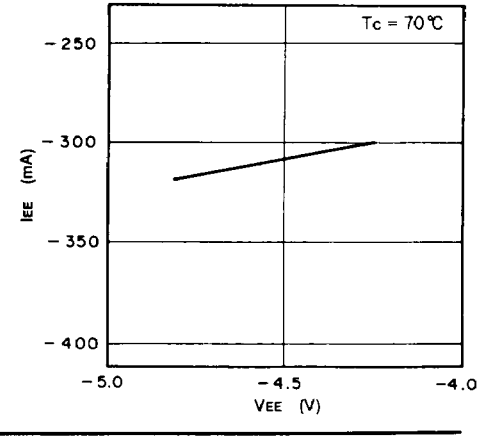
Differential linearity error vs. Supply voltage



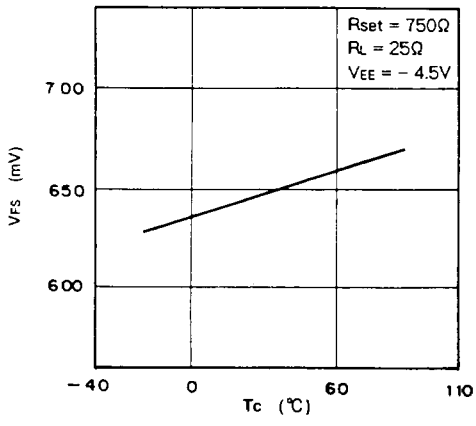
Power supply current vs. Tc



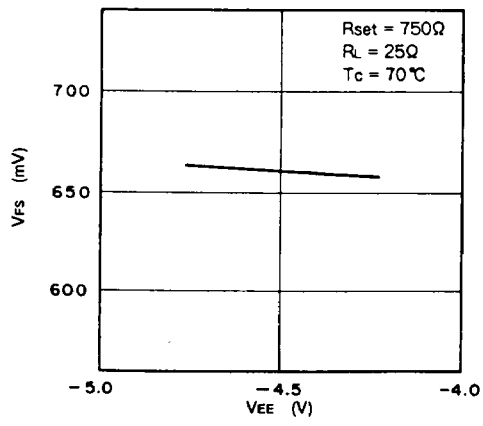
Power supply current vs. Supply voltage



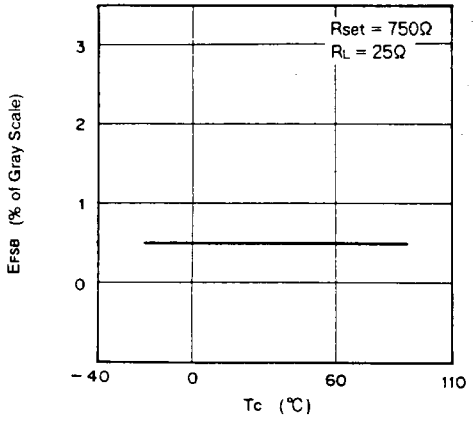
Full gray scale vs. Tc



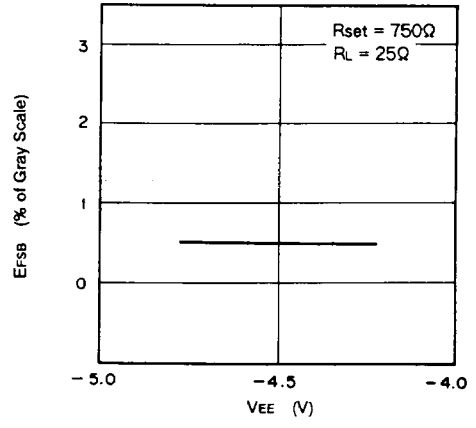
Full gray scale vs. Supply voltage



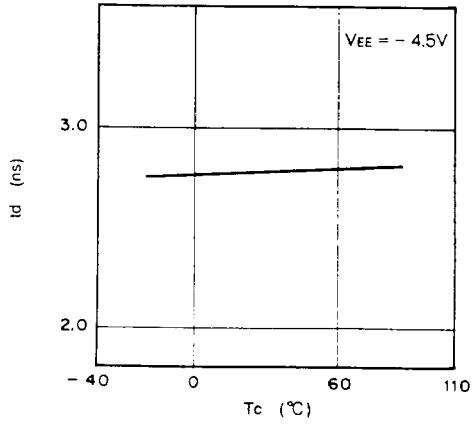
Full gray scale balance vs. Tc



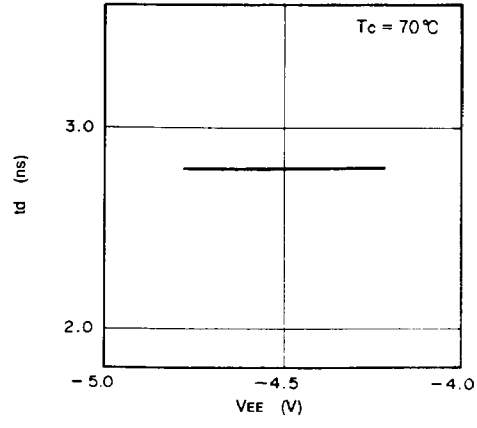
Full gray balance vs. Supply voltage



Output delay vs. Tc



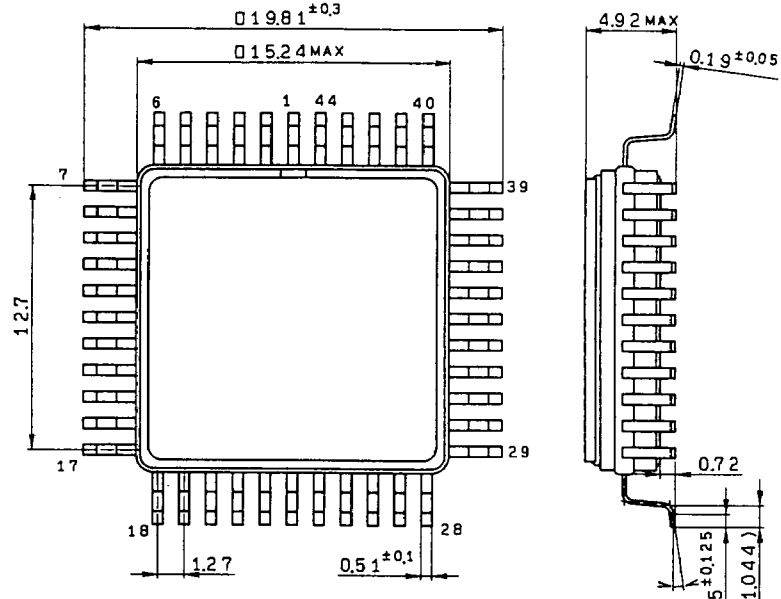
Output delay vs. Supply voltage



6

Package Outline Unit : mm

44pin QFP (Ceramic)

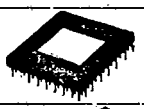
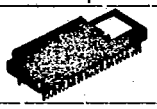


SONY NAME	QFP-44C-L01
EIAJ NAME	XQFP044-G-0000-A
JEDEC CODE	MO-084-AB *

* (Similar)

T-90-20

Sony Package Product Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	4-direction
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT PACKAGE		P	1.0mm 0.8mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull Wing	2-direction
	Standard chip carrier	PLCC	PLASTIC LEADED CHIP CARRIER		P	1.27mm (50MIL)	J-bend	4-direction
		LCC	LEAD LESS CHIP CARRIER		C	1.27mm (50MIL)	Lead less	Package side
	Shrink chip carrier	SPLCC (PLCC)	SHRINK PLASTIC LEADED CHIP CARRIER		P	1.27mm Max. (50MIL Max.)	J-bend	4-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEAD PACKAGE		P	1.27mm (50MIL)	J-bend	2-direction

*P……Plastic, C……Ceramic