

SONY®

# CXA1182Q-Z/S

## Servo Signal Processor for CD Player

**For the availability of this product, please contact the sales office.**

### Description

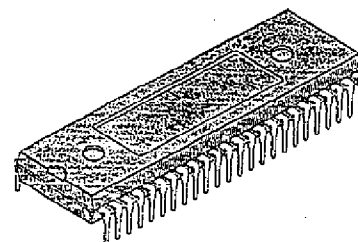
CXA1182 is a bipolar IC designed for the servo control of compact disc players.

### Features

- Single power supply, 5V  
Dual power supply,  $\pm 5V$
- Low power consumption  
 $\pm 5V$ : 165mW (Typ.), 5V: 100mW (Typ.)
- Servo functions same as the CX20108 (focus, tracking, and sled servo)
- Built-in LPF for spindle servo
- Built-in loop filter and VCO for EFM clock reproduction PLL
- Few external parts
- Built-in circuit to prevent sled runaway
- Built-in circuit for disc defects
- Built-in anti-shock circuit
- High-speed access through linear motor
- Microcomputer serial data bus common with CX23035 or CXD1135Q types
- Upward compatible with CX20108 for microcomputer software
- Peaks of focus search, track jump, and sled kick pulse can be set through external resistors.

CXA1182Q-Z  
48 pin QFP (Plastic)

CXA1182S  
48 pin SDIP (Plastic)



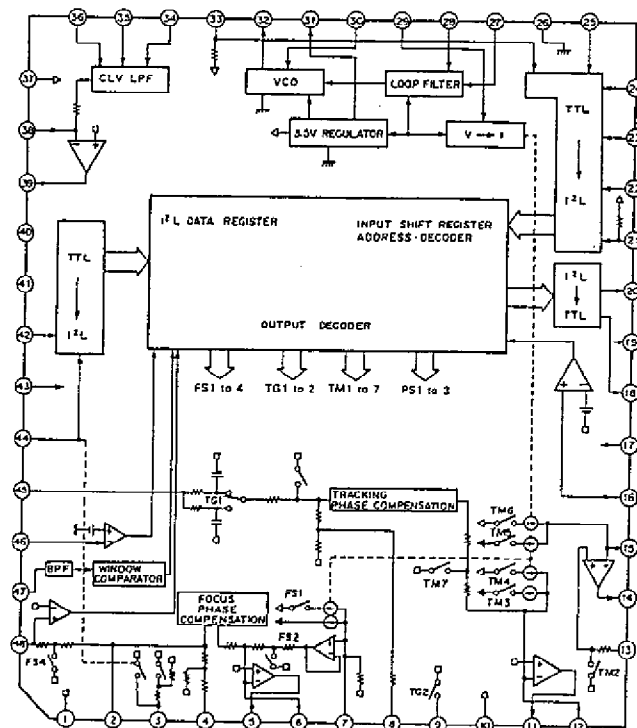
### Functions

- Focus servo control
- Tracking servo control
- Sled servo control
- Spindle servo  
LPF, drive amplifier
- EFM clock reproduction PLL  
Loop filter, 8.64 MHz VCO

### Structure

Bipolar silicon monolithic IC

### Block Diagram



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**Absolute Maximum Ratings (Ta = 25°C)**

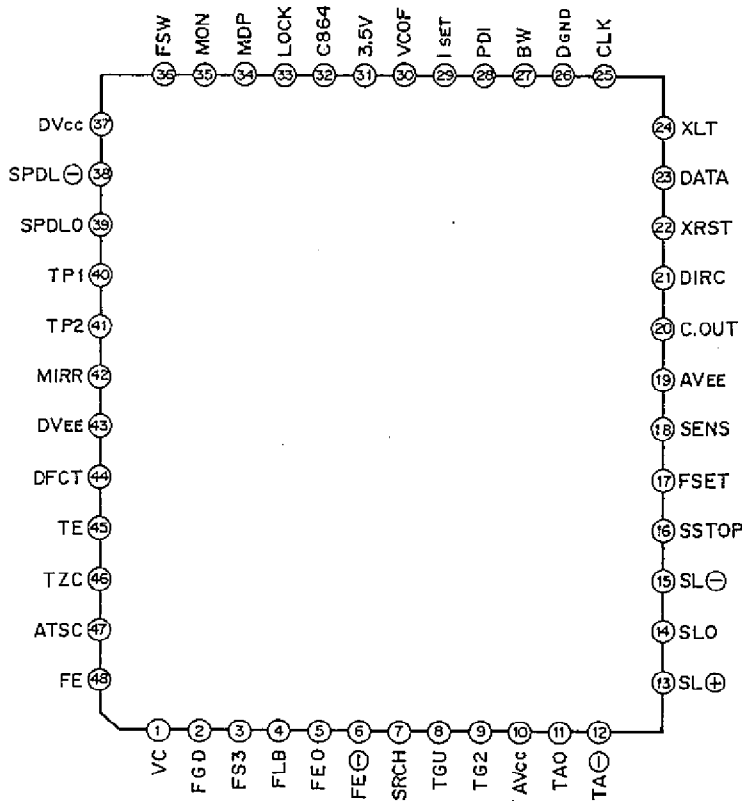
• Supply voltage	VCC - VEE	12	V
• Operating temperature	Topr	-20 to +75	°C
• Storage temperature	Tstg	-55 to +150	°C
• Allowable power dissipation	Pd	CXA1182Q 833	mW
		CXA1182S 1330	mW

**Recommended Operating Conditions**

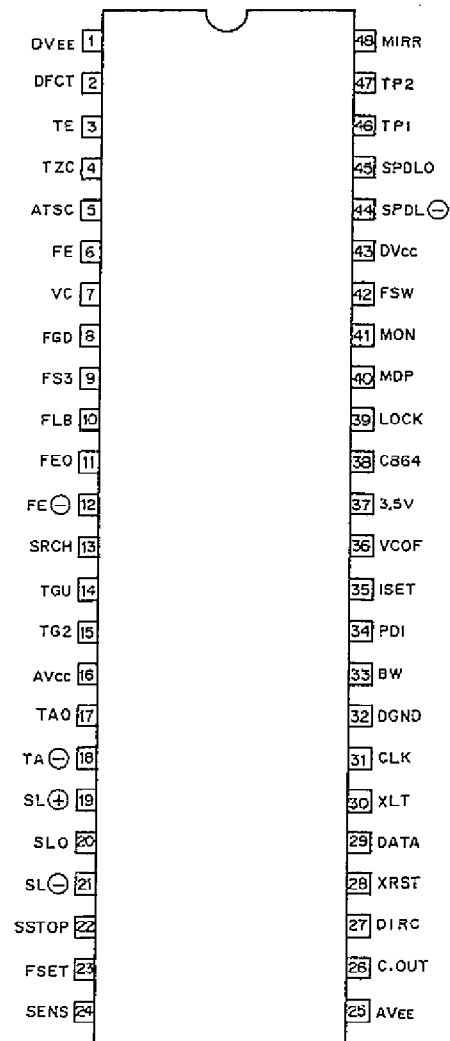
• Supply voltage	VCC - VEE	4 to 11	V
	VCC - DGND	4 to 5.5	V

**Pin Description**

CXA1182Q-Z



CXA1182S



Numbers in ( ) show CXA1182S

No.		Symbol	Equivalent Circuit	Description
Q-Z	S			
2	8	FGD		Connect a capacitor between this pin and pin 3 (9) to reduce the high-frequency gain.
3	9	FS3		The high-frequency gain of the focus servo can be changed by switching FS3 ON or OFF.
4	10	FLB		External time constant setting pin to raise the low bandwidth of the focus servo.
5	11	FEO		Focus drive output
11	19	TAO		Tracking drive output
14	20	SLO		Sled drive output
39	45	SPDLO		Spindle drive output
6	12	FE -		Inverse input pin for the focus amplifier.
7	13	SRCH		External time constant setting pin to generate focus search waveforms.

No.		Symbol	Equivalent Circuit	Description
Q-Z	S			
8	14	TGU		External time constant setting pin to switch the tracking high-frequency gain.
9	15	TG2		External time constant setting pin to change the tracking high-frequency gain.
12	18	TA -		Inverse input pin for the tracking amplifier.
13	19	SL +		Non-inverse input pin for the sled amplifier.
15	21	SL -		Inverse input pin for the sled amplifier.
16	22	SSTOP		Signal pin for detecting for the ON/OFF limit switch of the innermost part of the disc.

No.		Symbol	Equivalent Circuit	Description
Q-Z	S			
17	23	FSET		Setting pin for the peak frequency of the focus and/or the tracking phase compensation and the $f_0$ of CLV LPF.
18	24	SENS		Pin to output FZC, AS, TZC, and SSTOP by command from CPU.
20	26	C. OUT		
21	27	DIRC		Pin for one-track jump Contains a 47 k $\Omega$ pull-up resistor.
22	28	XRST		Reset input pin, reset at "L"
23	29	DATA		Serial data input from CPU
24	30	XLT		Latch input from CPU
25	31	CLK		Serial data transfer clock input from CPU
33	39	LOCK		Pin for the operation of the sled runaway prevention circuit at "L" Contains a 47 k $\Omega$ pull-up resistor.
27	33	BW		External time constant setting pin for the loop filter.
28	34	PDI		Input pin for the CX23035/CXD1135 phase comparator output PDO.
29	35	ISET		Input current to determine the peaks of focus search, track jump, and sled kick.

No.		Symbol	Equivalent Circuit	Description
Q-Z	S			
30	36	VCOF		The free-running frequency of VCO is almost proportional to the resistance value between this pin and pin 31 (37).
32	38	C864		VCO output pin of 8.64 MHz.
34	40	MDP		Connecting pin to the CX23035/CXD1135 MDP pin.
35	41	MON		Connecting pin to the CX23035/CXD1135 MON pin.
36	42	FSW		LPF time constant setting external pin for the CLV servo error signal.
38	44	SPDL -		Inverse input pin for the spindle drive amplifier.

No.		Symbol	Equivalent Circuit	Description
Q-Z	S			
40	46	TP1		<p>Pins 40 and 41 are equivalent to CXA1082's WDCK and FOK. However with CXA1182, they do not function. Here, set either DVEE and DGND to open or use WDCK and FOK.</p> <p>Mirror signal input pin</p> <p>Defect signal input pin. The defect counter-measure circuit operates at "H".</p>
41	47	TP2		
42	48	MIRR		
44	2	DFCT		
45	3	TE		Input pin for tracking error signals.
46	4	TZC		Input pin for the zero-cross tracking comparator.
47	5	ATSC		Input pin of the window comparator for ATSC detection.
48	6	FE		Input pin for focus error signals.

Electrical Characteristics

Ta = 25°C AV<sub>CC</sub>, DV<sub>CC</sub> = 2.5V AV<sub>EE</sub>, DV<sub>EE</sub> = -2.5V DGND = -2.5V

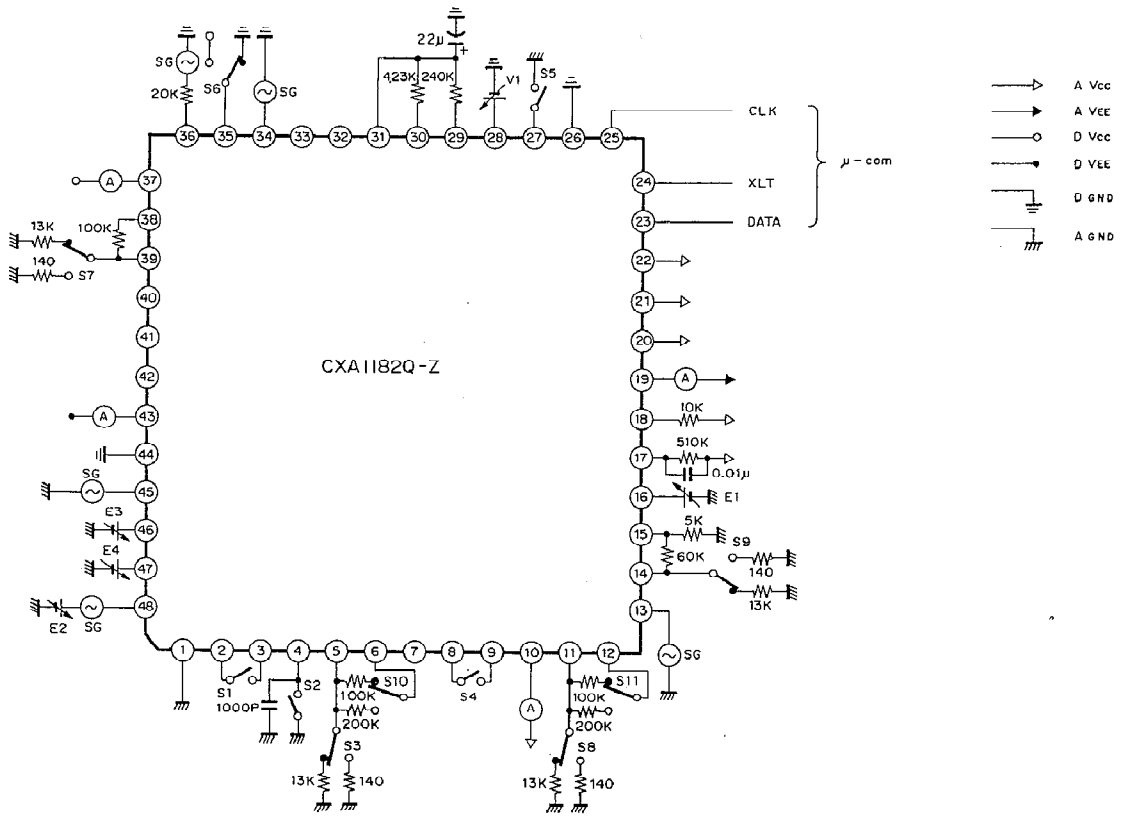
Test No.	Test items	Symbol	SW conditions											* SD	Bias conditions				Input point	Test point	Description of output waveform and test method	Min.	Typ.	Max.	Unit	
			S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11		E1	E2	E3	E4								
1	Supply current 1	AICC													00	0	0	0	0	10	Measure after resetting	2.8	5.5	8.2	mA	
2	Supply current 2	DICC																		37		10.8	15.0	19.2	mA	
3	Supply current 3	A, DIEE																		19 43		9.8	13.0	16.2	mA	
4	Supply current 4	JDGND																		26		4.8	7.5	10.2	mA	
5	DC voltage gain	GPEO													08					48		5	SG = 10 Hz, 200mVp-p	18.0	21.0	24.0
6	Feedthrough	VPEOF	○	○																		SG=10Hz, 40mVp-p, Gain difference between 08 and 00 of SD			-35	dB
7	Max. output voltage 1	VPEO1												○	08							SG = 0.5VDC	1.98			V
8	Max. output voltage 2	VPEO2												○	08							SG = -0.5VDC			-1.98	V
9	Max. output voltage 3	VPEO3			○									○	08							SG = 0.5VDC	1.18			V
10	Max. output voltage 4	VPEO4			○									○	08							SG = -0.5VDC			-1.18	V
11	Search output voltage 1	VSRCH1													02								-0.64	-0.55	-0.36	V
12	Search output voltage 2	VSRCH2													03								0.36	0.55	0.64	V
13	DC voltage gain	GTEO				○									25					45	11	SG = 10 Hz, 500mVp-p	11.6	14.6	17.6	dB
14	Feedthrough	VTEOF				○									13							SG=10Hz, 100mVp-p, Gain difference between 25 and 00 of SD			-39	dB
15	Max. output voltage 1	VTEP1												○	25							SG = -1.5VDC	1.98			V
16	Max. output voltage 2	VTEP2												○	25							SG = 1.5VDC			-1.98	V
17	Max. output voltage 3	VTEP3												○	25							SG = -1.5VDC	1.18			V
18	Max. output voltage 4	VTEP4												○	25							SG = 1.5VDC			-1.18	V
19	Jump output voltage 1	VJUMP1													2C								-0.64	-0.55	-0.36	V
20	Jump output voltage 2	VJUMP2													2B								0.36	0.55	0.64	V
21	DC voltage gain	GSLO													25					13	14	SG = 10 Hz, Openloop gain	50	56	62	dB
22	Max. output voltage 1	VSLP1													25							SG = 0.4VDC	1.98			V
23	Max. output voltage 2	VSLP2													25							SG = -0.4VDC			-1.98	V
24	Max. output voltage 3	VSLP3												○	25							SG = 0.4VDC	1.18			V

\*Serial data (hex)



Test No.	Test items	Symbol	SW conditions											*	Bias conditions				Input point	Test point	Description of output waveform and test method	Min.	Typ.	Max.	Unit		
			S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11		SD	E1	E2	E3								E4	
25	Max. output voltage 4	VSLP4													25	0	0	0	0	13	14	SG = -0.4VDC				-1.18	V
26	Feed through	VSTOF																				SG = 10kHz, 200mVp-p, Gain difference between 25 and 20 of SD				-34	dB
27	Kick output voltage 1	VKICK1													22								-0.75	-0.6	-0.45	V	
28	Kick output voltage 2	VKICK2													23								0.45	0.6	0.75	V	
29	Spindle servo gain	GSPO																		34	39	SG = 10Hz, 200mVp-p	14	16.5	19	dB	
30	Max. output voltage 1	VSPP1																				SG = 1.0VDC	1.78			V	
31	Max. output voltage 2	VSPP2																				SG = -1.0VDC				-1.78	V
32	Max. output voltage 3	VSPP3																				SG = 1.0VDC	1.13			V	
33	Max. output voltage 4	VSPP4																				SG = -1.0VDC				-1.13	V
34	PLL Reg. output voltage	Vreg																			31	DC voltage	3.3	3.5	3.85	V	
35	Self-running frequency	FVCO															0				32	V <sub>i</sub> = 0mV	2.4	8.6	9.7	MHz	
36	Frequency deviation 1	ΔF <sub>1</sub>																				Frequency deviation from FVCO, V <sub>i</sub> = 148mV	7	11	15	%	
37	Frequency deviation 2	ΔF <sub>2</sub>																				V <sub>i</sub> = -148mV	-15	-11	-7	%	
38	SENS low level	VSSENS																			18					-1.98	V
39	COUT low level	VCOUT																			20					-1.98	V
40	FZC threshold value	VTZC													00		*				48	18		39	50	61	mV
41	ATSC threshold value	VATSC1													10		0		*		47		* Value of E when SENS becomes High (=1.1V) by E1 to E4 varying	-45	-26	-7	mV
42	ATSC threshold value	VATSC2													10				*		47			7	26	45	mV
43	TZC threshold value	VTZC													20			*	0		46		SG = 0V	-20	0	20	mV
44	SSTOP threshold value	VSSTOP													30	*		0			16			-65	-50	-35	mV

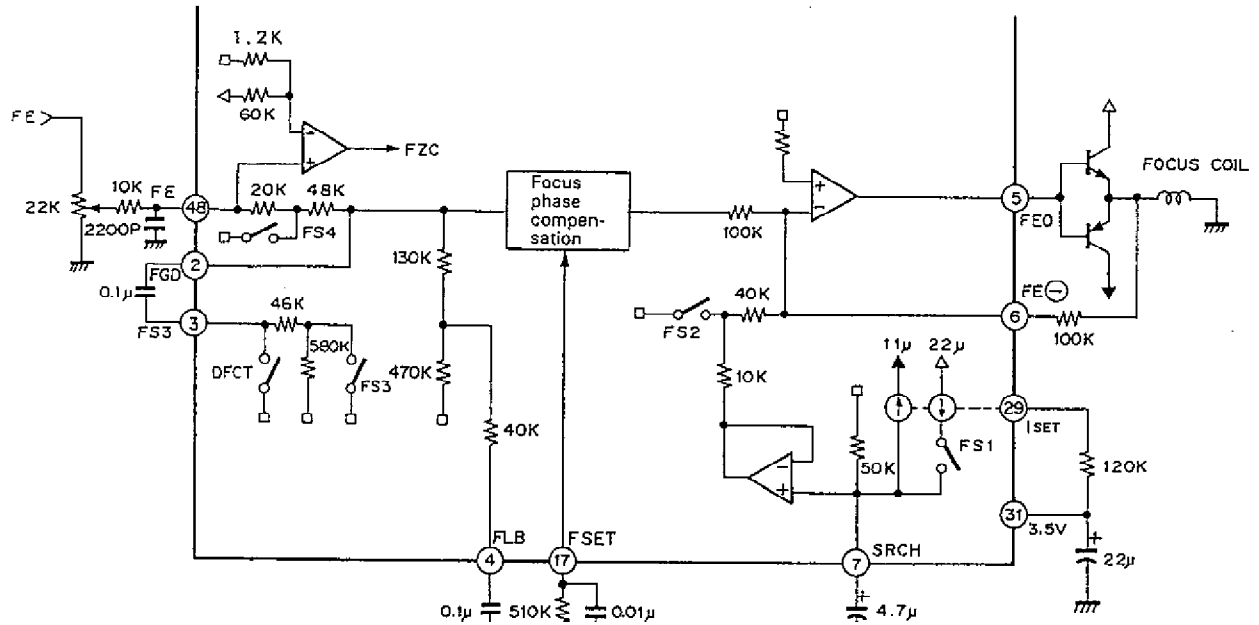
**Electrical Characteristics Test Circuit**  
 (See the Pin Configuration for CXA1182S)



Description of Functions

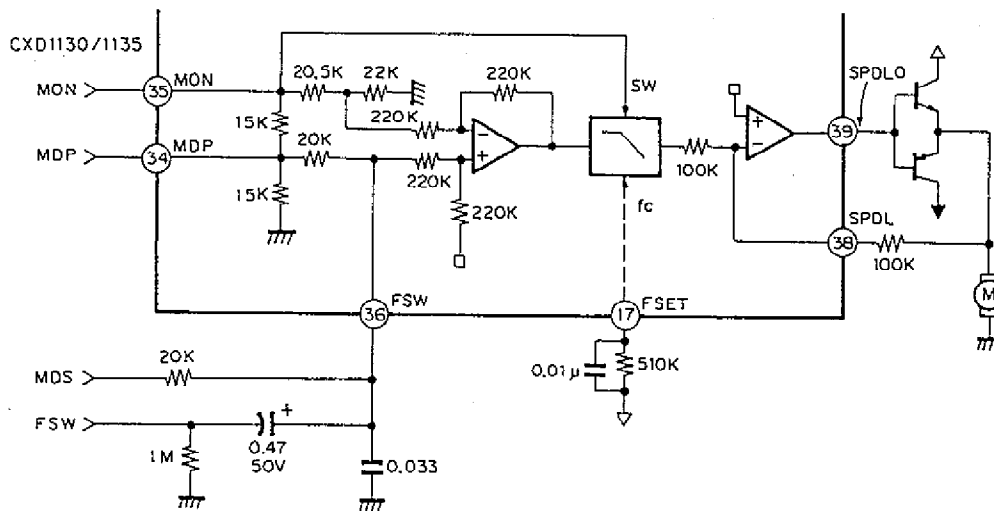
Focus servo system

(See the Pin Configuration for CXA1182S)





Spindle servo and LPF



The 200 Hz LPF is formed with 0.033  $\mu$ F and 20 k $\Omega$  connected to pin 36. The secondary LPF is formed with the built-in LPF ( $f_c$  up to 200 Hz with 510 k $\Omega$  for pin 17), and the carrier component of the CLV servo error signals MDS and MDP is eliminated.

In the CLV-S mode, FSW becomes L and pin 36 LPF  $f_c$  lowers, strengthening the filter further. By connecting the pin 17 resistor to Vcc, even if stability is not achieved,  $f_c$  does not vary with power supply voltage fluctuations.

Note) Use the phase compensation instead of MDS when CX23035 is used.

## Commands

The input data that activates this IC consists of 8 bits. It shall be represented as \$XX in two hexadecimal digits. (X Denotes 0 to F). Commands for the CXA1082AQ are classified into 4 types — \$0X to 3X.

### 1. \$0X [SENSE Pin 18 is "FZC"]

This command is related to the focus servo control.

The bit configuration is as follows:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	FS4	FS3	FS2	FS1

The four switches FS1 to FS4 are related to focusing, and correspond to D0 to D3.

\$00 At FS1 = 0, Pin 7 is charged to  $(22\mu\text{A} - 11\mu\text{A}) \times 50\text{ k}\Omega = 0.55\text{ V}$ .

If FS2 = 0, this voltage is not output and the output of Pin 5 remains 0 V.

\$02 From the above state, FS2 only becomes 1 and a negative output is output to Pin 5.

This voltage level is stipulated as follows:

$$(22\ \mu\text{A} - 11\ \mu\text{A}) \times 50\ \text{k}\Omega \times \frac{\text{Resistance value between Pin 5 and Pin 6}}{50\ \text{k}\Omega} \dots (1)$$

\$03 From the above state, FS1 becomes 1 and the current supply of +22  $\mu\text{A}$  is separated.

Then, the CR charge/discharge circuit is formed and Pin 7 voltage decreases as time passes, as shown in Fig. 1.



## 1) Description of FS4

This switch placed between focus error input 48 and the focus phase compensation, serves to switch on and off the focus servo.

\$00 → \$08  
Focus off ← Focus on

## 2) Focusing procedure

Assume the polarity is as follows:

- The searching lens moves away or toward the disc.
- At the same time, the output voltage of Pin 5 varies from negative to positive.
- Further on, the focus S-curve changes as follows:

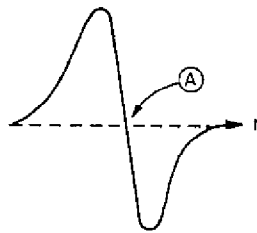


Fig. 3 S-curve

The focus servo is activated at the operating point **A** shown in Fig. 3. Generally, focus servo is switched on for focus searching while passing that **A** point. Moreover, a logical product (AND) is used with the Focus-OK signal to prevent malfunction.

Note here that  $\phi 08$  should be commanded in the shortest time after FZC changes from H to L. For this purpose, the (b) sequence required for software is better than (a).

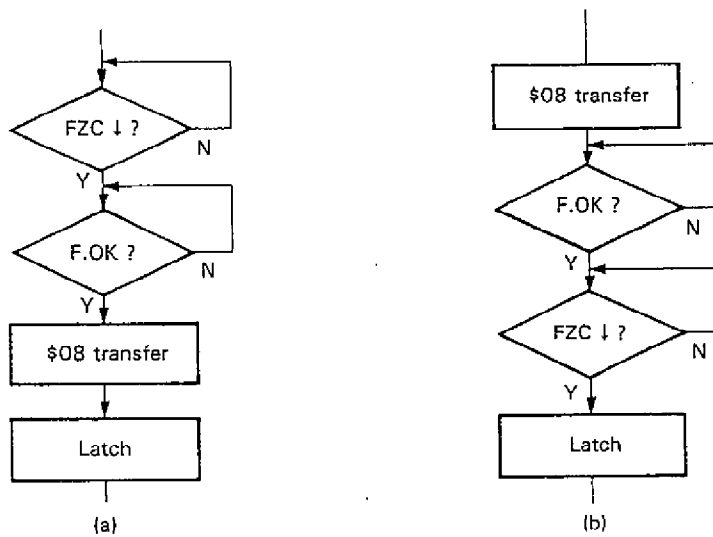


Fig. 5 Bad Sequence and Good Sequence



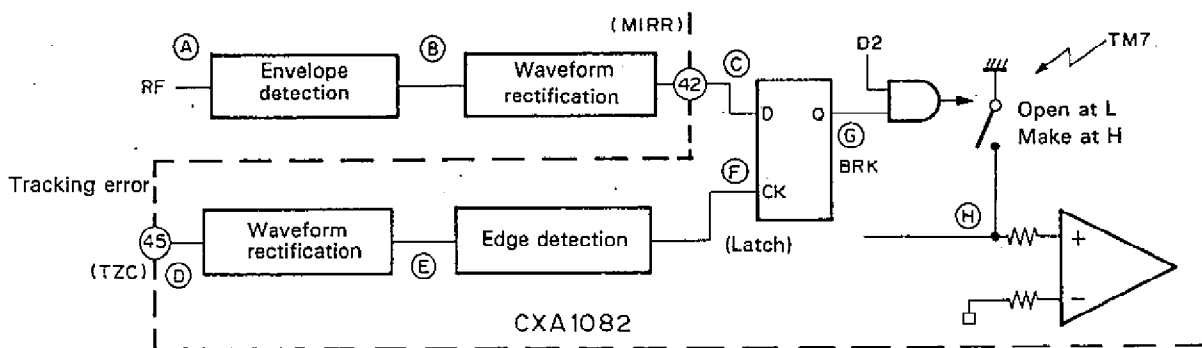
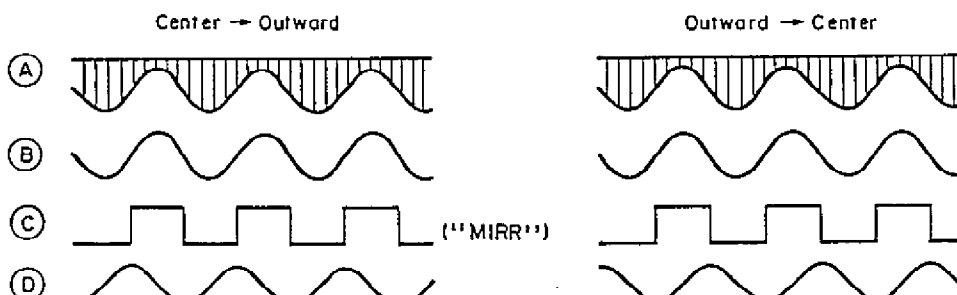


Fig. 6 TM7 Movement (Break Circuit)



DIRC Pin 21 and 1 Track Jump

Generally, for a 1-track jump, an acceleration pulse is added, then a deceleration pulse is given for a specified time from the moment the tracking error passes the 0 point after that, the tracking servo is switched on again. For the 100-track jump to be explained in the next item, as long as the number of tracks is about 100 there is no problem. But for the 1-track jump it must be exactly one. This is why the above complicated procedure is required. For the 1-track jump of a CD player, both the acceleration and deceleration take about 300 to 400  $\mu$ s. When software is used to execute this operation, the flow chart will be as shown in Fig. 9. Practically however, it takes time to transfer data.

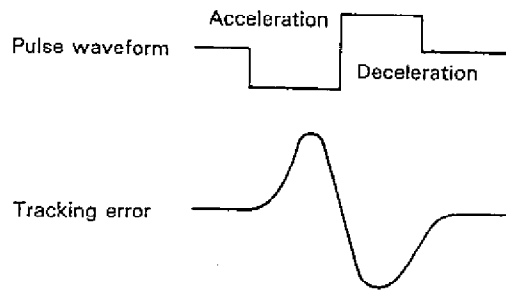


Fig. 8 Pulse Waveform and Tracking Error of 1-Track Jump



## 4. \$3X

This command is used for switching the Focus search and Sled kick peak value.

D0, D1 ..... Sled, NORMAL feed, high-speed feed

D2, D3 ..... Focus search peak switching

D7	D6	D5	D4	Focus search peak		Sled kick peak		Relative value
				D3 (PS3)	D2 (PS2)	D1 (PS1)	D0 (PS0)	
0	0	1	1	0	0	0	0	± 1
				0	1	0	1	± 2
				1	0	1	0	± 3
				1	1	1	1	± 4

## Others

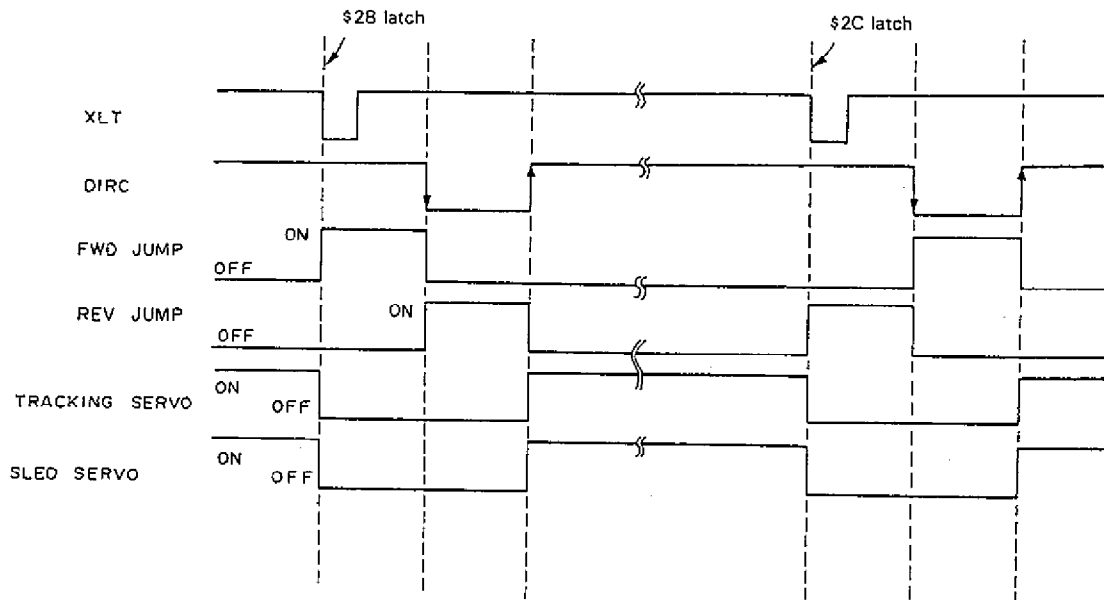
## 1. Connection of the power supply pin

	Vcc	Vss	VC
±5V dual power supply	+5V	-5V	0V
5V single power supply	+5V	0V	VC*

\*CXA1081

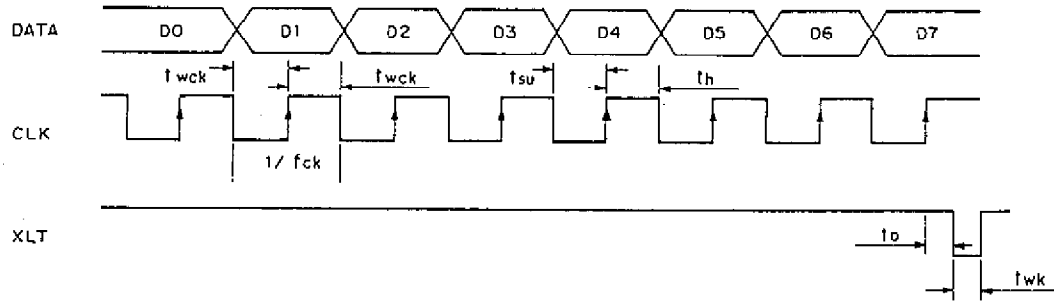
Parallel Direct Interface

1. DIRC



2. LOCK (Sled runaway prevention circuit)

CPU Serial Interface Timing Chart



$DV_{cc} - DGND = 4.5$  to  $5.5V$

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	$f_{ck}$			1	MHz
Clock pulse width	$t_{wck}$	500			ns
Hold time	$t_{su}$	500			ns
Setup time	$t_h$	500			ns
Delay time	$t_o$	500			ns
Latch pulse width	$t_{wl}$	1000			ns

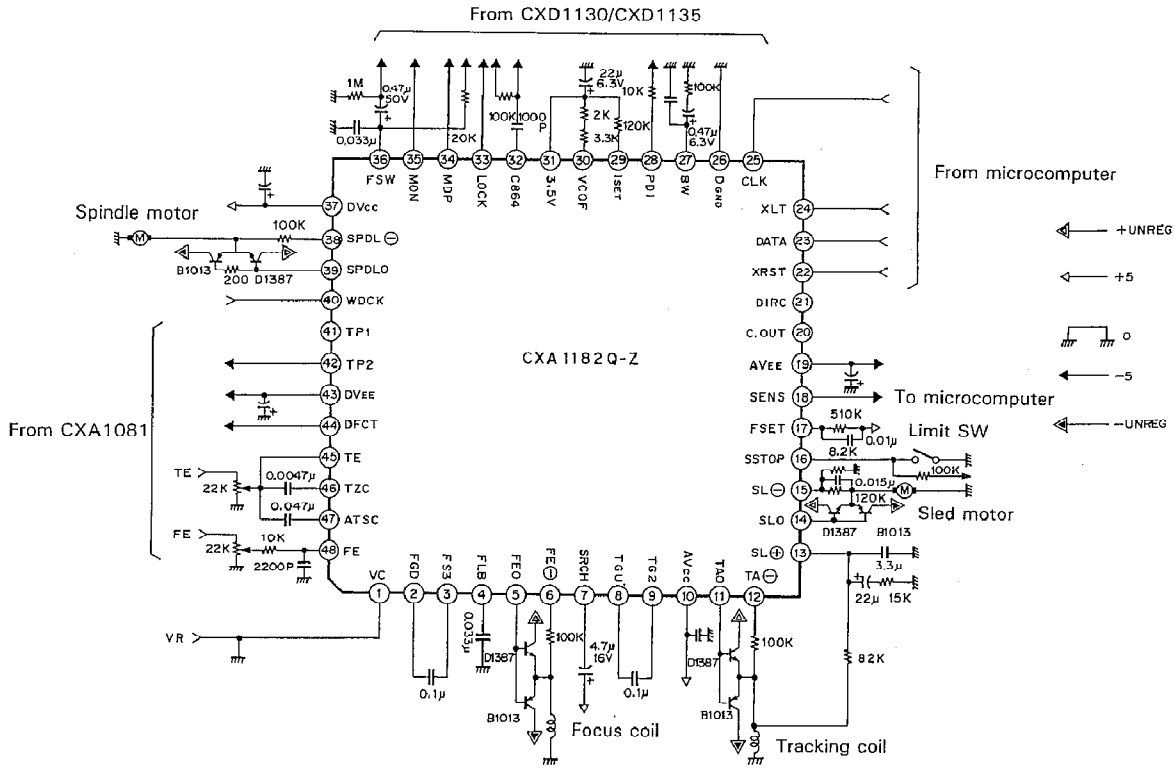
Serial Data Truth Table

Serial data	Hexa.	Function
FOCUS CONTROL		FS = 4321
0 0 0 0 0 0 0 0	\$00	0 0 0 0
0 0 0 0 0 0 0 1	\$01	0 0 0 1
0 0 0 0 0 0 1 0	\$02	0 0 1 0
0 0 0 0 0 0 1 1	\$03	0 0 1 1
0 0 0 0 0 1 0 0	\$04	0 1 0 0
0 0 0 0 0 1 0 1	\$05	0 1 0 1
0 0 0 0 0 1 1 0	\$06	0 1 1 0
0 0 0 0 0 1 1 1	\$07	0 1 1 1
0 0 0 0 1 0 0 0	\$08	1 0 0 0
0 0 0 0 1 0 0 1	\$09	1 0 0 1
0 0 0 0 1 0 1 0	\$0A	1 0 1 0
0 0 0 0 1 0 1 1	\$0B	1 0 1 1
0 0 0 0 1 1 0 0	\$0C	1 1 0 0
0 0 0 0 1 1 0 1	\$0D	1 1 0 1
0 0 0 0 1 1 1 0	\$0E	1 1 1 0
0 0 0 0 1 1 1 1	\$0F	1 1 1 1
TRACKING CONTROL		AS= 0      AS= 1
		TG= 2 1    TG= 2 1

Serial data	Hexa.	Function		
		DIRC=1 TM = 654321	DIRC=0 654321	DIRC=1 654321
0 0 1 0 0 0 0 0	\$20	000000	001000	000011
0 0 1 0 0 0 0 1	\$21	000010	001010	000011
0 0 1 0 0 0 1 0	\$22	010000	011000	100001
0 0 1 0 0 0 1 1	\$23	100000	101000	100001
0 0 1 0 0 1 0 0	\$24	000001	000100	000011
0 0 1 0 0 1 0 1	\$25	000011	000110	000011
0 0 1 0 0 1 1 0	\$26	010001	010100	100001
0 0 1 0 0 1 1 1	\$27	100001	100100	100001
0 0 1 0 1 0 0 0	\$28	000100	001000	000011
0 0 1 0 1 0 0 1	\$29	000110	001010	000011
0 0 1 0 1 0 1 0	\$2A	010100	011000	100001
0 0 1 0 1 0 1 1	\$2B	100100	101000	100001
0 0 1 0 1 1 0 0	\$2C	001000	000100	000011
0 0 1 0 1 1 0 1	\$2D	001010	000110	000011
0 0 1 0 1 1 1 0	\$2E	011000	010100	100001
0 0 1 0 1 1 1 1	\$2F	101000	100100	100001

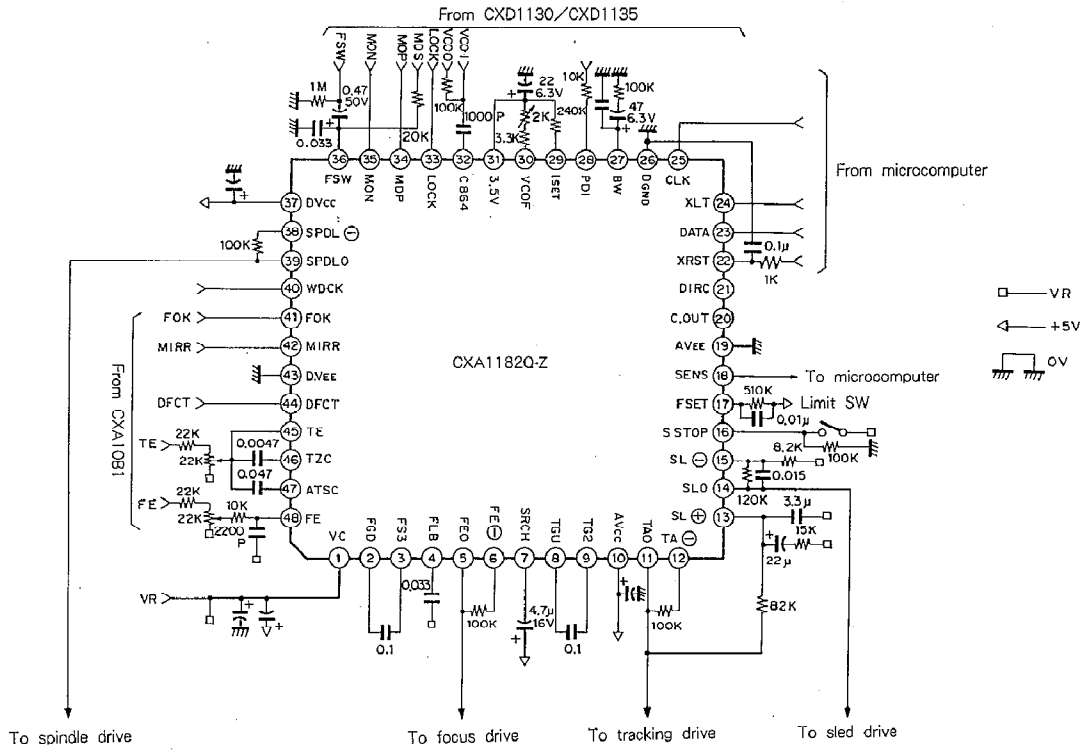
Application Circuit

- 1.  $\pm 5$  V dual power supply for CXA1182Q (48 pin QFP)
- (See the Pin Configuration for CXA1182S)





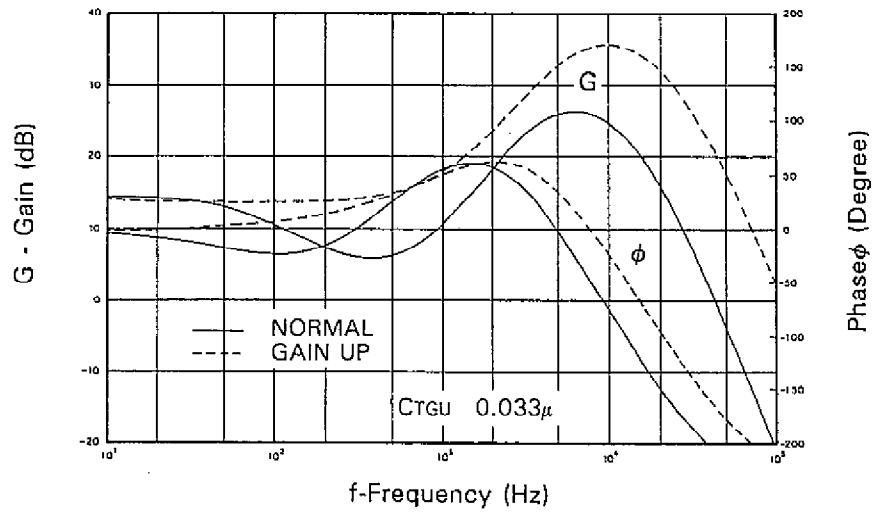
2. +5V single power supply for CXA1182Q (See the Pin Configuration CXA1182S)



Internal Phase Compensation Standard Circuit Design Data

Mode	Item	Symbol	SW conditions										SD	Bias conditions				Input point	Test point	Output waveform and description of test methods	Min.	Typ.	Max.	Unit						
			S1	S2	S3	S4	S5	S6	S7	S8	S9																			
Focus	1.2 kHz gain		O	O									08					48	5								21.5		dB	
	1.2 kHz phase		O	O									08															63		deg
	1.2 kHz gain		O	O									0C															16		dB
	1.2 kHz phase		O	O									0C															63		deg
Tracking	1.2 kHz gain					O							25						45	11								13		dB
	1.2 kHz phase					O							25															-125		deg
	2.7 kHz gain					O							25															26.5		dB
	2.7 kHz phase					O							25															-130		deg
Spindle	100 Hz phase																		34	39								-30		deg
	2 kHz gain																											-3.5		dB

Tracking frequency characteristics



FOCUS frequency characteristics



Package Outline Unit : mm

CXA1182Q-Z 48pin QFP (Plastic) 0.7g

