

8mm VCR Color Signal Processing

Description

The CXA1208R/Q is a consumer IC developed for 8mm VCR color signal processing. Usage in combination with CXA1207A allows for the processing of Y/C main signals.

Features

- Single 5V power supply
- Formation of chroma feedback comb filter possible through combination with CXA1207A
- No adjustment VCO
- NTSC/PAL correspondence
- Low power consumption (145mW at REC, 150mW at PB)

Functions

ACC, chroma emphasis/deemphasis, burst emphasis/deemphasis, XO/VXO, APC, AFC, APCID, AFCID, BID, ACK, APC compensation, HHK, PI/PS, frequency conversion system, chroma mute, 4.2V regulator

Structure

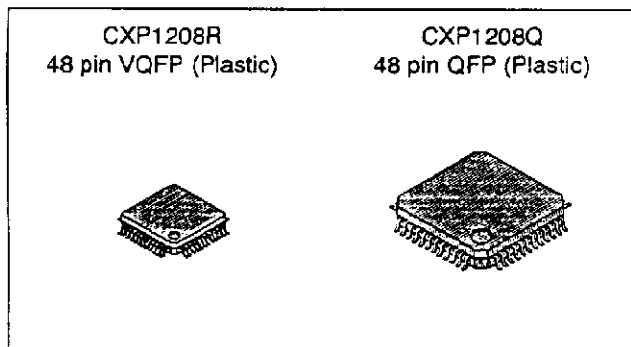
Bipolar silicon monolithic IC

Operating Condition

Supply voltage	Vcc	4.75 to 5.25	V
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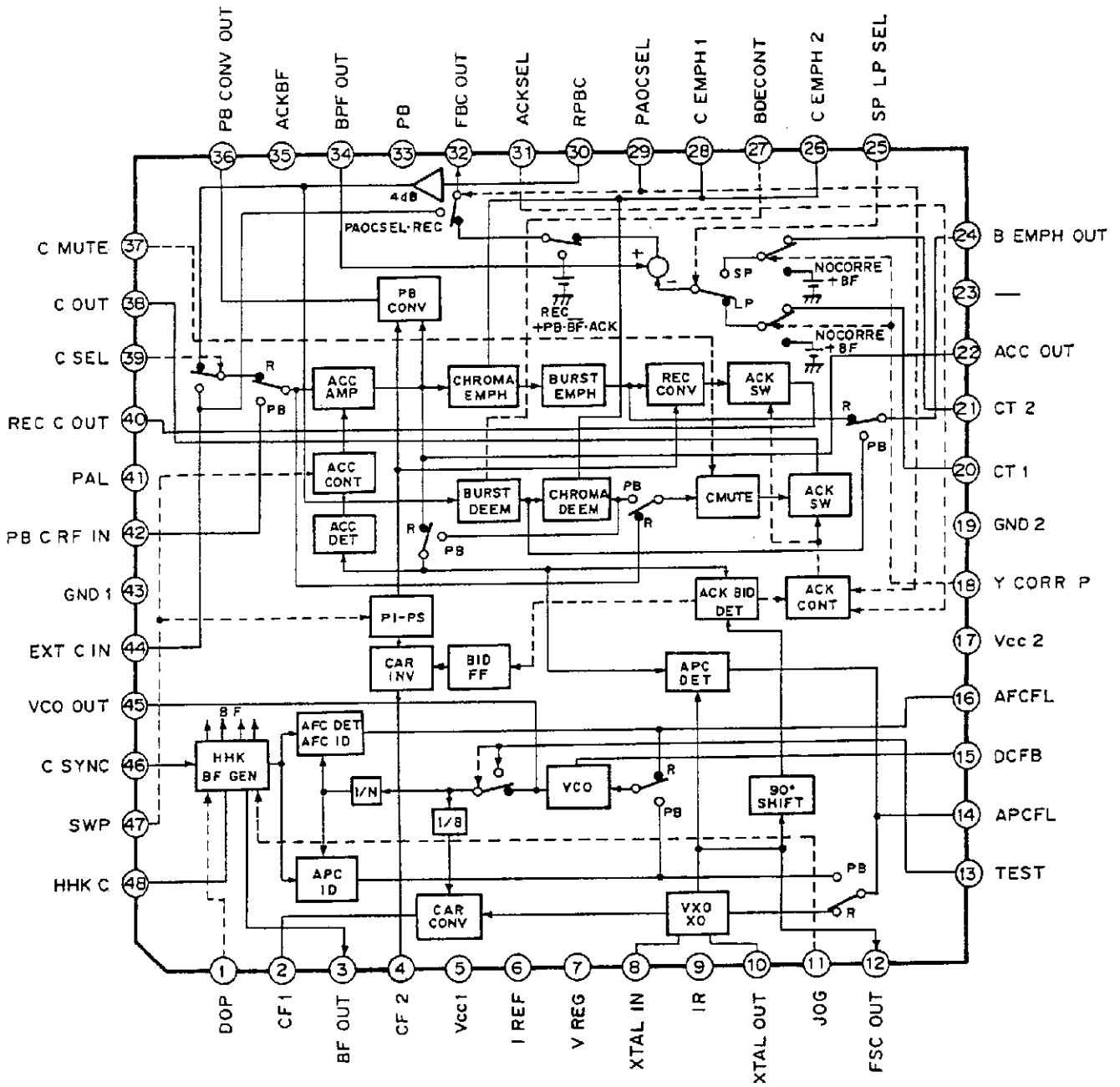
Absolute Maximum Ratings (Ta=25 °C)

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|-------------------------------|----------------|-----------------|--------------------------------|
| • Supply voltage | Vcc | 7 | V |
| • Operating temperature | Topr | -10 to +75 | °C |
| • Storage temperature | Tstg | -55 to +150 | °C |
| • Allowable power dissipation | P _D | (CXA1208R) 1100 | mW (When mounted on the board) |
| | | (CXA1208Q) 920 | mW (When mounted on the board) |



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Block Diagram and Pin Configuration



Pin Description

(Vcc=5.0V, Ta=25°C)

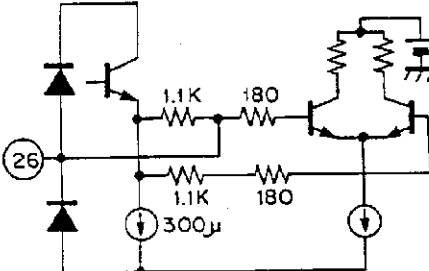
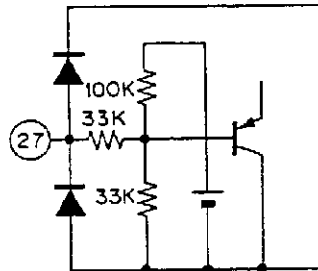
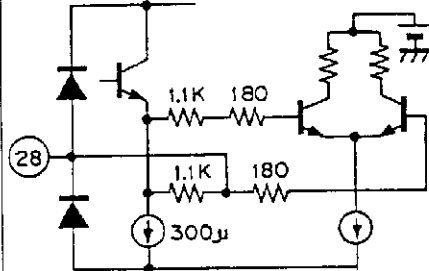
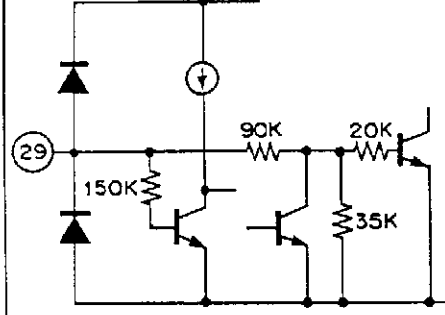
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	DOP	0V		<p>Drop out detection pulse is input. V_{TH} is at 2.1V. ($V_{MIN}=2.5V$) When a drop out detection pulse of Pin 11 (JOG) is input below 3.0V, the APC and ACC systems burst gate is turned off and the error is held.</p>
2	CF1	2.5V		<p>Carrier converter signal output pin. The spurious factor of (fsc+fcl) and (fsc-fcl) is contained.</p>
3	BF OUT	2.0/0V (When resistance applied)		<p>When a resistance (3.3kΩ) is applied to GND, the burst flag is output. There is no output in the vertical sync period.</p>
4	CF2	0V		<p>Pin 2 output filtrated through BPF (4.32MHz for NTSC and 5.17MHz for PAL). The standard input level is at 150mVp-p.</p>
5	Vcc1	5.0V		Power supply pin of sync block.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
6	IREF	2.1V		<p>A 100kΩ resistance is inserted to GND. This is the external reference current pin that produces the reference current.</p> $I_{REF} = \frac{V_6}{100K} \approx 21 \mu A$ <p>Watch for pin interference.</p>
7	VREG	4.2V	—	4.2V regulator output pin
8	XTAL IN	2.1V		<p>X'tal OSC reference input pin. Also, X'tal connecting pin. Watch for pin interference, floating capacitance.</p> <p>(PB)</p> <p>260mVp-p (For NTSC at PB)</p>
9	IR	0.9V		Decoupling pin
10	XTAL OUT	3.4V		<p>X'tal OSC reference output pin. Connects a X'tal between this pin and Pin 8.</p> <p>340mVp-p (For NTSC at PB)</p>

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
11	JOG	0V		<p>Control pin during JOG PB. When JOG mode is turned on, it switches to high speed ACC and raises the APC loop gain. Whether to turn off APC and ACC blocks burst flag with this pin's DC value, can be selected at Pin 1 (DOP).</p> <p>JOG mode where Pin 1 DOP is not controlled. (V_{TH} 3.0V)</p> <p>JOG mode where Pin 1 DOP is controlled</p> <p>NOR mode where Pin 1 DOP is controlled</p>
12	FSC OUT	2.3V		<p>VXO/XO outputs pass through LPF before being output from this pin. At the same time, this fsc is used for the clock frequency of the CCD delay line.</p> <p>(NTSC) 3.58MHz 460mVp-p</p> <p>(PAL) 4.43MHz 420mVp-p</p>
13	TEST	0V		<p>Turns to test mode with an external DC of 3.5 to 5.0V. At 4.2V DC center, input to the frequency divider is possible instead of VCO output. Normally used at GND.</p> <p>5V</p> <p>4.2V</p> <p>3.5V</p> <p>NORMAL</p> <p>0V</p>
14	APC FL	2.4V		<p>Connecting pin of external filter for APC.</p>

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
15	DCFB	2.4V		Connecting pin of external filter for no adjustment VCO.
16	AFC FL	2.4V (During REC)		Connecting pin of external filter for AFC.
17	Vcc2	5.0V	—	Power supply pin of main signal processing block.
18	Y CORR P	—		Input pin of the Y signal H correlation pulse from CXA1207A. At $V_{TH}=2.1V$, sets the chroma feedback comb filter to feedback ON at High (2.5V Min.) and to feedback OFF at Low (1.0V Max.).
19	GND2	0V	—	GND pin of main signal processing block.
20	CT1	—		When SP LP SEL (Pin 25) is at Low (LP), this pin becomes the input pin of the crosstalk (C+C ₀) from CXA1207A.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
21	CT2	—		<p>When SP LP SEL (Pin 25) is at High (SP), this pin becomes the input pin of the crosstalk (C+Cb) from CXA1207A.</p>
22	ACC OUT	2.0V (When resistance is applied)		<p>When a resistance (3.3kΩ) is applied to GND, ACC AMP output can monitor.</p> <p>During REC </p> <p>During PB </p>
23	—	—	—	Use in open condition.
24	B EMPH OUT	2.0V (When resistance is applied)		<p>When a resistance (3.3kΩ) is applied to GND, the signal can be monitored after chroma emphasis and burst emphasis during REC, or after burst deemphasis during PB.</p> <p>During REC During PB </p> <p>(75% color bar) NTSC</p>
25	SP LP SEL	0V		<p>SP/LP select control pin. At High (3.5V Min.) selects CT2 (Pin 21) input signal (SP) and at Low (0.5V Max.) CT1 (Pin 20) input signal (LP) to form a chroma feedback comb filter.</p>

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
26	C EMPH 2	2.4V		<p>Connects a coil for chroma emphasis phase matching between this pin and C EMPH 1 (Pin 28).</p> <p>During REC During PB</p> <p>420mVp-p 470mVp-p</p> <p>(75% color bar) NTSC</p>
27	B DE CONT	1.0V		<p>Adjusts burst deemphasis volume during PB. Can adjust the saturation of PB chroma signals. Normally kept open for use.</p>
28	C EMPH 1	2.4V		<p>Connecting pin of chroma emphasis BPF.</p> <p>During REC During PB</p> <p>380mVp-p 400mVp-p</p> <p>(75% color bar) NTSC</p>
29	PAO C SEL	0V		<p>Input DC level</p> <p>5.0 This pin is set to the value indicated during NT/PAL CAM REC. Pin 44 input is output at Pin 32.</p> <p>3.5</p> <p>2.0 When Pin 31 turns to High (over 3.5V) ACK SW is turned ON.</p> <p>1.0</p> <p>0.3</p> <p>0V Normal usage.</p> <p>NT/PAL CAM REC</p> <p>PAO</p> <p>NOR</p>

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
30	R P B C	—		<p>Input pin of the chroma signal after passage through the chroma comb filter. During REC, with C SEL (Pin 39) at Low, the input signal of this pin is processed.</p> <p>During REC During PB</p> <p>(75% color bar) NTSC</p>
31	ACK SEL	0.4V		<p>This pin selects ACK SW mode.</p> <p>5.0 PAO-ACK 3.5 2.0 NTSC/PAL signals are processed without ACK SW being activated. 1.0 0.3 ACK SW turns to ON/OFF according to ACK DET output. 0V</p>
32	FBC OUT	3.0V 1.3V (During PAOCSEL REC)		<p>Output pin for chroma signals to process comb filter. During PB and the formation of chroma feedback comb filter, (main signal ⊖ crosstalk) signals are output. (However during ACK, only burst signals are output.)</p> <p>Also, during REC, PAO C SEL (Pin 29) is at High and EXT C IN (Pin 44) input signals are output.</p> <p>(During PB)</p> <p>250 mVp-p NTSC (75% color bar)</p>
33	PB	0V		<p>REC/PB modes select pin.</p> <p>At High (3.5V Min.) : PB mode At Low (1.0V Max.) : REC mode</p>

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
34	BPF OUT	3.0V		<p>Input pin for signals passed through the external BPF ($f_0=3.58\text{MHz}$) after frequency conversion during PB.</p> <p>130 mVp-p</p> <p>NTSC (75% color bar)</p>
35	ACK • BF	4.3/0V (When resistance is applied)		<p>During ACK, BF pulse is output. In CXA1207A it is used for the replacement of the pedestal level. Output amplitude level becomes 4.3/0V. (When 10kΩ applied)</p> <p>However during V sync period it is not output.</p>
36	PB CONV OUT	2.8V (During PB)		<p>Frequency converted chroma signals are output during PB. After that they are input to BPF ($f_0=3.58\text{MHz}$).</p> <p>990 mVp-p</p> <p>NTSC (75% color bar)</p>
37	C MUTE	1.0V		<p>Select pin to mute color signals.</p> <p>With $V_{TH}=2.1\text{V}$, At High (2.6V Min.) : Mute is ON At Low (1.6V Max.) : Mute is OFF.</p>


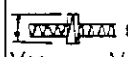
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
38	C OUT	2.1V		<p>Output pin for chroma signals during PB. Also, during REC, chroma input signals selected by C SEL (Pin 39), are output. During ACK, output DC turns to 0V.</p> <p>During REC During PB</p> <p>(75% color bar)</p>
39	C SEL	0V		<p>During REC, this pin selects the input pin for chroma signals. At High (3.5V Min.) EXTC IN (Pin 44) input At Low (1.0V Max.) RPBC (Pin 30) input are selected.</p>
40	REC C OUT	2.3V		<p>During REC, burst emphasis, chroma emphasis and frequency converted chroma signals are output. During ACK output DC turns to 0V.</p> <p>NTSC (75% color bar)</p>
41	PAL	0V		<p>Select pin for PAL signals processing.</p> <p>At High (3.5V Min.) turns to PAL mode. At Low (1.0V Max.) turns to NTSC mode.</p>



Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
42	PB C RF IN	2.8V (During PB)		<p>During PB, chroma RF signals are input. Typical input level is at 100mVp-p.</p> <p>(75% color bar)</p>
43	GND1	0V	—	GND pin for sync block.
44	EXT C IN	2.8V		<p>During REC, chroma signals are input. Typical level during 75% color bar input is at 314mVp-p. Input possible when C SEL (Pin 39) at High.</p>
45	VCO OUT	2.8/2.2V (When resistance is applied)		<p>Output pin of 378fH (NTSC) : 5.9MHz. To output it is necessary to apply a 10kΩ resistance to GND. Normally use as Vcc.</p>
46	C SYNC	—		<p>Composite sync input pin.</p>

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
47	SWP	2.0V		<p>RF SW pulse input pin. Used for ACC DET time constant and PI • PS selection.</p>
48	HHK C	3.5/1.0V		<p>Connecting pin of the charge/discharge capacitor for masking that turns C SYNC equivalent pulse to Half H Killer.</p>

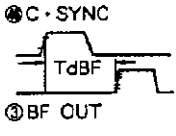
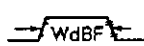
Electrical Characteristics

(Ta=25°C, Vcc=5V, See Electrical Characteristics Circuit)

No.	Test item	Symbol	Input conditions				SW set ON	Test point	Test method	Min.	Typ.	Max.	Unit ³⁷	
			Signal	Input pin	Level	Frequency								
1	Current circuit 1 (REC)	Icc REC						A	Current circuit during REC	21	29	37	mA	
2	Current circuit 2 (PB)	Icc PB					9	A	Current circuit during PB	22	30	38	mA	
3	Internal reference voltage source 1	VREG						4	Test DC voltage	4.05	4.2	4.35	V	
4	Internal reference voltage source 2	$\Delta VREG -$						4	At Vcc=4.75V: VREG1 $\Delta VREG - =$ VREG1 - VREG	-6	-1	0	mV	
5	Internal reference voltage source 3	$\Delta VREG +$						4	At Vcc=5.25V: VREG2 $\Delta VREG + =$ VREG2 - VREG	0	+1	+6	mV	
6	Reference current source	IREF						3	IREF= (No.3 Pin voltage) /100K	20.25	21	21.75	μ A	
7	ACC AMP(1)	Gain	GcENACC1	1	SG1	91 mVp-p	fsc	6	6	$\frac{V_6}{SG1}$	1.5	3.0	4.5	dB
		Secondary distortion	HD2ACC	1	SG1	91 mVp-p	fsc	6	6	$\frac{V_6(2fsc)}{V_6(fsc)}$			-35	dB
		Max. gain	GMAXACC	1	SG1	6 mVp-p	fsc	6	6	$\frac{V_6}{SG1}$	19	23		dB
		Min. gain	GMINACC	1	SG1	400 mVp-p	fsc	6	6	$\frac{V_6}{SG1}$		-10	-8	dB
8	ACC AMP gain (2)	GcENACC2	1	SG3	143 mVp-p	fsc	6, 10, 12	6	$\frac{V_6}{SG3}$	-2.8	-1.4	0	dB	
9	C OUT level (REC)	COUT REC	1	SG3	143 mVp-p	fsc	10, 12	8	$\frac{V_8}{SG3}$	-1.1	0.4	1.9	dB	
10	Gain difference between PB COUT and ACC CH	1ch output level	V01CH	1	SG2	100 mVp-p	fcl	8, 9, 11	8	Output chroma level V01CH 	180	260	350	mVp-p
		Gain difference	ΔGCH	5	SG2	100 mVp-p	fcl	8, 9, 11, 14	8	Test gain difference between respective channels	-0.5	0	0.5	dB
11	High speed ACC suppress ratio	FACC (JOG)	2	SG1	—	—	3, 6	6	See details 1 on Test method			-6	dB	
12	Burst emphasis characteristics	BE	1	SG1	91 mVp-p	fsc	7	7	V7 chroma burst signal ratio $\frac{V_{os}}{V_{oc}}$ 	4.8	5.8	6.8	dB	

No.	Test item	Symbol	Input conditions				SW set ON	Test point	Test method	Min.	Typ.	Max.	Unit			
			Signal	Input pin	Level	Frequency										
13	Chroma emphasis characteristics	Output level (1)	CE 0dB (fsc)	3	SG1	Vc= 200 mVp-p (0dB)	fsc	7	7	Chroma output level V70(fsc)	250	340	450	mVp-p		
		Emphasis characteristics (1)	CE 0dB (500K)				fsc+ 500kHz			$\frac{V70(fsc+500K)}{V70(fsc)}$	- 1.4	0.7	2.6	dB		
		Emphasis characteristics (2)	CE 0dB (- 500K)				fsc - 500kHz			$\frac{V70(fsc - 500K)}{V70(fsc)}$	- 1.4	0.7	2.6	dB		
		Output level (2)	CE - 10dB (fsc)			Vc= 83.2 mVp-p (- 10dB)	fsc			Chroma output level V71(fsc)	80	108	150	mVp-p		
		Emphasis characteristics (3)	CE - 10dB (500K)				fsc+ 500kHz			$\frac{V71(fsc+500K)}{V71(fsc)}$	1.4	3.2	5.4	dB		
		Emphasis characteristics (4)	CE - 10dB (- 500K)				fsc - 500kHz			$\frac{V71(fsc - 500K)}{V71(fsc)}$	1.4	3.2	5.4	dB		
14	REC C RF output level	VfCL	1	SG1	91 mVp-p	fsc		10	Chroma output level 	80	110	140	mVp-p			
15	REC C RF DC	ACK OFF	DC ACK OFF	1	SG1	12 mVp-p	fsc		9	Test output DC level	1.9	2.2	2.5	V		
		ACK ON	DC ACK ON	1	SG1	1 mVp-p	fsc		9	Test output DC level			100	mV		
16	Burst deemphasis	BDE	1	SG1	200 mVp-p	fsc		7, 9	7	V7 chroma burst signal ratio $\frac{V_{0B}}{V_{cc}}$ 	- 5.4	- 4.4	- 3.4	dB		
17	Carrier converter output level	Vcar	1	SG1	91 mVp-p	fsc			2	Test output level	110	150	190	mVp-p		
18	XO characteristics (NTSC)	Frequency deviation	Δf_{x0}						9	5	$\Delta f_{x0}=f_{sc} - f_{x0}$	- 50		50	Hz	
		Output level	Vx0							9	5	Test output level	380	480	580	mVp-p
		Secondary distortion	HD2x0								9	5	$\frac{Vs(2f_{sc})}{Vs(f_{sc})}$			- 25
19	XO characteristics (PAL)	Frequency deviation	Δf_{x0P}						1, 9	5	$\Delta f_{x0}=f_{scP} - f_{x0P}$	- 50		50	Hz	
		Output level	Vx0P							1, 9	5	Test output level	320	420	520	mVp-p
		Secondary distortion	HD2x0P								1, 9	5	$\frac{Vs(2f_{scP})}{Vs(f_{scP})}$			- 25

No.	Test item	Symbol	Input conditions				SW set ON	Test point	Test method	Min.	Typ.	Max.	Unit		
			Signal	Input pin	Level	Frequency									
20	REC APC pull in range (NTSC)	Upper side frequency	Δf_{vxo+}	1	SG1	91 mVp-p	fsc + Δ Hz		5	SG1 (fsc+1kHz) Upper side frequency that can be pulled in within 2 sec from input time	230			Hz	
		Lower side frequency	Δf_{vxo-}	1	SG1	91 mVp-p	fsc - Δ Hz		5	SG1 (fsc - 3kHz) Lower side frequency that can be pulled in within 2 sec from input time			- 230	Hz	
21	REC APC pull in range (PAL)	Upper side frequency	Δf_{vxo+}	4	SG1	91 mVp-p	fscP + Δ Hz	1	5	SG1 (fscP+1kHz) Upper side frequency that can be pulled in within 2 sec from input time	200			Hz	
		Lower side frequency	Δf_{vxo-}	4	SG1	91 mVp-p	fscP - Δ Hz	1	5	SG1 (fscP - 3kHz) Lower side frequency that can be pulled in within 2 sec from input time			- 200	Hz	
22	VCO sensitivity 1 (DCFB)	$f_{s\ vco1}$	DC	V1 V2	2.4V 1.6/3V	DC	4, 5, 9, 13	11	$\frac{f_{11}(3V) - f_{11}(1.6V)}{1.4}$	-1700	-1500	-1300	kHz/ V		
23	VCO sensitivity 2 (APCFL)	$f_{s\ vco2}$	DC	V1 V2	1.6/3V 2.4V	DC	4, 5, 9, 13	11	$\frac{f_{11}(3V) - f_{11}(1.6V)}{1.4}$	200	300	400	kHz/ V		
24	PB APC VCO frequency (NTSC)	Upper side pull in	$f_{vco}+3\%$	1	SG2	100 mVp-p	1.03fCL	8, 9, 11, 13	11	f_{11} : VCO oscillation frequency	6125979			Hz	
				7	SG4		1.03fH								
		Lower side pull in	$f_{vco} - 3\%$	1	SG2	100 mVp-p	0.97 fCL	8, 9, 11, 13	11		f_{11} : VCO oscillation frequency	5769126			Hz
				7	SG4		0.97fH								
25	PB APC VCO frequency (PAL)	Upper side pull in	$f_{vco}+3\%$	6	SG2	100 mVp-p	1.03fCLP	1, 8, 9, 11, 13	11	f_{11} : VCO oscillation frequency		6035156			Hz
				7	SG4		1.03 fHP								
		Lower side pull in	$f_{vco} - 3\%$	6	SG2	100 mVpp	0.97 fCLP	1, 8, 9, 11, 13	11		f_{11} : VCO oscillation frequency	5683594			Hz
				7	SG4		0.97 fHP								

No.	Test item		Symbol	Input conditions				SW set ON	Test point	Test method	Min.	Typ.	Max.	Unit	
				Signal	Input pin	Level	Frequency								
28	REC AFC VCO frequency (NTSC)	Upper side pull in	$f_{vco}+3\%$	7	SG4		1.03 fH	13	11	fH: VCO oscillation frequency		8125979		Hz	
		Lower side pull in	$f_{vco} - 3\%$	7	SG4		0.97 fH	13	11	fH: VCO oscillation frequency		5789128		Hz	
27	REC AFC VCO frequency (PAL)	Upper side pull in	$f_{vco}+3\%$	7	SG4		1.03 fHP	1, 13	11	fH: VCO oscillation frequency		6035156		Hz	
		Lower side pull in	$f_{vco} - 3\%$	7	SG4		0.97 fHP	1, 13	11	fH: VCO oscillation frequency		5683594		Hz	
28	PI characteristics	Phase 1	PI180	1	SG1	91 mVp-p	fsc	8, 9, 11	12	See details 2 on Test method		180		deg	
		Phase 2	PI0	1	SG1	91 mVp-p	fsc	8, 9, 11, 14	12	See details 2 on Test method		0		deg	
29	Burst flag	Phase	TdBF						2	1		3.4	4.0	4.8	μsec
		Width	WdBF							2	1		3.6	4.6	5.6

Note 1) Testing is performed with the input of 15.73426573kHz from SG4 to C SYNC (Pin 46) (when SW1 is OFF) for NTSC, and similarly the input of 15.625kHz (when SW1 is ON) for PAL. This excludes testing of T24, 25, 26 and 27.

Note 2) This IC specifications stipulate the following:

Chroma sub carrier waves for fsc (NTSC) at 3579545.455Hz

fscp (PAL) at 4433618.75Hz

Carrier waves converted to low band fcl (NTSC) at 743444.059Hz

fclp (PAL) at 732421.875Hz

The respective relation of $f_A=4.5\text{MHz}$ (NTSC) and $f_{AP}=5.5\text{MHz}$ (PAL) turns out as follows.

(NTSC)

$$f_A=4.5\text{MHz}$$

$$f_H = \frac{1}{286} f_A$$

$$f_{SC} = \frac{455}{2} f_H$$

$$f_{CL} = 47 \frac{1}{4} f_H$$

$$f_{VCO} = 378 f_H$$

(PAL)

$$f_{AP} = 5.5\text{MHz}$$

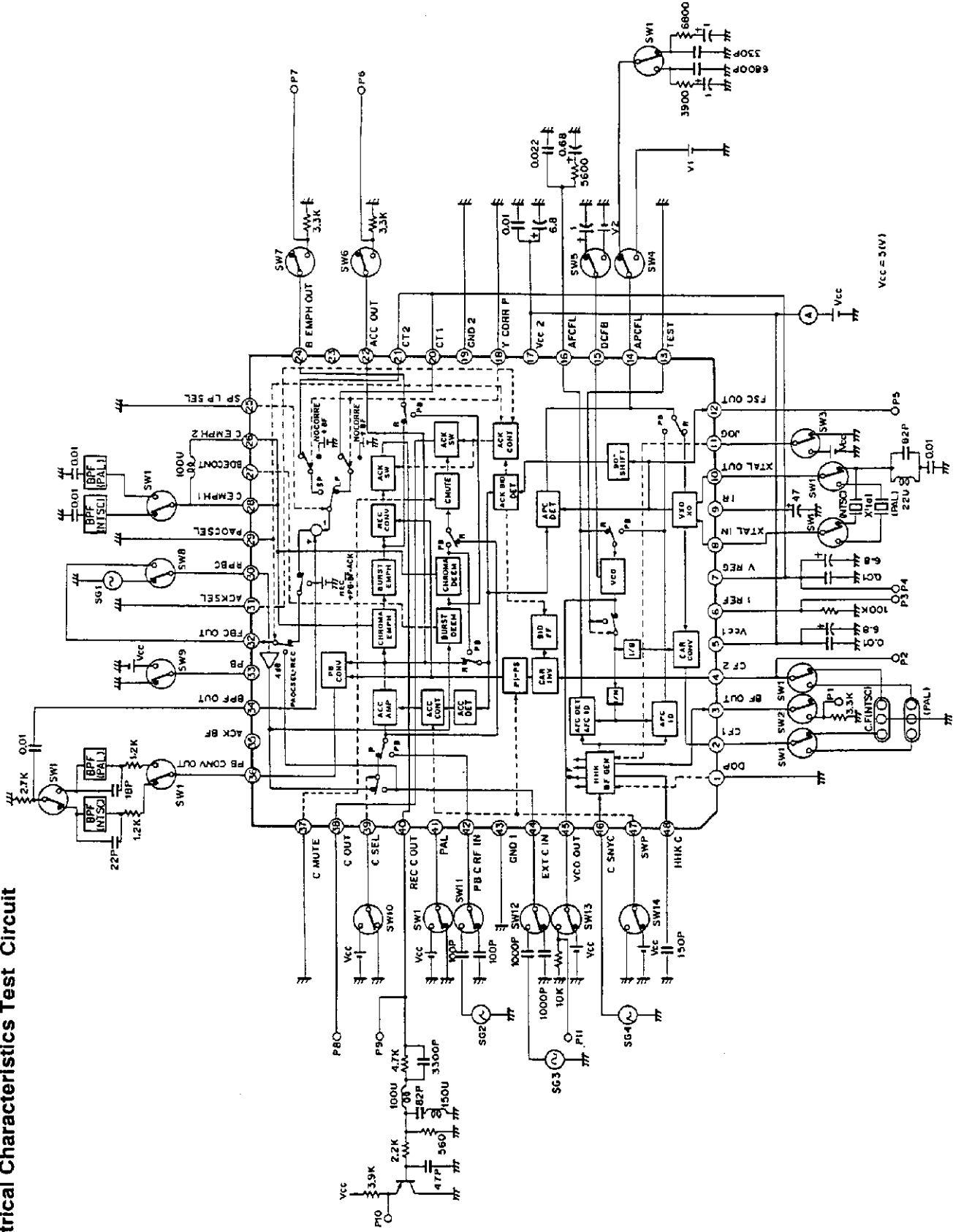
$$f_{HP} = \frac{1}{352} f_{AP}$$

$$f_{SCP} = (284 - \frac{1}{4} + \frac{1}{625}) f_{HP}$$


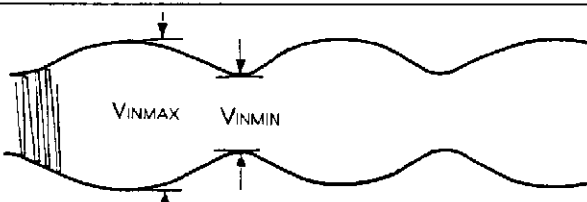
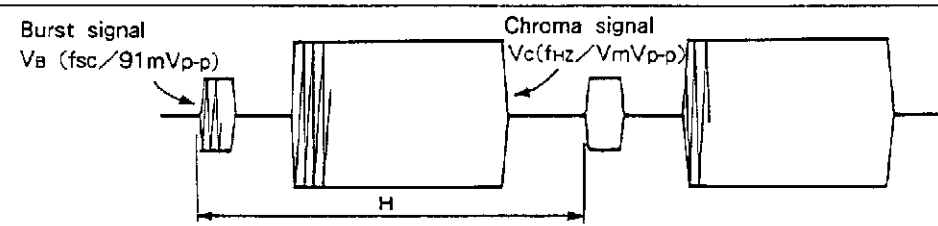
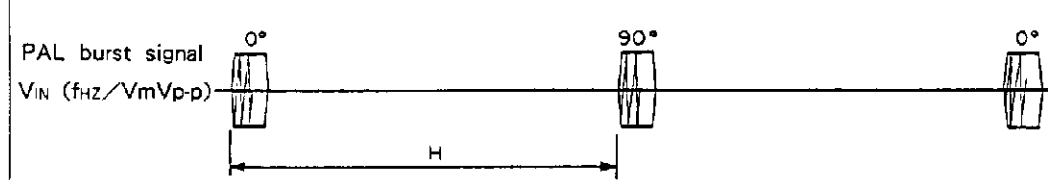
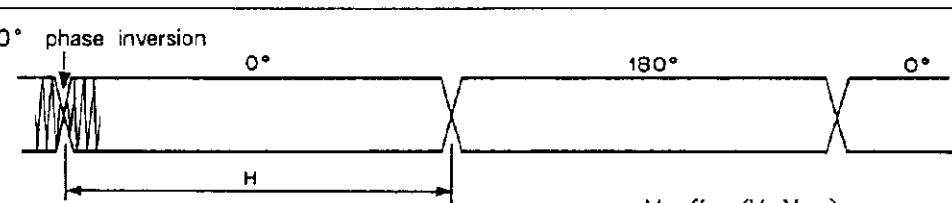
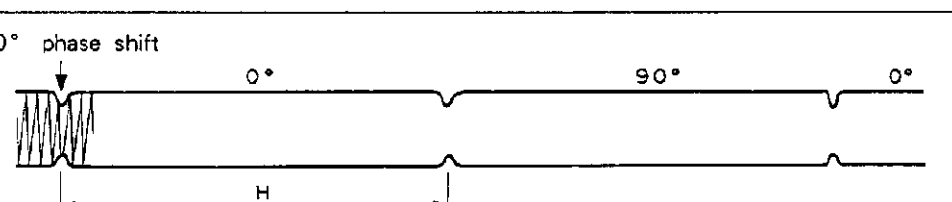
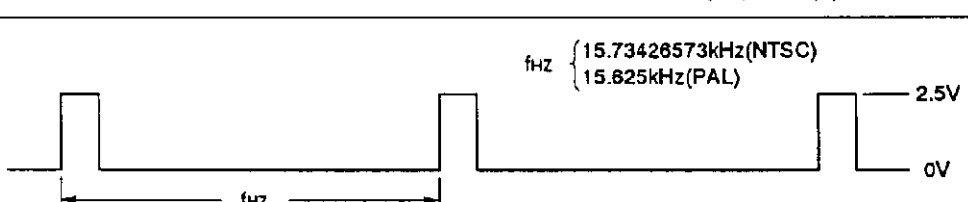
$$f_{CLP} = 46 \frac{7}{8} f_{HP}$$

$$f_{COP} = 375 f_{HP}$$

Electrical Characteristics Test Circuit

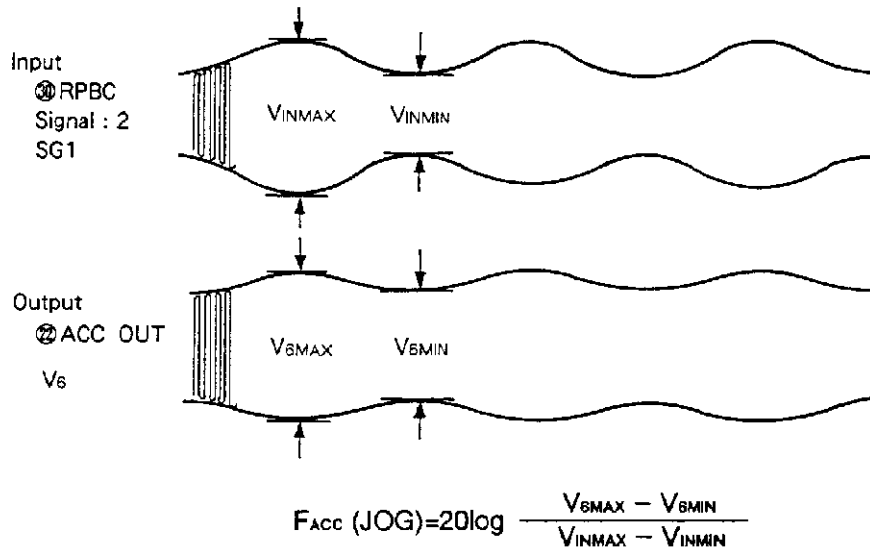


Input signal

Signal	Waveform	Signal source
1	 <p>$V_m V_{p-p}$</p> <p>f_{HZ}</p> <p>$V_{IN} (f_{HZ}/V_m V_{p-p})$</p>	SG1 SG2 SG3
2	 <p>V_{INMAX} V_{INMIN}</p> <p>$f_{sc}/91mV_{p-p}$ AM modulated to 60Hz, 35%.</p> <p>$\frac{V_{INMAX} - V_{INMIN}}{V_{INMAX} + V_{INMIN}} \times 100 = 35\%$</p>	SG1
3	 <p>Burst signal $V_a (f_{sc}/91mV_{p-p})$</p> <p>Chroma signal $V_c (f_{HZ}/V_m V_{p-p})$</p> <p>H</p>	SG1
4	 <p>PAL burst signal $V_{IN} (f_{HZ}/V_m V_{p-p})$</p> <p>$0^\circ$ 90° 0°</p> <p>H</p>	SG1
5	 <p>180° phase inversion</p> <p>0° 180° 0°</p> <p>H</p> <p>$V_{IN} (f_{HZ}/V_m V_{p-p})$</p>	SG2
6	 <p>90° phase shift</p> <p>0° 90° 0°</p> <p>H</p> <p>$V_{IN} (f_{HZ}/V_m V_{p-p})$</p>	SG2
7	 <p>f_{HZ} $2.5V$ $0V$</p> <p>$f_{HZ} \begin{cases} 15.73426573kHz(NTSC) \\ 15.625kHz(PAL) \end{cases}$</p> <p>* SG4 constant generation</p>	SG4

Test Method Details 1

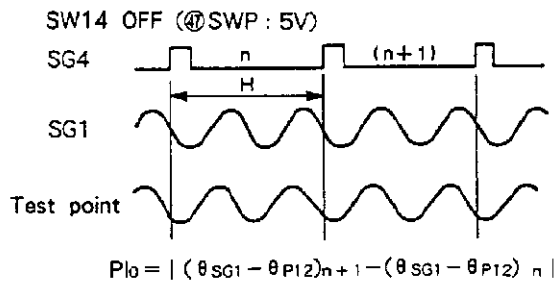
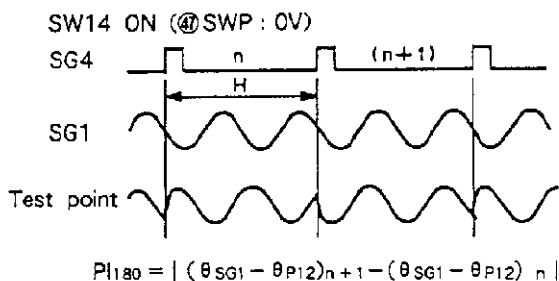
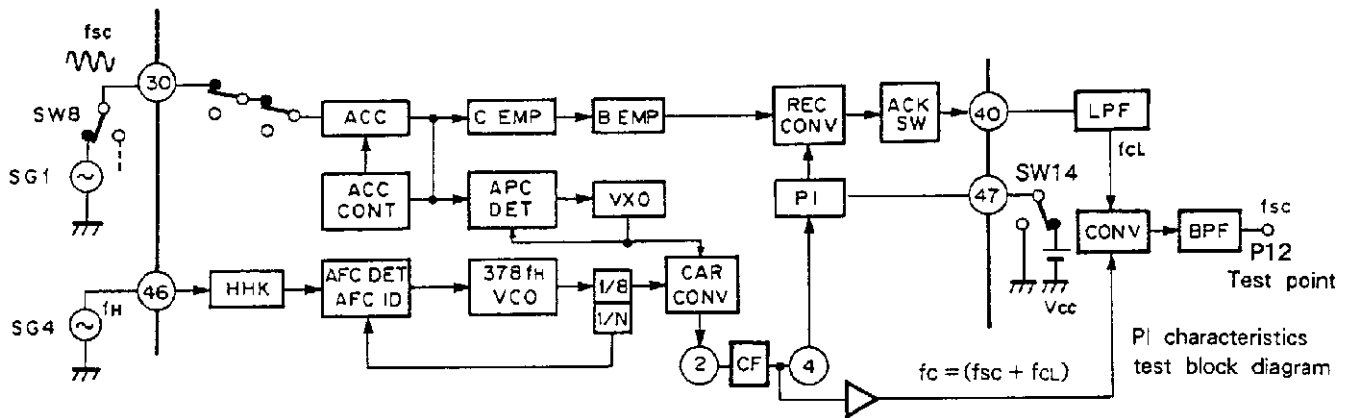
Turning JOG pin (Pin 11) to High=5V ($V_{TH}=1.4V$) produces high speed ACC mode.



Test Method Details 2

Because of the chroma crosstalk cancel in NTSC mode, PI method is performed. By turning the SWP input through Pin 47 from High to Low ($V_{TH}=2.1V$), the following is obtained.

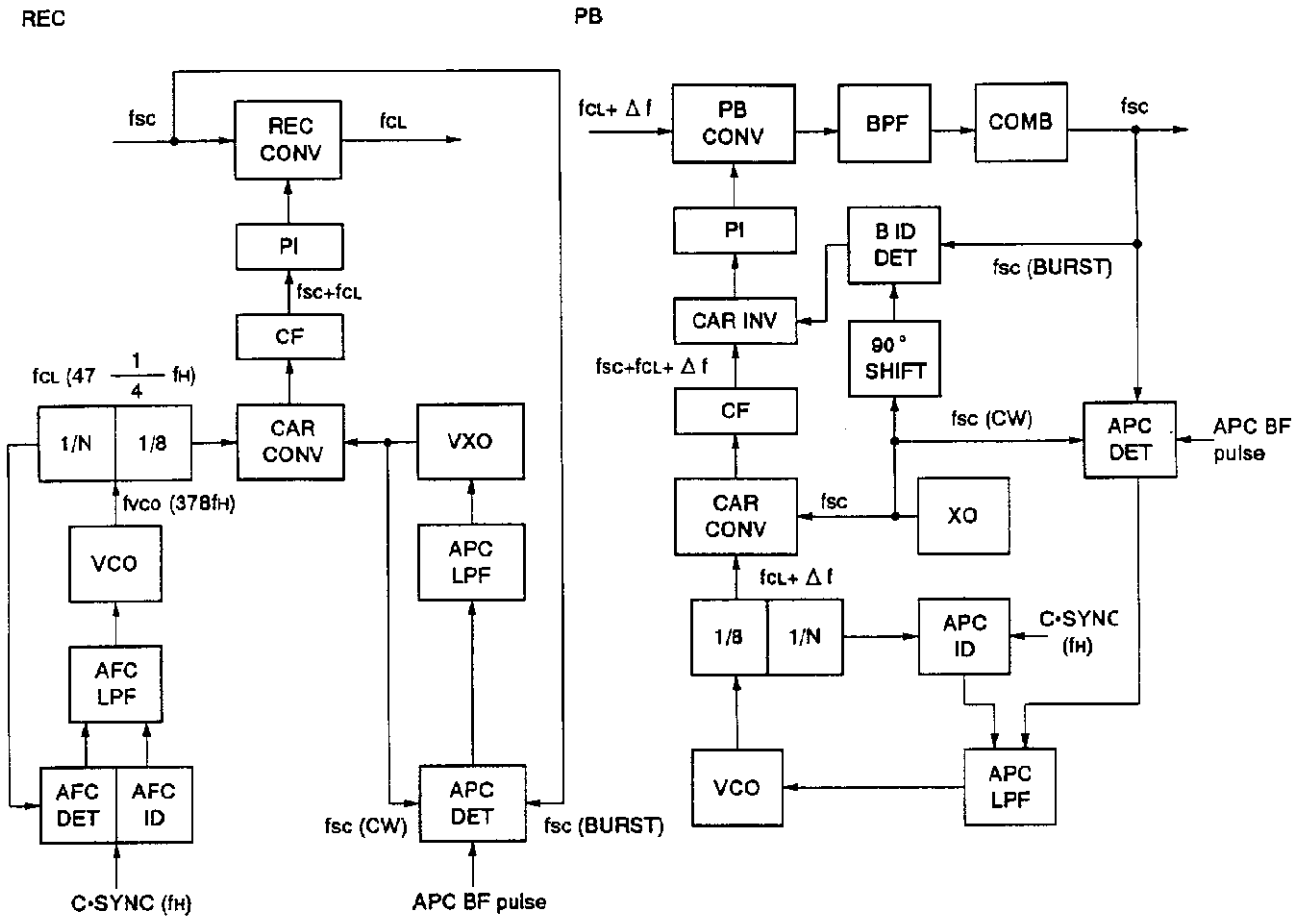
SWP { H (5V); PI OFF (Test Plo)
 L (0V); PI ON (Test PI180)



f_{sc} continuous wave is input through Pin 30. f_{cl} that was low band converted inside the IC at REC CONV and f_c ($f_c=274 \frac{3}{4} f_H$) output of Pin 4, are frequency converted outside the IC and f_{sc} is obtained. The phase relation of this waveform and the phase relation of the f_{sc} input are compared at the nH and $(n+1)H$ stage. Through testing it is confirmed that at SW14 ON there is a 180° phase difference, while at SW14 OFF there is a 0° phase difference.

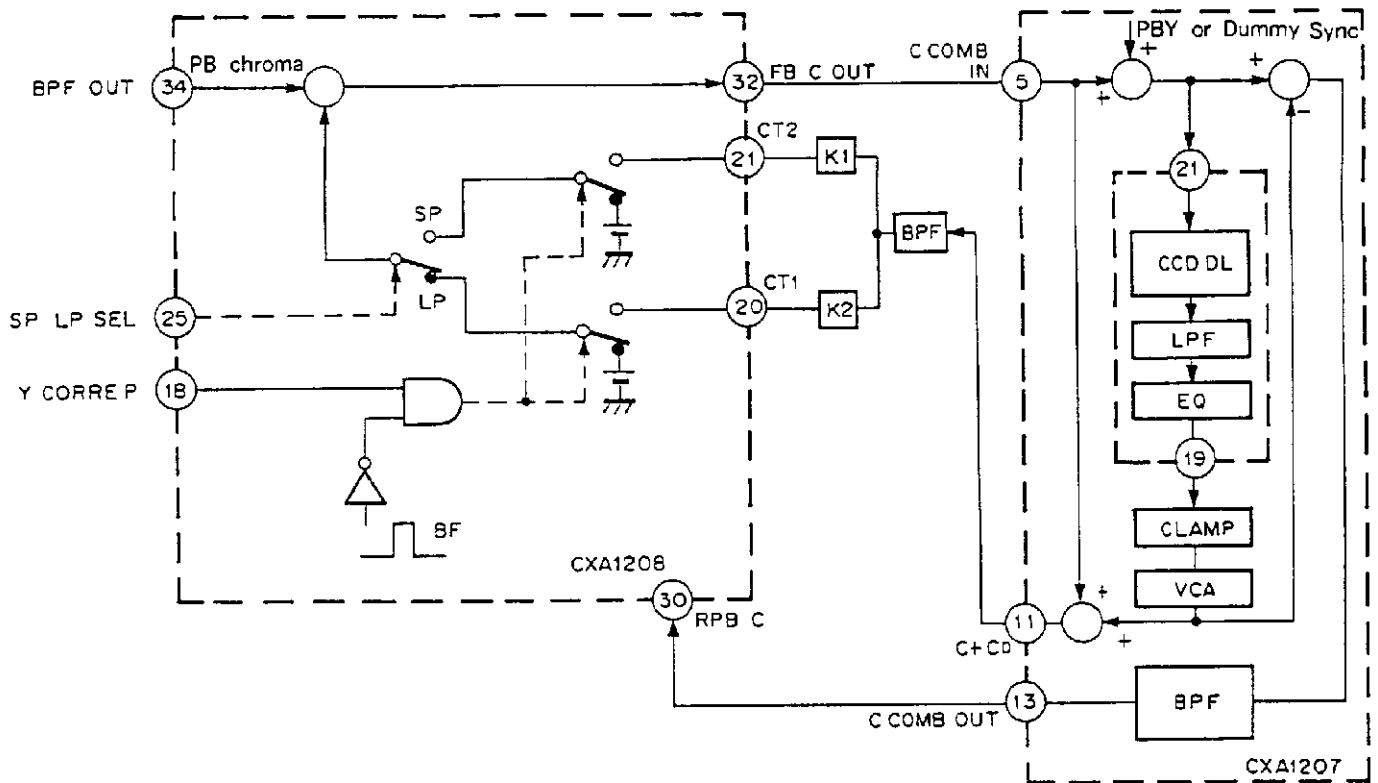
Description of Functions

1. Color sync block (NTSC)

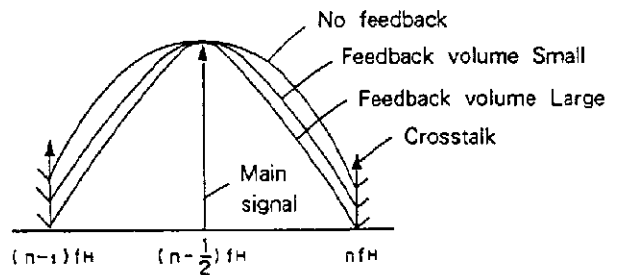


- REC AFC LOOP $f_{cl} (47 + \frac{1}{4}) f_H$ is composed from C SYNC (f_H).
- REC APC LOOP Composes a phase locked fsc continuous wave at the input chroma burst.
- REC AFC ID Pulls in VCO in the vicinity of the lock point with the rising edge or other.
- PB APC LOOP PB chroma burst is phase locked at the XO fsc.
- PB APC ID Prevents PB APC LOOP mislock.
- PB BURST ID During a phase relation where APC response speed is slow, inverts the carrier phase to hasten the pull in.

2. PB chroma feedback comb filter



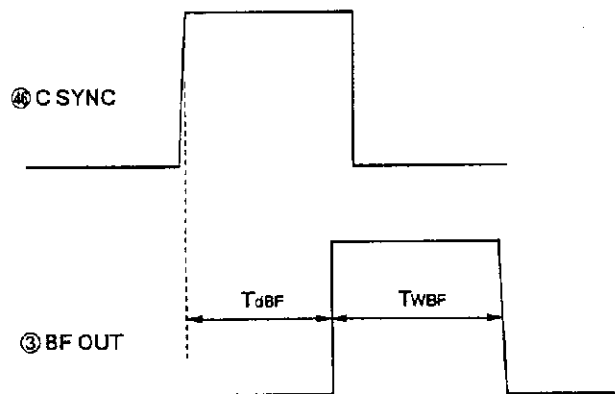
The chroma feedback comb filter is composed as shown in the Fig. above. By selecting the constant of the external ATT (K_1 , K_2) the tooth depth of the comb can be varied.



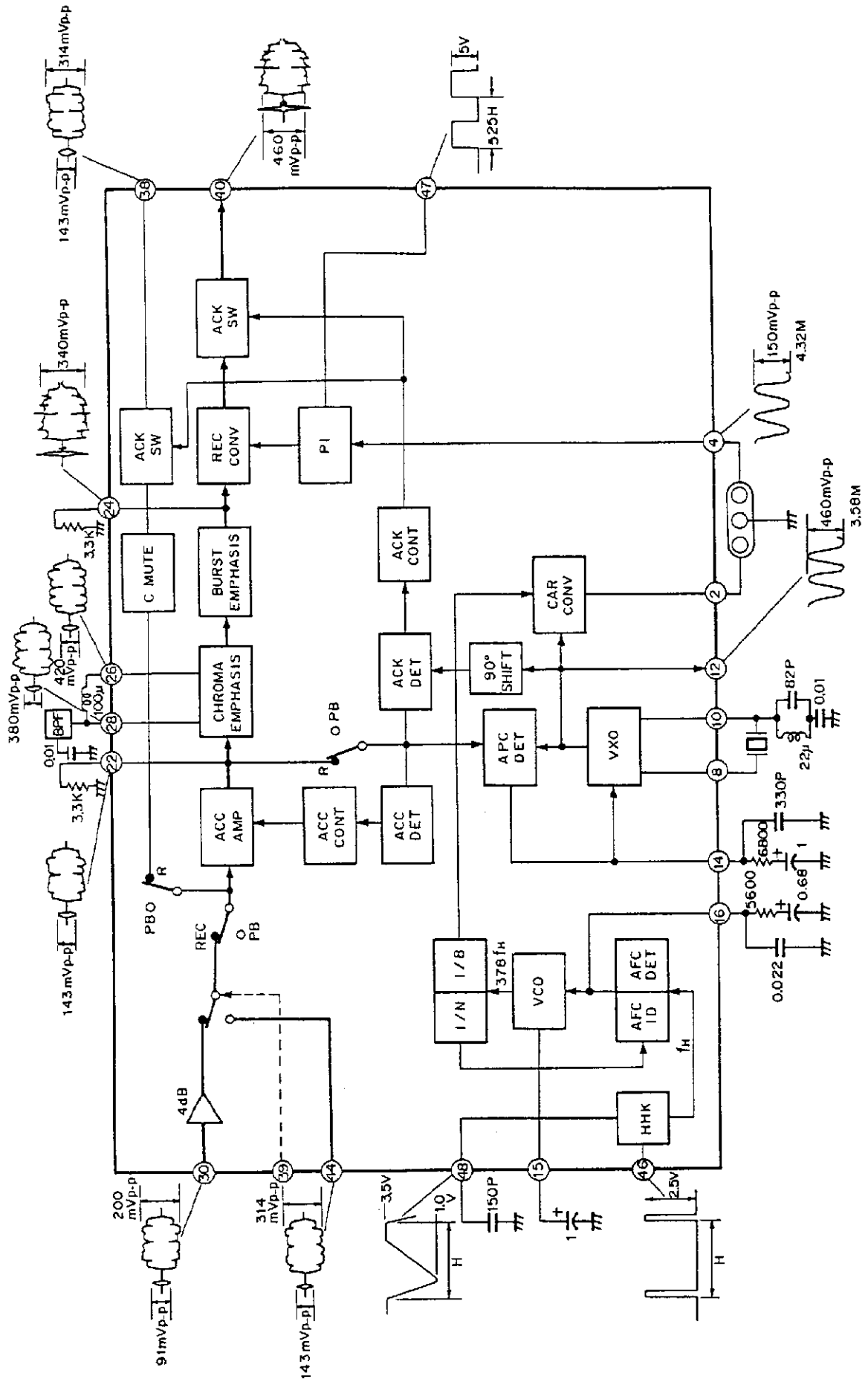
3. BF OUT pulse

Considering usage in conjunction with CXA1207A BF pulse timing changes respectively with the following modes.

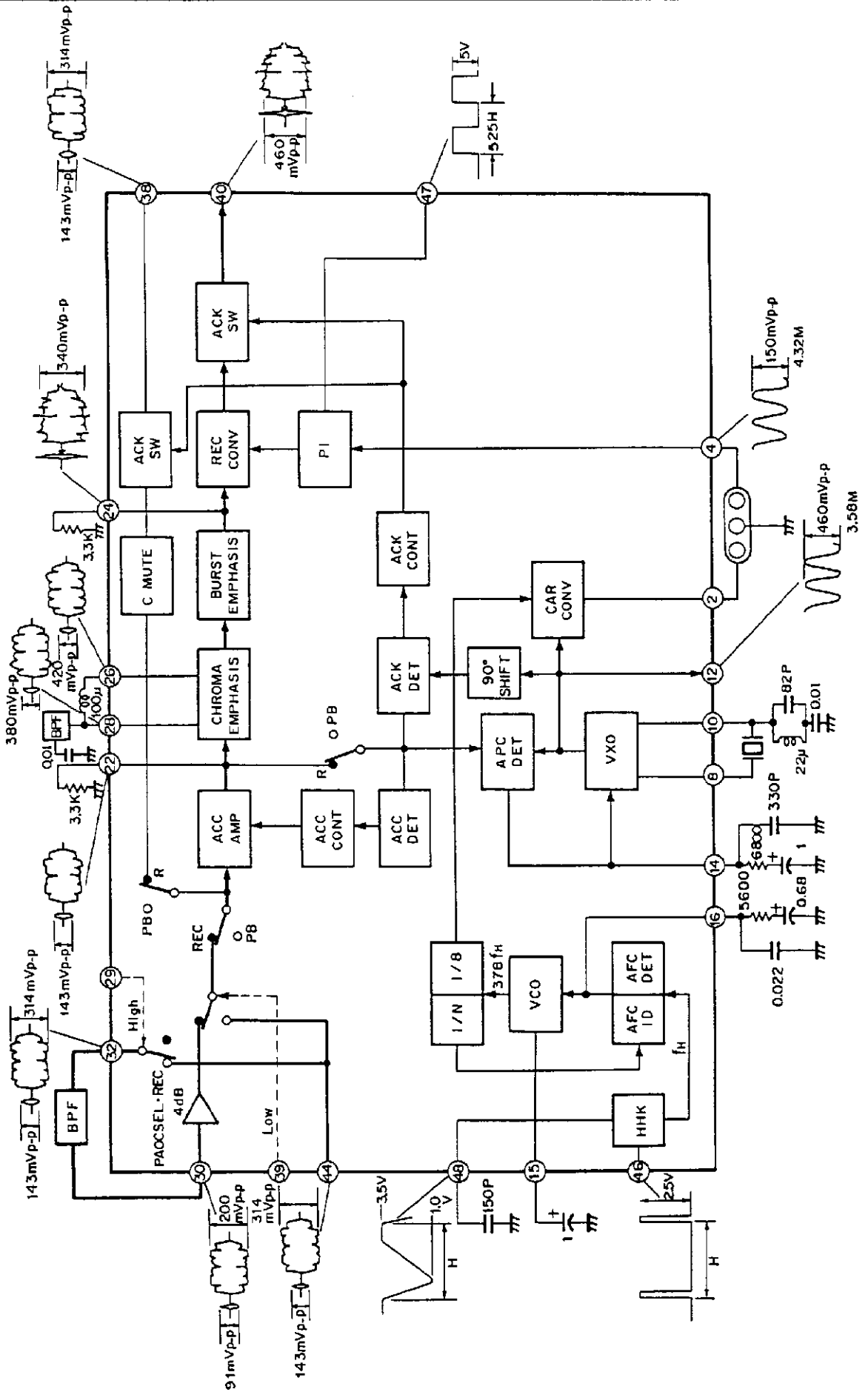
- NTSC•REC : $T_{dBf}(NT•REC)$
- PAL•REC : $T_{dBf}(NT•REC)$ +100nsec
- PB : $T_{dBf}(NT•REC)$ -250nsec
- Width : T_{wbf} is constant



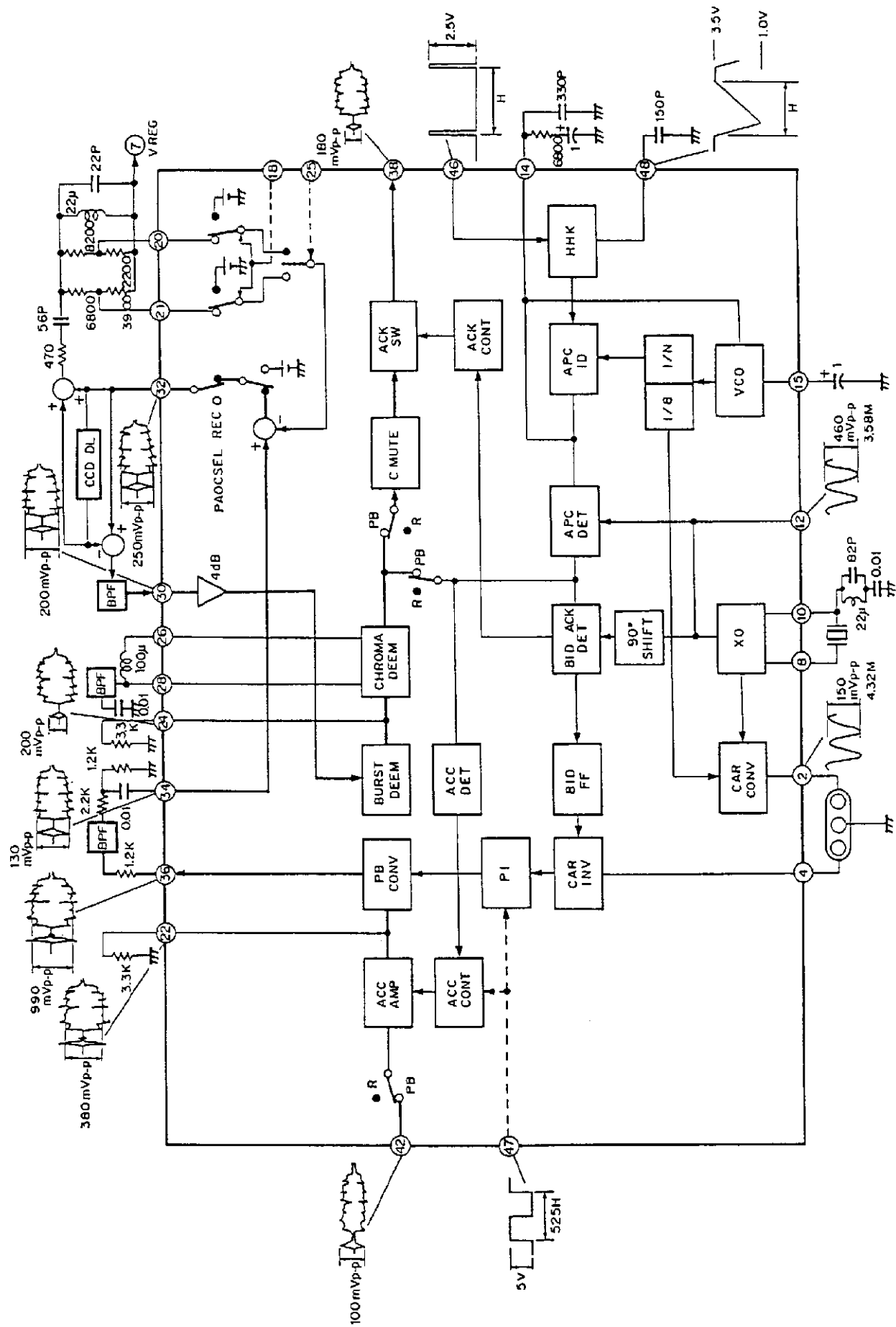
NORMAL REC Block Diagram (NTSC)



CAMERA REC Block Diagram (NTSC)



PB Block Diagram (NTSC)



Adjustment Sequence Modes

- **16**, **9** and **14** indicate the data value numbers of the CXA1207A BUS DECODER.
- Recording : The CXA1207A BUS DECODER **19** PB=Low, and the CXA1208 Pin 33 (PB) is Low.
- Playback : The CXA1207A BUS DECODER **19** PB=High, and the CXA1208 Pin 33 (PB) is High.

Adjustment Procedures for CXA1207A and CXA1208 (See Application Circuit)

1. REC Y level adjustment

Mode : Recording, **16** Video AGC=High
 Input signal : Color bar 500mVp-p (CXA1207A Pin 32 VIN 1)
 Adjustment method : With 75Ω connection to the CXA1207A Pin 38 VIDEO OUT, adjust RV102 (EE LEVEL) to get 1Vp-p.

2. Y/C separation adjustment

Mode : Recording
 Input signal : Color bar 500mVp-p (CXA1207A Pin 32 VIN 1)
 Adjustment method : Adjust in sequence RV113 (YC SEP), RV110 (COMB ADJ), RV113 (YC SEP), so that the CXA1207A Pin 11 C+C_D residual chroma component is minimum.

3. IR adjustment

Mode : Recording, with 2.5V to 3.5V applied to CXA1207A Pin 51 SWP.
 Input signal : Color bar 500mVp-p (CXA1207A Pin 32 VIN 1)
 Adjustment method : Adjust the IR adjustment variable resistor (RV109), so that the CXA1207A Pin 7 Y COMB OUT residual chroma component is minimum. The residual chroma component should be -20dB (Typ.) to the input chroma level.

4. Emphasis input Y level adjustment

Mode : Recording
 Input signal : Color bar 500mVp-p (CXA1207A Pin 32 VIN 1)
 Adjustment method : Adjust RV115 (EMPH Y LEVEL), so that the CXA1207A Pin 3 EMPH IN Y signal level is 500mVp-p.

5. YFM carrier adjustment

Mode : Recording, **9** E=Low (Normal mode), **9** E=High (Hi8 mode)
 Input signal : 100% white 500mVp-p (CXA1207A Pin 32 VIN 1)
 Adjustment method : Watching the signal on the CXA1207A Pin 43 Y RF OUT with a spectral analyzer, adjust RV119 (CAR) so that the H SYNC spectrum (carrier) is 4.2MHz in Normal mode and 5.7MHz in Hi8 mode.

6. YFM deviation adjustment

Mode : Recording, **9** E=Low (Normal mode), **9** E=High (Hi8 mode)
 Input signal : 100% white 500mVp-p (CXA1207A Pin 32 VIN 1)
 Adjustment method : Watching the signal on the CXA1207A Pin 43 Y RF OUT with a spectral analyzer, adjust RV120 (DEV) so that the 100% white Y level spectrum is 5.4MHz in Normal mode and 7.7MHz in Hi8 mode.

7. Playback Y level adjustment

Mode : Playback, 14 W CCD=Low (Using 1 CCD delay line), 14 W CCD=High (Using 2 CCD delay lines)
Input signal : PB Y RF 100mVp-p (CXA1207A Pin 41 PB RF IN)
Adjustment method : Adjust RV114 (PB Y LEVEL 1) to get 500mVp-p on the CXA1207A Pin 21 DL IN1 when using 1 CCD delay line and on the CXA1207A Pin 15 DL IN2 when using 2 CCD delay lines.

8. Playback Y level 2 adjustment

Mode : Playback
Input signal : PB Y RF 100mVp-p (CXA1207A Pin 41 PB RF IN)
Adjustment method : With 75 Ω connection to the CXA1207A Pin 38 VIDEO OUT, adjust RV121 (PB Y LEVEL 2) to get 1Vp-p.

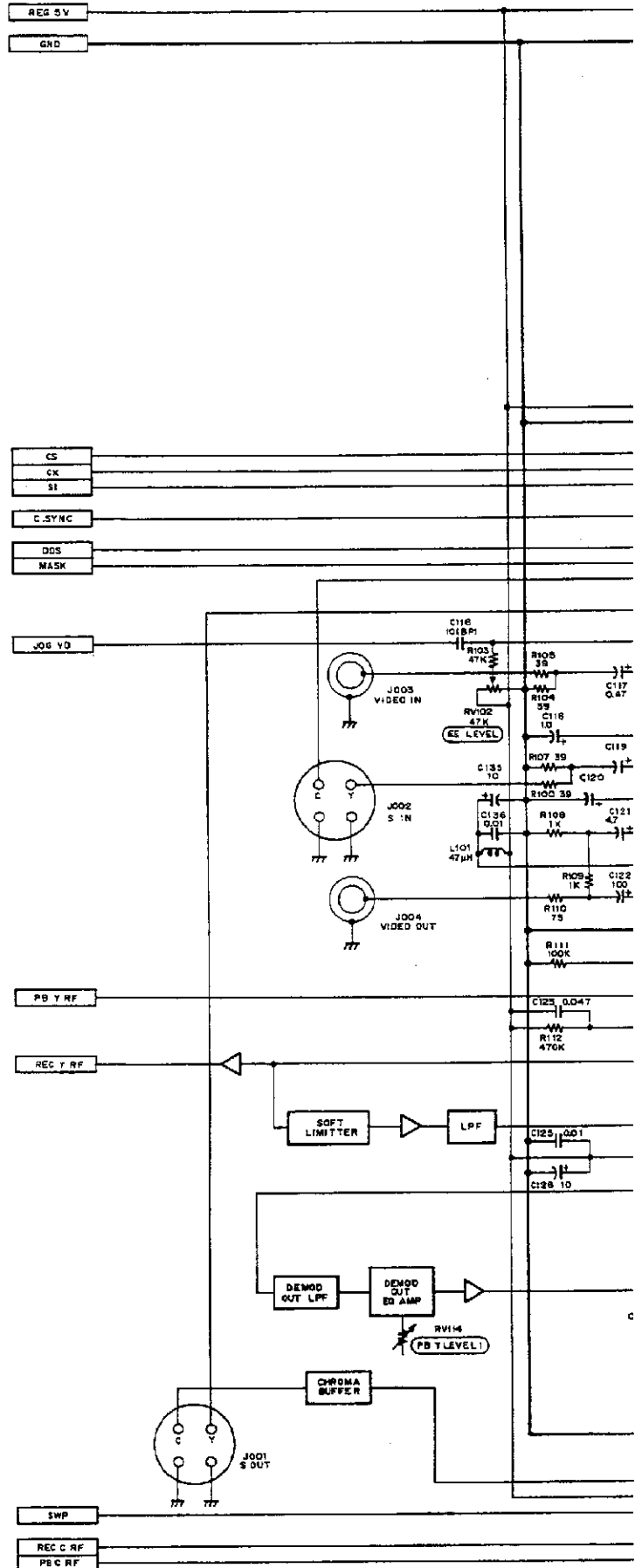
9. Chroma emphasis fo adjustment

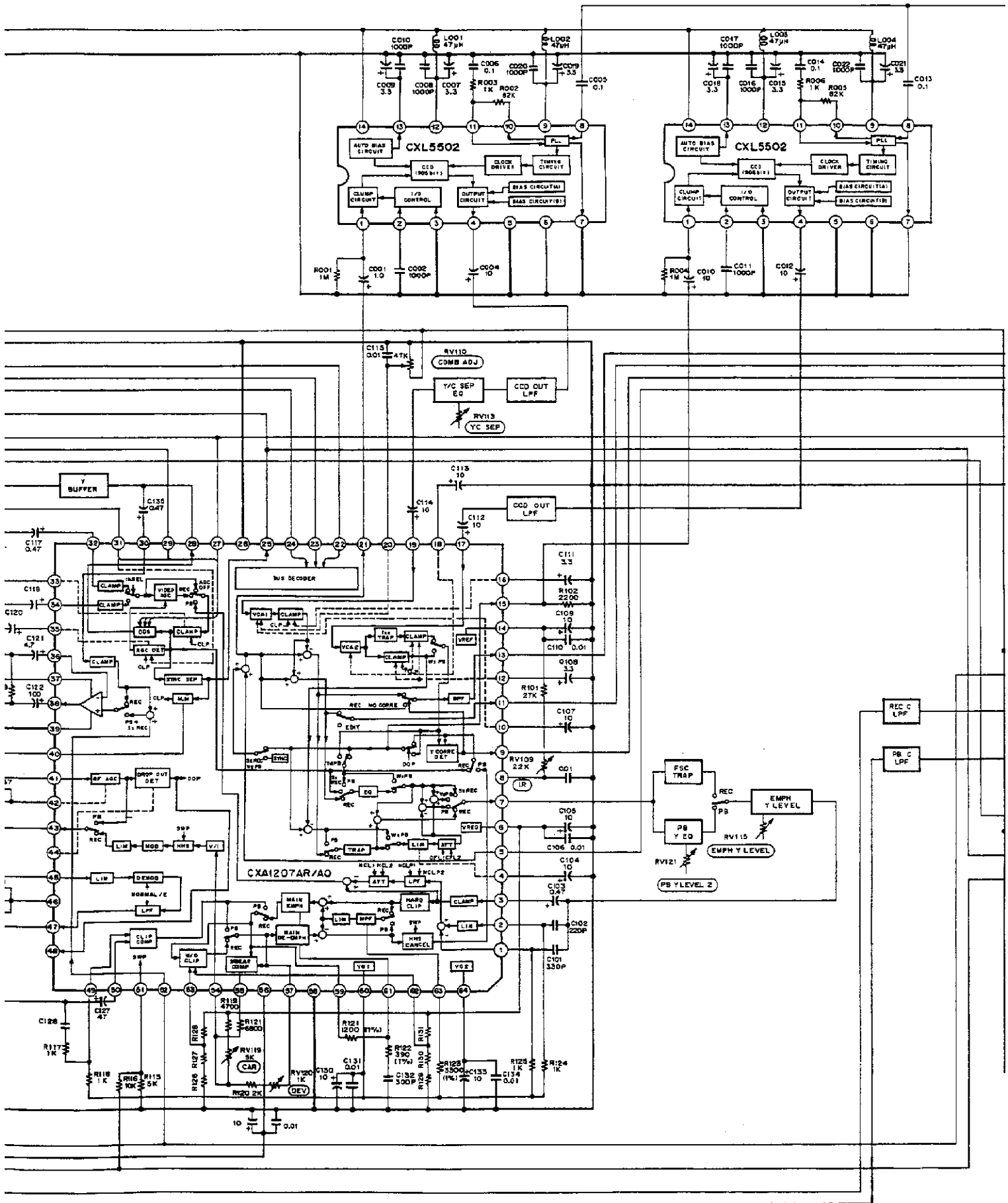
Mode : Recording
Input signal : Color bar 500mVp-p (CXA1207A Pin 32 VIN 1)
Adjustment method : Adjust the core of the C EMPH FL107 attached to the CXA1208 Pin 28 C EMPH 1, so that the level of the flat portion of the chroma signal on the CXA1208 Pin 24 B EMPH OUT is minimum. (The CXA1208 Pin 24 should have 3.3k Ω connected to ground.)

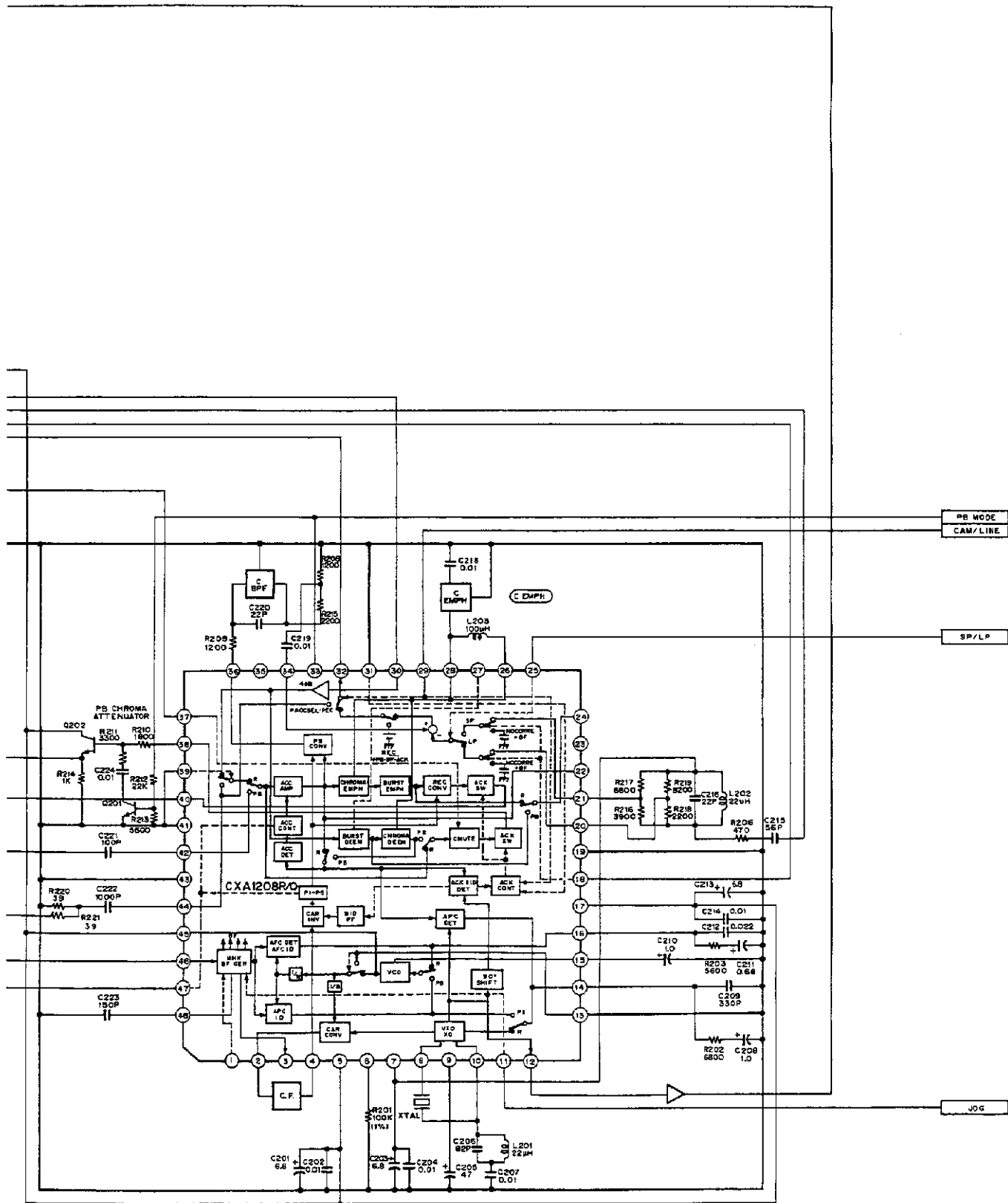
Precautions on Usage of CXA1208R/Q

- (1) When FSC OUT (Pin 12) signal is utilized as the CCD clock frequency, be careful with the routing. Avoid by all means crossing signal lines.
- (2) X'tal (crystal) fo varies according to the floating capacity, and others. Set as close to the IC as possible, and keep wiring short.
- (3) HHK C capacity 150P of Pin 48 determines BF timing. Accordingly set close to the IC to avoid the influence of the floating capacity, and others, and keep wiring short. Also, use a CH for temperature compensation of the type that does not sustain much effects from temperature differences.
- (4) I REF (Pin 6) resistance 100K, determines the external reference current. Employ a metallic film resistance and of allowable difference $\pm 1\%$.

Application Circuit (NTSC, Hi8 mode)

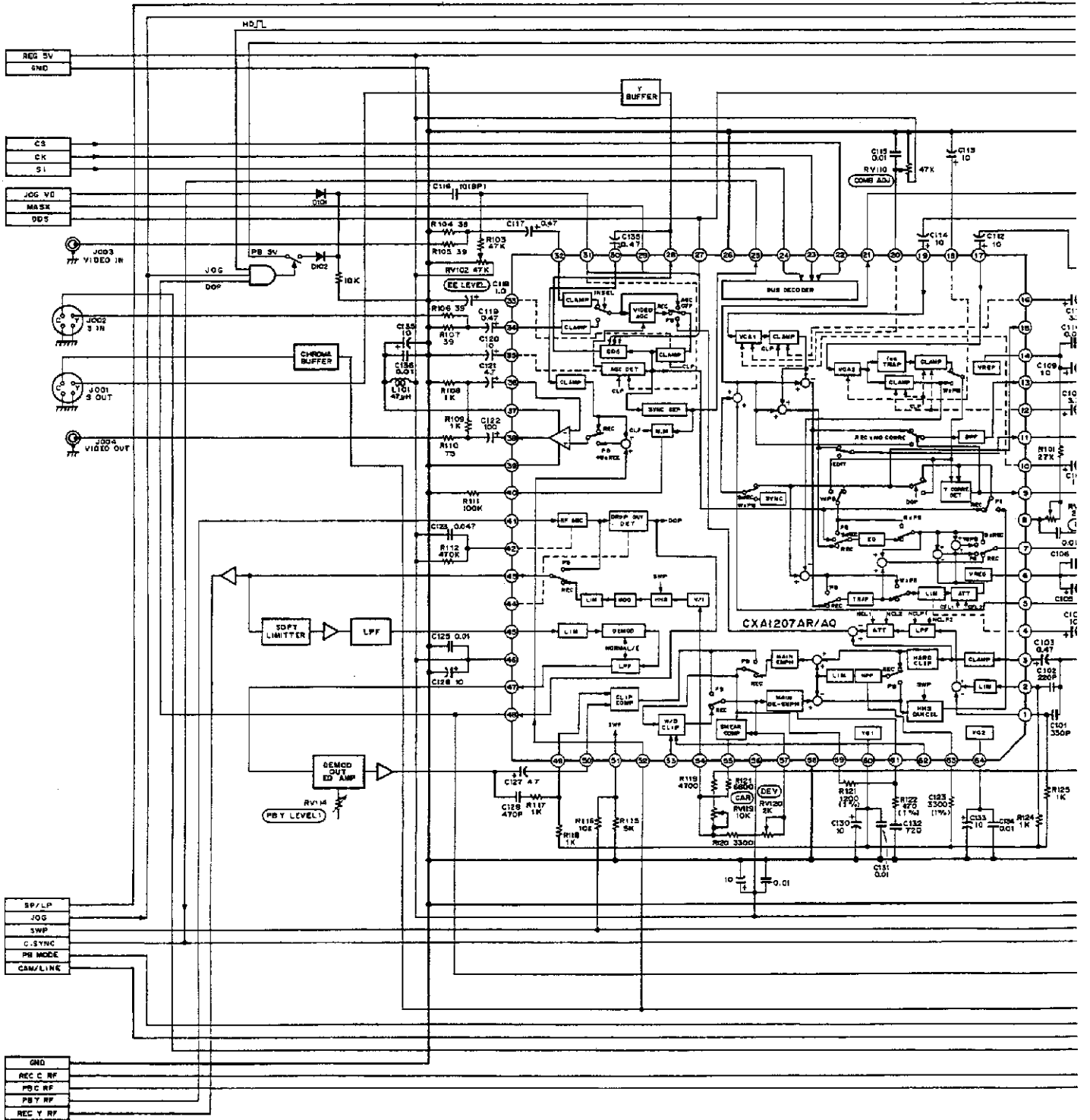


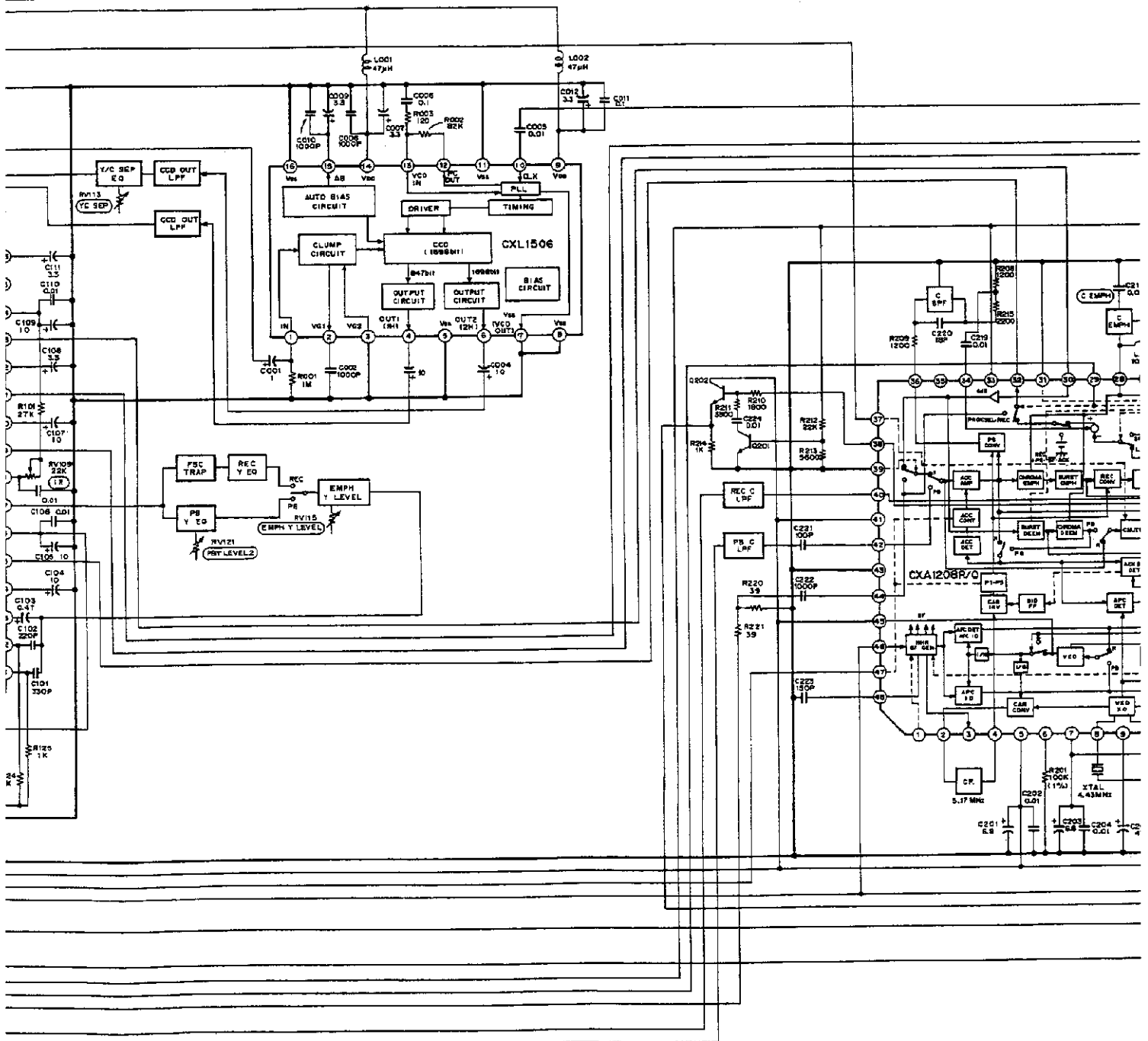


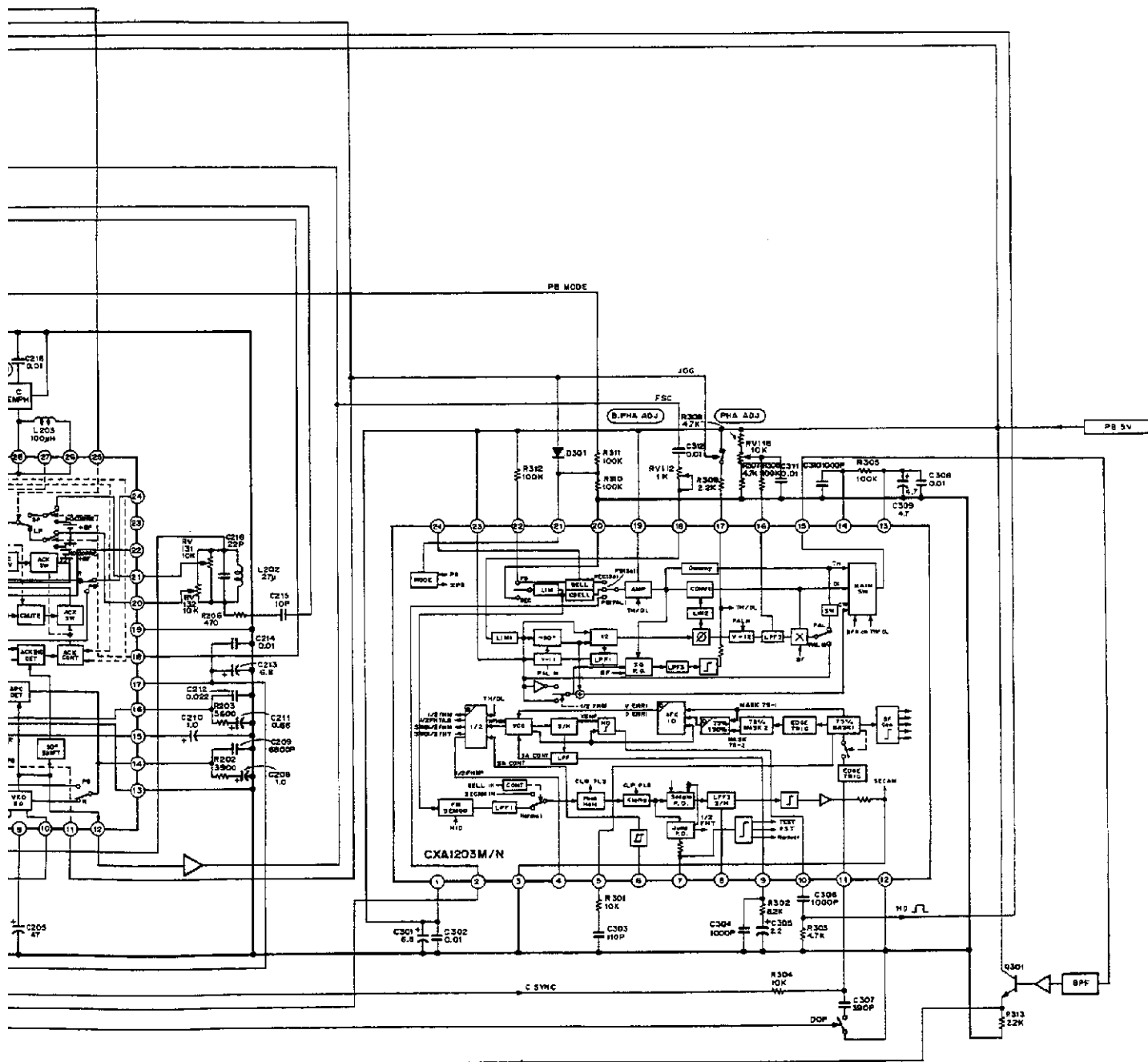


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit (PAL, Normal mode)

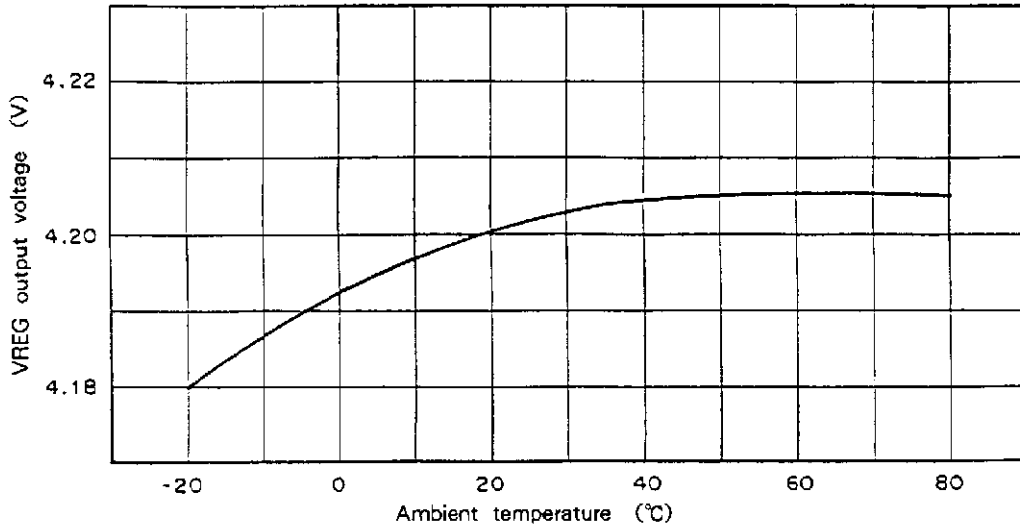




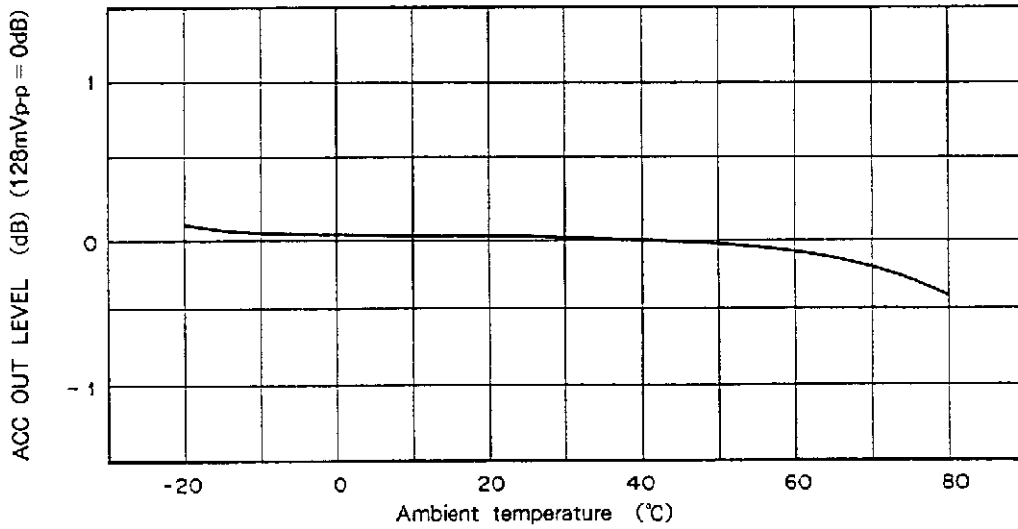


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

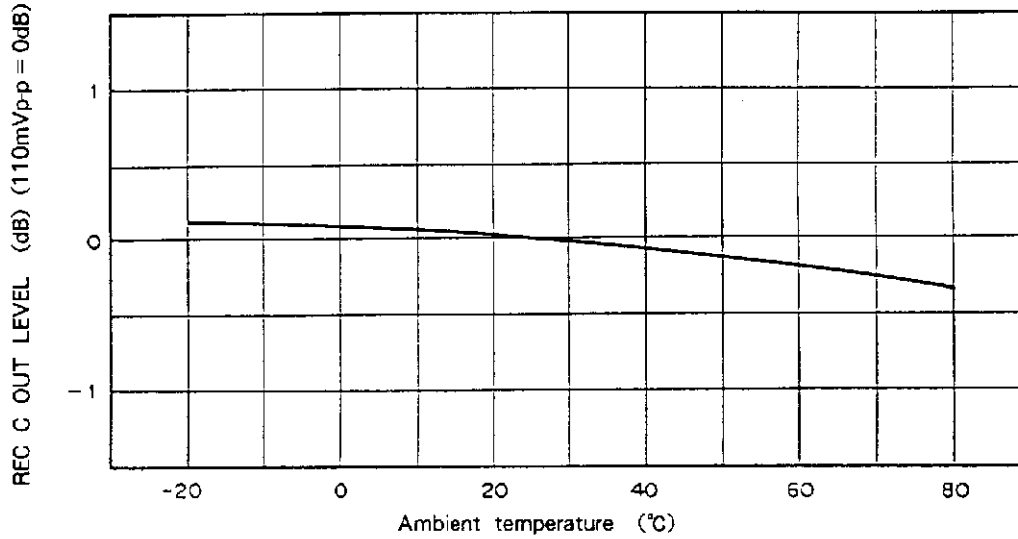
VREG temperature characteristics

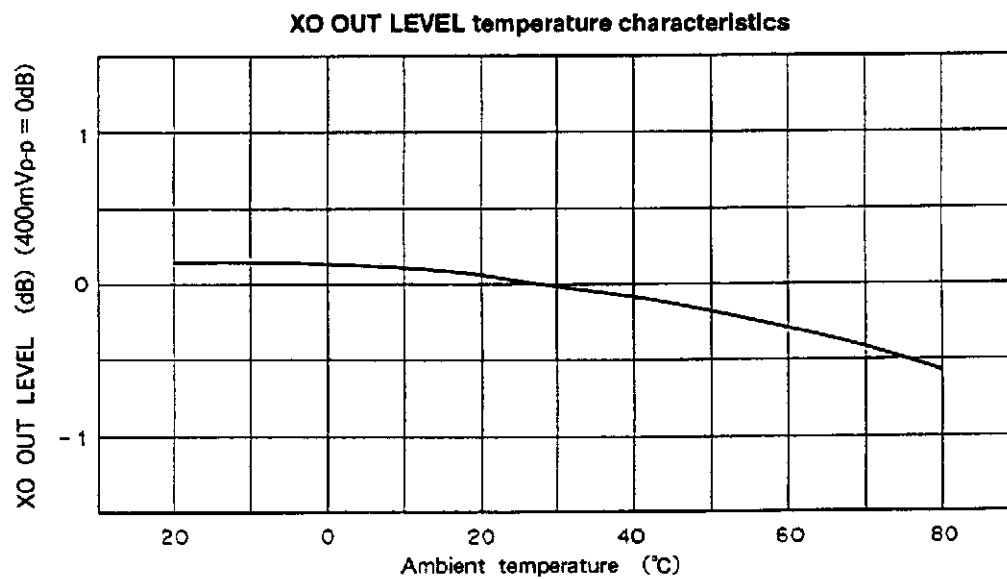
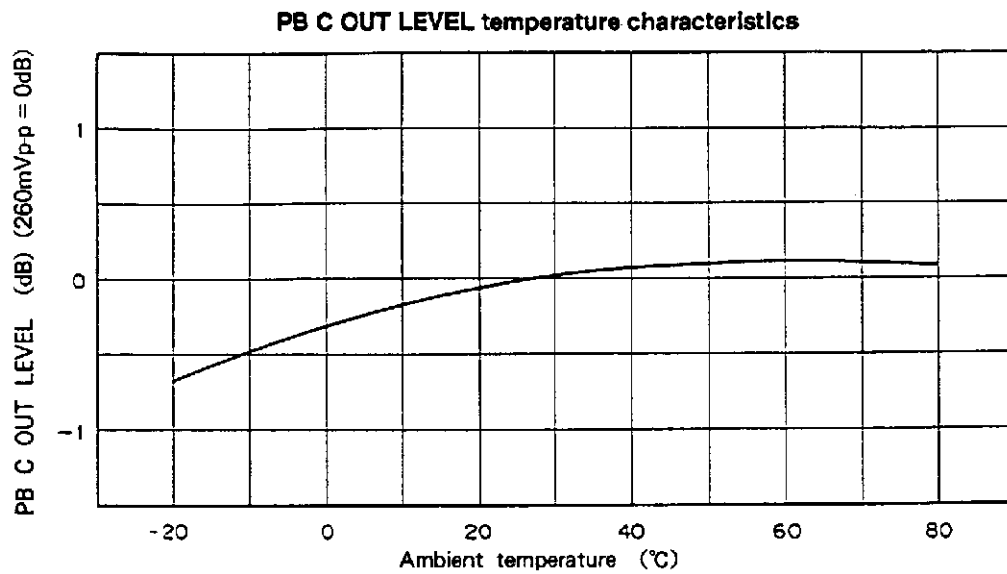
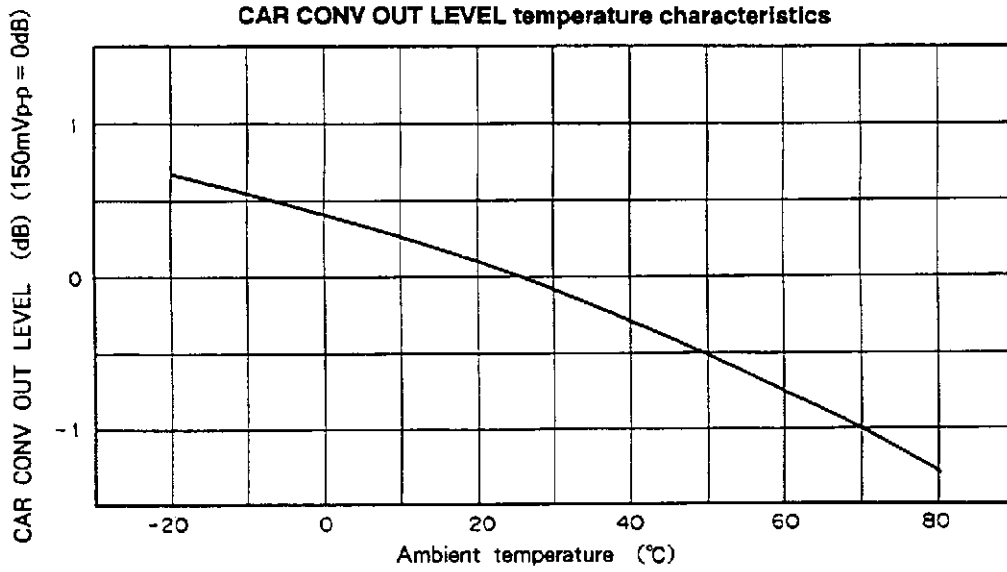


ACC OUT LEVEL temperature characteristics

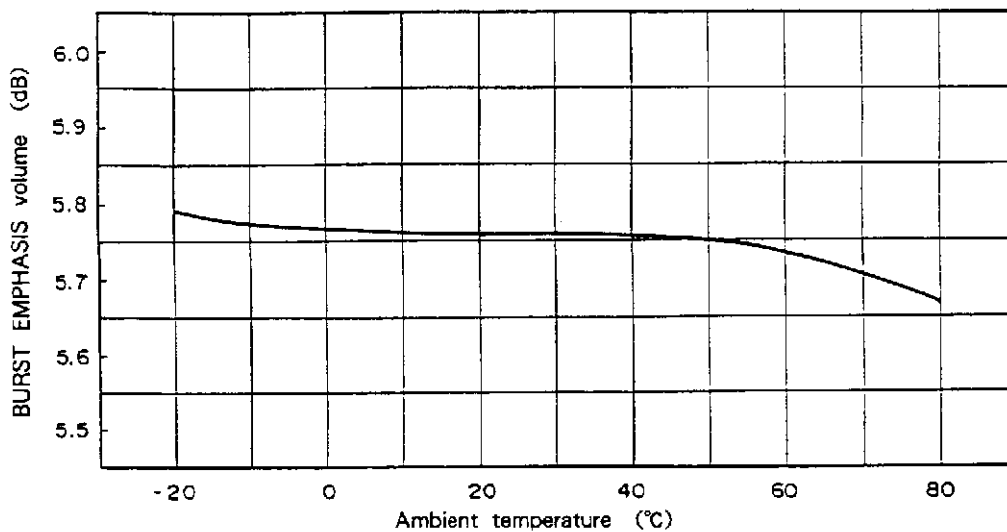


REC C OUT LEVEL temperature characteristics

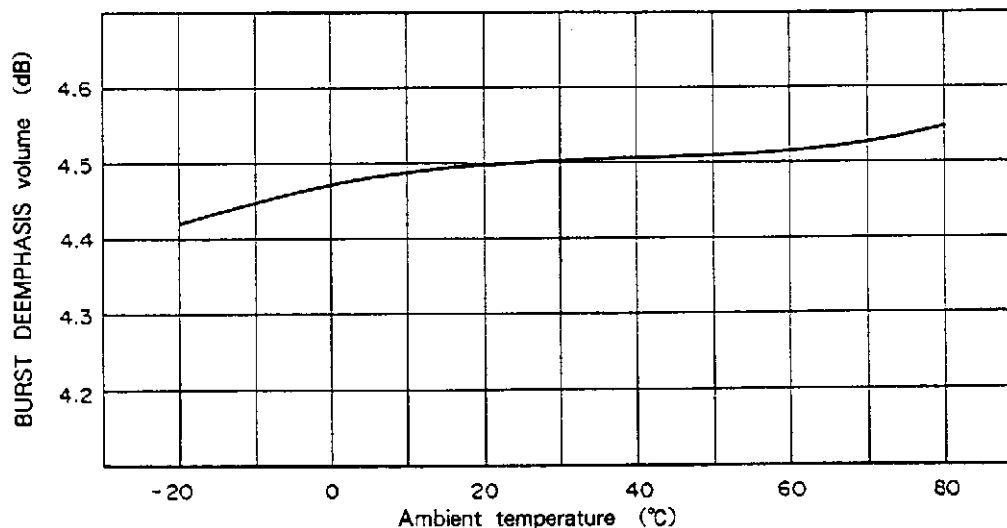




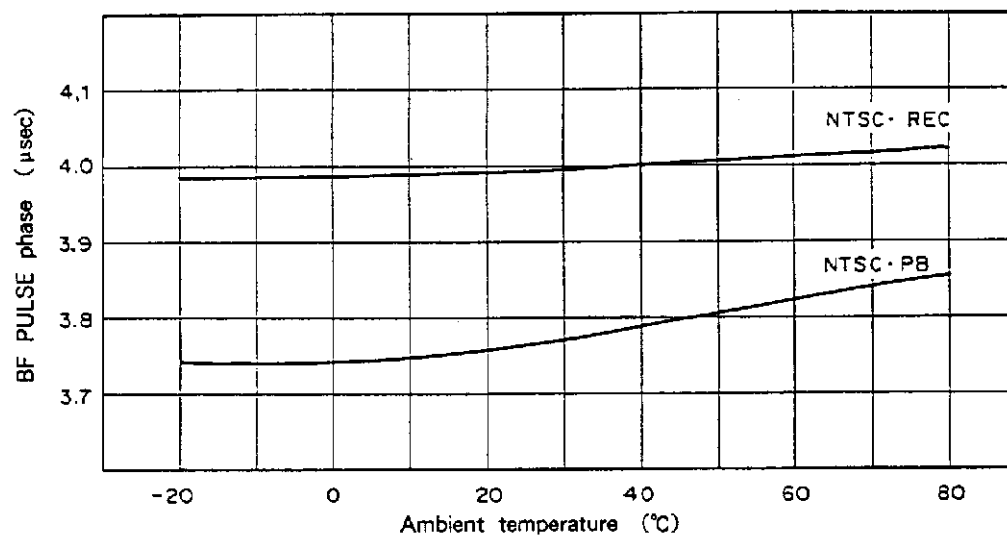
BURST EMPHASIS temperature characteristics



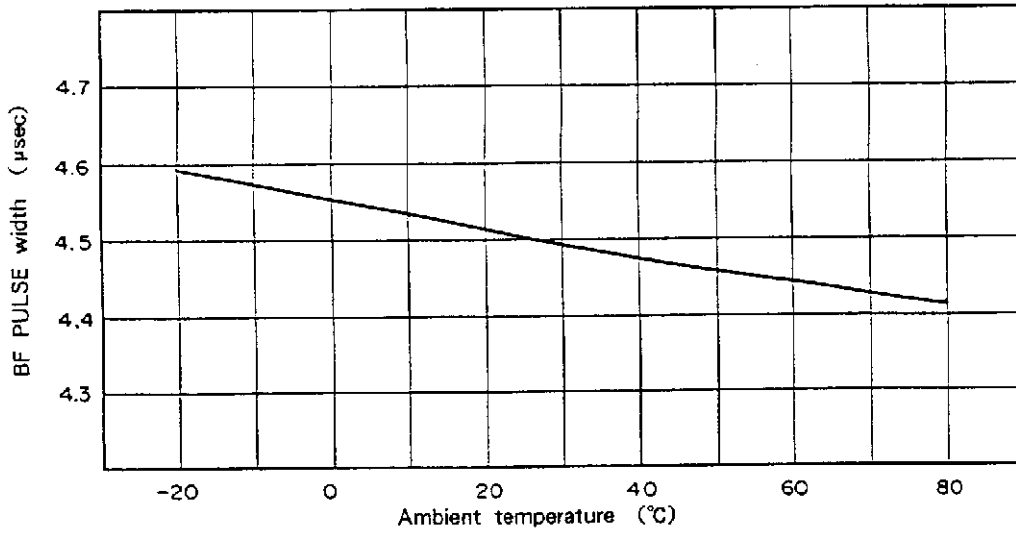
BURST DEEMPHASIS temperature characteristics



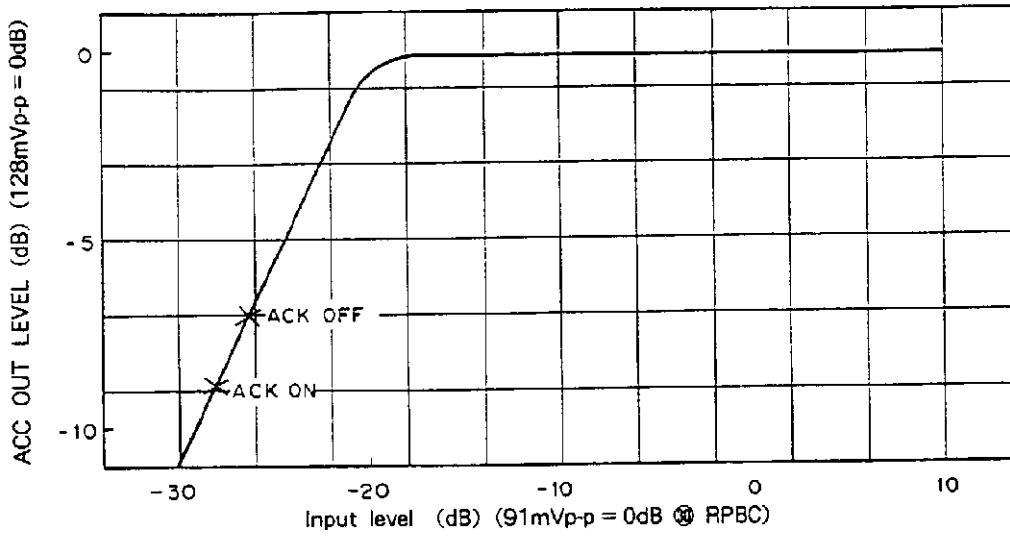
BF PULSE phase temperature characteristics



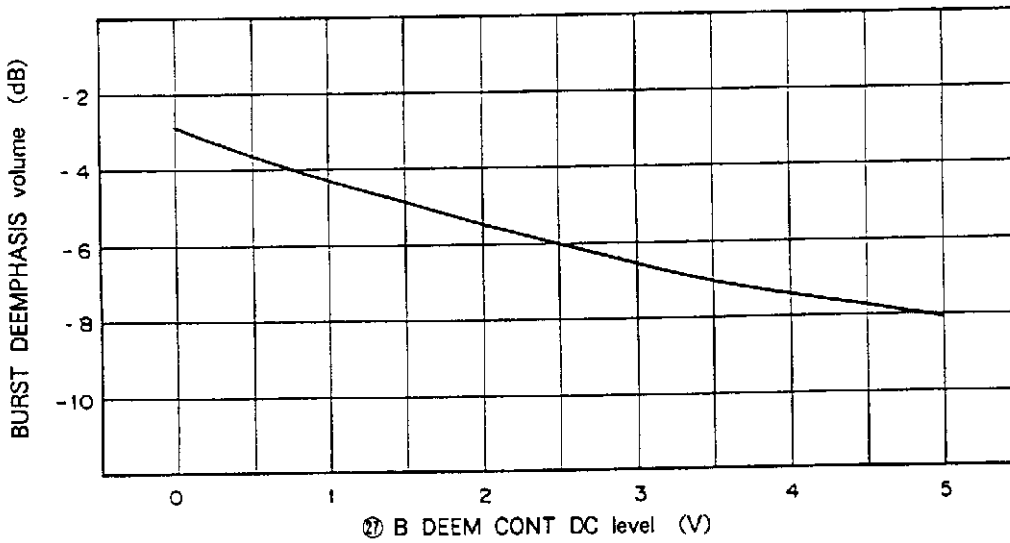
BF PULSE width temperature characteristics



ACC characteristics



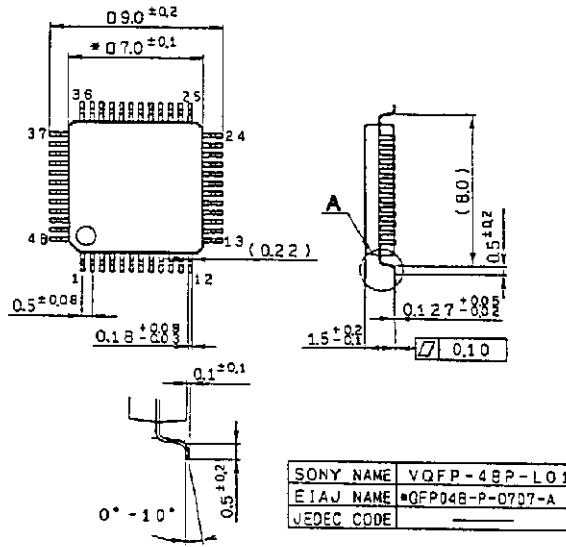
BURST DEEMPHASIS control characteristics



Package Outline Unit: mm

CXA1208R

48pin VQFP (Plastic) 0.2g

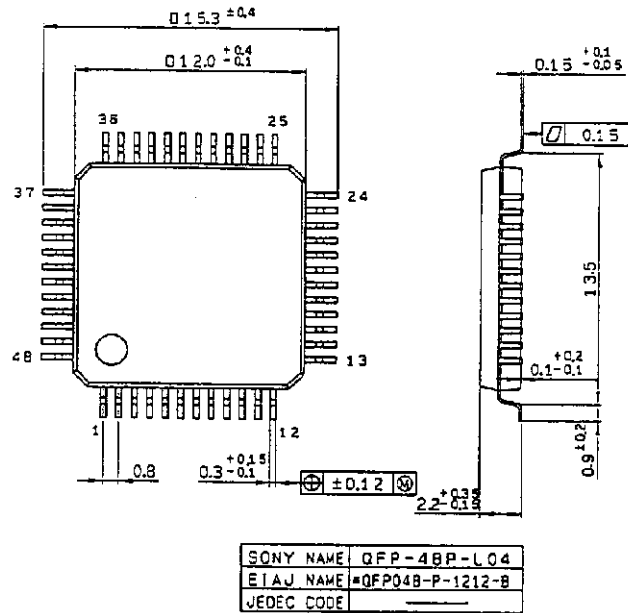


Detailed diagram of A

Note) Dimensions marked with * does not include resin residue.

CXA1208Q

48pin QFP (Plastic) 0.7g



NOTE : PALLADIUM PLATING

This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).