SONY

CXA1709P

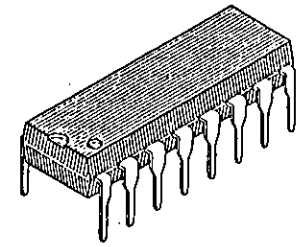
Pre-driver for Ultra-High Resolution Computer Display

For the availability of this product, please contact the sales office.

Description

The CXA1709P is a bipolar IC designed for use in ultra-high resolution computer displays.

16 pin DIP (Plastic)



Features

- Built-in super wide-band amplifier (250 MHz/-3dB typ.)
- 1 channel to 1 package
- Contrast can be controlled by DC.
- Rise/fall time of 2ns or less due to output amplitude of 4 V_{P-P}
- Drive adjustment for the three channels (R, G, B) is easily accomplished because the contrast characteristic is linear.

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	14	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1040	mW

Operating Conditions

• Recommended supply voltage	12.0	V
• Operating range	12 ±0.5	V

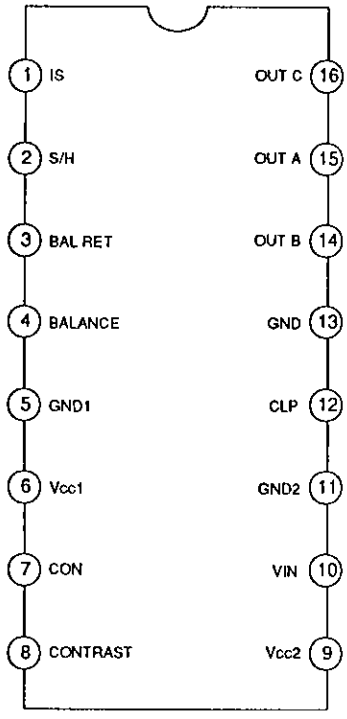
Structure

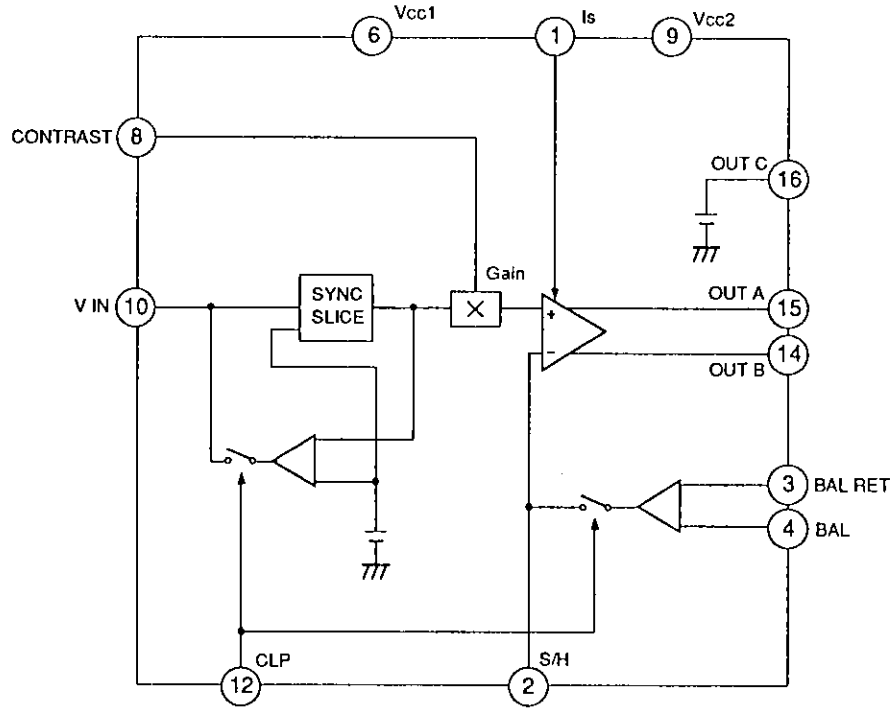
Bipolar silicon monolithic IC

Applications

Pre-driver for ultra-high resolution computer displays

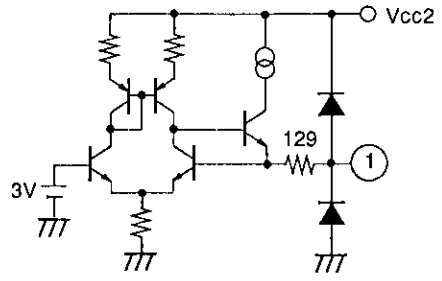
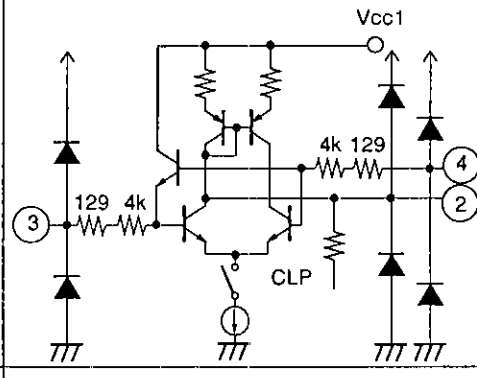
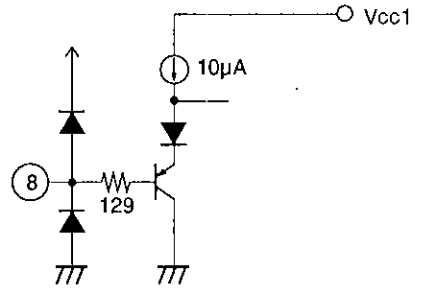
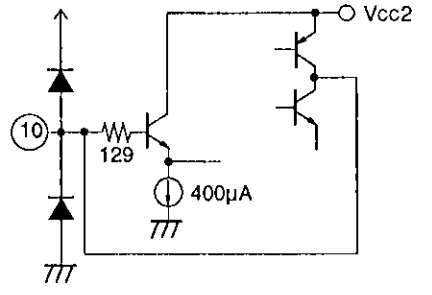
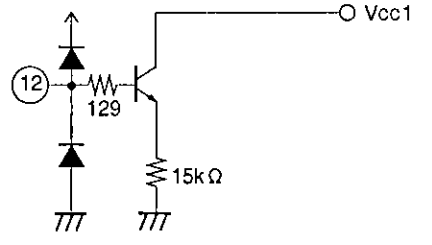
Block Diagram and Pin Configuration

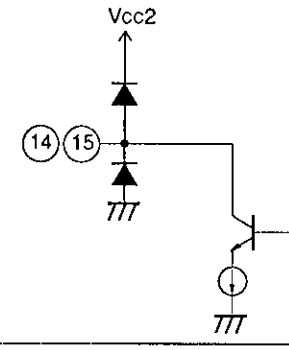
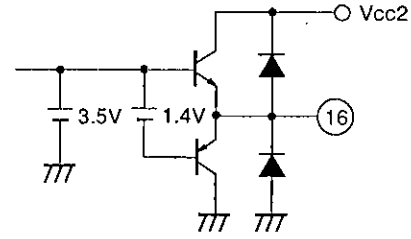




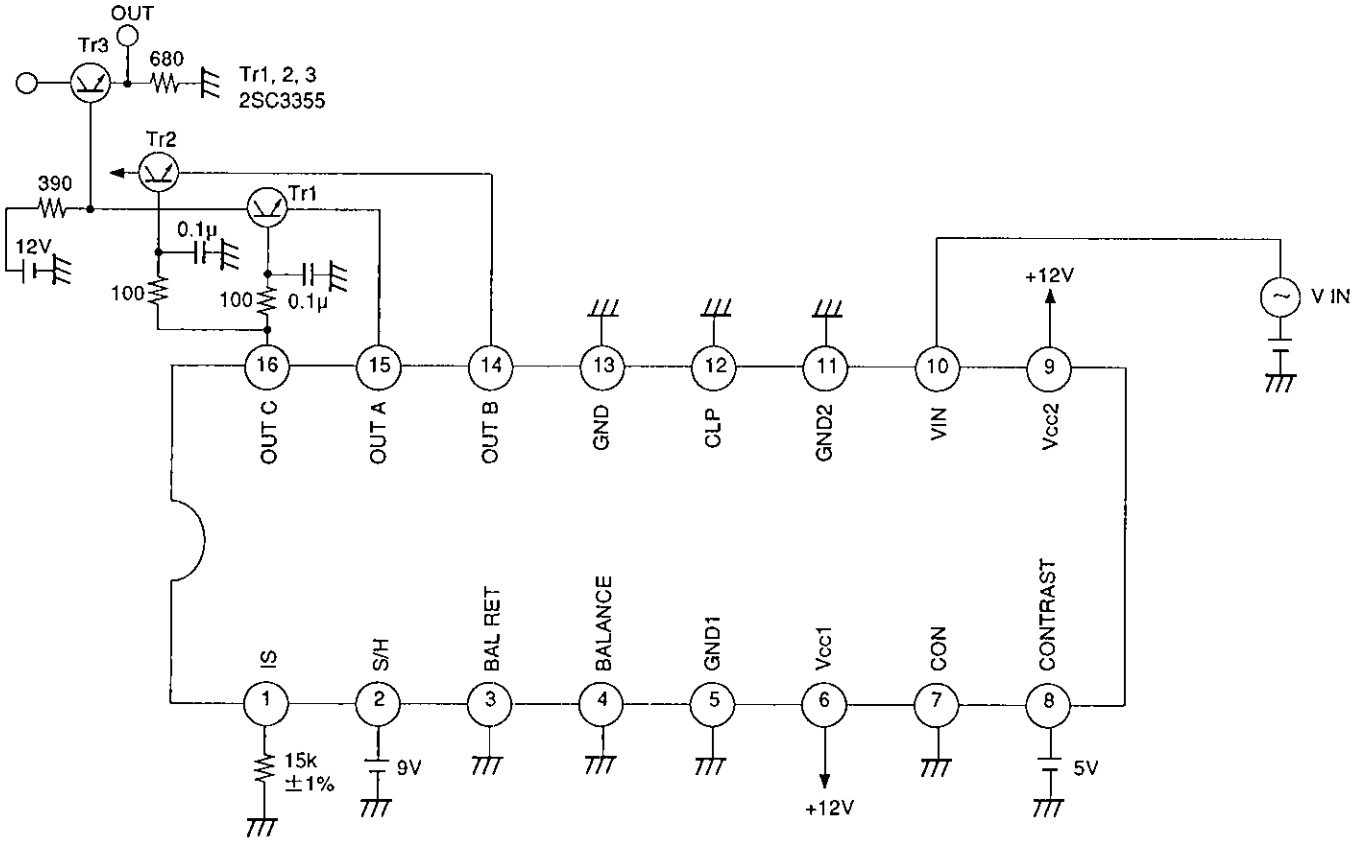
E93580-TE

Pin Description

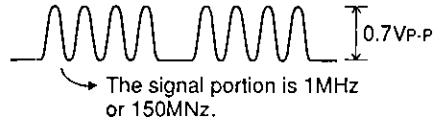
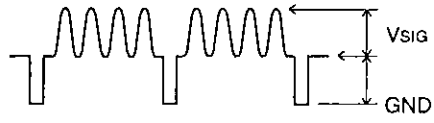
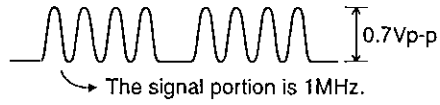
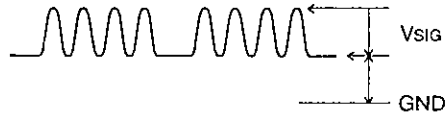
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	IS	3V		Determines a reference current source. Connect a 15 kΩ metal film resistor between Pin 1 and GND.
2	S/H	8V		Connect a capacitor for clamp.
3	BAL RET	4V		Inputs a feedback signal from the drive stage to stabilize the DC bias at cathode drive stage.
4	BALANCE	4V		Sets a output DC level.
8	CONTRAST	—		Contrast control. Control is possible between 0 to 5 V DC.
10	VIN			Video signal input.
12	CLP	—		Clamp pulse input.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
14	OUT B			Negative polarity output signal.
15	OUT A			Positive polarity output signal.
16	OUT C	2.6V		2.6V power supply output.
6	Vcc1	12V		Supply voltage for control system.
9	Vcc2	12V		Supply voltage for pre-amplifier block.
5	GND1	0		GND for control system.
11	GND2	0		GND for pre-amplifier block.
7	CON	0		Connect to GND.

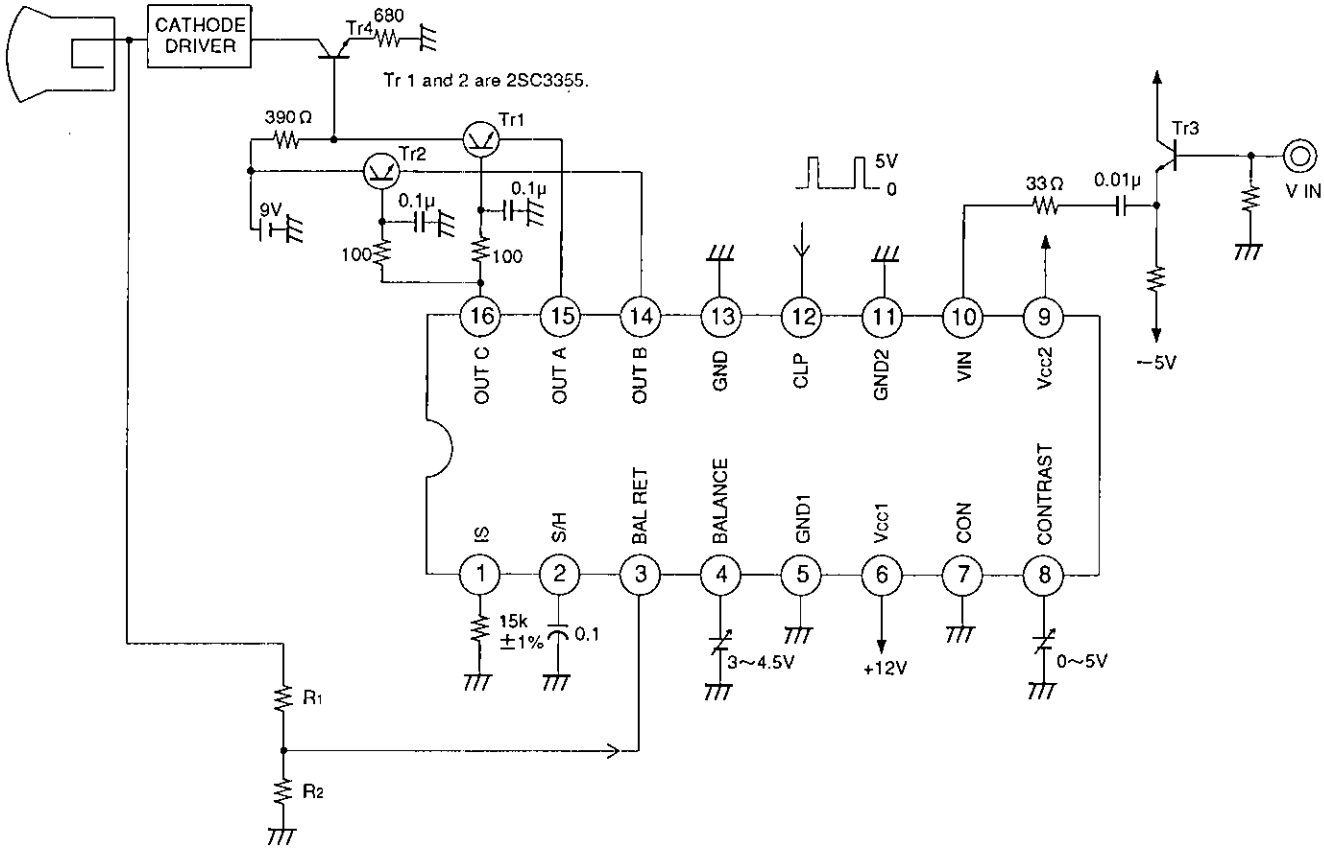
Electrical Characteristics Measurement Circuit



Electrical Characteristics

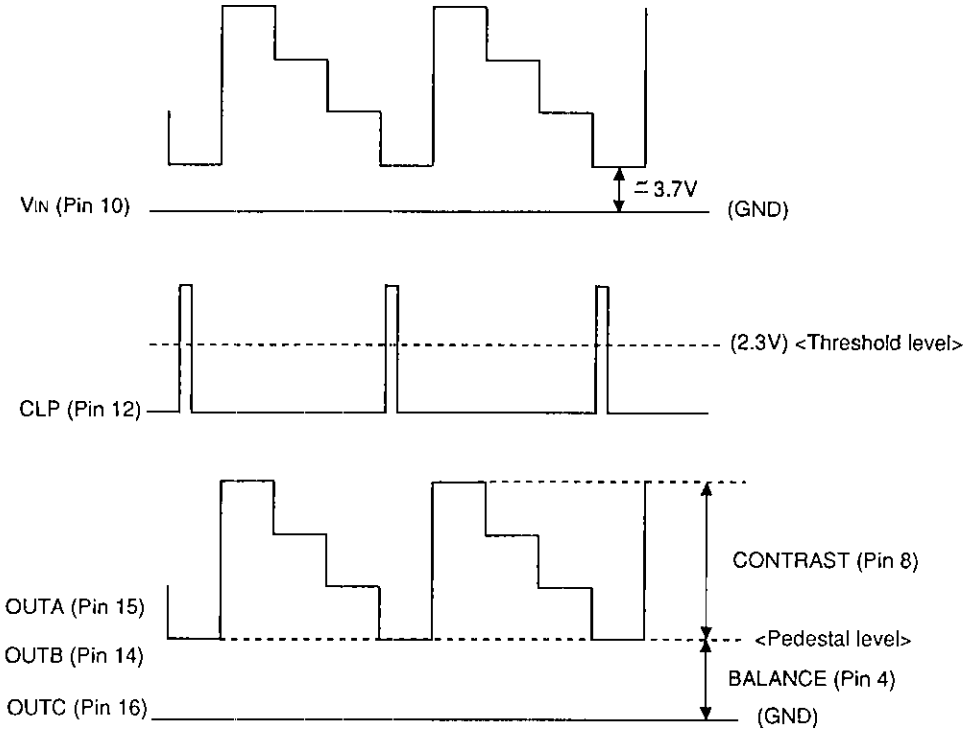
No.	Item	Symbol	Input conditions and measurements	Min.	Typ.	Max.	Unit
1	Supply current	ICC	Measure the inflow current at Pins 6 and 9 at no signal, no load.		33	45	mA
2	Frequency response	f150MHz	R. G. B input  R. G. B output  Input: Input 0.7 VP-P, 1 MHz or 150 MHz and measure the output amplitude VSIG. Specifications can be obtained through the following formula, assuming VSIG1 for1MHz and VSIG150 for 150MHz. $f_{1\text{-}150} = 20 \log \left(\frac{V_{SIG150}}{V_{SIG1}} \right)$ (dB) * Measure VSIG peak to peak.	−3.0	+1.0	—	dB
3	Contrast control	CONTMAX	R. G. B input  R. G. B output  Input: Measure the output amplitude VSIG at 0.7 VP-P, 1 MHz. The specifications can be obtained though the following formula. $CONT_{MAX\ (MIN)} = 20 \log \left(\frac{V_{SIG}}{0.7} \right)$ (dB)	13.5	15.0	—	dB

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Input/Output Pulse Waveforms and Description of Operation

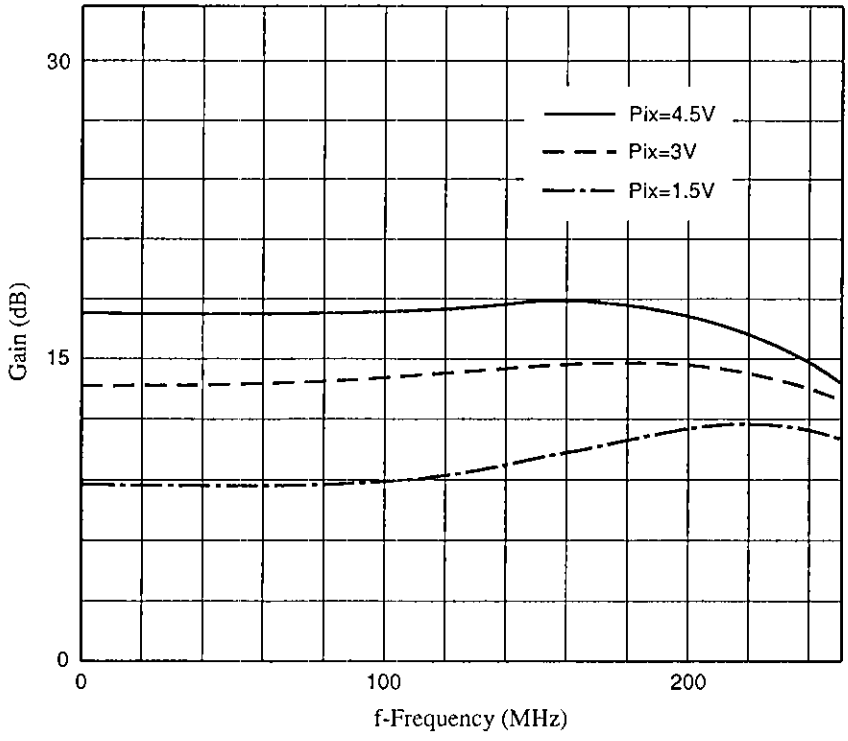


1. Contrast
   Gain is controlled on the VIN (Pin 10) input signal, using the DC voltage input from CONTRAST (Pin 8). The control range is from -20 to 15 dB (typ.).

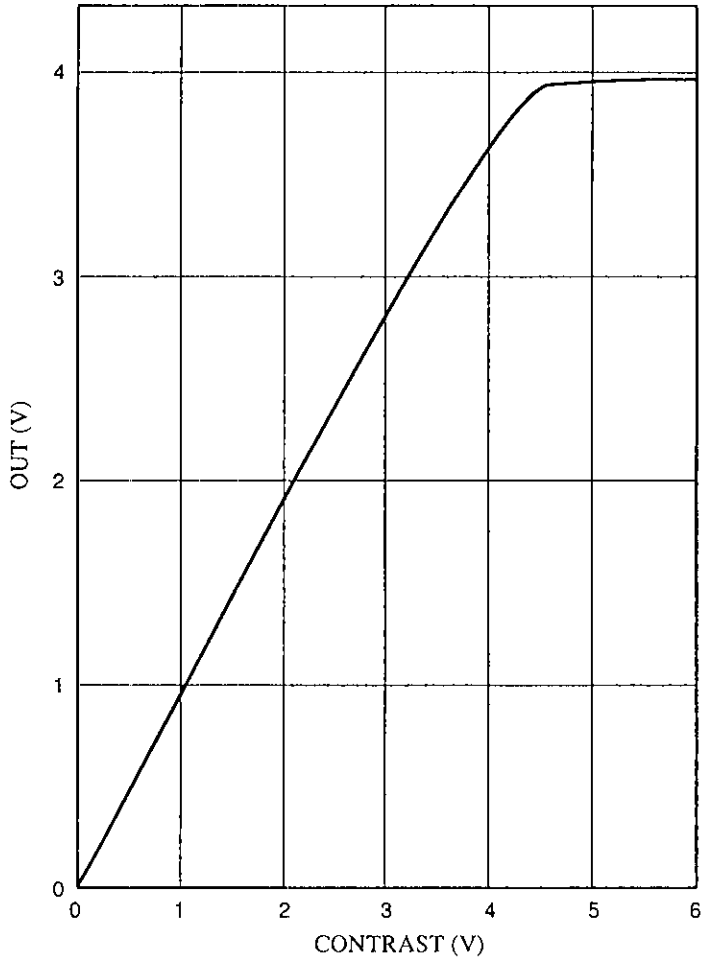
2. Pedestal Clamp
   The pedestal level is clamped while CLAMP (Pin 12) is high. The threshold level of the clamp pulse is approximately 2.3 V. Note that 300 ns are required for clamp time.
   The output DC level can be varied by the DC input from BALANCE (Pin 4). In this time, the emitter follower output at the external transistor should not be below 2 V or low.

3. The output signal is amplified by the external power amplifier and drives the CRT. The amplified signal voltage is fed back to Pin 3. Then, set the R1 and R2 values so that the pedestal level at Pin 3 is 4 ± 0.5 V.

Frequency response

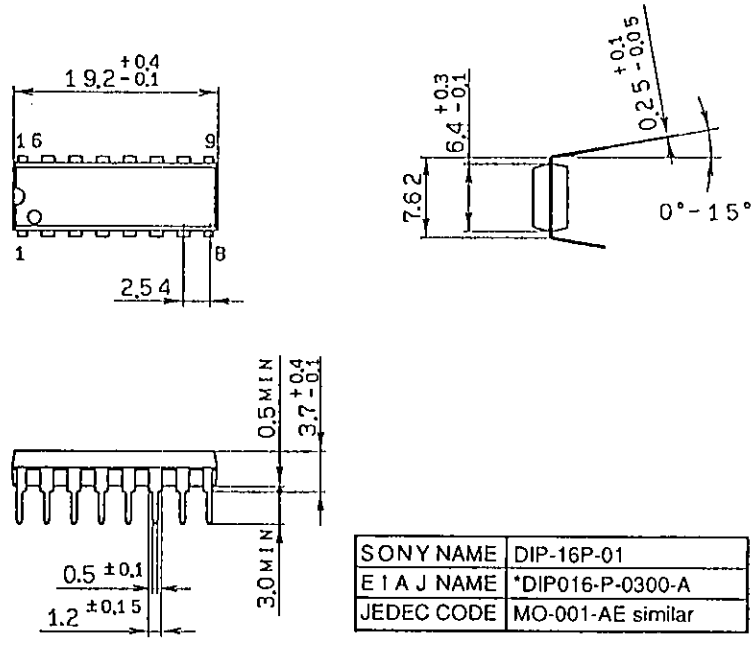


Gain control characteristics



Package Outline Unit : mm

16pin DIP (Plastic) 300mil 1.0g



SONY NAME	DIP-16P-01
EIAJ NAME	*DIP016-P-0300-A
JEDEC CODE	MO-001-AE similar