SONY

CXA1843Q

High-Speed Sample-and-Hold IC

For the availability of this product, please contact the sales office.

Description

The CXA1843Q is a bipolar IC designed to sample-and-hold video and various other signals with high speed. It is ideal for video and other signal conversions.

Features

- Maximum operating rate = 33MHz (min.)
- Low power consumption: 320mW
- S/H clock pulse generator circuit
- Built-in clock pulse generator for A/D converter

Applications

When used in combination of the CXA1844Q, the CXA1843Q achieves A/D conversion.

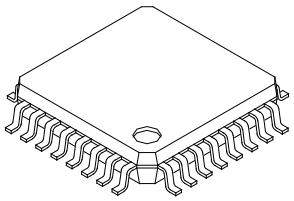
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	7	V
	V_{EE}	–7	V
• Input voltage			
(VIN pin)	V_{IN}	V_{EE} to AV_{CC} + 0.3	V
(REFIN pin)	V_{REFIN}	+1 to AV_{CC} + 0.3	V
(CLKIN pin)	V_{CLK}	GND – 0.5 to DV_{CC} + 0.3	V
(REX 2, 3, 4 pins)	$V_{REX2, 3, 4}$	GND to GND + 4	V
• Reference voltage			
(REFFB pin)	V_{REFFB}	V_{EE} to +3	V
(REFOUT pin)	V_{REFOUT}	V_{EE} to AV_{CC} + 0.3	V
• Output current			
(REFFOUT pin)	I_{REFOUT}	–1 to +1	mA
(SHOUT pin)	I_{SHOUT}	–12 to +12	mA
(CLKOUT pin)	I_{ADC}	–1.5 to +1.5	mA
• Storage temperature			
	Tstg	–65 to +150	°C
• Allowable power dissipation			
	P_D	1.1	W

Operating Conditions

• Supply voltage	V_{CC}	4.75 to 5.25	V
	V_{EE}	–4.75 to –5.25	V
• Operating temperature			
	Topr	–20 to +75	°C

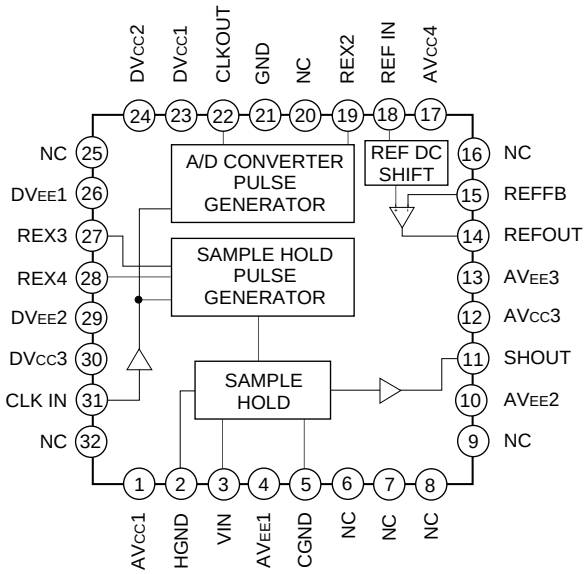
32 pin QFP (Plastic)



Structure

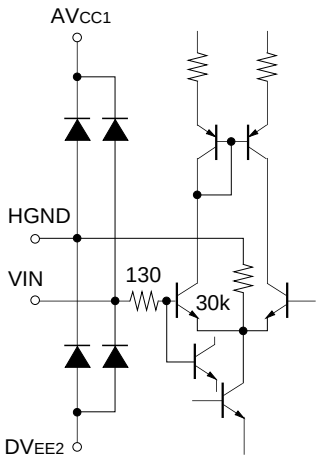
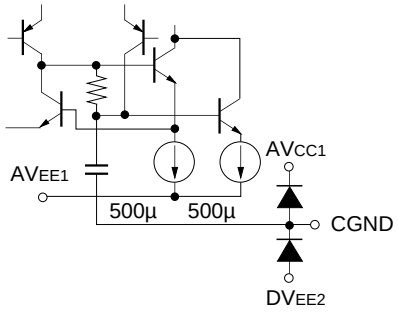
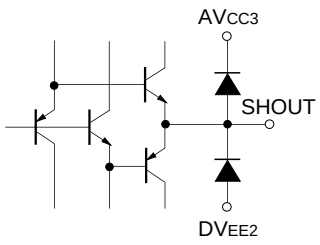
Bipolar silicon monolithic IC

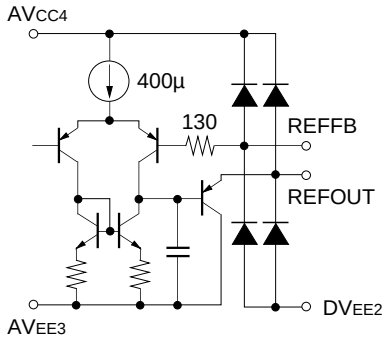
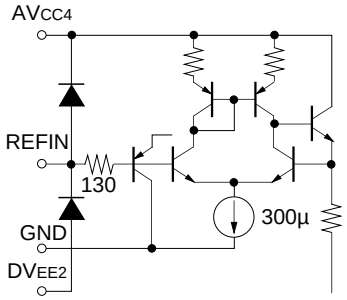
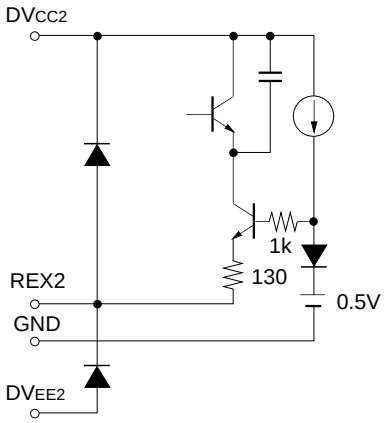
Block Diagram and Pin Configuration

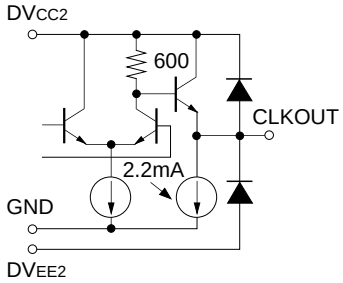
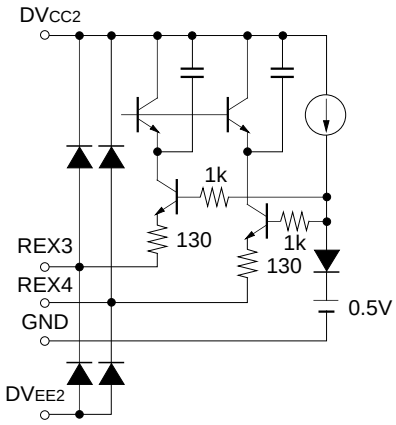
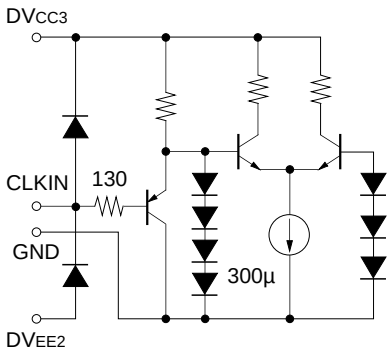


E92855B7Y

Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	AV_{CC1}	5V (Typ.)		Analog positive power supply.
2	HGND	0V		Internal resistance GND for sample-and-hold.
3	VIN	—		Sample-and-hold-input.
4	AV_{EE1}	–5V (Typ.)		Analog negative power supply.
5	CGND	0V		Internal capacitance GND for sample-and-hold.
6	NC	—		Connect to AGND.
7	NC	—		Connect to AGND.
8	NC	—		Connect to AGND.
9	NC	—		Connect to AGND.
10	AV_{EE2}	–5V (Typ.)		Analog negative power supply.
11	SHOUT			Sample-and-hold output.

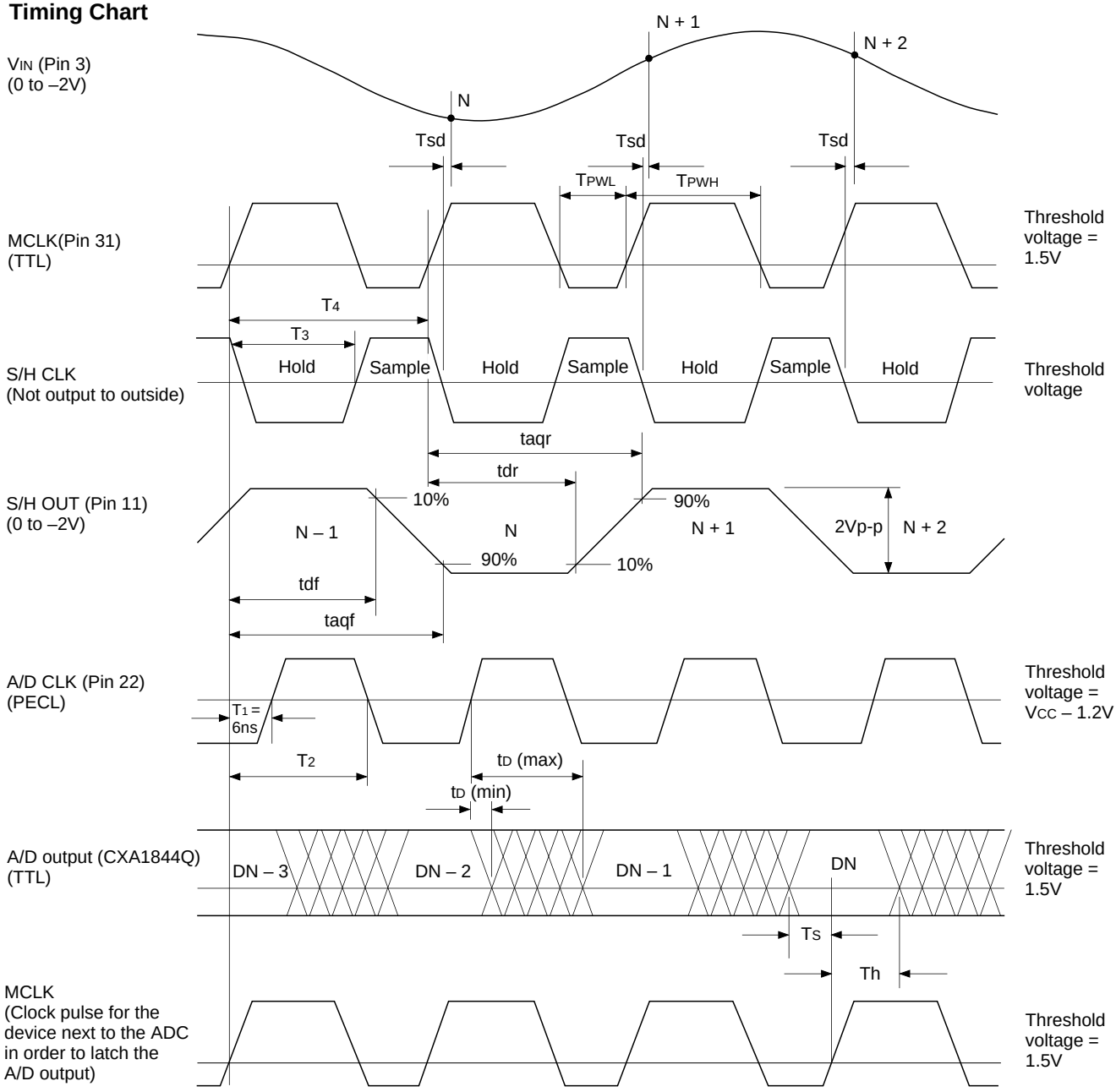
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
12	AV_{CC3}	5V (Typ.)		Analog positive power supply.
13	AV_{EE3}	–5V (Typ.)		Analog negative power supply.
14	REFOUT	–2.8V (As shown in the Application Circuit, PNP TR. is connected and 2.5V is applied to Pin18.)		Connect the base of the external PNP transistor to create a –2V power supply.
15	REFFB	–2V (As shown in the Application Circuit, PNP TR. is connected and 2.5V is applied to Pin18.)		Connect the emitter of the external PNP transistor to create a –2V power supply.
16	NC	—		Connect to AGND.
17	AV_{CC4}	5V (Typ.)		Analog positive power supply.
18	REFIN	2.5V (Typ.)		External DC input for adjusting the –2V power supply.
19	REX2	Approx. 0.5V (When external resistor is connected between Pin 19 and AGND)		Connect external resistor that determines the time interval (T_2) between master clock (MCLK) rise and A/D converter clock (A/D CLK) fall. (Normally connect to 1.6kΩ)
20	NC	—		Connect to AGND.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
21	GND	0V		GND
22	CLKOUT	H: DV_{CC2} – 0.78V L: DV_{CC2} – 1.52V (Typ.)		A/D converter clock (A/D CLK) output.
23	DV_{CC1}	5V (Typ.)		Digital positive power supply.
24	DV_{CC2}	5V (Typ.)		Digital positive power supply.
25	NC	—		Connect to DGND
26	DV_{EE1}	–5V (Typ.)		Digital negative power supply.
27	REX3	Approx. 0.5V When external resistor is connected between Pin 27 and DGND		Connect external resistor that determines the time interval (T_3) between master clock (MCLK) rise and sample-and-hold internal clock (S/H CLK) rise. (Normally connect 2.7kΩ)
28	REX4	Approx. 0.5V When external resistor is connected between Pin 28 and DGND		Connect external resistor that determines the time interval (T_4) between master clock (MCLK) rise and sample-and-hold internal clock (S/H CLK) rise. (Normally connect 1.5kΩ)
29	DV_{EE2}	–5V (Typ.)		Digital negative power supply.
30	DV_{CC3}	5V (Typ.)		Digital positive power supply.
31	CLKIN	—		Master clock (MCLK) input. TTL level. (Vth = 1.5V)
32	NC	—		Connect to DGND.

Electrical Characteristics (Ta = 25°C, V_{CC} = 5V, V_{EE} = –5V)

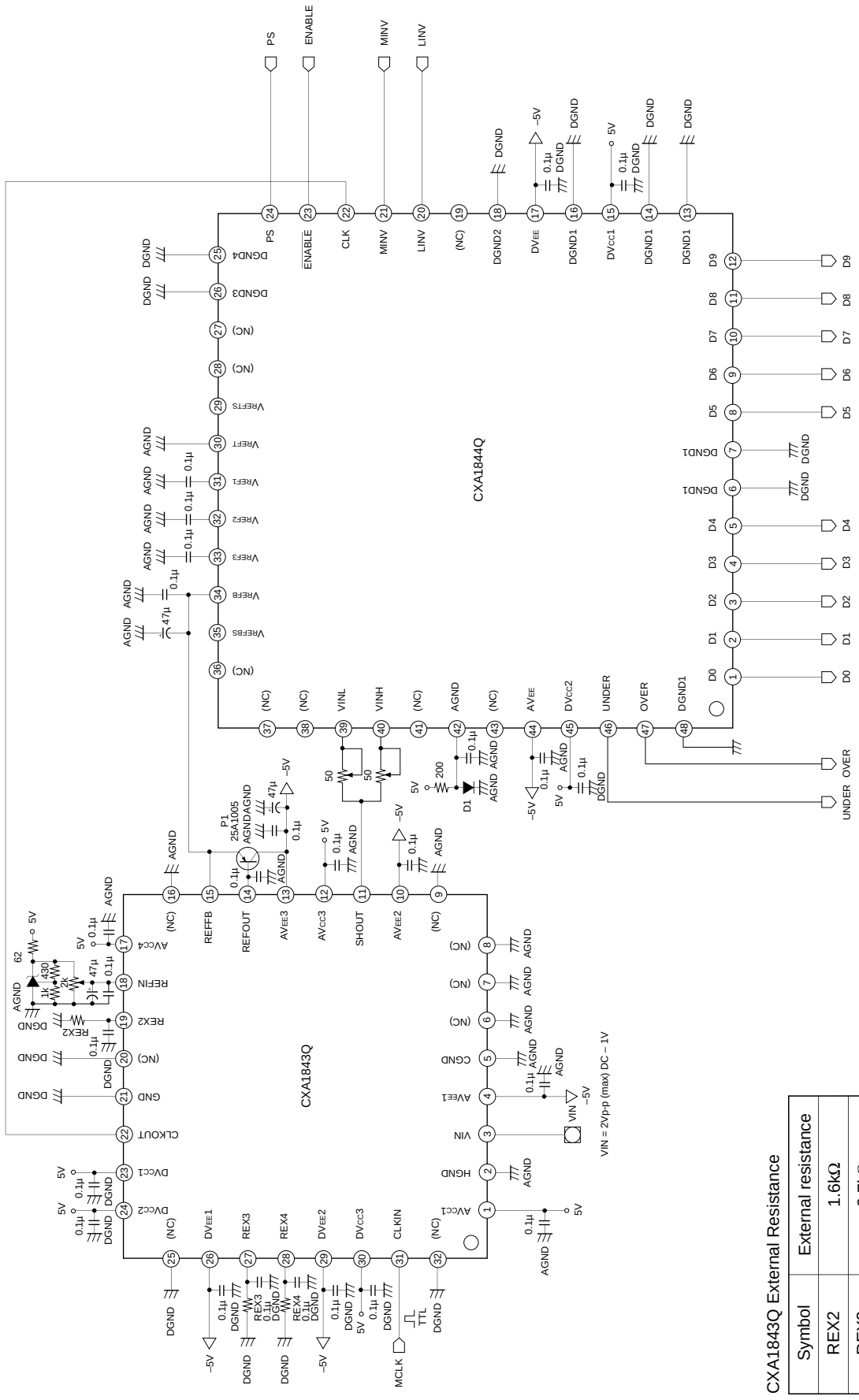
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximun operating rate	F_C		33			MHz
Current consumption	I_{CC}		32	41	50	mA
	I_{EE}		–28	–23	–18	mA
S/H Amplifier Block						
V_{IN} input current	I_{VIN}	V_{IN} = –1V	1	20	50	µA
V_{IN} input voltage range	V_{IN}	F_{IN} = 1kHz, distortion factor ≤ –55dB	–2.2		0.2	V
Droop	HMDR	V_{IN} = –2V to 0V	–20	20	80	mV/µs
Feed through	HMTH	F_{IN} = 16.5MHz (2Vp-p)	–40	–50	–70	dB
S/H output offset voltage	V_{OFFSET}	V_{IN} = –1V, F_{CLK} = 33MHz	55	90	120	mV
S/H output gain	Gsh	F_{IN} = 1kHz (2Vp-p), F_{CLK} = 33MHz	–0.5	0.3	0.5	dB
S/H output frequency response	Fsh	20Log (V_O (16.5MHz)/V_O (200kHz)), Sampling time = 14ns	–1	0.2	1	dB
S/H output slew rate	SR	C_L = 50pF	140	160	200	V/µs
Reference Amplifier Block						
REFIN input current	I_{REFIN}	V_{REFIN} = 2.5V	0	1	10	µA
REFFB output voltage	V_{REFFB}	V_{REFIN} = 2.5V	–2.2	–2.0	–1.8	V
Digital I/O Block						
CLKIN input current	I_{CLKL}	V_{CLKIN} = 0V	–10	–6	0	µA
	I_{CLKH}	V_{CLKIN} = 5V	0	0	1	µA
CLKIN input voltage	V_{CLKL}				0.8	V
	V_{CLKH}		2.0			V
CLKIN clock width	T_{PWH}		9			ns
	T_{PWL}		9			ns
A/D clock low level	V_{ADCL}			V_{CC} – 1.52	V_{CC} – 1.40	V
A/D clock high level	V_{ADCH}		V_{CC} – 0.90	V_{CC} – 0.78		V

Timing Chart



MCLK:	System master clock.
S/H CLK:	This clock actuates the internal sample-and-hold circuit. The internal clock pulse circuit generates the S/H CLK, which is not output outside the IC.
A/D CLK:	This clock actuates the A/D converter. The internal clock buffer circuit generates the A/D CLK. This clock has the level where +5V is shifted from the ECL level.
T_{PWH}, T_{PWL}:	S/H CLKIN input clock width
Tsd:	S/H sampling delay for the S/H internal clock
T_1:	Fixed time interval between master clock rise and A/D CLK rise, T_1 = 6ns (typ.)
T_2:	Time interval between MCLK rise and A/D CLK fall
T_3:	Time interval between MCLK rise and S/H CLK rise
T_4:	Time interval between MCLK rise and S/H CLK fall
taqf, tdf:	10%/90% falling output delay of S/H from MCLK rise
taqr, tdr:	10%/90% rising output delay of S/H from MCLK rise
t_D (min., max.):	Minimum/maximum output delay of A/D converter (Refer to the CXA1844Q specification.)
Ts:	Setup time of A/D output and MCLK
Th:	Hold time of A/D output and MCLK

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

CXA1843Q External Resistance

Symbol	External resistance
REX2	1.6kΩ
REX3	2.7kΩ
REX4	1.5kΩ

* Metal film resistors must be connected to the REX2 to REX4 pins.

Notes on Operation

(1) In circuit board layout, it is necessary that the AGND and DGND patterns be as large as possible and that double or more layer pattern be used to make low impedance.

(2) To prevent digital system noise interference with the analog system, the AGND and DGND, AV_{CC} and DV_{CC}, AV_{EE} and DV_{EE} on the PCB must be separated from each other. However, connect the AV_{EE} and DV_{EE} with coil and others to prevent the generation of differential voltage.

(3) The AV_{CC}, DV_{CC}, AV_{EE} and DV_{EE} pins must be connected to the AGND or DGND respectively via ceramic chip capacitors those are 0.1µF or more, as close to the pin as possible.

(4) The length of the wiring between the S/H SHOUT and A/D converter V_{IN} should be as short as possible.

(5) The range of the signal input to V_{IN} (Pin 3) of the sample-and-hold circuit is 0 to –2V.

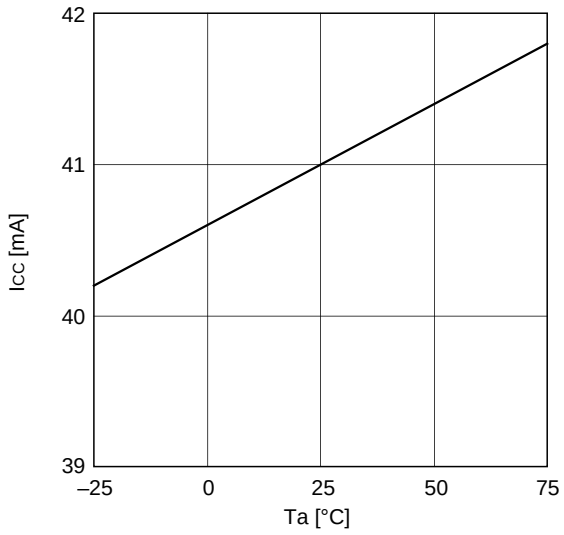
(6) Adjust the V_{REFIN} applied voltage so that V_{REFFB} = f – 2V.

(7) As shown in the Block Diagram, the amplifier input and output are internally connected to the REFOUT and REFFB pins. To generate REFFB voltage for the reference voltage of A/D converter, the connection of an external PNP transistor ($h_{FE} \geq 100$ (typ.)) is required as shown in the Application Circuit.

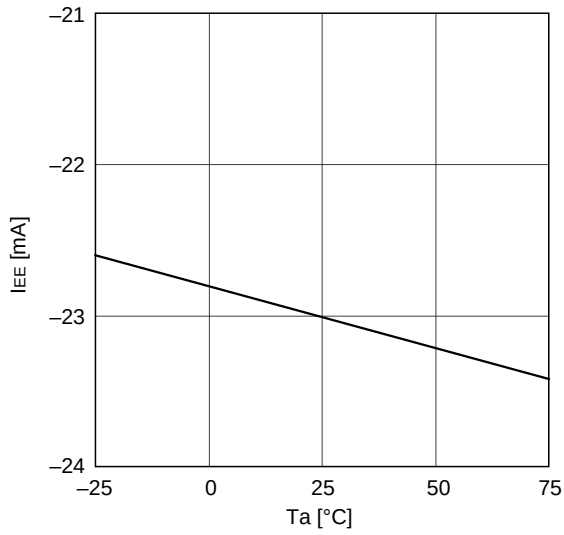
(8) Make the S/H DV_{CC2} voltage equal to the A/D converter DV_{CC1} voltage.

Example of Representative Characteristics

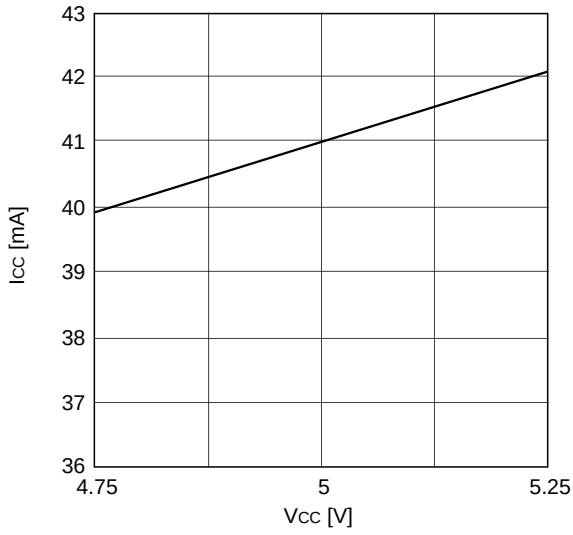
ICC vs. Ta



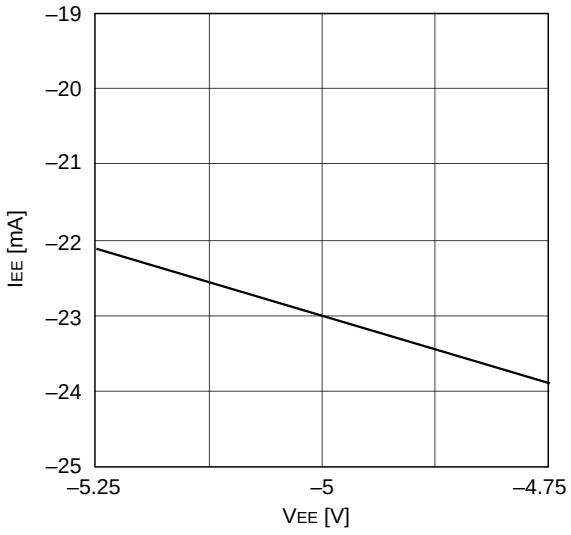
IEE vs. Ta



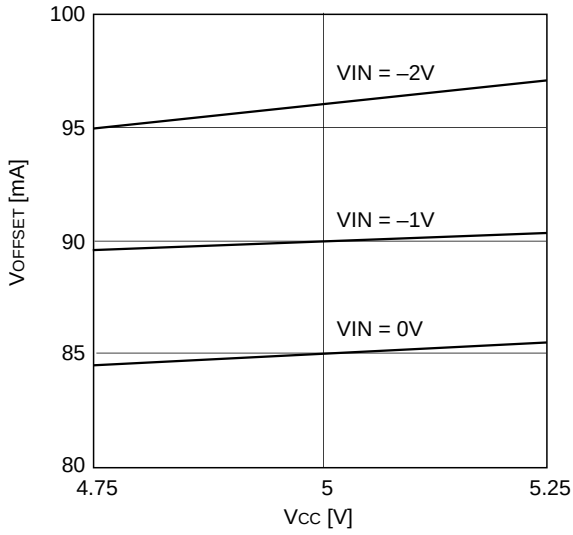
ICC vs. VCC



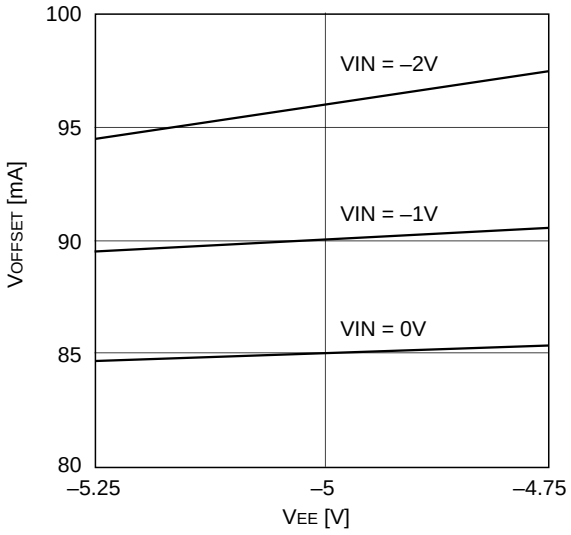
IEE vs. VEE



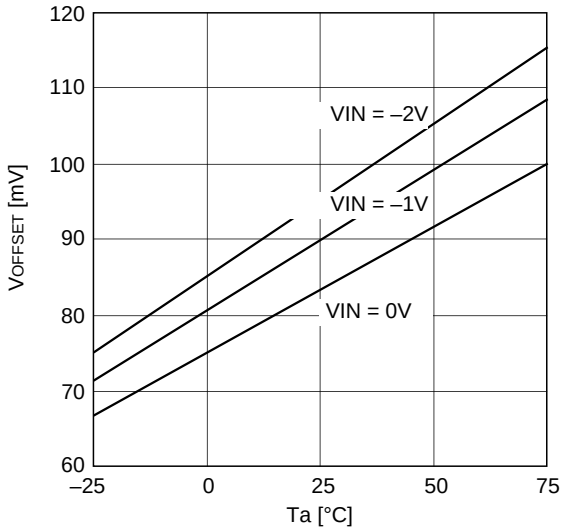
VOFFSET vs. VCC



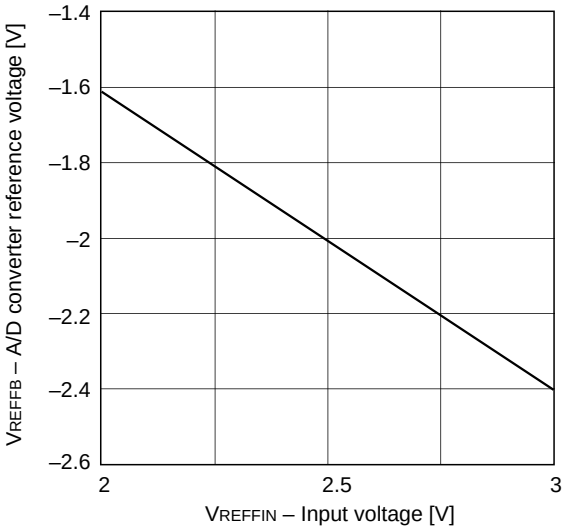
VOFFSET vs. VEE



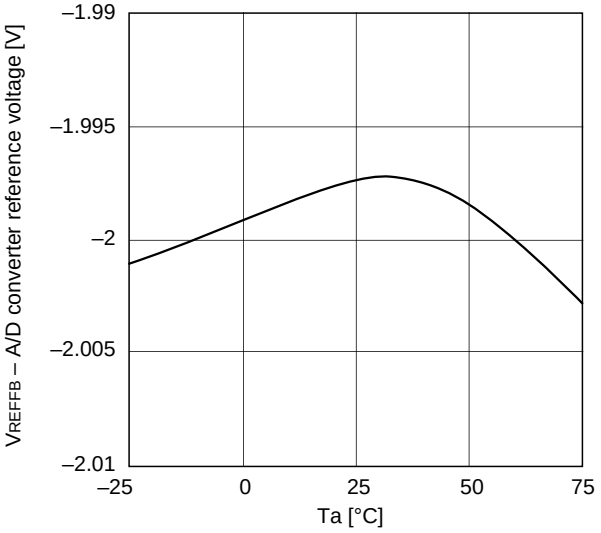
VOFFSET vs. Ta



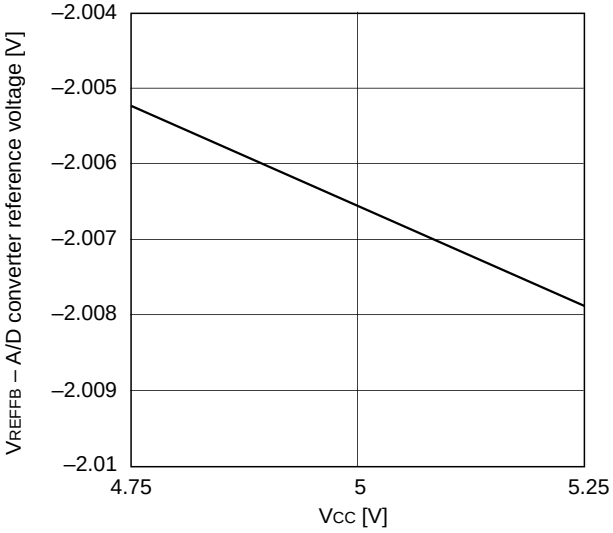
A/D converter reference voltage vs. Input voltage



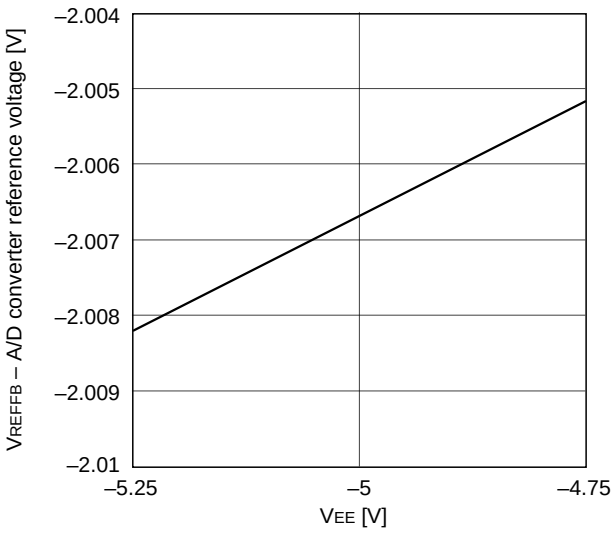
A/D converter reference voltage vs Ta (VREFFIN = 2.5V)



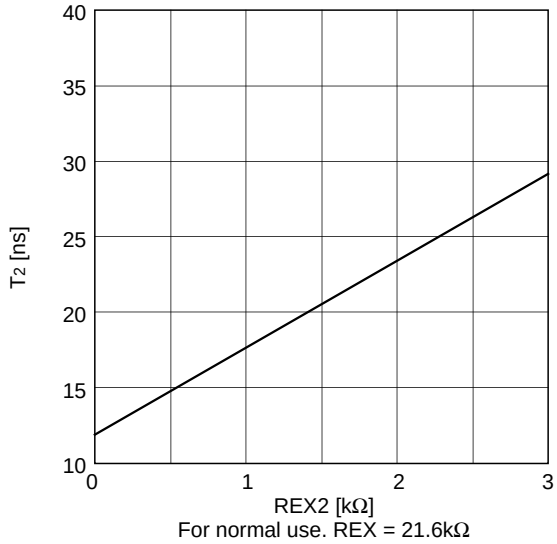
A/D converter reference voltage vs. VCC (VREFFIN = 2.5V)



A/D converter reference voltage vs. VEE (VREFFIN = 2.5V)

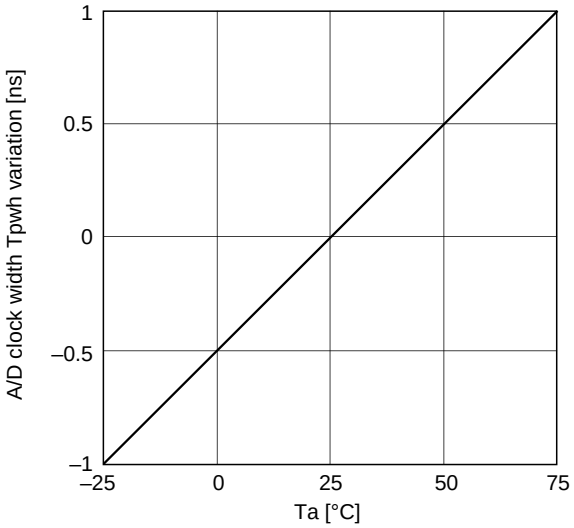


T_2 vs. REX2

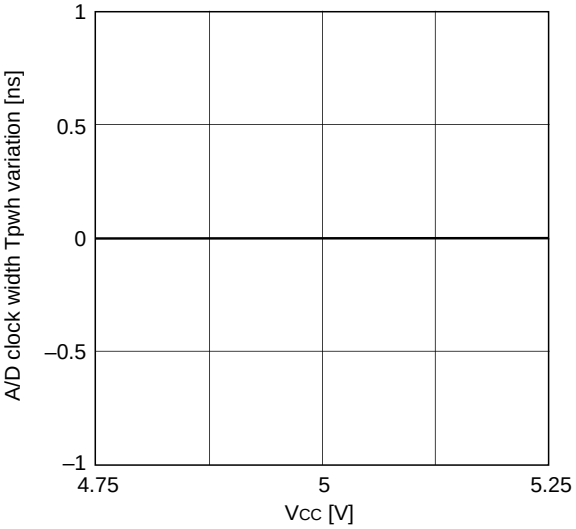


For normal use. REX = 21.6kΩ

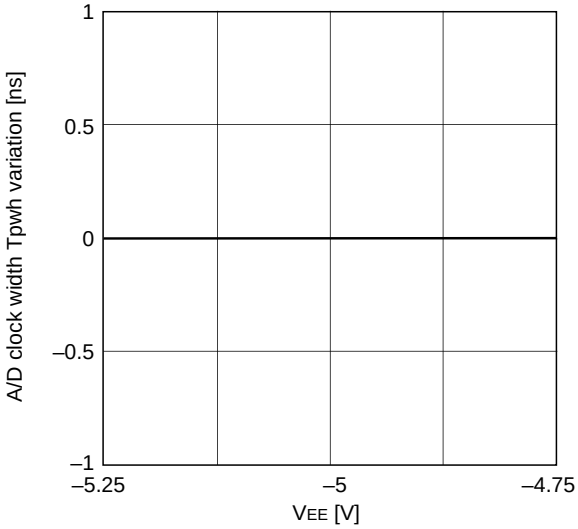
A/D clock width Tpwh (T_2-T_1) variation vs. Ta (Ta = 25°C typ.)



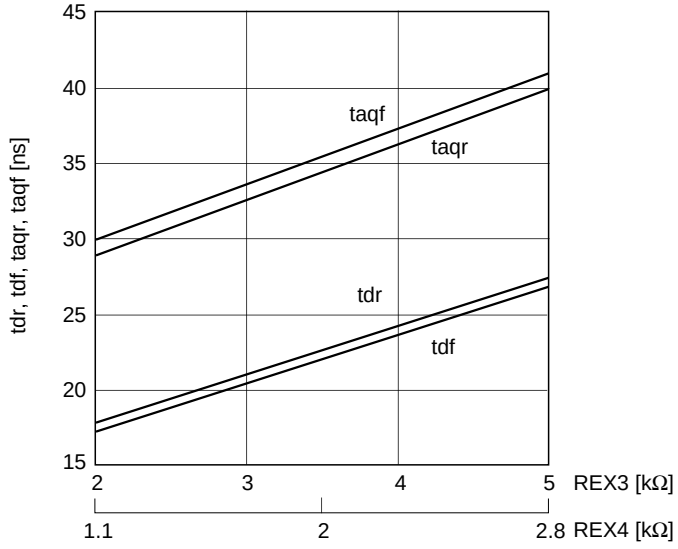
A/D clock width Tpwh (T_2-T_1) variation vs. V_{CC} (V_{CC} = 5.0V typ.)



A/D clock width Tpwh (T_2-T_1) variation vs. V_{EE} (V_{EE} = –5.0V typ.)

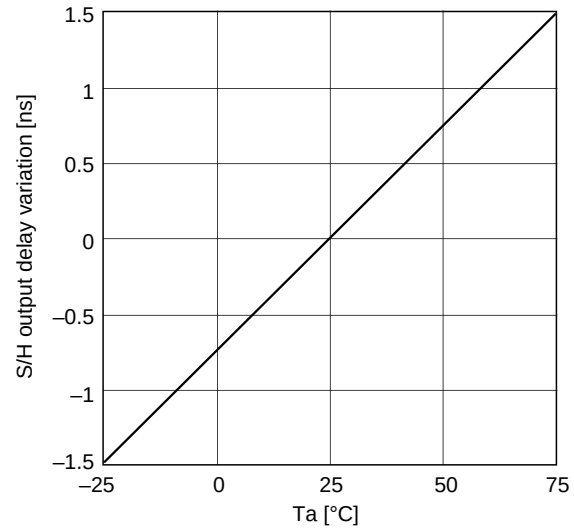


S/H output delay (tdr, tdf) vs. REX3 (taqr, taqf) vs. REX4

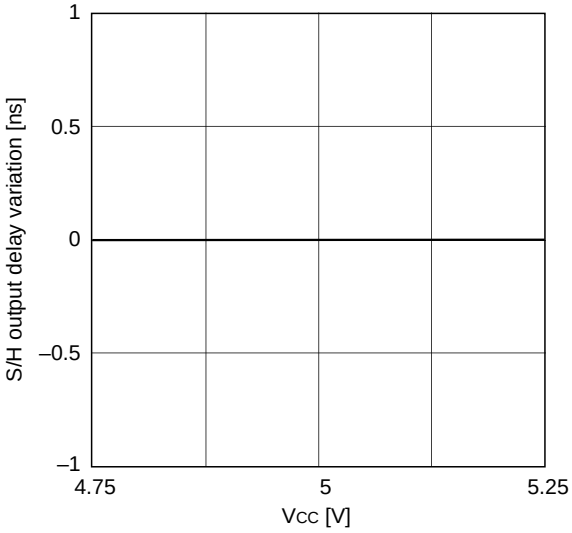


For normal use, REX3 = 2.7kΩ
REX4 = 1.5kΩ

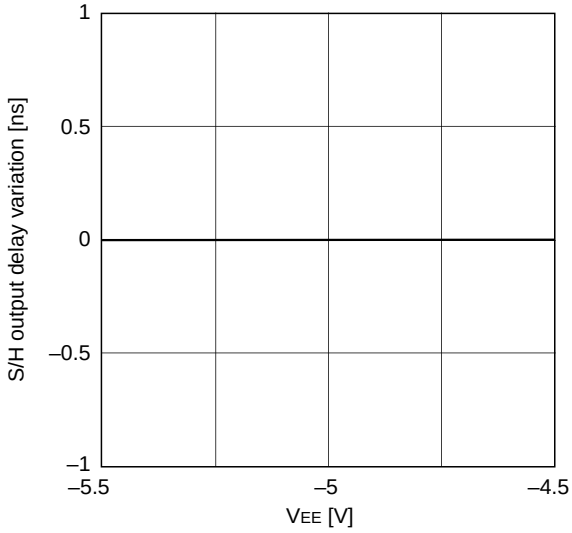
S/H output delay variation vs. Ta (Ta = 25°C typ.)



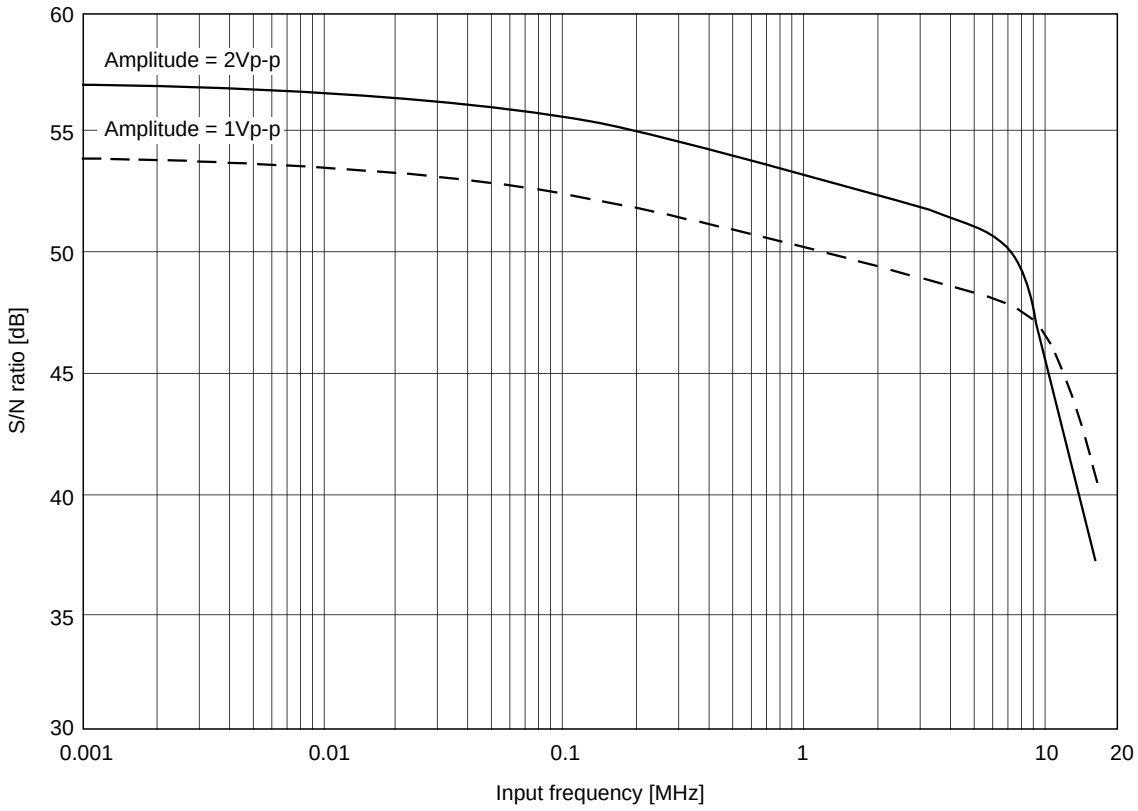
S/H output delay variation vs. V_{CC}
(V_{CC} = 5.0V typ.)



S/H output delay variation vs. V_{EE}
(V_{EE} = –5.0V typ.)



Input frequency vs. S/N ratio for CXA1843Q + CXA1844Q (clock frequency = 33MHz)



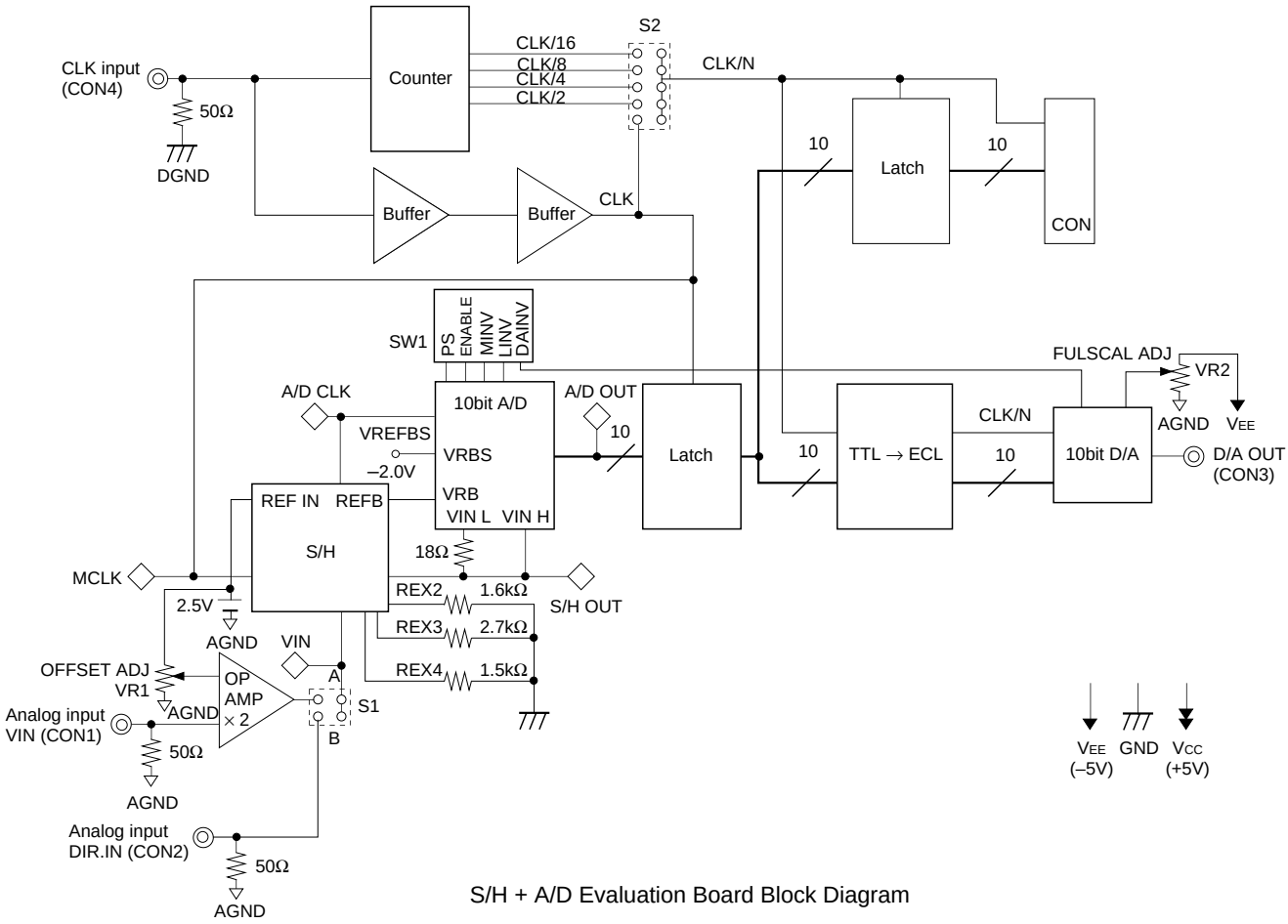
S/H + A/D EVALUATION BOARD

The S/H + A/D Evaluation Board is a printed circuit board for evaluating the 10-bit 33MSPS high speed sample-and-hold IC (CXA1843Q) and 2-step A/D converter (CXA1844Q). This board is designed to enable users to make full use of the performance of CXA1843Q + CXA1844Q and evaluate them easily.

Features

• Resolution	10bit
• Maximum operating conversion speed	33MSPS
• 2 types analog input	V_{IN} input (OP AMP input) and DIR. IN input (AC coupled input) are available.
• Analog input dynamic range	2Vp-p
• Digital output level	TTL
• Power supply voltage	±5V
• Built-in D/A converter (For evaluation)	Generates the analog waveform.

Block Diaram



S/H + A/D Evaluation Board Block Diagram

Connection and Setting for S/H + A/D Evaluation Board

1. Power supply voltage (CON6)

Item	Min.	Typ.	Max.	Unit	Typical current	Unit
Vcc	+4.75	+5.0	+5.25	V	220	mA
V_{EE}	–5.25	–5.0	–4.75	V	–400	mA

2. Analog input (CON1, CON2) and offset adjustment (VR1)

[V_{IN} Input] (CON1)

When the amplitude of an analog input signal supplied to the sample-and-hold is 1Vp-p and its input range is within 1.0V to –0.9V, the board is able to amplify its amplitude by two times using the operation amplifier. The S1 selector should be short-circuited at side A and opened at side B, and the analog input is added from CON1. In this case, offset adjustment is required at the VR1, so that the dynamic range of the analog input signal can be set to a value between 0V to –2V by monitoring the V_{IN} pin.

[DIR IN. Input] (CON2)

When the input supplied to the sample-and-hold is a recurring signal (sine wave, etc.) without offset, it is added using the AC coupled input from CON2 by connecting a 10kΩ resistor to side A and a 0.1µF capacitor to side B of the S1 selector. In this case, offset adjustment is required at the VR1, so that the dynamic range of the analog input signal can be set to a value between 0V to –2V by monitoring the V_{IN} pin.

						S1 setting	
Item	Min.	Typ.	Max.	Amplitude	Unit	A	B
V_{IN} input (CON1)	–0.9		1.0	1.0	V	short	open
DIR. IN input (CON2)	–2.0	0	2.0	2.0	V	10kΩ	0.1µF

(CON1 and CON2 are terminated to AGND at 50Ω on the board.)

3. Clock input (CON4)

TTL compatible
Use in the 30 to 70% CLK duty range
(CON4 is terminated to DGND at 50Ω on the board.)

4. Digital output (CON5)

TTL compatible
C-MOS (ACT series) output

5. D/A out (CON3) and full-scale adjustment (VR2)

The output waveforms of the D/A converter are output from CON3. When an oscilloscope or other such instrument is used for monitoring, a 50Ω terminating resistor is required. The full-scale output voltage must also be adjusted. And the output amplitude should also be adjusted to 1Vp-p by the VR2.

Item	Min.	Typ.	Max.	Unit
D/A OUT	–1.0		0	V

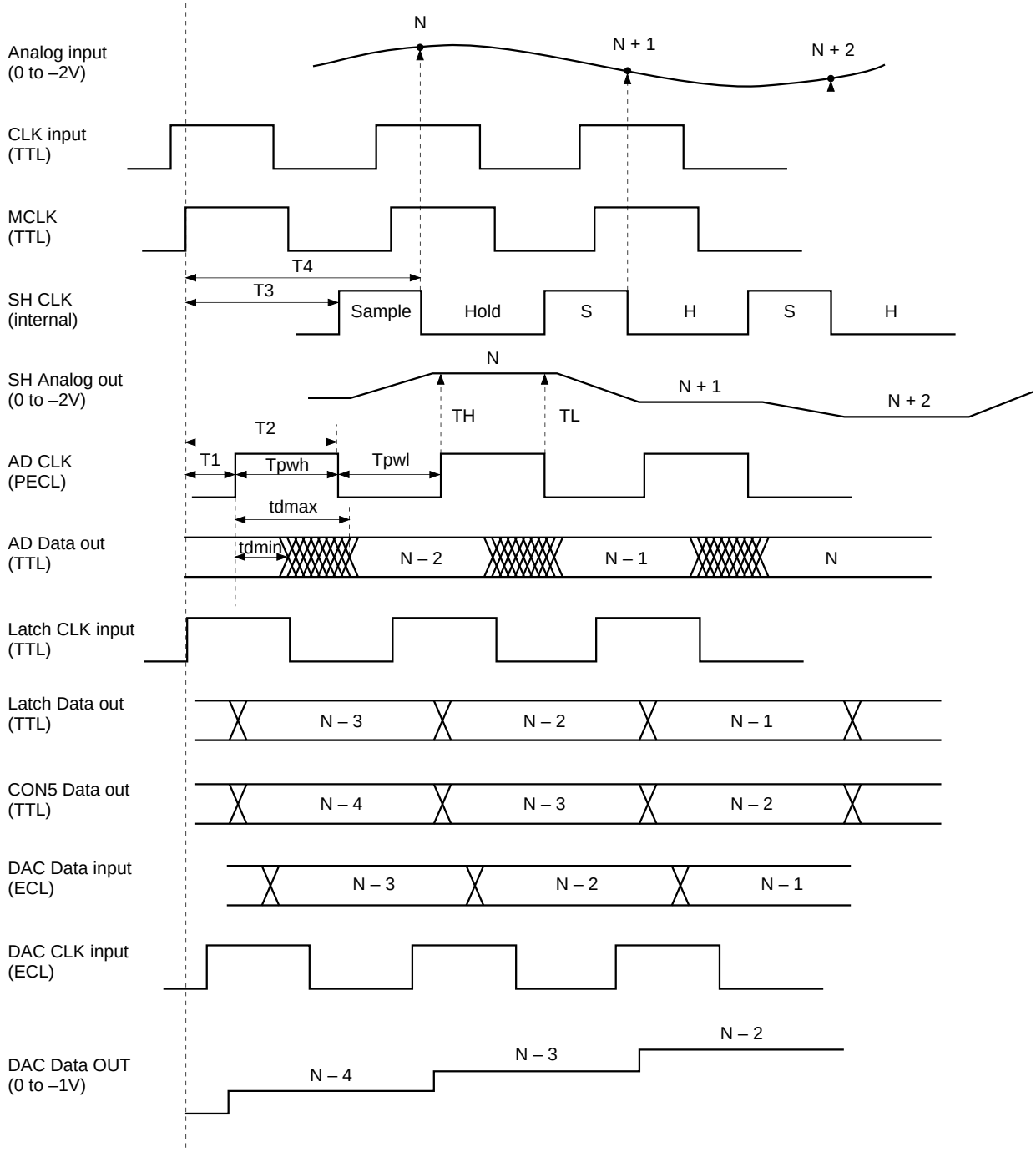
6. SW1 setting

These are the switches for PS, ENABLE, MINV, and LINV of the A/D converter and the DAINV of the D/A converter. Normally all are used ON.

7. S2 setting

This is the selection of the frequency division ratio for the clock which is supplied to the D/A converter. Normally, 1/1 is used but the ratios from 1/2 to 1/16 are also used for the envelope test or other tests.

CXA1843Q + CXA1844Q PCB Timing Chart



Item	Symbol	Min.	Typ.	Max.	Unit
S/H CLK delay	T3		20		ns
	T4		33		ns
A/D CLK delay	T1		6		ns
	T2		20		ns
A/D CLK width	tpwh	14			ns
	tpwl	13			ns
A/D output data delay	td	4		18	ns

S/H + A/D Evaluation Board Parts List

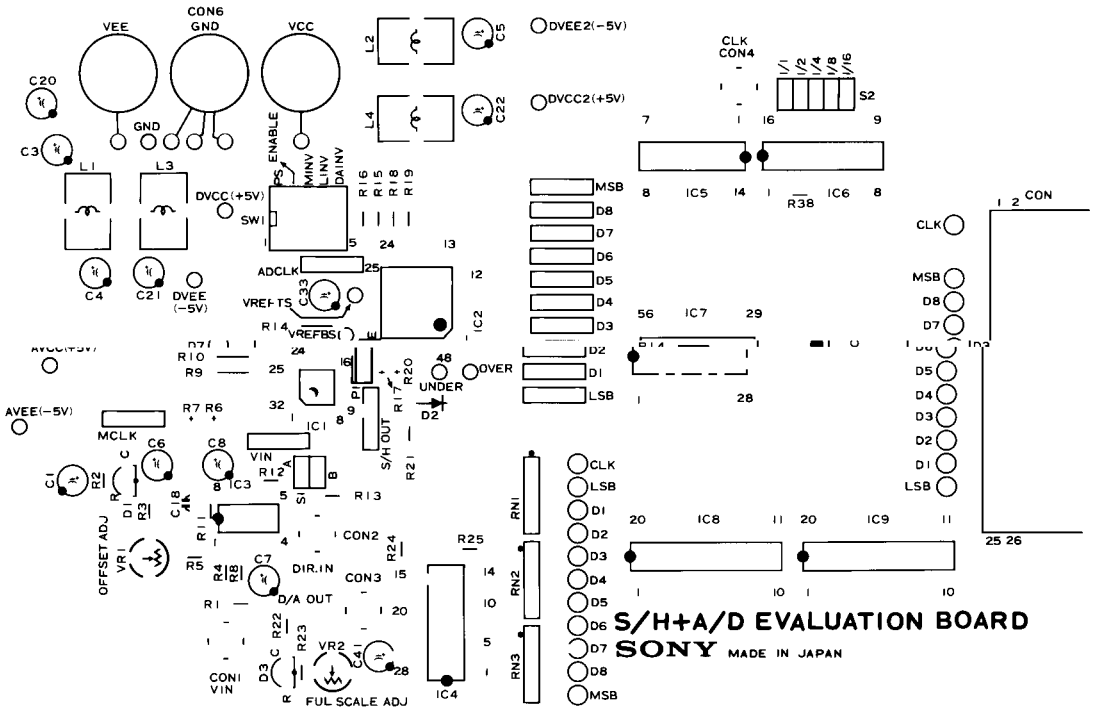
(No.)	(Product Name)	(Function)	(No.)	(Product Name)	(Function)
IC.1	CXA1843Q	Sample Hold	R1, 13, 38	FRD-25SR (0.25W)	51Ω
IC.2	CXA1844Q	10bit ADC	R21, 25	FRD-25SR (0.25W)	100Ω
IC.3	CLC505	OP-AMP	R2, 22	FRD-25SR (0.25W)	270Ω
IC.4	CX20201A-1	DAC	R3, 4	FRD-25SR (0.25W)	470Ω
IC.5	74ACT34	Buffer	R23	FRD-25SR (0.25W)	1kΩ
IC.6	74ACT163	Counter	R12	FRD-25SR (0.25W)	4.7kΩ
IC.7	74ACT16821	Latch	R5, 8, 15, 16, 18, 19	FRD-25SR (0.25W)	10kΩ
IC.8, 9	MB767	ECL → TTL level translator	R24	FRD-25SR (0.25W)	51kΩ
D1, 3	TL431CP	3-pin shunt regulator	R11	FRD-25SR (0.25W)	150kΩ
D2	1S1555	Diode	R9	SN14C2F	1.5kΩ
P1	2SA1175	PNP transistor	R14	SN14C2F	1.6kΩ
SW.1	DSS-105	Switch	R10	SN14C2F	2.7kΩ
CON.1 to 4	TMA5502-10	SMA connector	R6, 7, 17, 20	Chip resistor	
CON.5	FAP-2601-1201	Flat cable connector	RN1 to 3	RGLD 4X621J	620Ω
CON.6	TJ-563	Power supply connector	C2, 9 to 17, 19, 23 to 32	Chip capacitor	0.1µF
S1.3	JX-1	Short-pin	34 to 40, 42 to 60		
VR1.2	RJ-6P	2kΩ volume resistor	C1, 6 to 8, 33, 41	Tantalum capacitor	1µF (Voltage proof of 35V)
C1 to 11	LS-2S	Check pin	C3 to 5, 20 to 22		33µF (Voltage proof of 35V)
			C18	Ceramic capacitor	100pF
			L1 to 4	SF-T5-30-03	30µF

Precautions

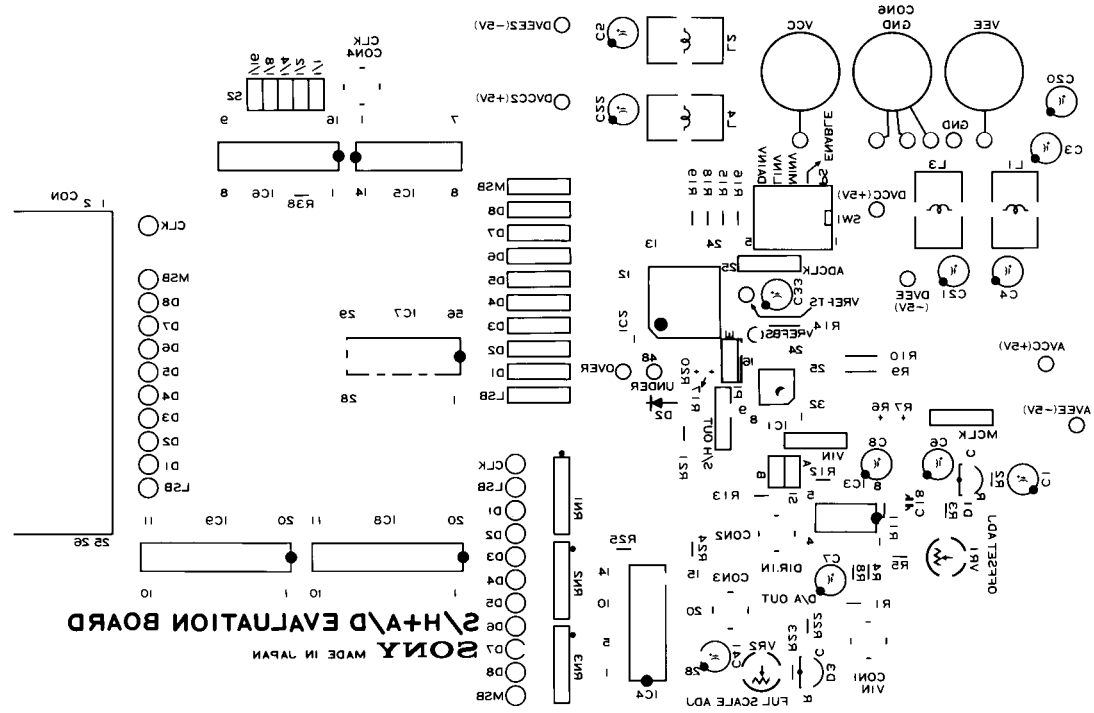
1. The monitoring pins are designed to be easily grounded in order to minimize distortions occurring when monitoring waveforms on an oscilloscope. Waveform monitoring is facilitated by using the grounded tip (part No. 013-1185-00) made by Tektronix at the end of the probe.

2. VR1 and VR2 are optimally adjusted and set before the board is shipped.

3. REX2, REX3, REX4 (R14, R10, R9) on the board use metal-oxide resistor, and T2, T3, T4 are optimally adjusted and set within the range of 1MHz to 33MHz.

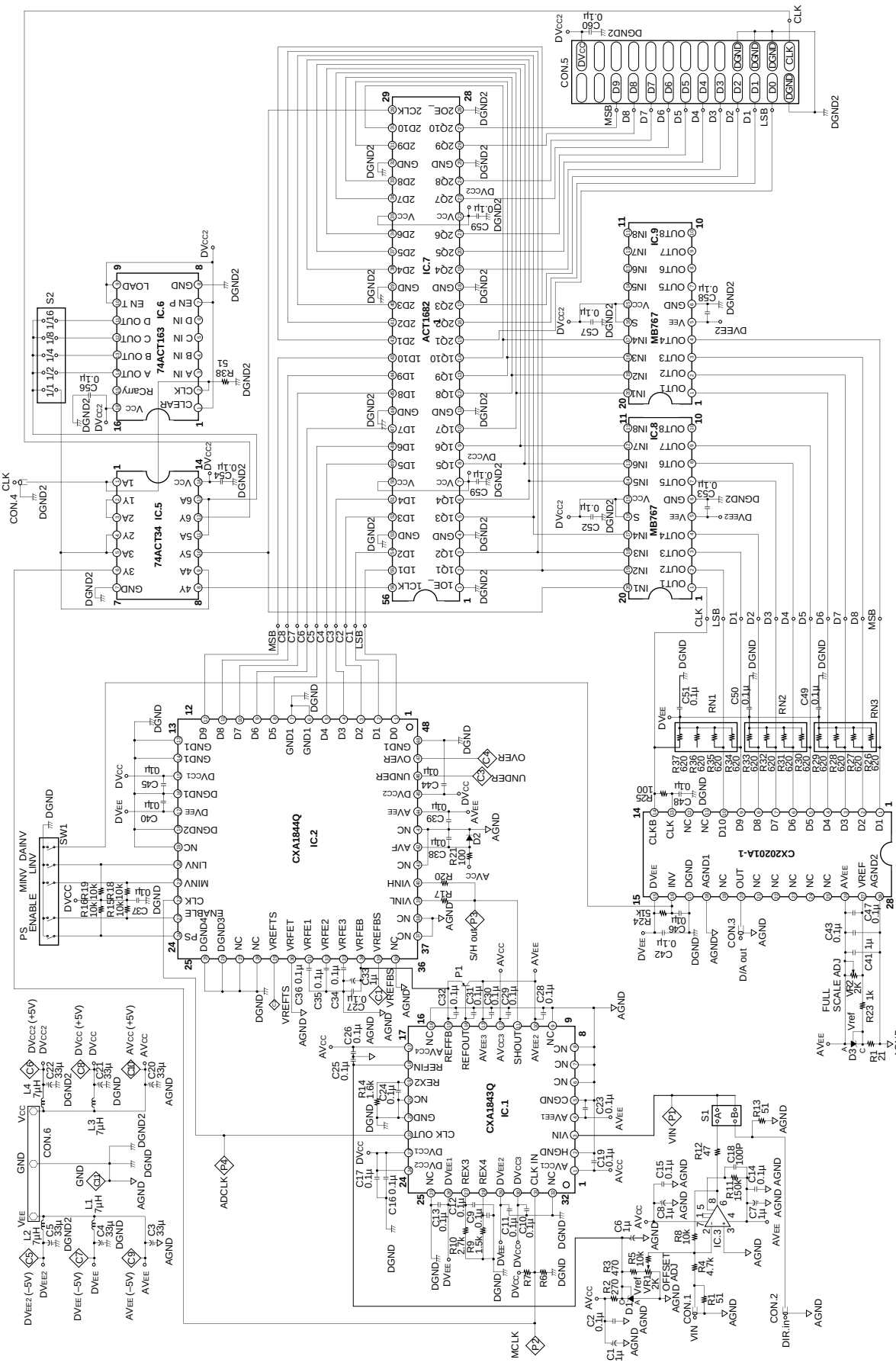


S/H + A/D EVALUATION BOARD (Component Side)



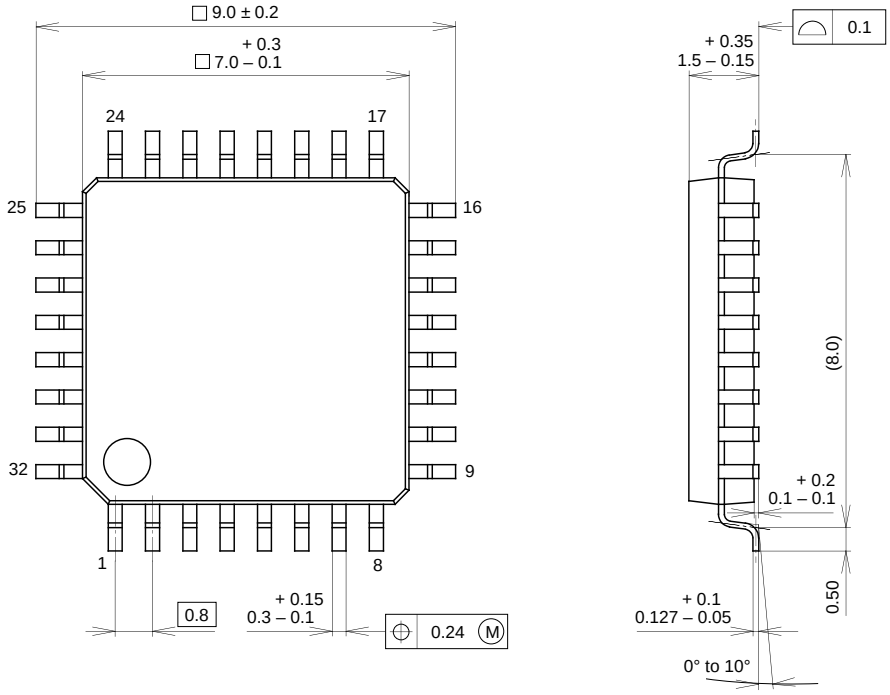
S/H + A/D EVALUATION BOARD (Solder Side)

S/H + A/D Evaluation Board



Package Outline Unit: mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g