

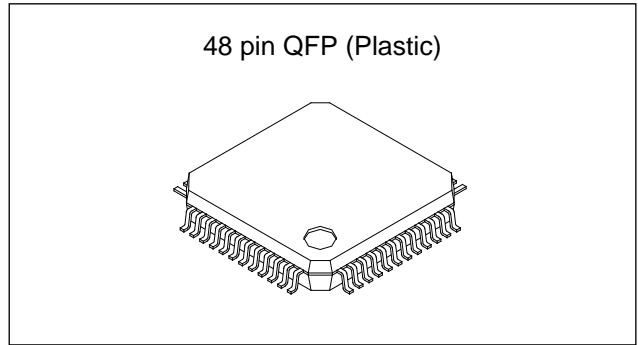
6-bit 140MSPS Flash A/D Converter

Description

The CXA1866Q is a 6-bit ultra-high-speed flash A/D converter IC capable of digitizing analog signals at the maximum rate of 140MSPS. The digital input level is compatible with ECL 100K/10KH/10K.

Features

- Ultra-high-speed operation with maximum conversion rate of 140MSPS
- Low input capacitance: 7pF
- Wide analog input bandwidth: 210MHz
- Low power consumption: 325mW
- Low error rate
- Excellent temperature characteristics
- 1 : 2 demultiplexed output (TTL level)



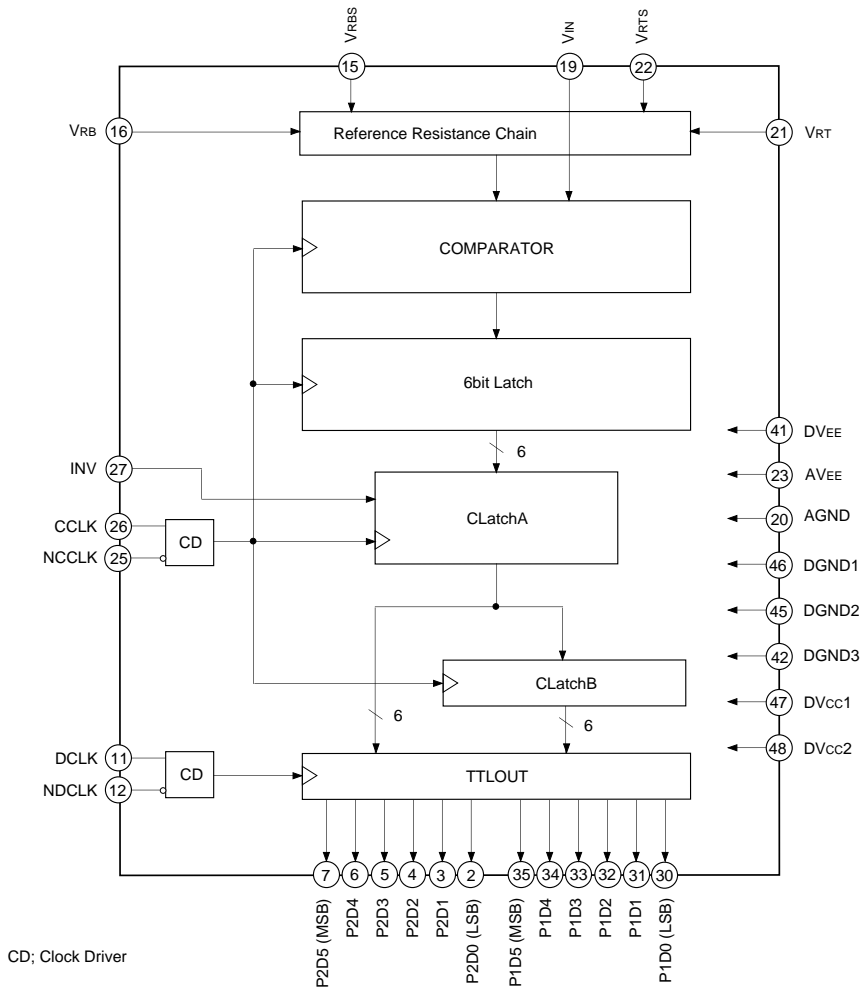
Structure

Bipolar silicon monolithic IC

Applications

- Magnetic recording (PRML)
- Communications (QPSK, QAM)
- Liquid crystal display

Block Diagram



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**Absolute Maximum Ratings** (Ta = 25°C)

• Supply voltage	AV <sub>EE</sub> , DV <sub>EE</sub>	-7.0 to +0.5	V
	DV <sub>CC</sub> *1	0.5 to +7.0	V
• Analog input voltage	V <sub>IN</sub>	-2.7 to +0.5	V
• Reference input voltage	V <sub>RT</sub> , V <sub>RB</sub>	-2.7 to +0.5	V
	V <sub>RT</sub> - V <sub>RB</sub>	2.5	V
• Digital input voltage	D <sub>IN</sub> *2	-4.0 to +0.5	V
	CCLK - NCCLK  ,   DCLK - NDCLK	2.5	V
• Digital output current	ID <sub>0</sub> to ID <sub>6</sub>	-30 to +30	mA
• Storage temperature	T <sub>stg</sub>	-65 to +150	°C
• Ambient operating temperature	T <sub>a</sub>	-20 to +75	°C
• Allowable power dissipation	P <sub>D</sub>	750	mW

**Recommended Operating Conditions**

		Min.	Typ.	Max.	
• Supply voltage	AV <sub>EE</sub> , DV <sub>EE</sub>	-5.5	-5.2	-4.75	V
	AV <sub>EE</sub> - DV <sub>EE</sub>	-0.05	0	0.05	V
	AGND - DGND*3	-0.05	0	0.05	V
	DV <sub>CC</sub> *1	4.75	5.0	5.25	V
• Reference input voltage	V <sub>RT</sub>	-0.1	0	0.1	V
	V <sub>RB</sub>	-2.2	-2.0	-0.8	V
• Analog input voltage	V <sub>IN</sub>	V <sub>RB</sub>		V <sub>RT</sub>	
• Digital input voltage	D <sub>IN</sub> (H)	-1.1			V
	D <sub>IN</sub> (L)			-1.5	V
• CCLK, NCCLK frequency	F <sub>cclk</sub>			140	MHz
• DCLK, NDCLK frequency	F <sub>dclk</sub>			70	MHz
• CCLK, NCCLK duty	D <sub>cclk</sub>	40	50	60	%
• DCLK, NDCLK duty	D <sub>dclk</sub>	40	50	60	%
• CCLK-DCLK time difference*4	tdcd	-T <sub>PWL</sub> + 2	0	T <sub>PWH</sub> + 1	ns
• Operating temperature	T <sub>a</sub>	-20		+75	°C

\*1 DV<sub>CC</sub> = DV<sub>CC1</sub>, DV<sub>CC2</sub>

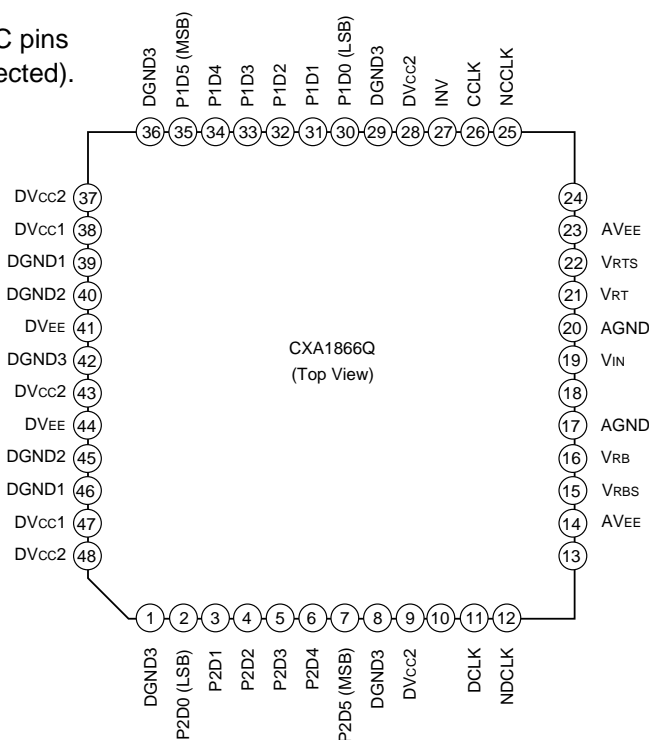
\*3 DGND = DGND1, DGND2, DGND3

\*2 D<sub>IN</sub> = CCLK, NCCLK, DCLK, NDCLK, INV

\*4 Refer to the Timing Chart 1 for T<sub>PWL</sub>, T<sub>PWH</sub>.

**Pin Configuration.**

Pins without names are NC pins  
(not connected).



Pin Description and I/O Pin Equivalent Circuit

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
21	V <sub>RT</sub>	I	0V		Top reference voltage input (= 0V). This is the top reference voltage supplied to the internal resistance chain. The external input can be set in accordance with the peak value on the plus side of the input analog signal amplitude.
22	V <sub>RTS</sub>	O	0V		V <sub>RT</sub> sense output. This is the voltage sense pin for V <sub>RT</sub> .
16	V <sub>RB</sub>	I	-2V		Bottom reference voltage input (= -2V). This is the bottom reference voltage supplied to the internal resistance chain. The external input can be set in accordance with the peak value on the minus side of the input analog signal amplitude.
15	V <sub>RBS</sub>	O	-2V		V <sub>RB</sub> sense output. This is the voltage sense pin for V <sub>RB</sub> .
19	V <sub>IN</sub>	I	V <sub>RTS</sub> to V <sub>RBS</sub>		Analog input. The input range is 2Vp-p.
26	CCLK	I	ECL		CCLK clock input. This is the conversion clock, and is an ECL level input.
25	NCCLK	I	ECL		CCLK inversion clock input. This is an ECL level input. When left open, this input goes to the ECL threshold potential (-1.3V). Only CCLK input can be used for operation with the NCCLK input left open, but complementary input is recommended to attain fast and stable operation.
11	DCLK	I	ECL		DCLK clock input. This is the 1:2 DMPX latch clock; input a clock of 1/2 frequency of CCLK. Data are output from DMPX port 1 and port 2 synchronously with the rising edge of this signal. This is an ECL level input.
12	NDCLK	I	ECL		DCLK inversion clock input. This is an ECL level input. When left open, this input goes to the ECL threshold potential (-1.3V). Only DCLK input can be used for operation with the NDCLK input left open, but complementary input is recommended to attain fast and stable operation.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
27	INV	I	ECL		<p>Digital output polarity inversion input. This is an ECL level input. This input inverts the polarity of the digital outputs P1D0 to P1D5, and P2D0 to P2D5. (Refer to the Output Code Table.)</p> <p>When left open, this signal is maintained at the low level.</p>
30	P1D0	O	TTL		<p>These pins are for the 6 bits of digital output data for DMPX port 1. P2D5 is the MSB, and P2D0 is the LSB. These are TTL level outputs.</p>
31	P1D1				<p>These pins are for the 6 bits of digital output data for DMPX port 2. P2D5 is the MSB, and P2D0 is the LSB. These are TTL level outputs.</p>
32	P1D2				
33	P1D3				
34	P1D4				
35	P1D5				
2	P2D0				
3	P2D1				
4	P2D2				
5	P2D3				
6	P2D4				
7	P2D5				
38, 47	DVcc1	—	+5.0V		+5V power supply for TTL level internal circuit.
9, 28, 37, 43, 48	DVcc2	—	+5.0V		+5V power supply for TTL level output buffers (P1D0 to P2D5).
39, 46	DGND1	—	0V		Ground for DVEE digital circuit.
40, 45	DGND2	—	0V		Ground for DVcc1 digital circuit.
1, 8, 29, 36, 42	DGND3	—	0V		Ground for DVcc2 digital circuit.
17, 20	AGND	—	0V		Ground for AVEE analog circuit . Used as the ground for the comparator input buffers, latches, etc. Separated from DGND.
41, 44	DVEE	—	-5.2V		-5.2V power supply for digital circuit. Connected internally with AVEE. (Resistance is 4 to 6Ω.)
14, 23	AVEE	—	-5.2V		-5.2V power supply for analog circuit. Connected internally with DVEE. (Resistance is 4 to 6Ω.)

**Electrical Characteristics**

(Ta = 25°C, AV<sub>EE</sub> = DV<sub>EE</sub> = -5.2V, DV<sub>CC</sub> = 5V, V<sub>RT</sub> = 0V, V<sub>RB</sub> = -2V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n			6		bits
DC characteristics						
Integral linearity error	EIL	F <sub>c</sub> = 140MHz			±0.2	LSB
Differential linearity error	EDL	F <sub>c</sub> = 140MHz			±0.2	LSB
No missing code				Guaranteed		
Analog input						
Analog input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = -1V + 0.07V <sub>rms</sub> , DC ≤ V <sub>IN</sub> ≤ 70MHz		7		pF
Analog input resistance	R <sub>IN</sub>	-2V ≤ V <sub>IN</sub> ≤ 0V	200			kΩ
Input bias current	I <sub>IN</sub>	-2V ≤ V <sub>IN</sub> ≤ 0V			110	μA
Reference input						
Reference resistance	R <sub>REF</sub>			225		Ω
Reference resistance current	I <sub>ref</sub>			9		mA
Offset voltage	V <sub>RT</sub> V <sub>RB</sub>	EOT EOB			25 25	mV mV
Digital input						
Logic high level	V <sub>IH</sub>		-1.13			V
Logic low level	V <sub>IL</sub>				-1.50	V
Logic high current	I <sub>IH</sub>	V <sub>IH</sub> = -0.8V	0		50	μA
Logic low current	I <sub>IL</sub>	V <sub>IL</sub> = -1.6V	-50		50	μA
Input capacitance				3.5		pF
Switching characteristics						
Maximum conversion frequency	F <sub>C</sub>	Error rate 1E-9 TPS*1	140			MSPS
Aperture jitter	T <sub>aj</sub>			5.0		ps
Sampling delay	T <sub>ds</sub>			1.0		ns
Digital output						
Logic high level	V <sub>OH</sub>	I <sub>OUT</sub> = -2mA	2.7			V
Logic low level	V <sub>OL</sub>	I <sub>OUT</sub> = 1mA			0.5	V
Output delay	t <sub>do</sub>	Z <sub>L</sub> = 25pF	2.0		8.0	ns
Output rising time	t <sub>r</sub>	Z <sub>L</sub> = 25pF, 0.5V to 2.4V		1.2		ns
Output falling time	t <sub>f</sub>	Z <sub>L</sub> = 25pF, 0.5V to 2.4V		1.2		ns
Dynamic characteristics						
Analog amplitude input bandwidth	F <sub>inb</sub>	V <sub>IN</sub> = 2V <sub>p-p</sub> , p-p value = 3dB down input frequency	210			MHz
S/N ratio	SNR1 SNR2 SNR3	F <sub>c</sub> = 140MHz, F <sub>in</sub> = 1MHz F <sub>c</sub> = 140MHz, F <sub>in</sub> = 35MHz F <sub>c</sub> = 140MHz, F <sub>in</sub> = 70MHz		36 34 32		dB dB dB
Error rate		F <sub>c</sub> = 140MHz, error > 4LSB		10 <sup>-9</sup>		TPS*1
Power supply						
Supply current	I <sub>CC</sub> I <sub>EE</sub>	DV <sub>CC</sub> = +5V AV <sub>EE</sub> = DV <sub>EE</sub> = -5.2V	-60	20 -40	32	mA mA
Power consumption	P <sub>d</sub>			325		mW

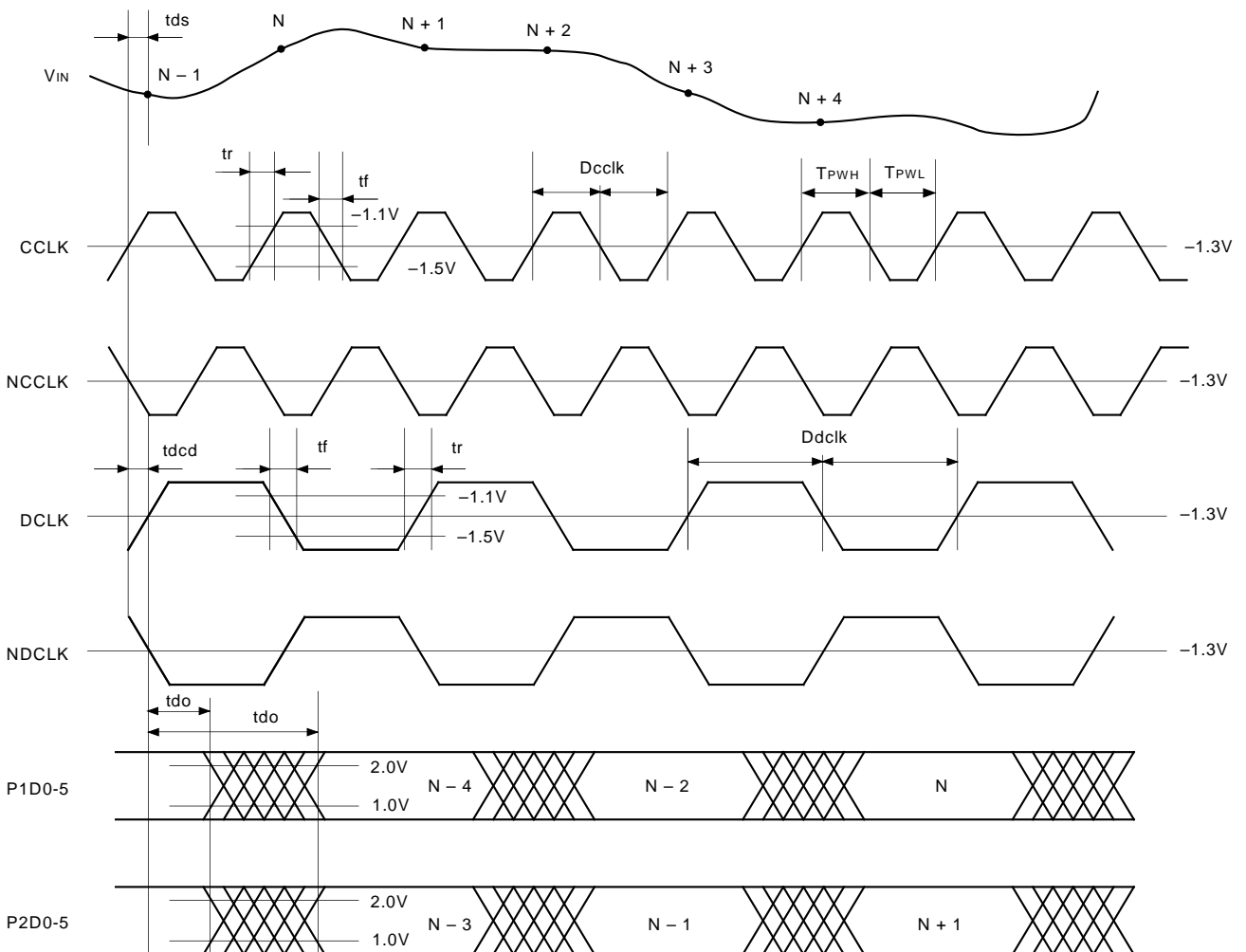
\*1 TPS: Times Per Sample

Output Code Table

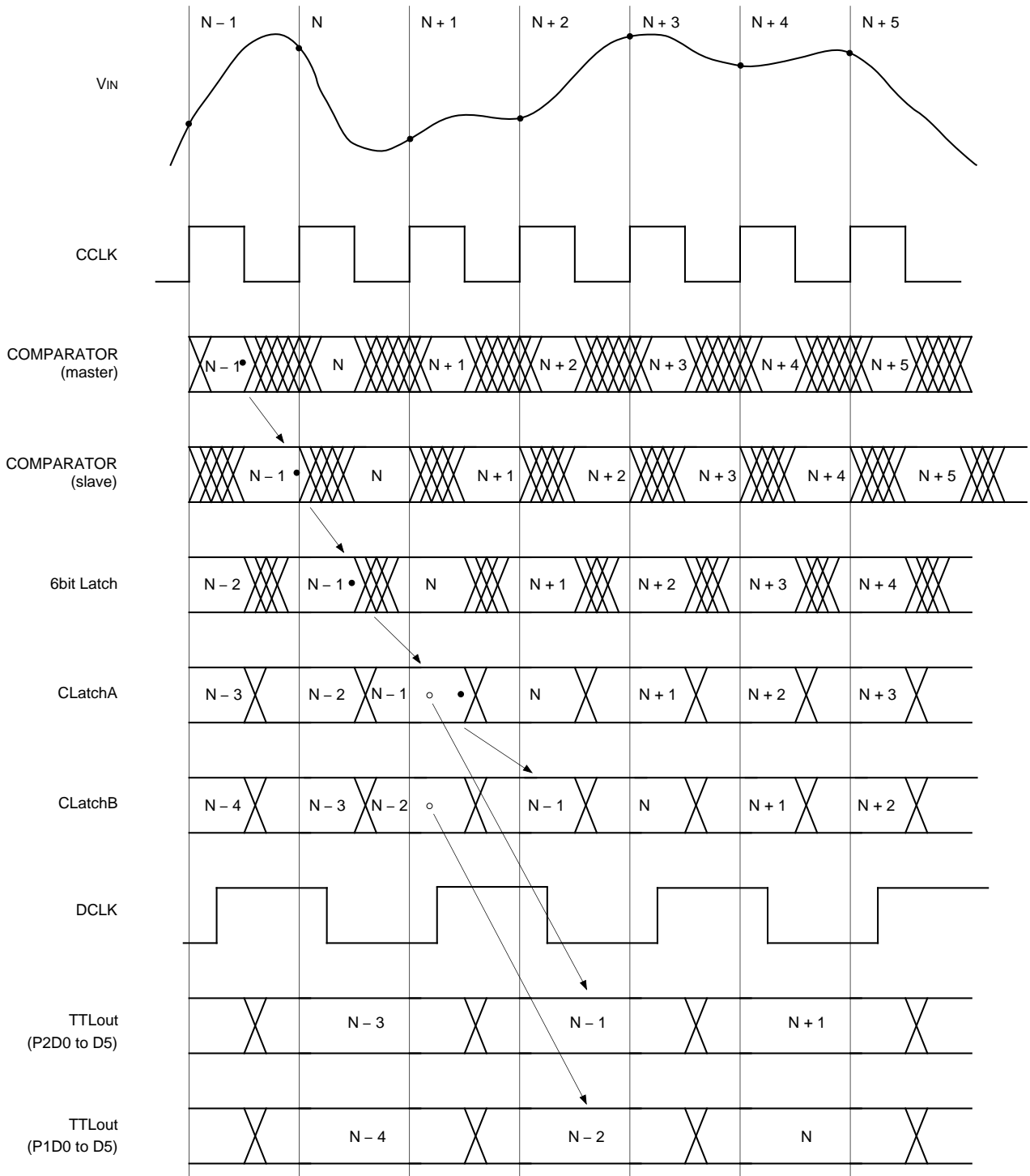
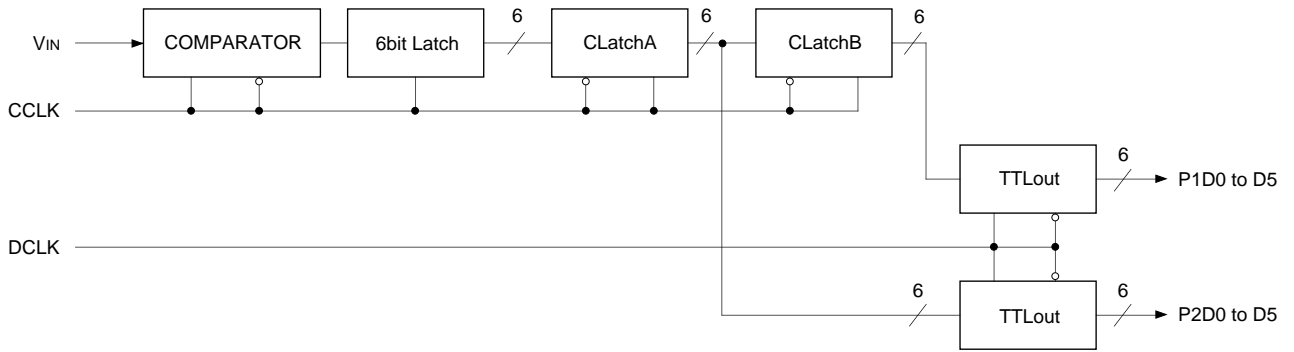
V <sub>IN</sub>	STEP	INV = 0		INV = 1	
		D5	D0	D5	D0
0V	0	000000	111111	111111	111111
	1	000001	111110	111110	111110
-1V		:	:	:	:
	31	011111	100000	100000	100000
	32	100000	011111	011111	011111
-2V		:	:	:	:
	63	111110	000001	000001	000001
		111111	000000	000000	000000

\* INV = 0: low level; INV = 1: high level

Timing Chart 1

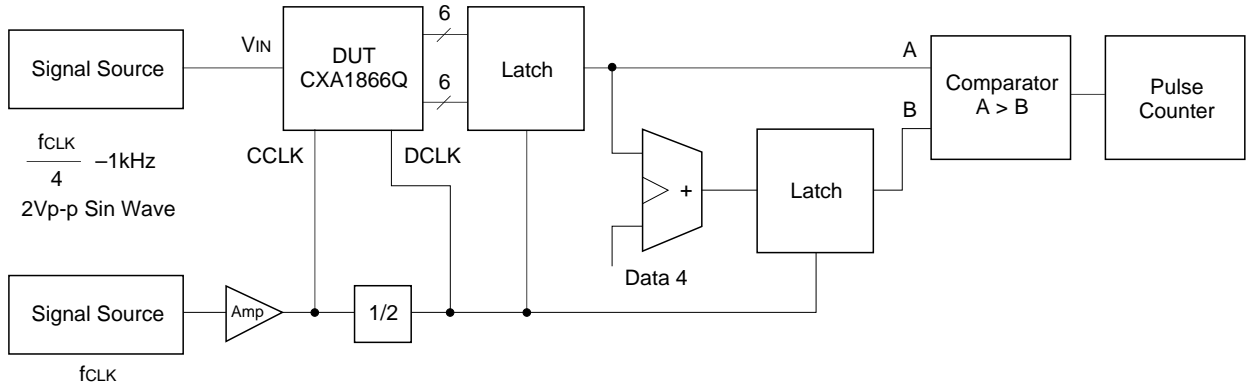


Timing Chart 2



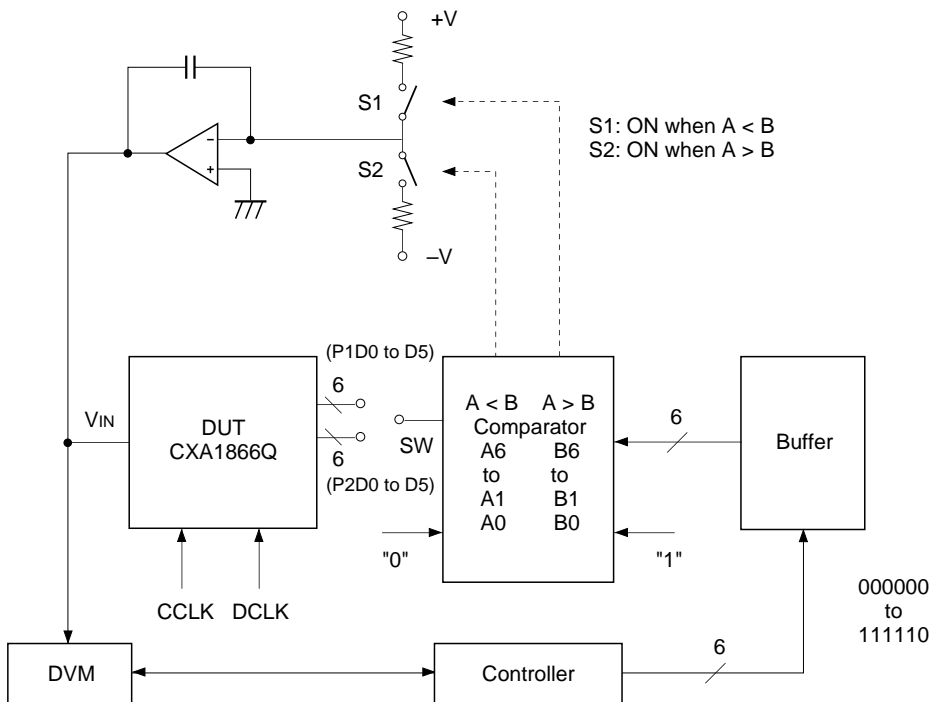
**Electrical Characteristics Measurement Circuit**

**Maximum conversion rate measurement circuit**



**Integral linearity error measurement circuit**

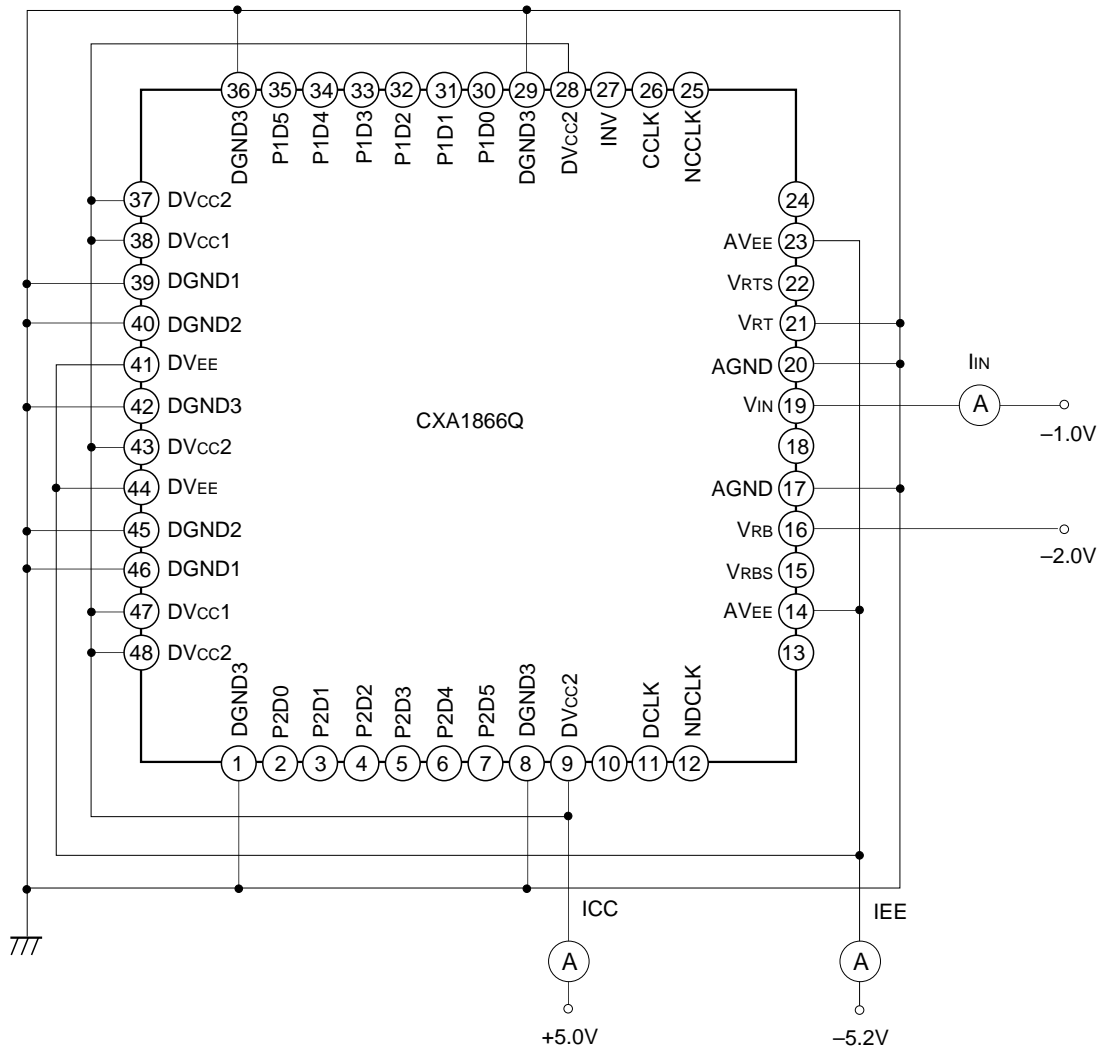
**Differential linearity error measurement circuit**





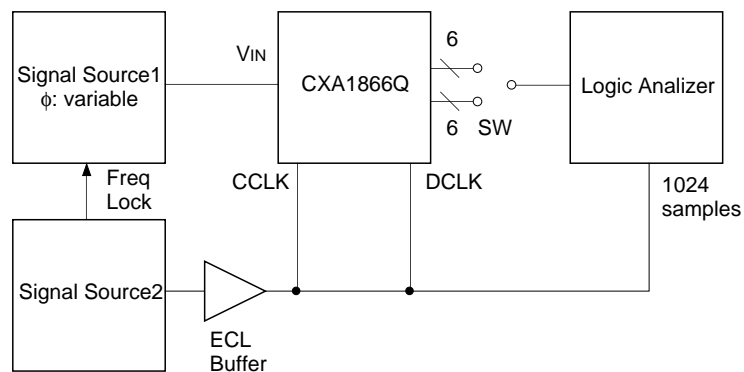
**Current consumption measurement circuit**

**Analog input bias measurement circuit**

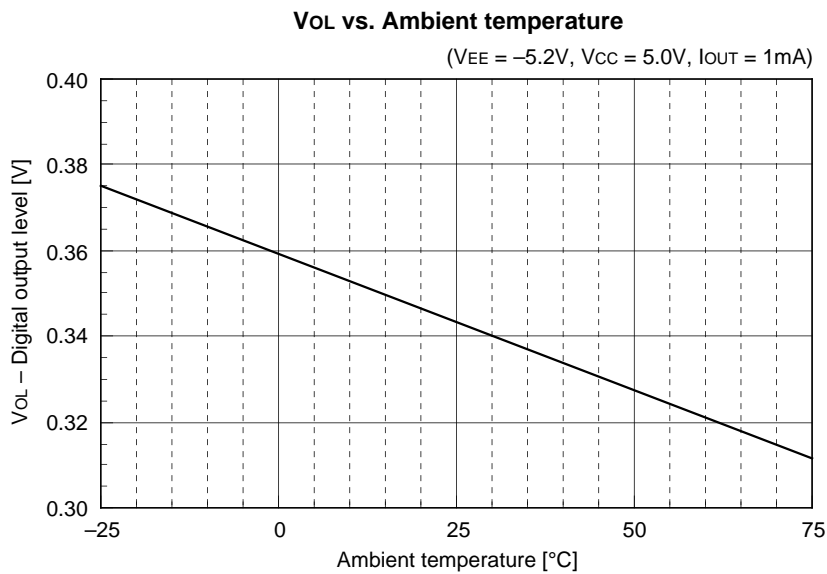
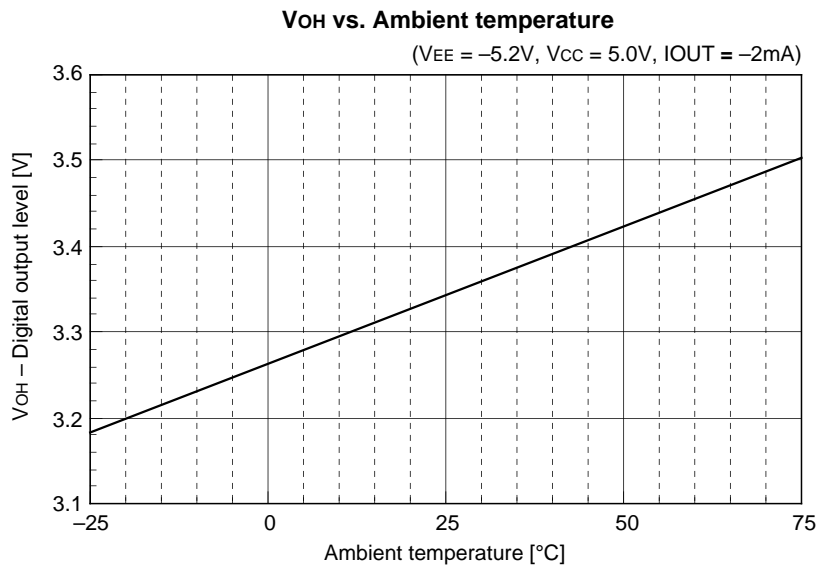
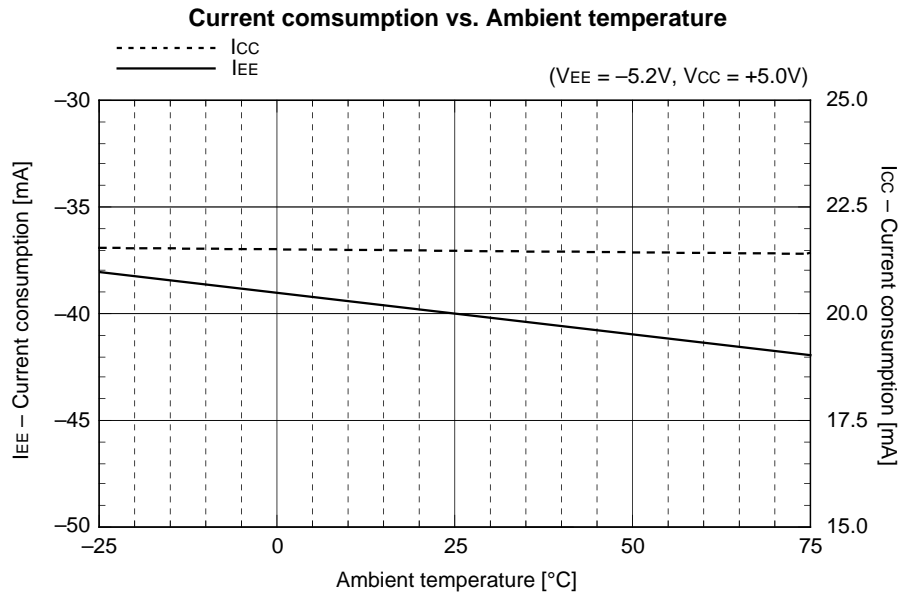


**Sampling delay measurement circuit**

**Aperture jitter measurement circuit**

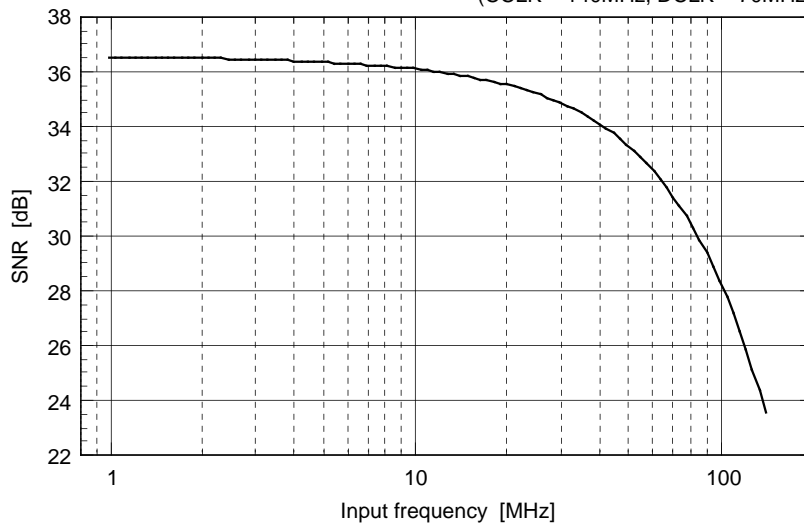


Electrical Characteristics



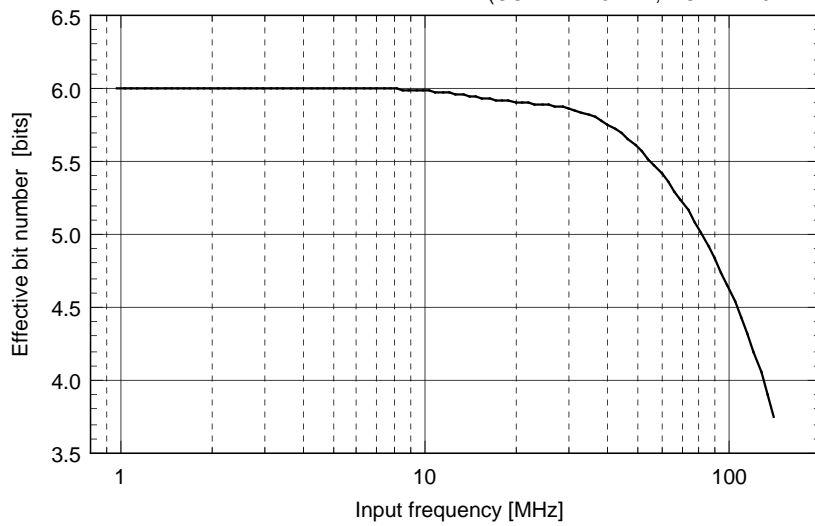
**SNR vs. Input frequency**

(CCLK = 140MHz, DCLK = 70MHz)



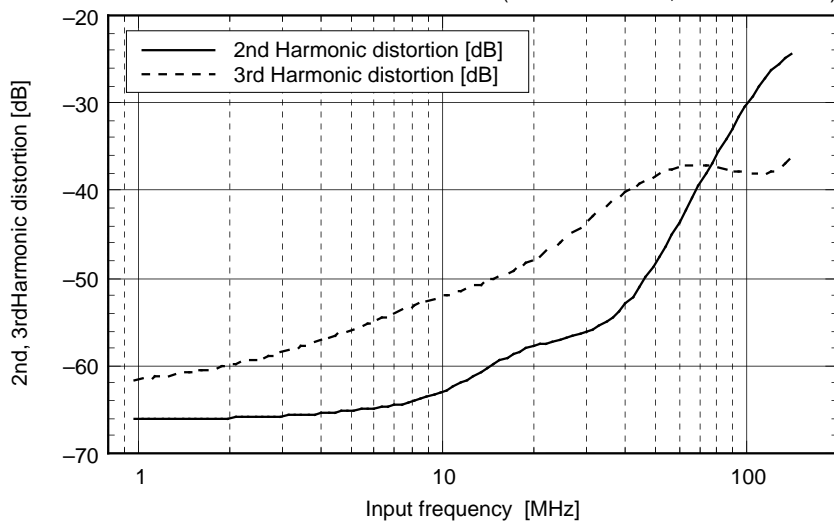
**Effective bit number vs. Input frequency**

(CCLK = 140MHz, DCLK = 70MHz)



**2nd, 3rd Harmonic distortion vs. Input frequency**

(CCLK = 140MHz, DCLK = 70MHz)



## Notes on Operation

The CXA1866Q is a high speed A/D converter with ECL level logic input and demultiplexed TTL level output. Take notice of the followings to ensure optimum performance from this IC.

### <<Power Supply and Grounding>>

- Grounding has a profound influence on converter performance. The higher the frequency is, the more important the way of grounding becomes.
- The ground pattern should be as large as possible. It is recommended to make the power supply and ground patterns wider at an inner layer using the multi-layer board.
- To prevent interference between the AGND and DGND patterns and between the  $AV_{EE}$  and  $DV_{EE}$  lines, make sure the respective patterns are separated. To prevent a DC offset in the power supply pattern, connect the  $AV_{EE}$  and  $DV_{EE}$  lines at one point each via a ferrite-bead filter. Shorting analog and digital ground patterns in one place immediately under the A/D converter improves A/D converter performance.
- Ground the power supply pins ( $AV_{EE}$ ,  $DV_{EE}$ ,  $DV_{CC}$ ) as close to each pin as possible with a  $0.1\mu\text{F}$  or larger ceramic chip capacitor. (Connect the  $AV_{EE}$  pin to the AGND pattern,  $DV_{EE}$  to DGND, and  $DV_{CC}$  to DGND.)

### <<Analog Input>>

- Make the connection between the  $V_{IN}$  pin and the analog input source as short as possible.
- There is a slight offset voltage at reference voltage pins  $V_{RT}$  and  $V_{RB}$ . If it presents no problem in the application, the voltage can be applied directly. However, if the reference voltage is to be set precisely, apply it via a feedback circuit created using the  $V_{RTS}$  and  $V_{RBS}$  pins.
- Make adequate by-pass for high frequency noise at  $V_{RT}$  and  $V_{RB}$ . The  $V_{RT}$  pin is normally connected to AGND on the board. Bypass the  $V_{RB}$  pin to the AGND pattern with a  $0.1\mu\text{F}$  or larger ceramic chip capacitor as short as possible. The  $10\mu\text{F}$  tantalum capacitor connected to  $V_{RB}$  in the Application Circuit is to stop oscillation in the reference voltage generation circuit.

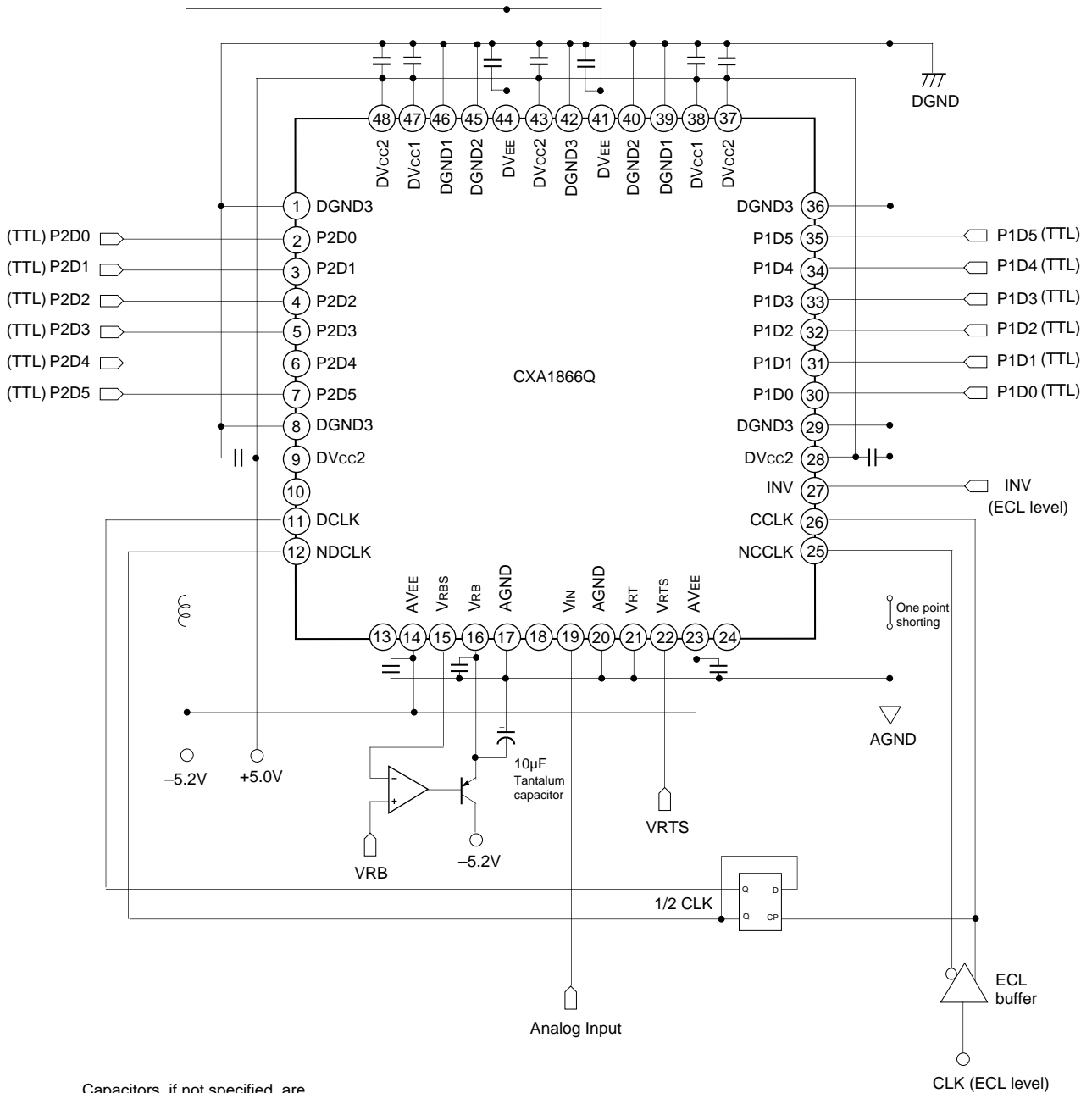
### <<Digital Input>>

- Noise at the INV pin may cause misoperation of which the cause is extremely hard to identify. If it is OK for the set voltage level to be low only, leave the pin open. If a high level voltage have to be input, bypass the INV pin to DGND with an about  $0.1\mu\text{F}$  ceramic chip capacitor as short as possible. It is recommend that high level input voltage is about  $-0.5\text{V}$  to  $-1.0\text{V}$ , and low level input voltage is about  $-1.6\text{V}$  to  $-2.5\text{V}$ . When inputting a high level voltage, avoid connecting directly to DGND.
- The CXA1866Q has input pins for two clocks: CCLK and DCLK. For CCLK, which is used for the internal comparator, input an ECL level clock with up to the maximum conversion frequency. For DCLK, which is used for the multiplex output, input an ECL level clock with a rate half that of CCLK. Take notice of the timing between CCLK and DCLK.
- It is recommended that differential signals be input to the clock input pins CCLK, NCCLK, DCLK and NDCLK. The A/D converter can be driven only by the clock input pins CCLK and DCLK, but there is a risk of unstable characteristics at maximum speeds.
- If the NCCLK and NDCLK pins are not used, bypass these pins to DGND with an about  $0.1\mu\text{F}$  capacitor. In this time, about  $-1.3\text{V}$  voltage is generated at the NCCLK and NDCLK pins. However, this is too weak to be used as threshold voltage  $V_{BB}$ ; it can not directly drive even one ECL input load.
- The clock duty cycle is designed for use at 50%. Any diversion from this percentage will have a slight effect on the maximum performance of the A/D converter, but there is no great need for adjustment.

### <<Digital Output>>

- P1D0 (LSB) to P1D5 (MSB), and P2D0 (LSB) to P2D5 (MSB) are demultiplex digital outputs (2 systems), and are output using the DCLK timing. The polarity of the output data can be inverted using the INV signal.

Application circuit



**CXA1866Q-PCB (6bit, 140MSPS, ADC Evaluation Board)****Description**

The CXA1866Q PCB is a tool for customers to evaluate the performance of the CXA1866Q (6bit, 140MHz, TTL demultiplexed output, high-speed A/D converter). In addition to indispensable features such as the reference voltage generator, this tool equips.

The input voltage offset generator, clock decimator, output data latches, 10-bit high-speed DAC  $\times$  2, and 26-pin cable connector for 2-system digital output.

This evaluation board provides full performance of the CXA1826Q and it is designed to facilitate evaluation.

**Features**

- Resolution: 6bits
- Maximum conversion rate: 140MHz
- Supply voltage: +5.0V, -5.2V
- Conversion for clock input level: Sine wave converted to ECL level signal
- Reference voltage adjustment circuit for the A/D converter
- Built-in clock frequency decimation circuit: (1/2)

**Supply Current**

Item	Min.	Typ.	Max.	Unit
V <sub>EE</sub> (-5.2V)		2.0	2.2	A
V <sub>CC</sub> (+5.0V)		0.6	0.7	A

**Analog Input**

Item	Min.	Typ.	Max.	Unit
Input voltage (AMP. IN)	-0.5		+0.5	V
(DIR. IN)	-2.0		0	V
Input impedance		50		$\Omega$

**Clock Input**

Item	Min.	Typ.	Max.	Unit
Input voltage (Peak to Peak)	0.6	1.0		Vp-p
Input impedance		50		$\Omega$

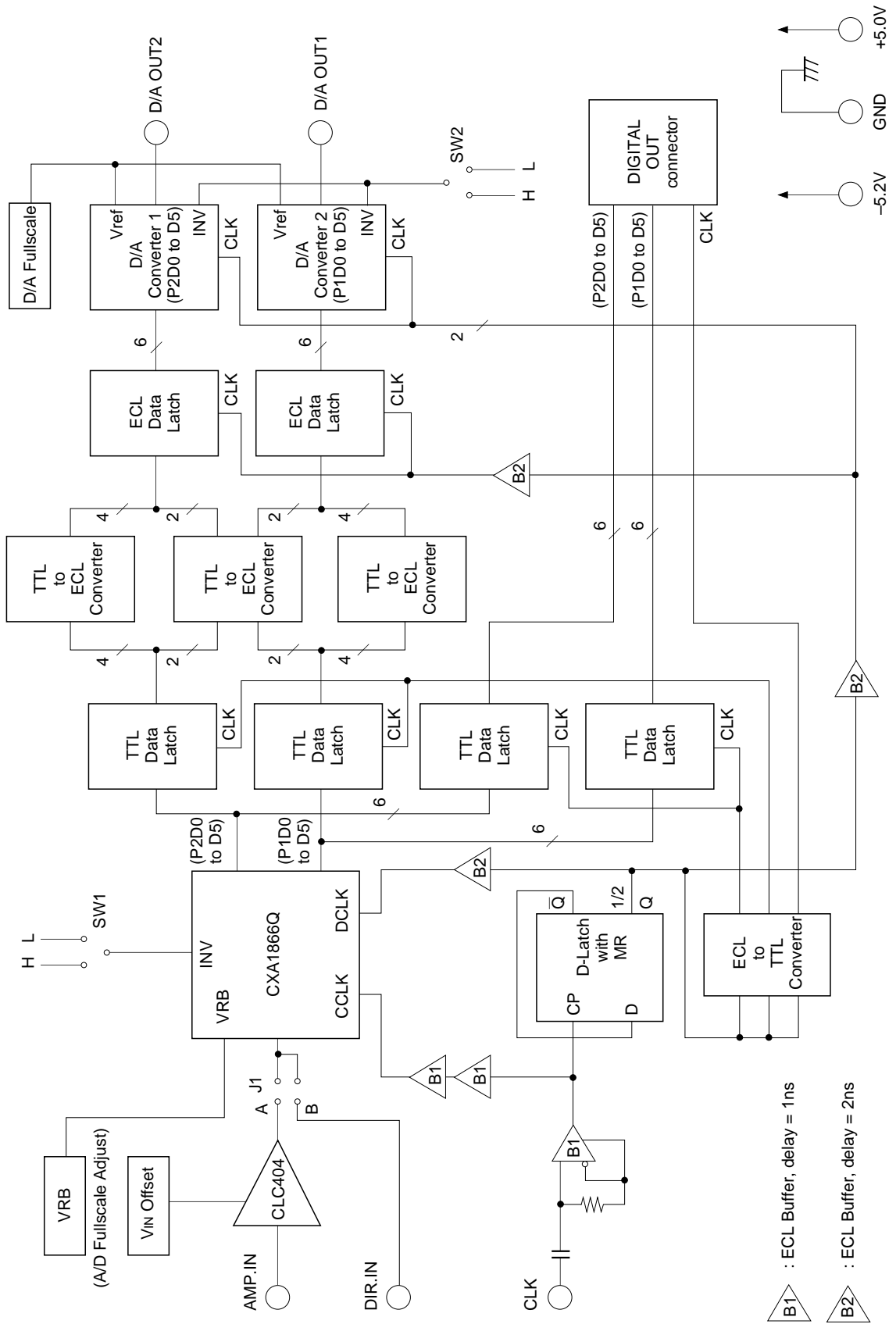
**Digital Output**

TTL level, demultiplexed output

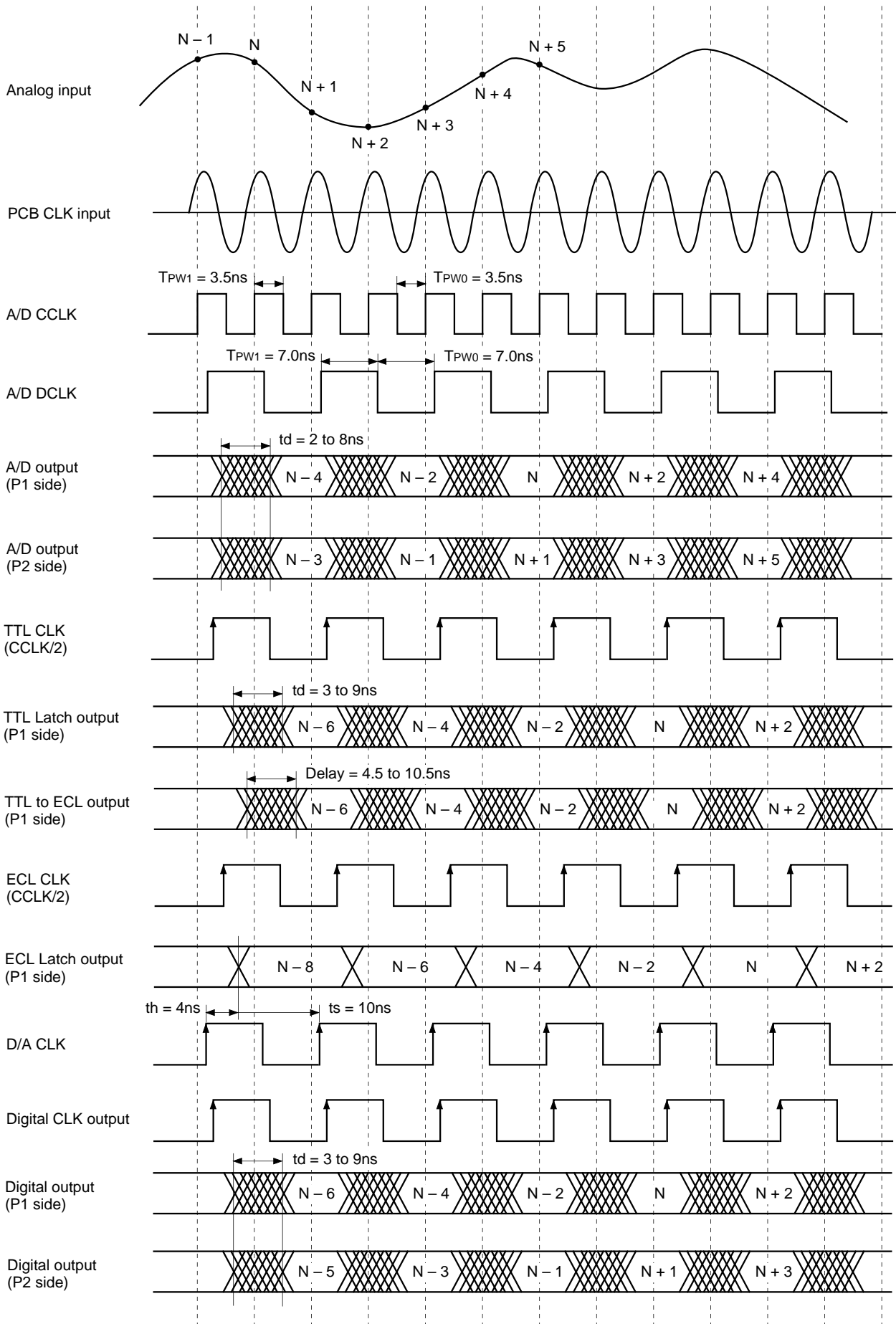
**Clock Output**

TTL level, Single output

Block Diagram



Timing Chart



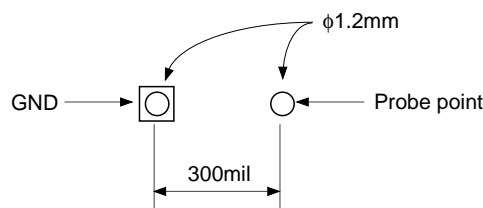


**Adjustment Methods and Notes on Operation**

- 1)  $V_{IN}$  Offset (VR1)  
The volume to adjust the AMP. IN input signal range (0V center assumed) with the A/D converter input range.
- 2) A/D Full Scale (VR2)  
The volume to adjust A/D converter VRB voltage (-2V typ.).
- 3) D/A Full Scale (VR3)  
The volume to adjust D/A converter reference voltage (-1V typ.).
- 4) Input pins  
DIR. IN .....Used to directly input to A/D converter from signal generator.  
AMP. IN.....Used to input to A/D converter after amplifying the signal generator input to that of -2 times by operational amplifier.  
CLK .....Clock input for A/D converter and peripheral ICs. Input a sine wave of 1Vp-p.
- 5) Output pins  
D/A OUT1 .....Analog output of D/A converter for (P1D0 to D5) data from A/D converter.  
D/A OUT2 .....Analog output of D/A converter for (P2D0 to D5) data from A/D converter.  
DIGITAL OUT .....Output of TTL CLK (1/4 decimation) and digital data (P1D0 to D5, P2D0 to D5).
- 6) J1 short bar is provided to use analog input pins AMP. IN and DIR. IN.

Analog input method	A	B	Offset
AMP. IN input	SHORT	OPEN	Adjust with VR1.
DIR. IN input with DC coupled	OPEN	SHORT	Input a offset signal.
DIR. IN input with AC coupled	1k $\Omega$	0.1 $\mu$ F	Adjust with VR1.

- 7) SW1 (A/D INV), SW2 (D/A INV)  
SW1: Output inversion (INV) switch of the CXA1866Q A/D converter  
SW2: Output inversion (INV) switch of the CX20201 D/A converter
- 8) Waveform probe pins P5, P6, P7, P9 and P11 through P38 are devised to facilitate GND connection in order to reduce the distortion. As shown in the diagram below, the distance between the probe point and the GND is 300 mils, and there is  $\phi$ 1.2mm throughhole at each. The signal and GND locations are suit for a Tektronix GND tip (part number 013-1185-00).



**Digital Out Connector Pin Assignment**

Pin No.	Assignment	Pin No.	Assignment
A1	P2D0	B1	GND
A2	P2D1	B2	GND
A3	P2D2	B3	GND
A4	P2D3	B4	GND
A5	P2D4	B5	GND
A6	P2D5	B6	GND
A7	P1D0	B7	GND
A8	P1D1	B8	GND
A9	P1D2	B9	GND
A10	P1D3	B10	GND
A11	P1D4	B11	GND
A12	P1D5	B12	GND
A13	CLK	B13	GND

## Part list

## RESISTOR:

R5, R6, R17, R18	51Ω
R3, 4, 15, 20, 21, 22, 24, 27	82Ω
R30, 33, 39, 41, 43, 45, 47	82Ω
R49, 51, 53, 55, 57, 59, 61	82Ω
R63, R78 to R91	82Ω
R1, 2, 14, 19, 23, 25, 26, 28	130Ω
R29, 32, 38, 40, 42, 44, 46	130Ω
R48, 50, 52, 54, 56, 58, 60	130Ω
R62, R64 to R77	130Ω
R10, R12	240Ω
R34 to R37, R93	270Ω
R31, R94	330Ω
R8	510Ω
R16	560Ω
R13, R92	1kΩ
R11	1.3kΩ
R7	11kΩ
R9	22kΩ

## VARIABLE RESISTOR:

VR1, 2, 3	2kΩ (RJ-5W202)
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## CAPACITOR:

C1	0.1μF (CERAMIC)
C5, C65, C67	3.3μF (TANTALUM)
C11, C12, C15	1μF (TANTALUM)
C68, C69	33μF (TANTALUM)
OTHER	0.1μF (CHIP CAPACITOR)

## TRANSISTOR:

Q1	2SA970
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## IC:

IC2	10H116
IC3	10H131
IC4	10116
IC5	10H125
IC6 to 9	74AS574
IC10, 11, 12	10H124
IC13, 14	10H176
IC15, 16	CX20201A
IC17, IC20	TL431CLP
IC18	CLC404AJP
IC19	TL4558P

## DIODE:

D1 to D6	1S2076A
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## FERRITE BEAD:

L1, L2, L3	ZBF253D-00
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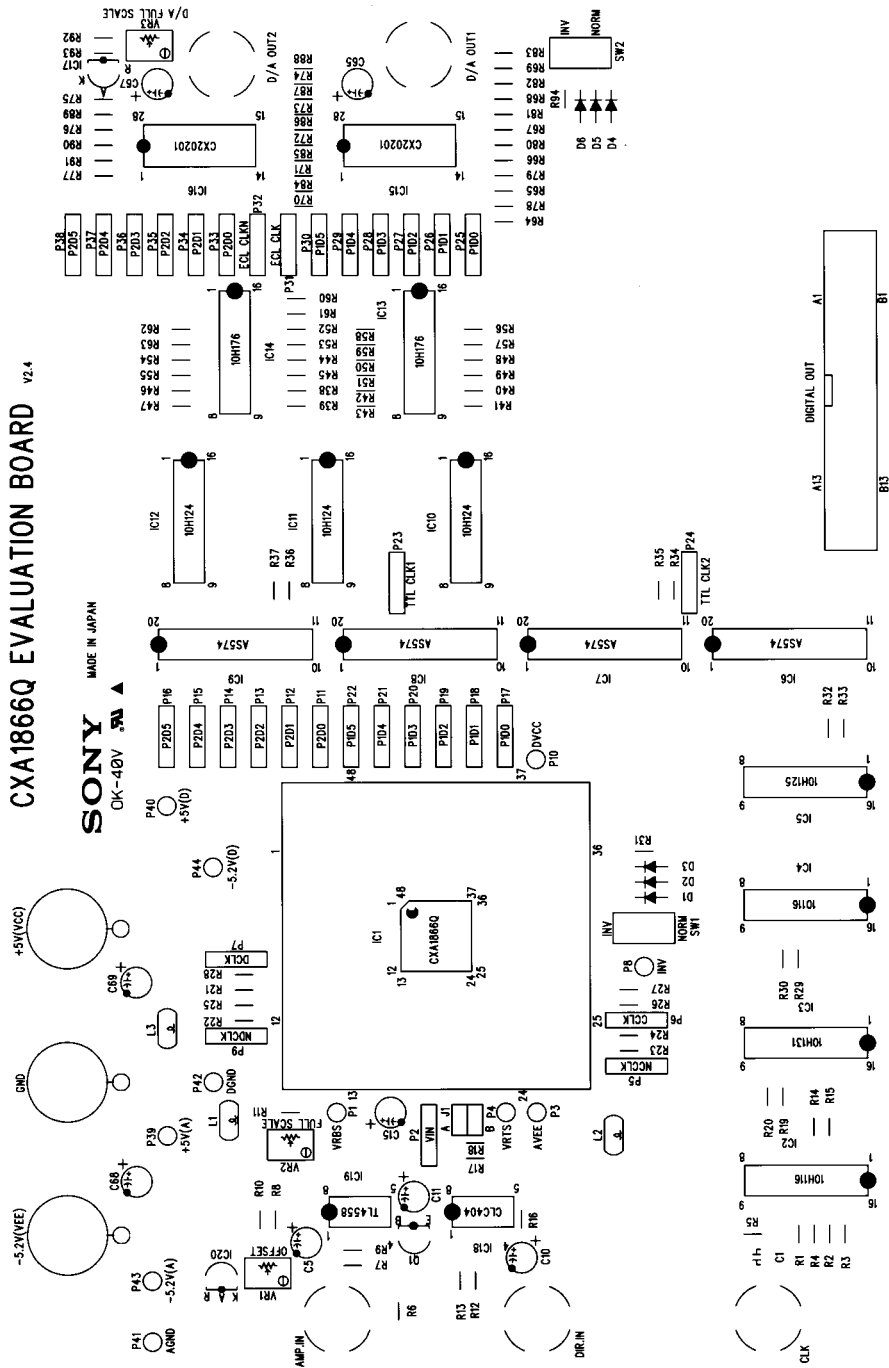
## SWITCH:

SW1, SW2	AT1D-2M3-10
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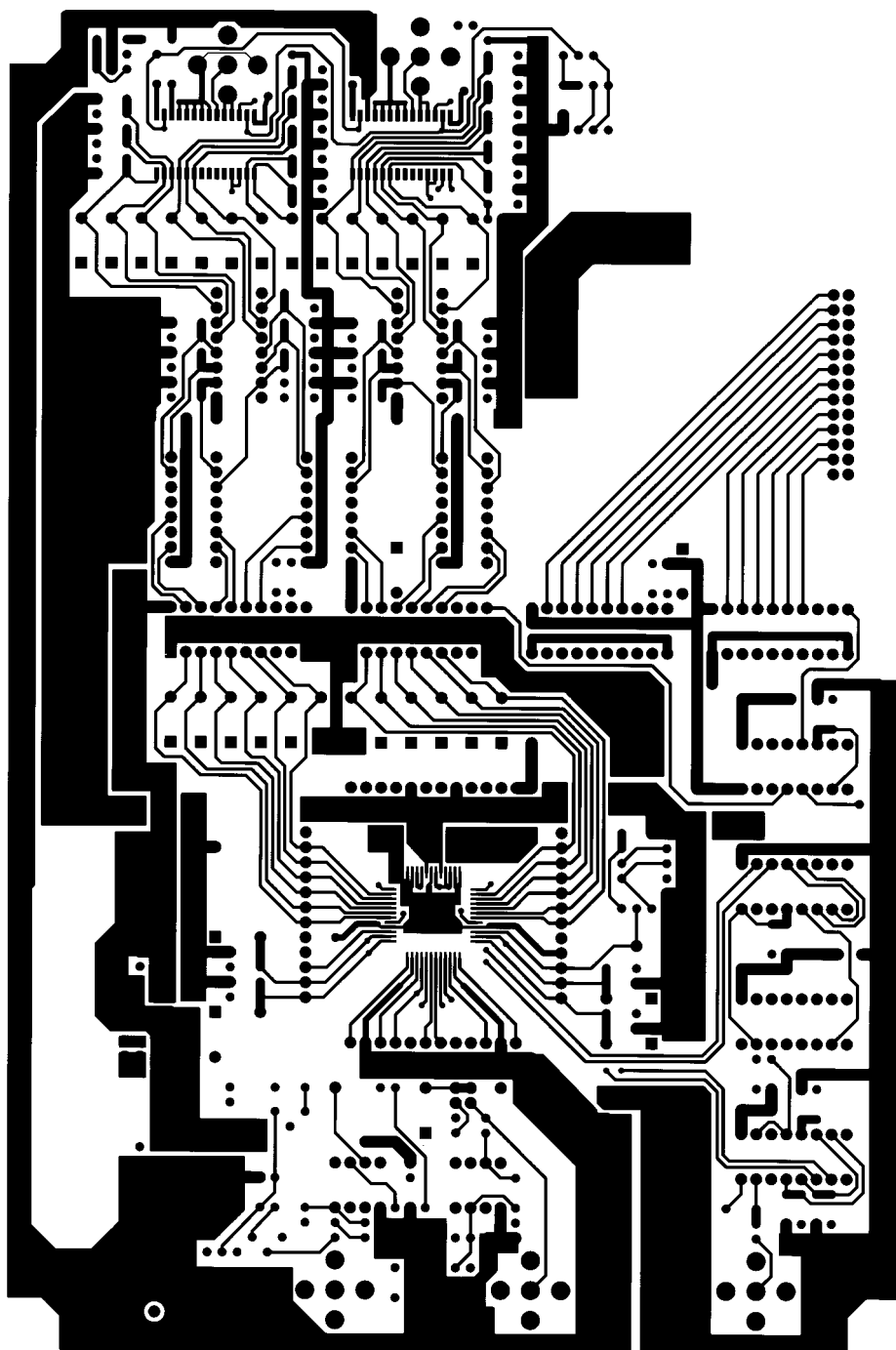
## OTHERS:

BNC CONNECTOR	BNC-R-PC
DIGITAL OUT CONNECTOR	HIF3FB-26PA-2.54DS
JUMPER LINE	JX-1

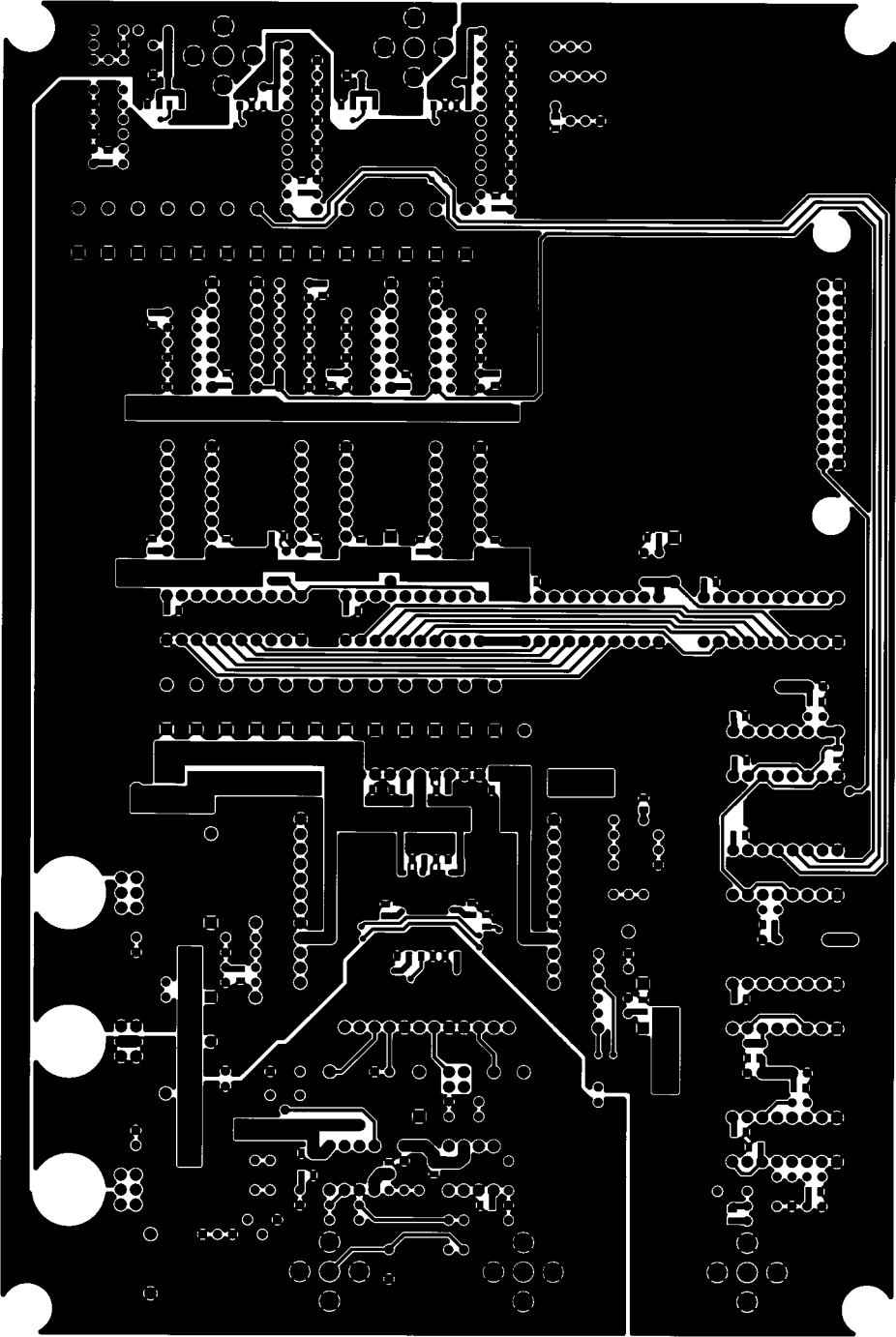
Part Layout



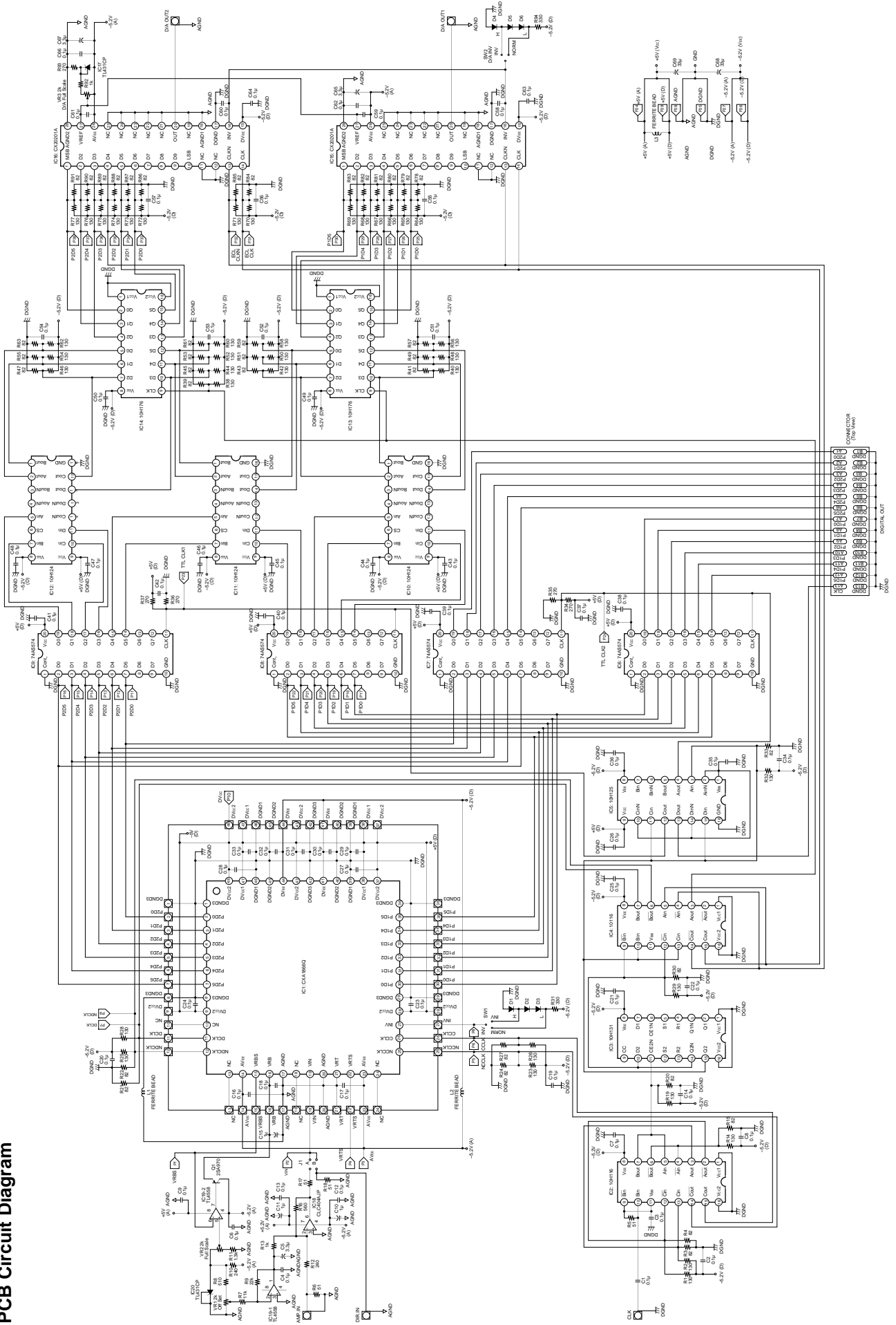
Printed Pattern (Component plane)



Printed Pattern (Solder plane)



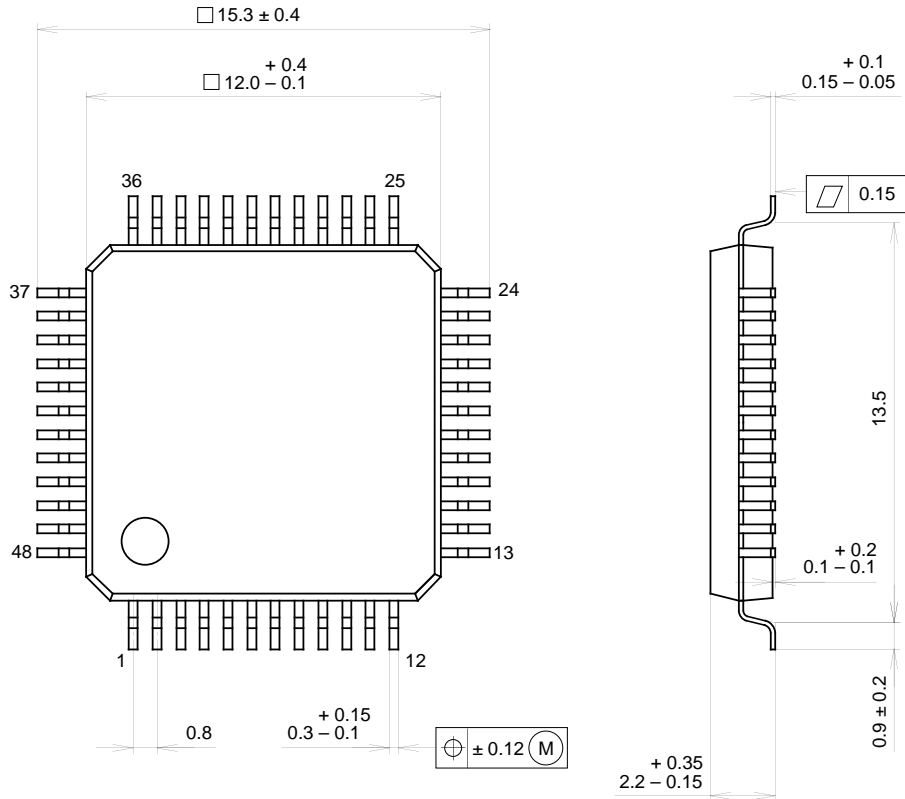
PCB Circuit Diagram



Package Outline

Unit: mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

NOTE : PALLADIUM PLATING

This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).