SONY

CXA1982Q

RF Signal Processing Servo Amplifier for CD players

For the availability of this product, please contact the sales office.

Description

The CXA1982Q is a bipolar IC with built-in RF signal processing and various servo ICs. A CD player servo can be configured by using this IC, DSP and driver.

Features

- Low operating voltage ($V_{CC} - V_{EE}$ = 2.8 to 4.0V)
- Low power consumption (36mW, V_{CC} = 3.0V)
- Supports pickup of either current output, voltage output
- Supports tracking system balance adjustment externally
- Single power supply and positive/negative dual power supplies

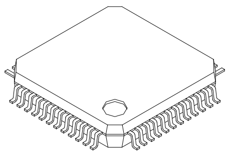
Applications

- RF I-V amplifier, RF amplifier
- Focus and tracking error amplifier
- APC circuit
- Mirror detection circuit
- Defect detection and prevention circuits
- Focus servo control
- Tracking servo control
- Sled servo control

Structure

Bipolar silicon monolithic IC

48 pin QFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

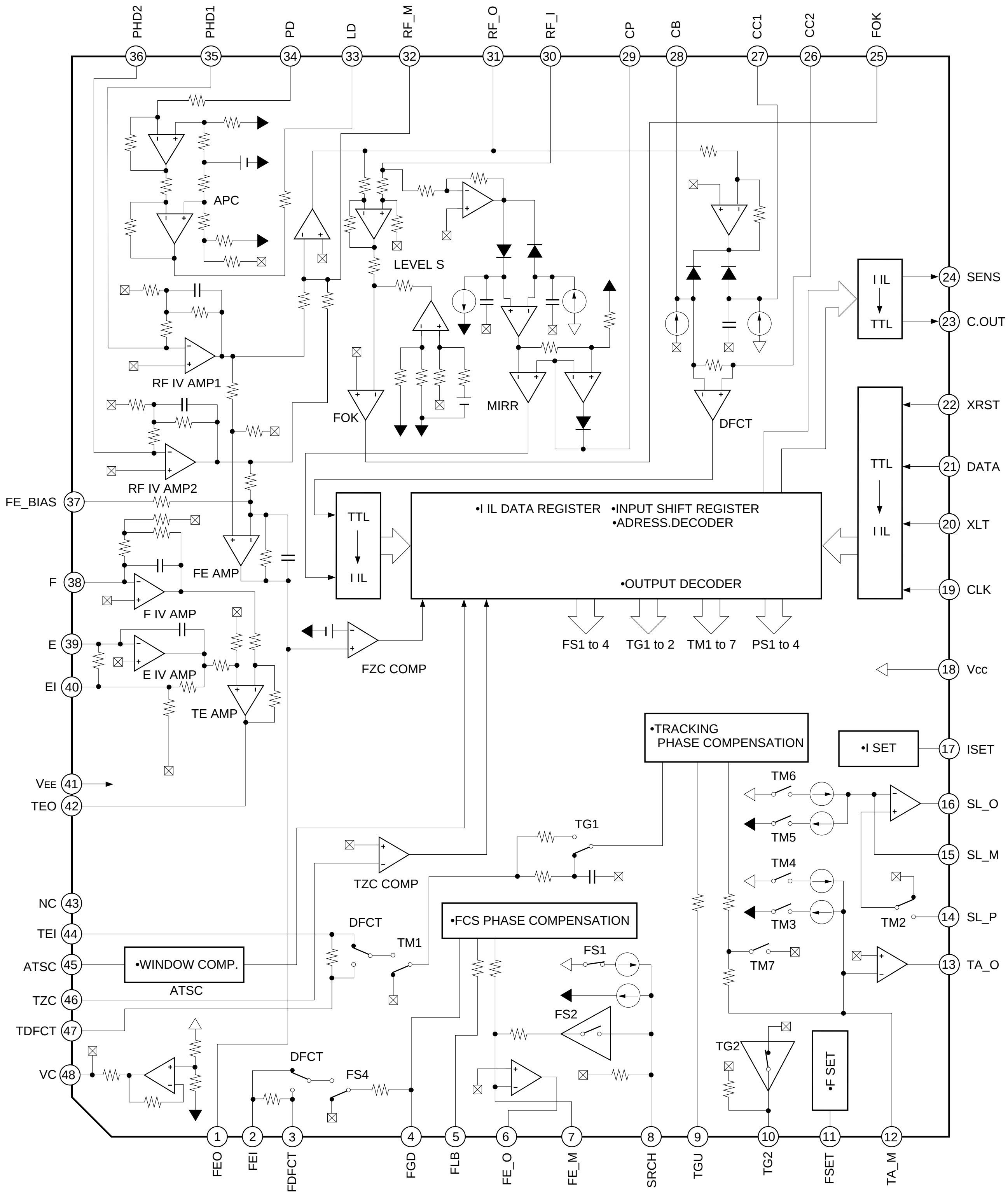
• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	833	mW

Recommended Operating Condition

Operating supply voltage

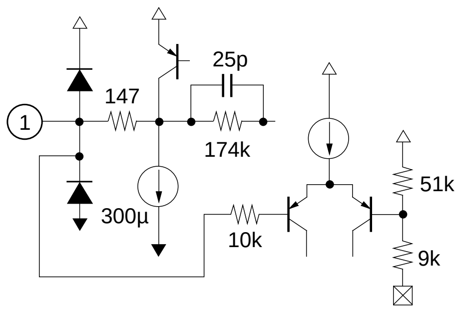
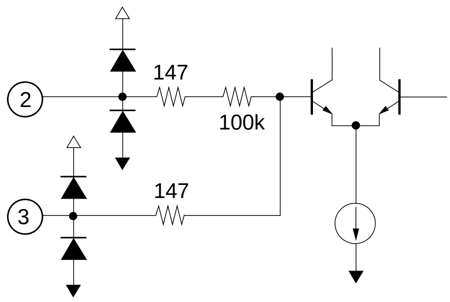
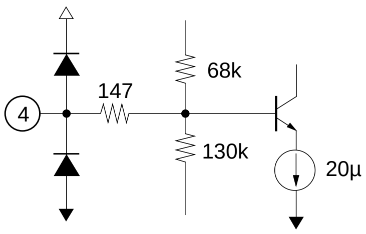
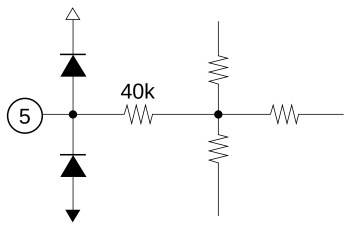
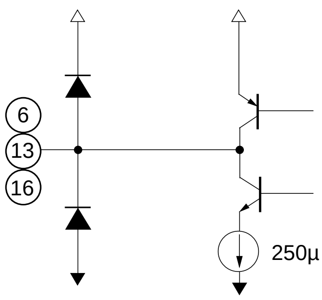
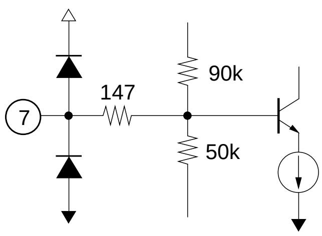
$V_{CC} - V_{EE}$	2.8 to 4.0	V

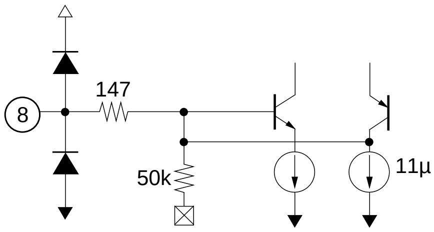
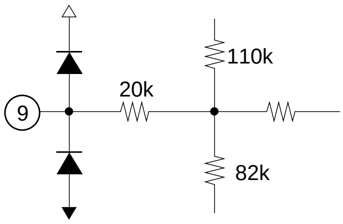
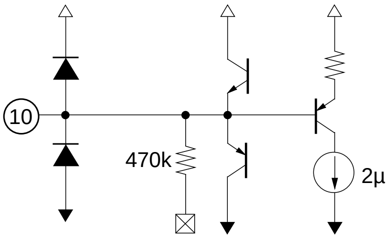
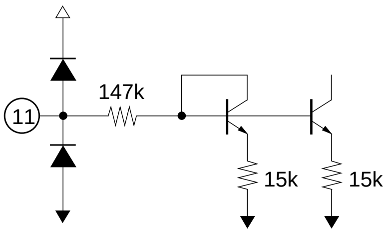
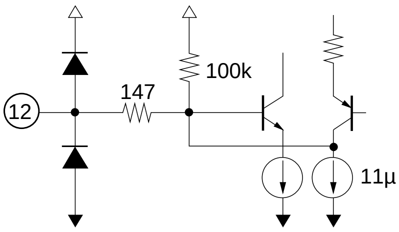
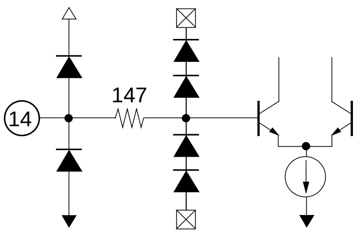
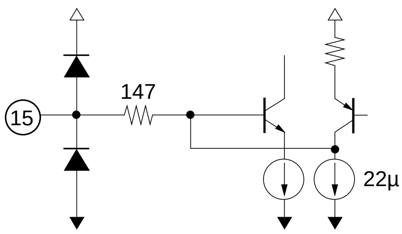
Block Diagram

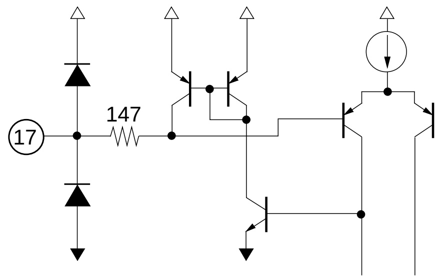
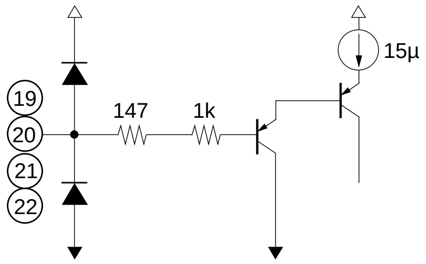
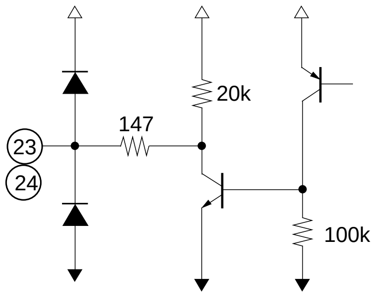
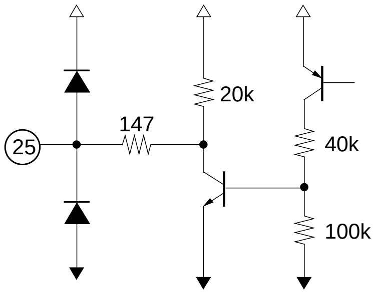
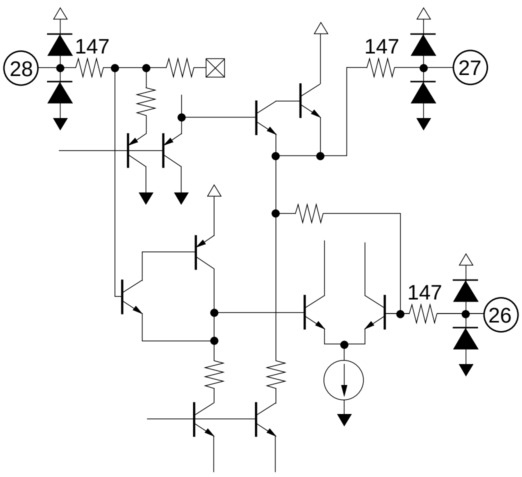


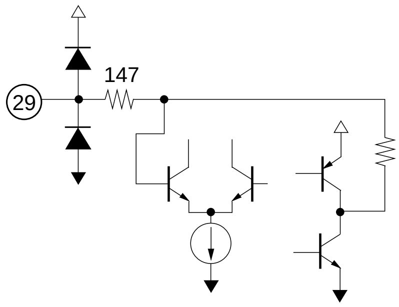
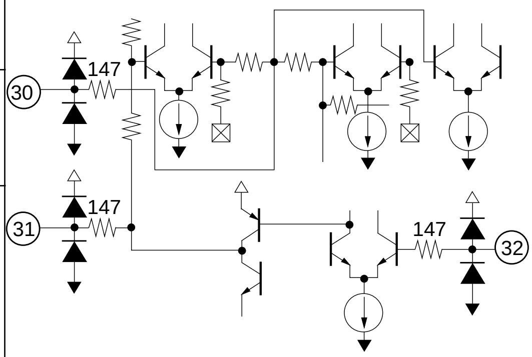
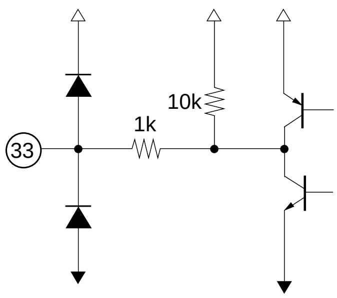
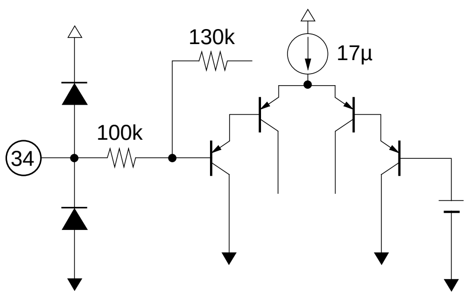
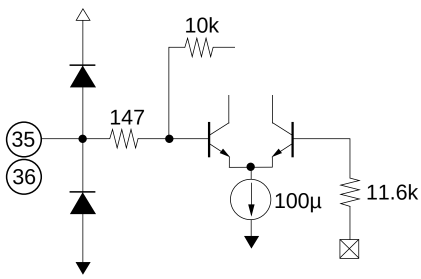
- The switch state in Block Diagram is for initial resetting.
- Switch turns to ∘ side for 1 and to • side for 0 in Serial Data Truth Table.
- DFCT switch turns to ∘ side when defect signal generates for DEFECT = E in Serial Data Truth Table.
- TG1 switch turns to ∘ side and TG2 switch is left open when TG1 and TG2 (address 1 : D3) is 1.

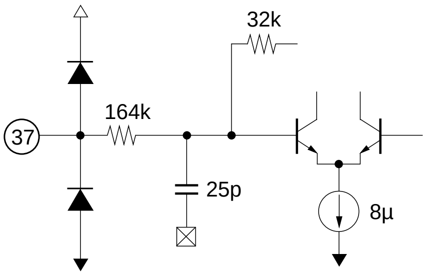
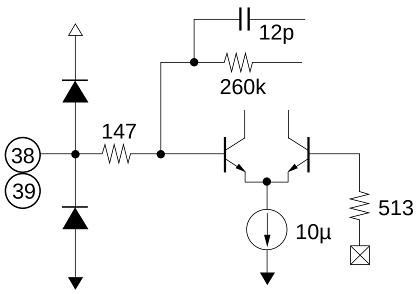
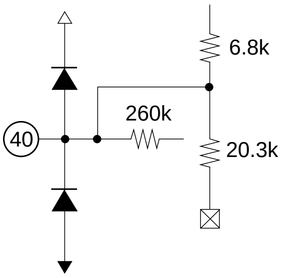
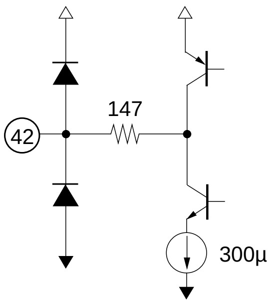
Pin Description

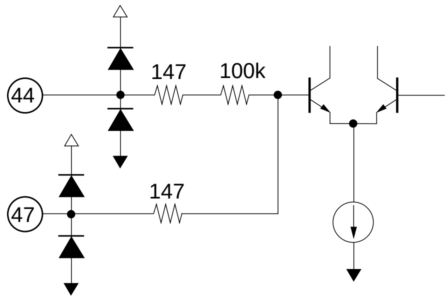
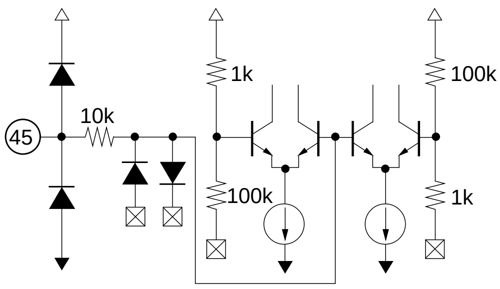
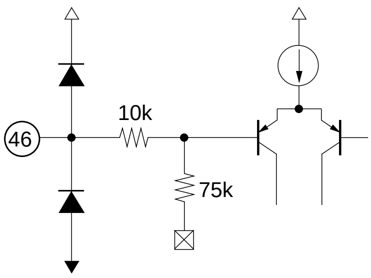
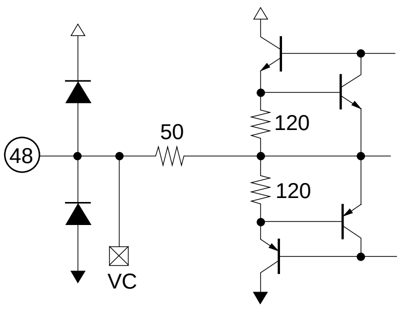
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>1</td><td>FEO</td><td>O</td><td></td><td>Focus error amplifier output. Connected internally to the FZC comparator input.</td></tr>
<tr><td>2</td><td>FEI</td><td>I</td><td rowspan="2"></td><td>Focus error input.</td></tr>
<tr><td>3</td><td>FDFCT</td><td>I</td><td>Capacitor connection pin for defect time constant.</td></tr>
<tr><td>4</td><td>FGD</td><td>I</td><td></td><td>Ground this pin through a capacitor when decreasing the focus servo high-frequency gain.</td></tr>
<tr><td>5</td><td>FLB</td><td>I</td><td></td><td>External time constant setting pin for increasing the focus servo low-frequency.</td></tr>
<tr><td>6</td><td>FE_O</td><td>O</td><td rowspan="3"></td><td>Focus drive output.</td></tr>
<tr><td>13</td><td>TA_O</td><td>O</td><td>Tracking drive output.</td></tr>
<tr><td>16</td><td>SL_O</td><td>O</td><td>Sled drive output.</td></tr>
<tr><td>7</td><td>FE_M</td><td>I</td><td></td><td>Focus amplifier inverted input.</td></tr>
</table>

Pin No.	Symbol	I/O	Equivalent circuit	Description
8	SRCH	I		External time constant setting pin for generating focus servo waveform.
9	TGU	I		External time constant setting pin for switching tracking high-frequency gain.
10	TG2	I		External time constant setting pin for switching tracking high-frequency gain.
11	FSET	I		High cut-off frequency setting pin for focus and tracking phase compensation amplifier.
12	TA_M	I		Tracking amplifier inverted input.
14	SL_P	I		Sled amplifier non-inverted input.
15	SL_M	I		Sled amplifier inverted input.

Pin No.	Symbol	I/O	Equivalent circuit	Description
17	ISET	I		Setting pin for Focus search, Track jump, and Sled kick current.
19	CLK	I		Serial data transfer clock input from CPU. (no pull-up resistance)
20	XLT	I		Latch input from CPU. (no pull-up resistance)
21	DATA	I		Serial data input from CPU. (no pull-up resistance)
22	XRST	I		Reset input; resets at Low. (no pull-up resistance)
23	C. OUT	O		Track number count signal output.
24	SENS	O		Outputs FZC, DFCT, TZC, gain, balance, and others according to the command from CPU.
25	FOK	O		Focus OK comparator output.
26	CC2	I		Input for the DEFECT bottom hold output with capacitance coupled.
27	CC1	O		DEFECT bottom hold output.
28	CB	I		Connection pin for DEFECT bottom hold capacitor.

Pin No.	Symbol	I/O	Equivalent circuit	Description
29	CP	I		Connection pin for MIRR hold capacitor. MIRR comparator non-inverted input.
30	RF_I	I		Input for the RF summing amplifier output with capacitance coupled.
31	RF_O	O		RF sunning amplifier output. Eye-pattern check point.
32	RF_M	I		RF summing amplifier inverted input. The RF amplifier gain is determined by the resistance connected between this pin and RFO pin.
33	LD	O		APC amplifier output.
34	PD	I		APC amplifier input.
35 36	PHD1 PHD2	I I		RF I-V amplifier inverted input. Connect these pins to the photo diode A + C and B + D pins.

Pin No.	Symbol	I/O	Equivalent circuit	Description
37	FE_BIAS	I		Bias adjustment of focus error amplifier.
38 39	F E	I I		F I-V and E I-V amplifier inverted input. Connect these pins to photo diodes F and E.
40	EI	—		I-V amplifier E balance adjustment.
42	TEO	O		Tracking error amplifier output. E-F signal is output.
43	NC	—		

Pin No.	Symbol	I/O	Equivalent circuit	Description
44	TEI	I		Tracking error input.
47	TDFCT	I		Capacitor connection pin for defect time constant.
45	ATSC	I		Window comparator input for ATSC detection.
46	TZC	I		Tracking zero-cross comparator input.
48	VC	O		$(V_{CC} + V_{EE})/2$ DC voltage output.

Electrical Characteristics

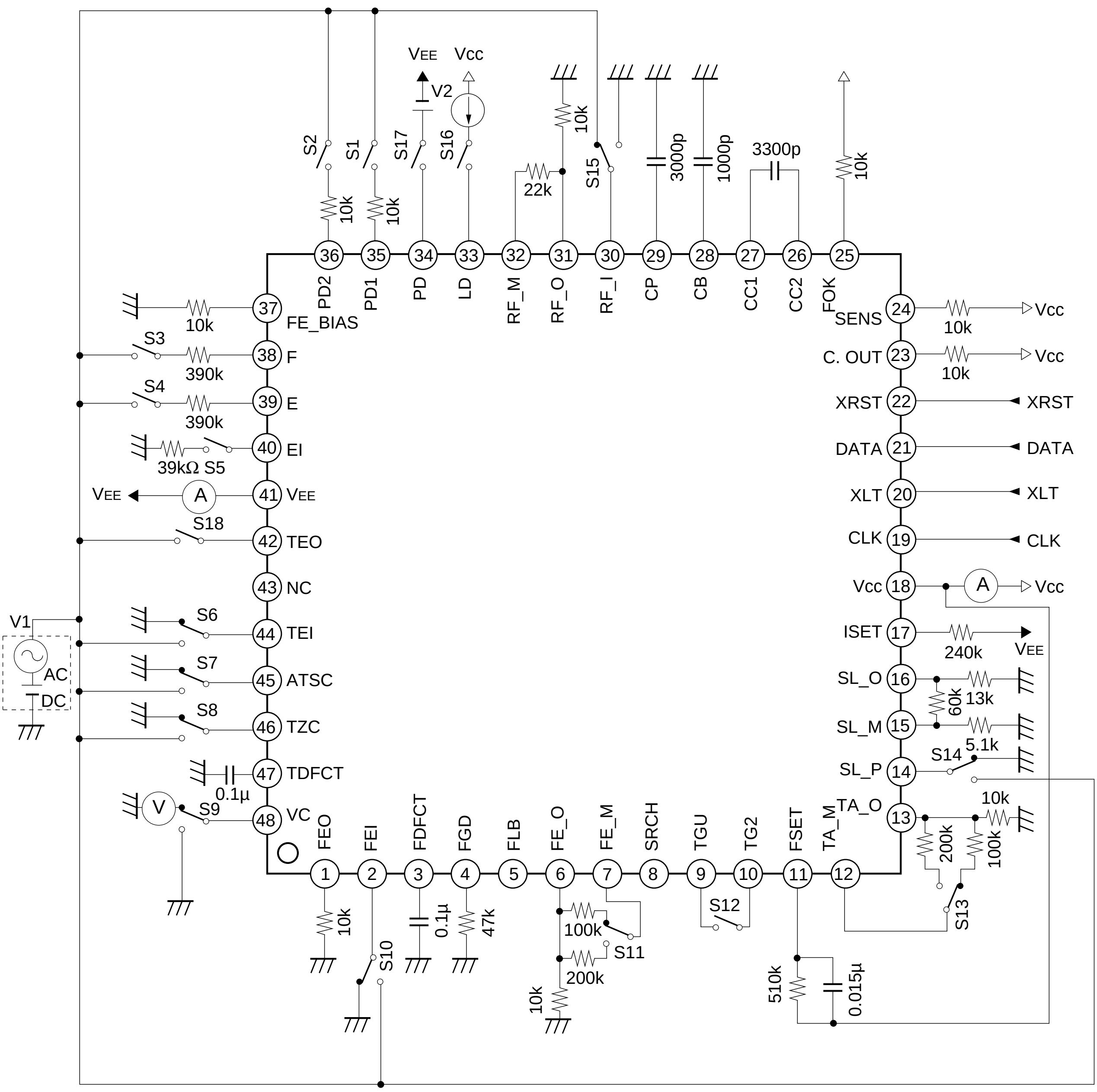
(V_{CC} = 1.5V, V_{EE} = –1.5V, Ta = 25°C)

	Item		SW conditions 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	SD	Measurement pin	Measurement conditions	Ratings Min.	Typ.	Max.	Unit
T1	Current consumption 1																				RST	18		8	12	18	mA
T2	Current consumption 2																					41		–18	–12	–8	mA
T3	RF amplifier	Offset																				31		–50	0	50	mV
T4	RF amplifier	Voltage gain	O	O																			1kHz input ratio	25.1	28.1	31.1	dB
T5	RF amplifier	Max. output voltage-High	O																				V1 = 100mV$_{DC}$	1.2	1.3	—	V
T6	RF amplifier	Max. output voltage-Low		O																			V1 = –100mV$_{DC}$	—	–0.9	–0.3	V
T7	FE amplifier	Offset																				1		–120	0	120	mV
T8	FE amplifier	Voltage gain 1	O																				V1 = 1kHz I/O ratio	27.0	30.0	33.0	dB
T9	FE amplifier	Voltage gain 1		O																			V1 = 1kHz I/O ratio	27.0	30.0	33.0	dB
T10	FE amplifier	Voltage gain difference																						–3.0	0	3.0	dB
T11	FE amplifier	Max. output voltage-High		O																			V1 = 100mV$_{DC}$	1.0	1.3	—	V
T12	FE amplifier	Max. output voltage-Low	O																				V1 = 100mV$_{DC}$	—	–1.3	–1.0	V
T13	TE amplifier	Offset																				42		–25	0	25	mV
T14	TE amplifier	Voltage gain F_0			O																		V1 = 1kHz	7.3	10.3	13.3	dB
T15	TE amplifier	Voltage gain E_0				O	O																V1 = 1kHz EI: 39kΩ	7.2	10.2	13.2	dB
T16	TE amplifier	Max. output voltage-High			O																		V1 = 1V$_{DC}$	1.2	1.45	—	V
T17	TE amplifier	Max. output voltage-Low				O	O																V1 = 1V$_{DC}$ EI: 39kΩ	—	–1.33	–1.0	V
T18	APC	Output voltage 1																	O			33	V2 = 120mV	–900		–300	mV
T19	APC	Output voltage 2																	O				V2 = 145mV	–400		900	mV
T20	APC	Output voltage 3																	O				V2 = 170mV	350		1500	mV
T21	APC	Output voltage 4																O	O				0.8mA sink	–200		500	mV
T22	VC	Center amplifier output offset									O											48		–100		100	mV

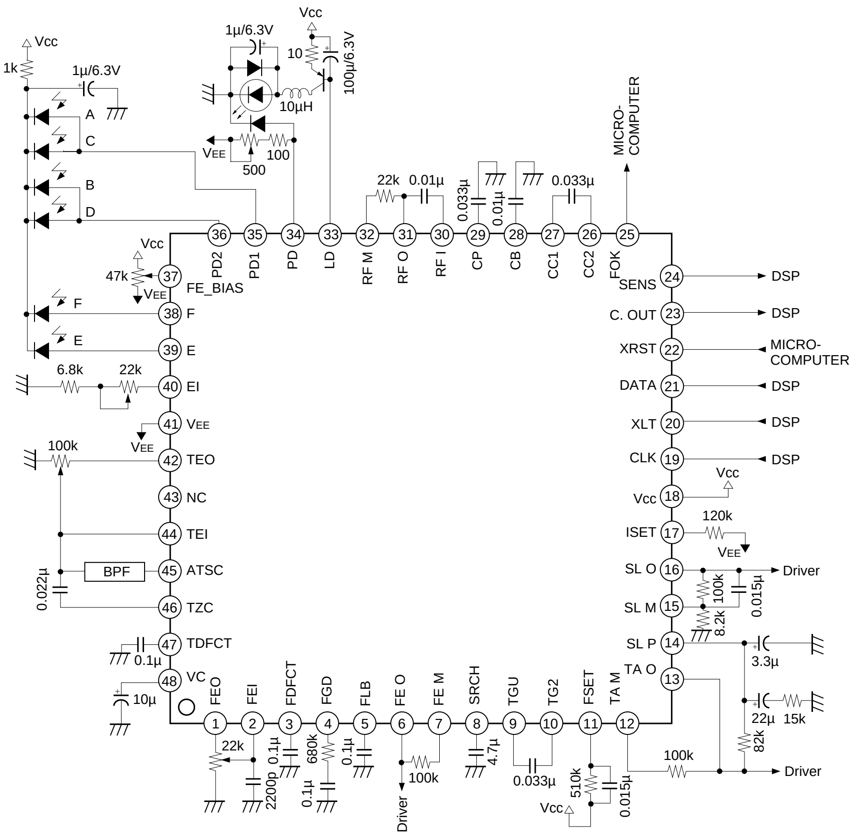
		Item	SW conditions																		SD	Measure-ment pin	Measurement conditions	Ratings			Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18				Min.	Typ.	Max.	
T23	FCS servo	DC voltage gain										O									08	6		18	21.0	24	dB
T24		FCS total gain																			↓	↓	T23+ T8 (or T9)	49	51	53	dB
T25		Feed through										O									00		Output gain difference between SD = 00 and SD = 08.			–35	dB
T26		Max. output voltage-High										O	O								08		V1 = 200mVDC	1.0	1.3	—	V
T27		Max. output voltage-Low										O	O								08		V1 = –200mVDC	—	–1.3	–1.0	V
T28		Search voltage (–)																			02			–640	–500	–360	mV
T29		Search voltage (+)																			03	↓		360	500	640	mV
T30		FZC threshold	O																		00	24	Pin 1 threshold	185	225	265	mV
T31	TRK servo	DC voltage gain						O													25	13		12.25	14.6	17.6	dB
T32		TRK total gain																			↓	↓	T31+ T14	22.9	24.9	26.9	dB
T33		Feed through						O															Output gain difference between SD = 20 and SD = 25.			–39	dB
T34		Max. output voltage-High						O							O								V1 = –0.5VDC	1.0	1.3		V
T35		Max. output voltage-Low						O							O						↓		V1 = +0.5VDC		–1.3	–1.0	V
T36		Jump output voltage (–)																			2C			–640	–500	–360	mV
T37		Jump output voltage (+)																			28	↓		360	500	640	mV
T38		ATSC threshold (–)							O												25	10		–25	–15	–7	mV
T39		ATSC threshold (+)							O												25	↓		7	15	25	mV
T40		TZC threshold								O											25	24		–20	0	20	mV
T41	FOK	FOK threshold																O			38	25		–400	–356	–330	mV

	Item		SW conditions																		SD	Measurement pin	Measurement conditions	Ratings			Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18				Min.	Typ.	Max.	
T42	Sled servo	DC open gain														O					25	16		50			dB
T43		Feed through														O					20	↓	Output gain difference between SD = 20 and SD = 25.			–34	dB
T44		Max. output voltage-High														O					25	↓	V1 = +0.4VDC	1.0	1.3		V
T45		Max. output voltage-Low														O					↓	↓	V1 = –0.4VDC		–1.3	–1.0	V
T46		Kick voltage (–)																			23	↓		–750	–600	–450	mV
T47		Kick voltage (+)																			22	↓		450	600	750	mV
T48	MIRR	Max. operating frequency								O							O				14	23	Measures at C. OUT pin.	30			kHz
T49		Min. input operating voltage								O							O				↓	↓	Measures at C. OUT pin.			0.3	Vp-p
T50		Max. input operating voltage								O							O				↓	↓	Measures at C. OUT pin.	1.8			Vp-p
T51	DEFECT	Min. operating frequency	O	O																	10	24	Measures at SENS pin.			1	kHz
T52		Max. operating frequency	O	O																	↓	↓	Measures at SENS pin.	2.5			kHz
T53		Min. input operating voltage	O	O																	↓	↓	Measures at SENS pin.			0.5	Vp-p
T54		Max. input operating voltage	O	O																	↓	↓	Measures at SENS pin.	1.8			Vp-p

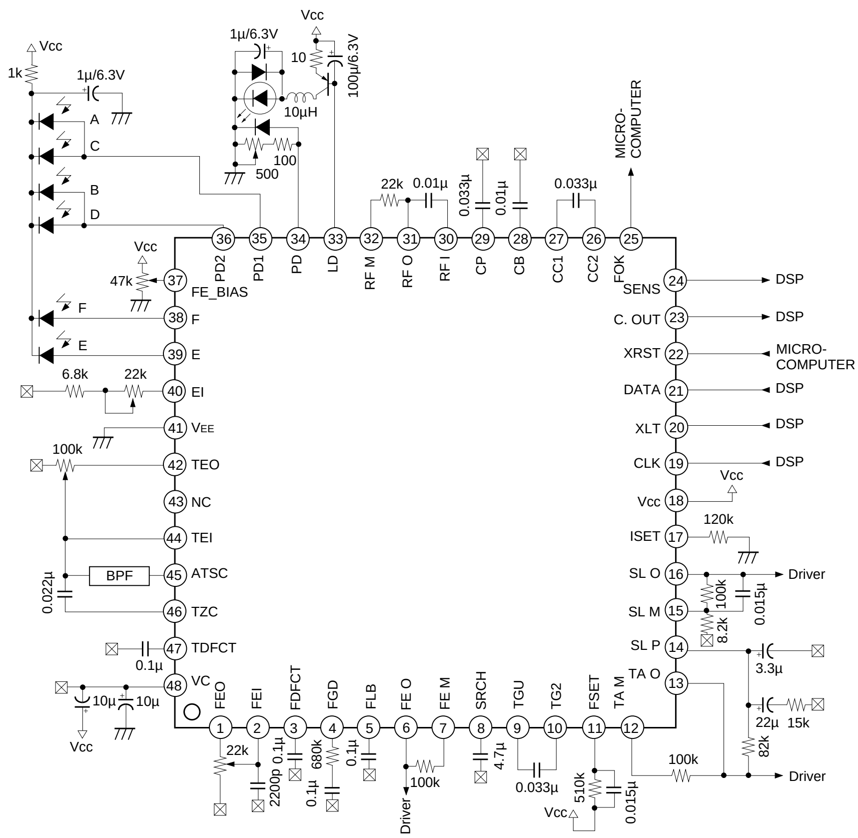
Electrical Characteristics Measurement Circuit



Application Circuit (Dual ±1.5V power supplies)



Application Circuit (Single +3V power supply)

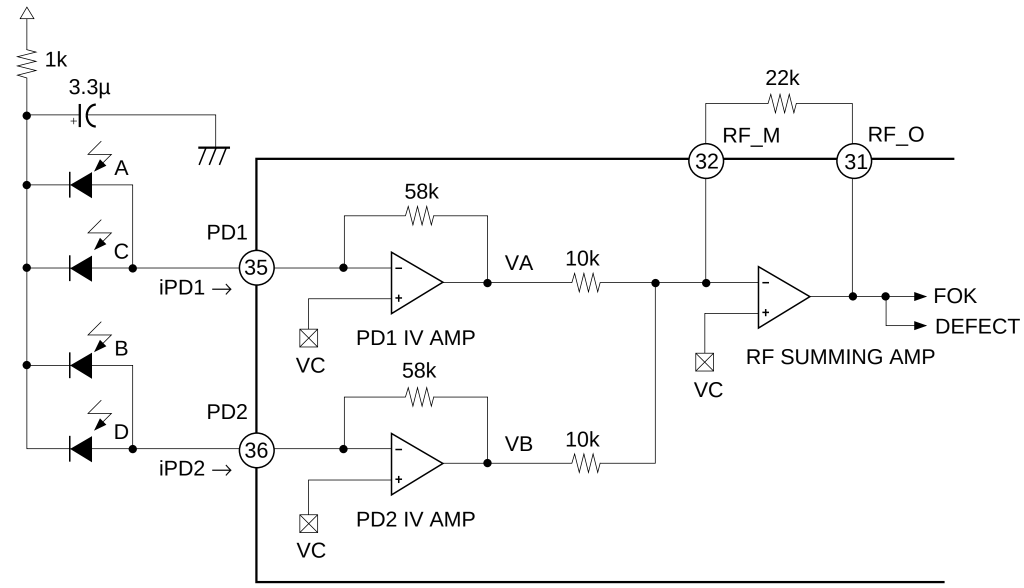


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Functions

RF Amplifier

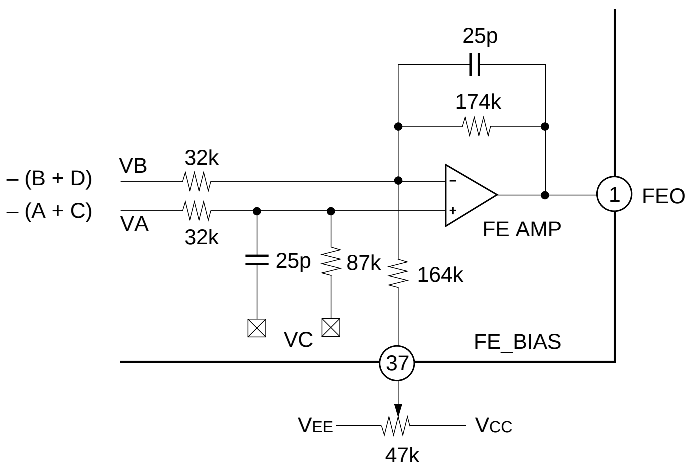
The photo diode currents input to the input pins (PD1 and PD2) are each I-V converted via a 58kΩ equivalent resistor by the PD I-V amplifiers. these signals are added by the RF summing amplifier, and the photo diode (A + B + C + D) current-voltage converted voltage is output to the RFO pin. An eye-pattern check can be performed at this pin.



The low frequency component of the RFO output voltage is $V_{RFO} = 2.2 \times (V_A + V_B) = 127.6k\Omega \times (iPD1 + iPD2)$.

Focus Error Amplifier

The focus error amplifier calculates the difference between output VA and VB of the RF I-V amplifier, and output current-voltage converted voltage of the photo diode (A + C – B – D).

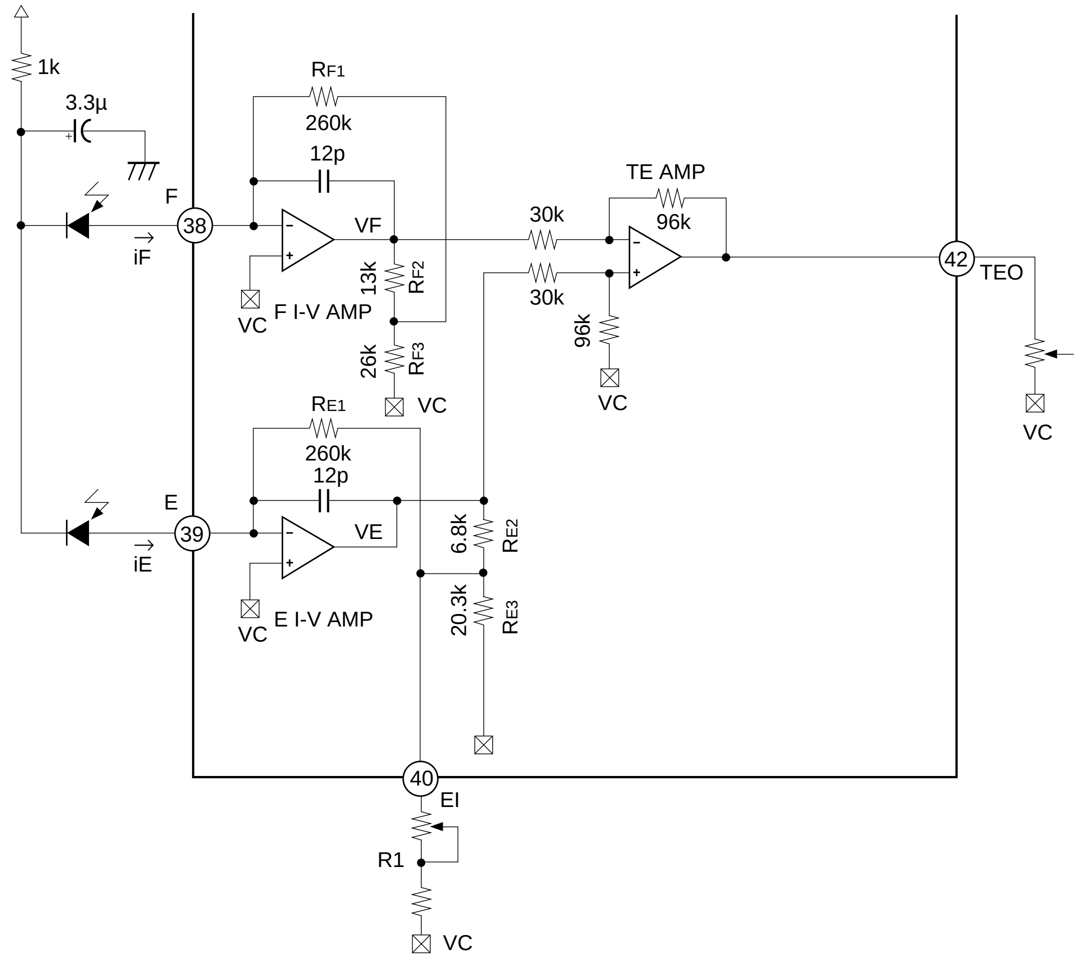


The FEO output voltage (low frequency) is $V_{FEO} = 5.4 \times (V_A - V_B) = (iPD2 - iPD1) \times 315k\Omega$.

Be aware that the rotation of the focus bias volume has reversed for the usual CD RF IC.

Tracking Error Amplifier

The photo diode currents input to E and F pins are each current-voltage converted by the E I-V and F I-V amplifiers.



Tracking system balance adjustment is performed by varying the resistance externally attached to EI pin.
This external resistance sets combined feed back resistance of the T-configured E I-V AMP.

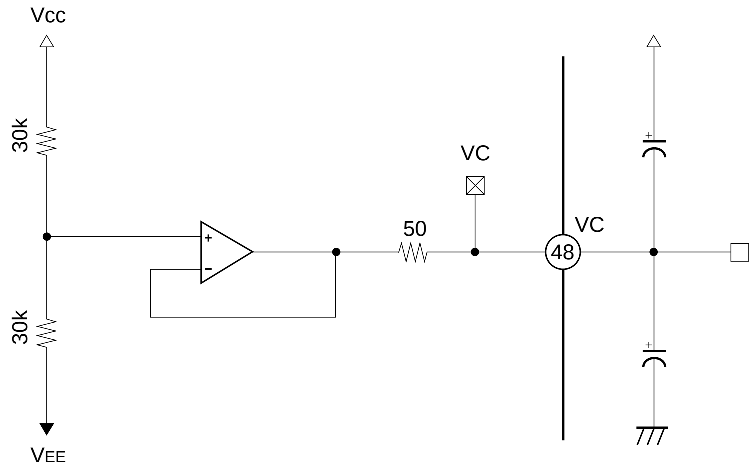
$$\text{F I-V AMP feedback resistance} = R_{F1} + R_{F2} + \frac{R_{F1} \times R_{F2}}{R_{F3}} = 403k\Omega$$

$$\text{E I-V AMP feedback resistance} = R_{E1} + R_{E2} + \frac{R_{E1} \times R_{E2}}{R_x} \quad (R_x = R1 // R_{E3})$$

Gain adjustment is performed by adjusting external variable resistor of TEO pin.

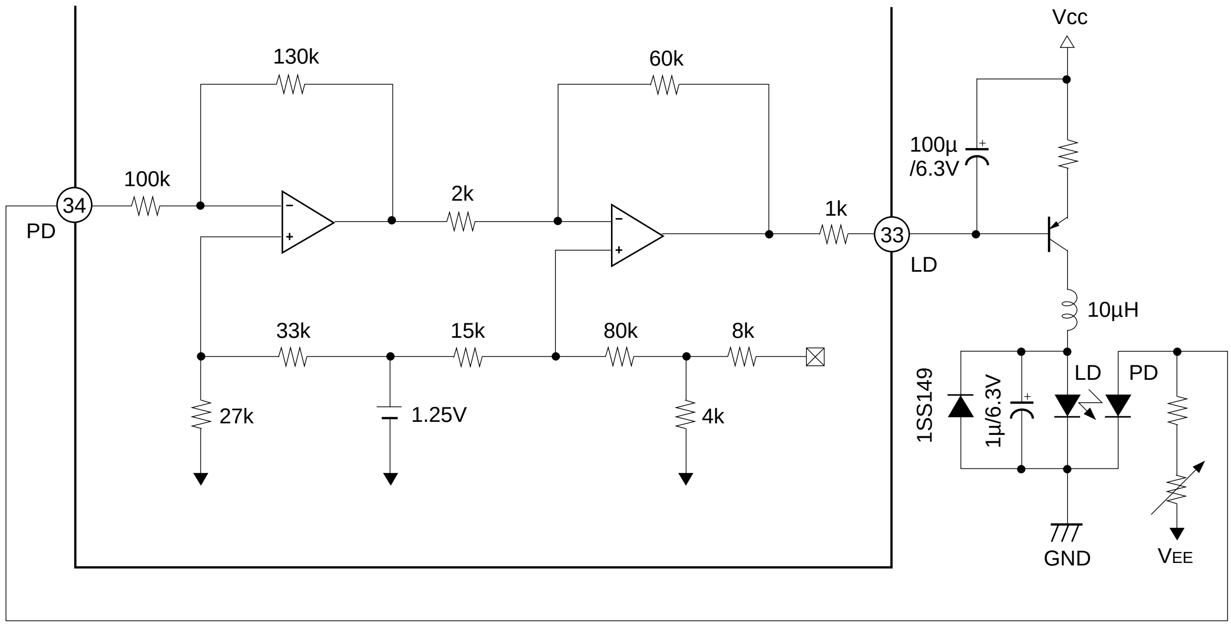
Center Voltage Generation Circuit

(Single voltage application; Connect to GND when it's positive/negative dual power supplies.)
Maximum current is approximately ±3mA. Output impedance is approximately 50Ω.

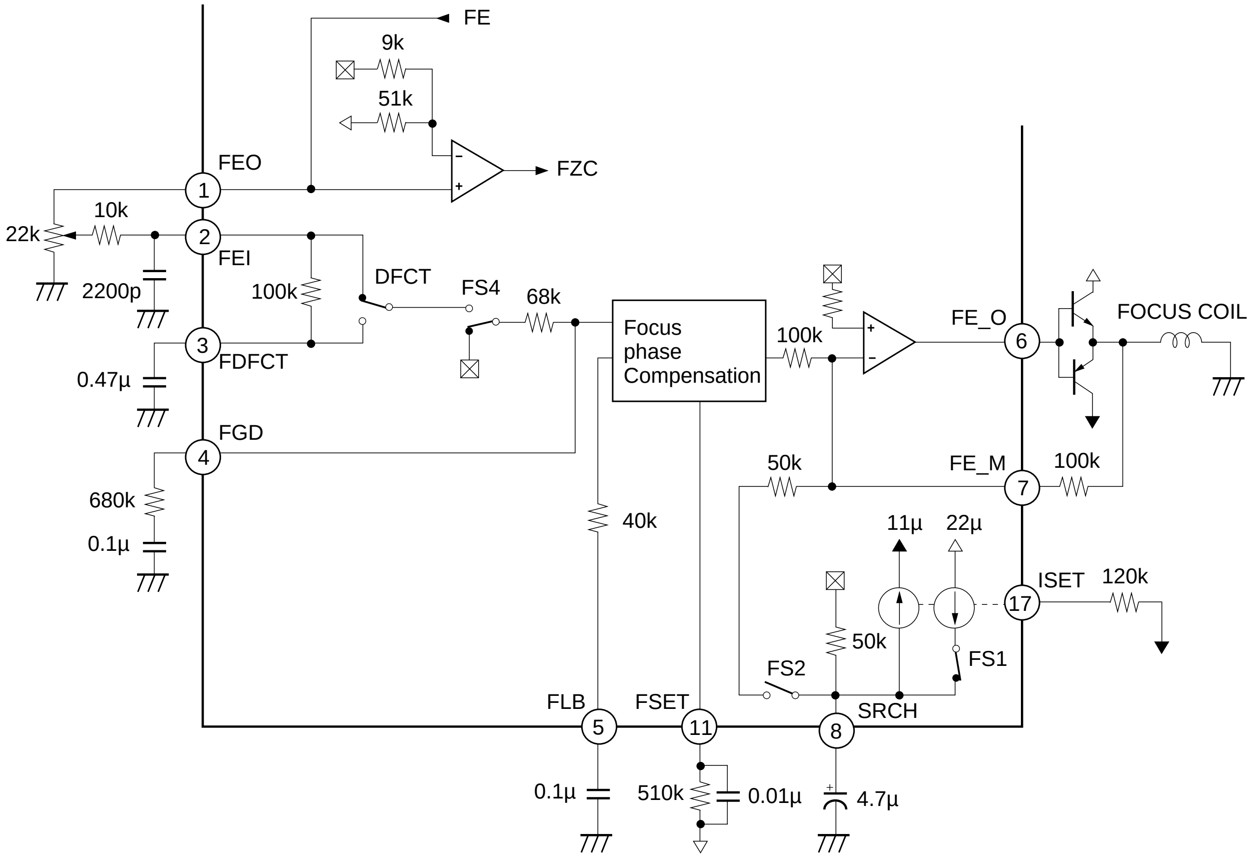


APC Circuit

When driving a constant current, the optical output by the laser diode possesses large negative temperature characteristics. Therefore, the current must be controlled with the monitor photo diode to ensure the output remains constant.



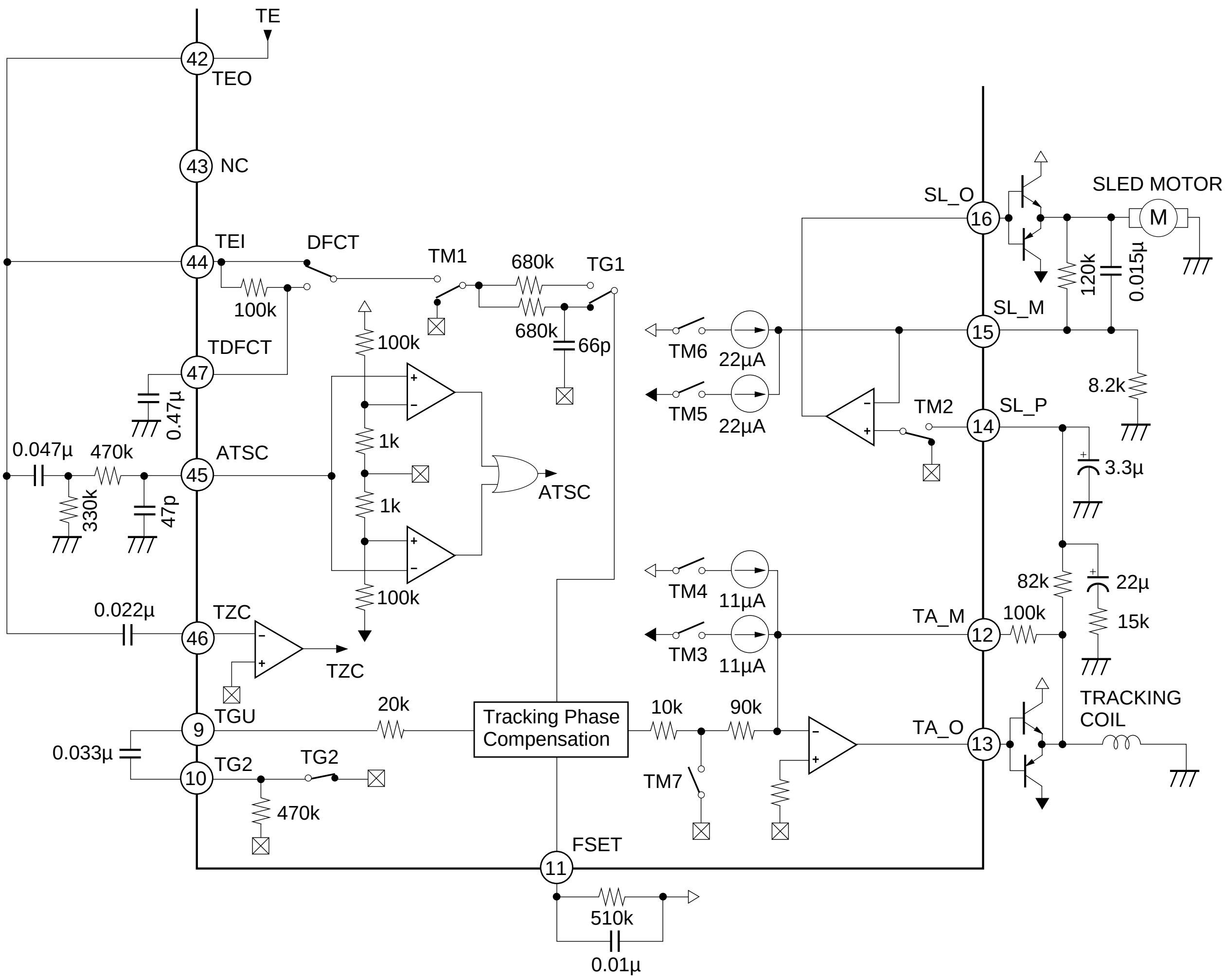
Focus Servo



The above figure shows a block diagram of the focus servo.
Ordinarily the FE signal is input to the focus phase compensation circuit through a 68kΩ resistance; however, when DFCT is detected, the FE signal is switched to pass through a low-pass filter formed by the internal 100kΩ resistance and the capacitance connected to Pin 3. When this DFCT prevention circuit is not used, leave Pin 3 open. The defect switch operation can be enabled and disabled with command.

The capacitor connected between Pin 5 and GND is a time constant to raise the low frequency in the normal playback state.
The peak frequency of the focus phase compensation is approximately 1.2kHz when a resistance of 510Ω is connected to Pin 11.
The focus search height is approximately ±1.1Vp-p when using the constants indicated in the above figure. This height is inversely proportional to the resistance connected between Pin 17 and VEE. However, changing this resistance also changes the height of the track jump and sled kick as well.
The FZC comparator inverted input is set to 15% of V_{CC} and VC (Pin 48); (V_{CC} – VC) × 15%.
* 510kΩ resistance is recommended for Pin 11.

Tracking Sled Servo



The above figure shows a block diagram of the tracking and sled servo.

The capacitor connected between Pins 9 and 10 is a time constant to decrease the high-frequency gain when TG2 is OFF. The peak frequency of the tracking phase compensation is approximately 1.2kHz when a 510kΩ resistance connected to Pin 11. In the CXA1782, TG1 and TG2 are inter-linked switches.

To jump tracks in FWD and REV directions, turn TM3 or TM4 ON. During this time, the peak voltage applied to the tracking coil is determined by the TM3 or TM4 current and the feedback resistance from Pin 12. To be more specific,

Track jump peak voltage = TM3 (or TM4) current × feedback resistance value

The FWD and REV sled kick is performed by turning TM5 or TM6 ON. During this time, the peak voltage applied to the sled motor is determined by the TM5 or TM6 current and the feedback resistance from Pin 15;

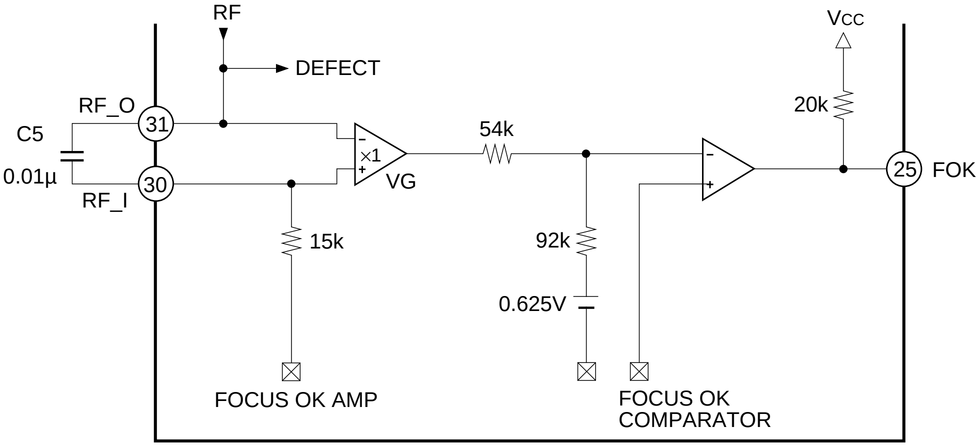
Sled kick peak voltage = TM5 (or TM6) current × feedback resistance

The values of the current for each switch are determined by the resistance connected between Pin 17 and VEE. When this resistance is 120kΩ:

TM3 (or TM4) = ±11μA, and TM5 (or TM6) = ±22μA.

As is the case with the FE signal, the TE signal is switched to pass through a low-pass filter formed by the internal resistance (100kΩ) and the capacitance connected to Pin 47.

Focus OK Circuit



The focus OK circuit creates the timing window okaying the focus servo from the focus search state.

The HPF output is obtained at Pin 30 from Pin 31 (RF signal), and the LPF output (opposite phase) of the focus OK amplifier output is also obtained.

The focus OK output reverses when $V_{RFI} - V_{RFO} \approx -0.37V$.

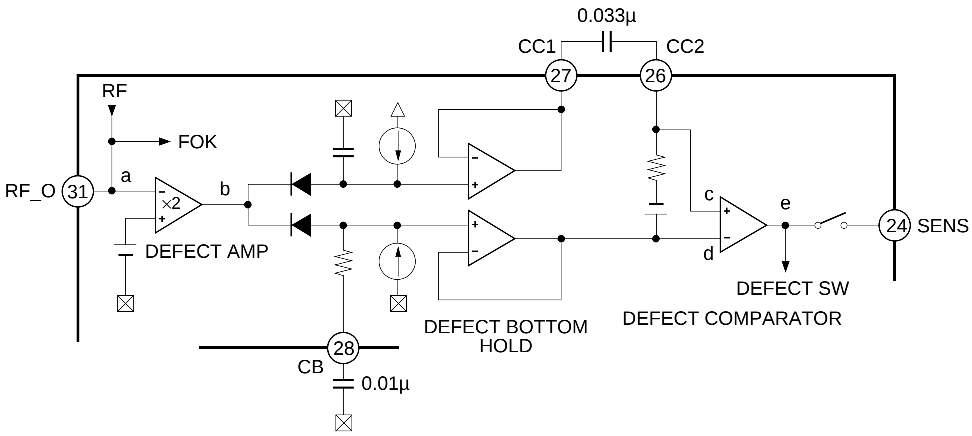
Note that, C5 determines the time constant of the HPF for the mirror circuit and the LPF of the focus OK amplifier. Ordinarily, with a C5 equal to 0.01µF selected, the fc is equal to 1kHz, and block error rate degradation brought about by RF envelope defects caused by scratched discs can be prevented.

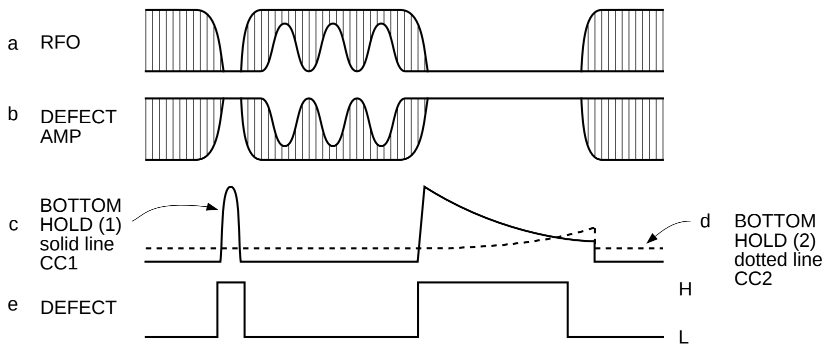
DEFECT Circuit

After inversion, RF_O signal is bottom held by means of the long and short time constants. The long time-constant bottom hold keeps the mirror level prior to the defect.

The short time-constant bottom hold responds to a disc mirror defect in excess of 0.1msec, and this is differentiated and level-shifted through the AC coupling circuit.

The long and short time-constant signals are compared to generate at mirror defect detection signal.

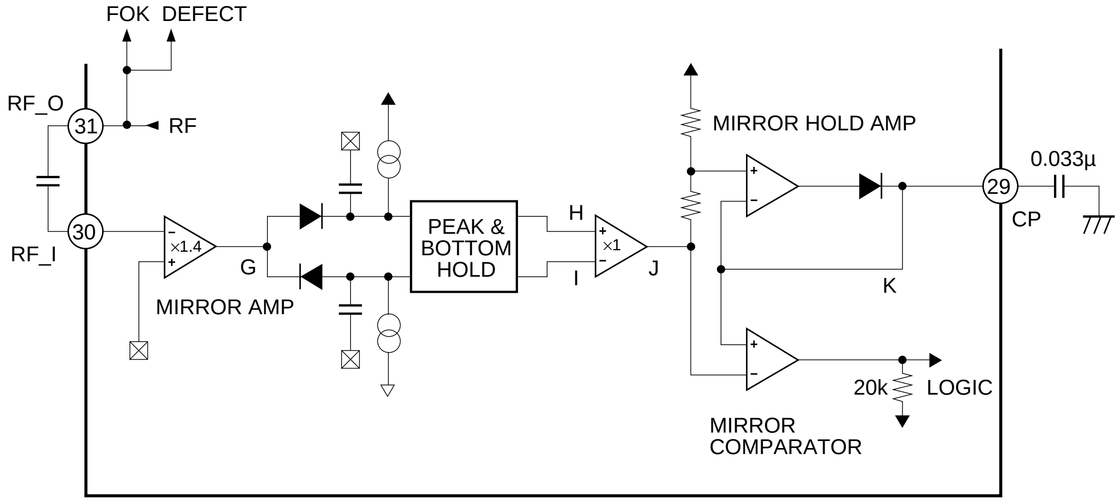


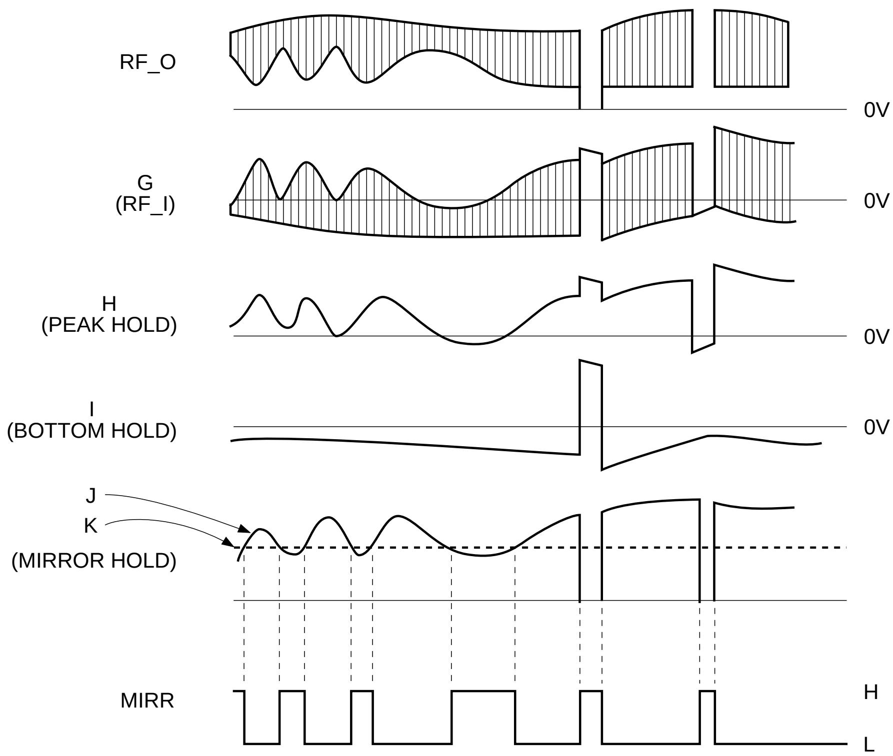


Mirror Circuit

The mirror circuit performs peak and bottom hold after the RFI signal has been amplified.

The peak and bottom holds are both held through the use of a time constant. For the peak hold, a time constant can follow a 30kHz traverse, and, for the bottom hold, one can follow the rotation cycle envelope fluctuation.





The DC playback envelope signal J is obtained by amplifying the difference between the peak and bottom hold signals H and I. Signal J has a large time constant of 2/3 its peak value, and the mirror output is obtained by comparing it to the peak hold signal K. Accordingly, when on the disc track, the mirror output is Low; when between tracks (mirrored portion), it is High; and when a defect is detected, it is High. The mirror hold time constant must be sufficiently large compared with the traverse signal.

In the CXA1982Q, this mirror output is used only during braking operations, and no external output pin is attached. Accordingly, when connecting DSP such as the CXD2500 with MIRR input pin, input the C. OUT output to the MIRR input of the DSP.

Commands

The input data to operate this IC is configured as 8-bit data; however, below, this input data is represented by 2-digit hexadecimal numerals in the form $XX, where X is a hexadecimal numeral between 0 and F.
Commands for the CXA1982Q can be broadly divided into four groups ranging in value from $0X to $2X.

1. $0X (“FZC” at SENS pin (Pin 24))

These commands are related to focus servo control.
The bit configuration is as shown below.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	FS4	DEFECT	FS2	FS1

Four focus-servo related switches exist: FS1, FS2, FS4, and DEFECT corresponding to D0 to D3, respectively.

$00 When FS1 = 0, Pin 8 is charged to (22µA – 11µA) × 50kΩ = 0.55V.
If, in addition, FS2 = 0, this voltage is no longer transferred, and the output at Pin 6 becomes 0V.

$02 From the state described above, the only FS2 becomes 1. When this occurs, a negative signal is output to Pin 6. This voltage level is obtained by equation 1 below.

$$(22\mu A - 11\mu A) \times 50k\Omega \times \frac{\text{resistance between Pins 6 and 7}}{50k\Omega} \quad \cdots\cdot \quad \text{Equation 1}$$

$03 From the state described above, FS1 becomes 1, and a current source of +22µA is split off.
Then, a CR charge/discharge circuit is formed, and the voltage at Pin 8 decreases with the time as shown in Fig. 1 below.

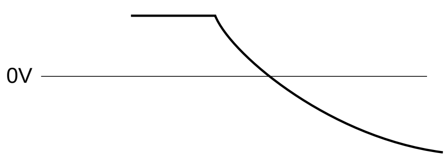


Fig. 1. Voltage at Pin 8 when FS1 gose from 0 → 1

This time constant is obtained with the 50kΩ resistance and an external capacitor.

By alternating the commands between $02 and $03, the focus search voltage can be constructed. (Fig. 2)

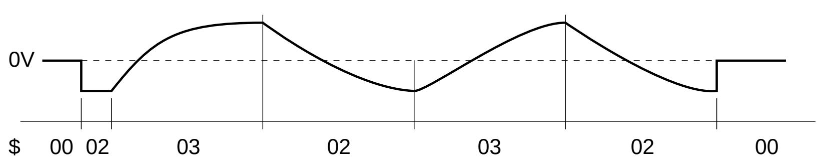


Fig. 2. Constructing the search voltage by alternating between $02 and $03. (Voltage at Pin 6)

$04 When the fact that the RF signal is missing is detected and the scratches on the disc are detected with DEFECT = 0, DFCT (FS3) is turned ON.

1-1. FS4

This switch is provided between the focus error input (Pin 2) and the focus phase compensation, and is in charge of turning the focus servo ON and OFF.

$00 → $08
Focus OFF ← Focus ON

1-2. Procedure of focus activation

For description, suppose that the polarity is as described below.
a) The lens is searching the disc from far to near;
b) The output voltage (Pin 6) is changing from negative to positive; and
c) The focus S-curve is varying as shown below.

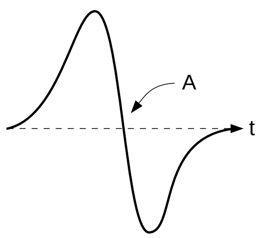


Fig. 3. S-curve

The focus servo is activated at the operating point indicated by A in Fig. 3. Ordinarily, focus searching and the turning the focus servo switch ON are performed during the focus S-curve transits the point A indicated in Fig. 3. To prevent misoperation, this signal is ANDed with the focus OK signal.
In this IC, FZC (Focus Zero Cross) signal is output from the SENS pin (Pin 24) as the point A transit signal. In addition, focus OK is output as a signal indicating that the signal is in focus (can be in focus in this case).
Following the line of the above description, focusing can be well obtained by observing the following timing chart.

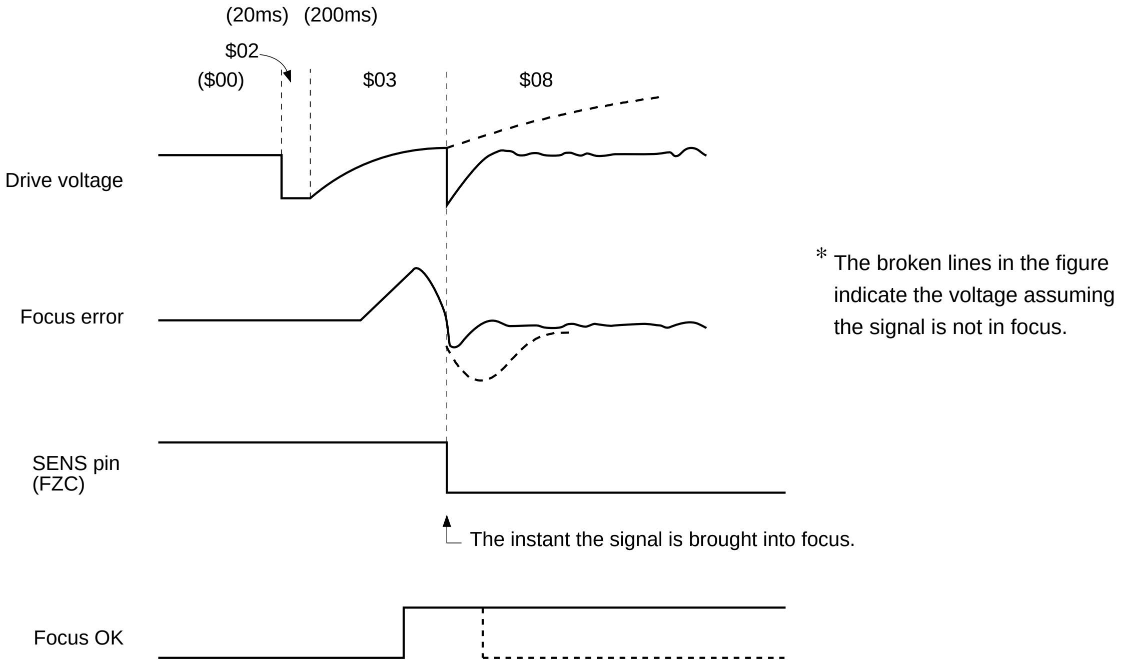


Fig. 4. Focus ON timing chart

Note that the time from the High to Low transition of FZC to the time command $08 is asserted must be minimized. To do this, the software sequence shown in B is better than the sequence shown in A.

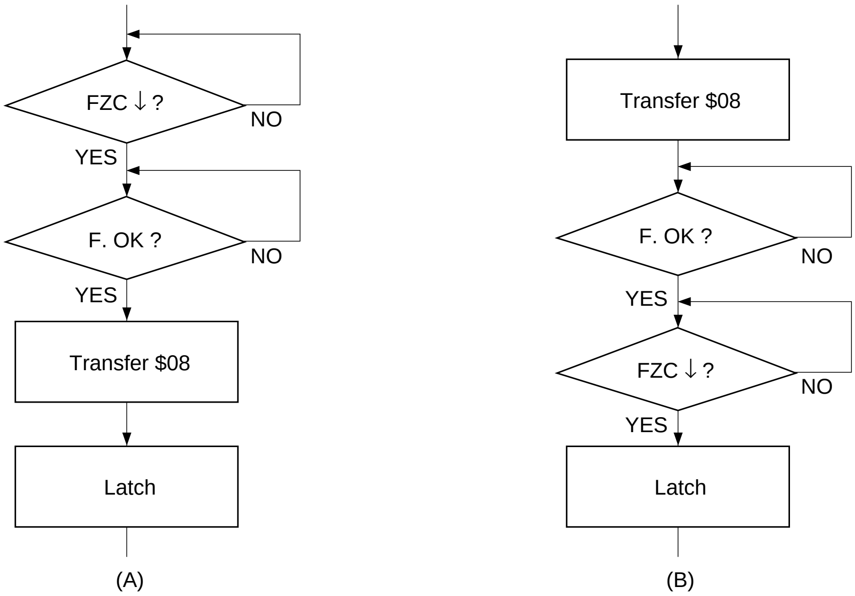


Fig. 5. Poor and good software command sequences

1-3. SENS pin (Pin 24)

The output of the SENS pin differs depending on the input data as shown below.

$0X: FZC
$1X: DEFECT
$2X: TZC
$3X: PROHIBITED
$4X to 7X: HIGH-Z

2. $1X ("DEFECT" at SENS pin (Pin 24))

These commands deal with switching TG1/TG2, brake circuit ON/OFF, and the sled kick output.

The bit configuration is as follows

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	TG1, TG2 ON/OFF	Break circuit ON/OFF	Sled kick height	

Sled kick height		Relative value
D1 (PS1)	D0 (PS0)	
0 0	0 1	±1 ±2
1 1	0 1	±3 ±4

TG1, TG2

The purpose of these switches is to switch the tracking servo gain Up/Normal. TG1 and TG2 are interlinked switches. The brake circuit (TM7) is to prevent the occurrence of such frequently occurring phenomena as extremely degraded actuator settling due to the servo motor exceeding the linear range causing what should be a 100-track jump to fall back down to a 10-track jump after a 100 or 10-track jump has been performed. To do this, when the actuator travels radially; that is, when it traverses from the inner track to the outer track of the disc and vice versa, the brake circuit utilizes the fact that the phase relationship between the RF envelope and the tracking error is 180°out-of-phase to cut the unneeded portion of the tracking error and apply braking.

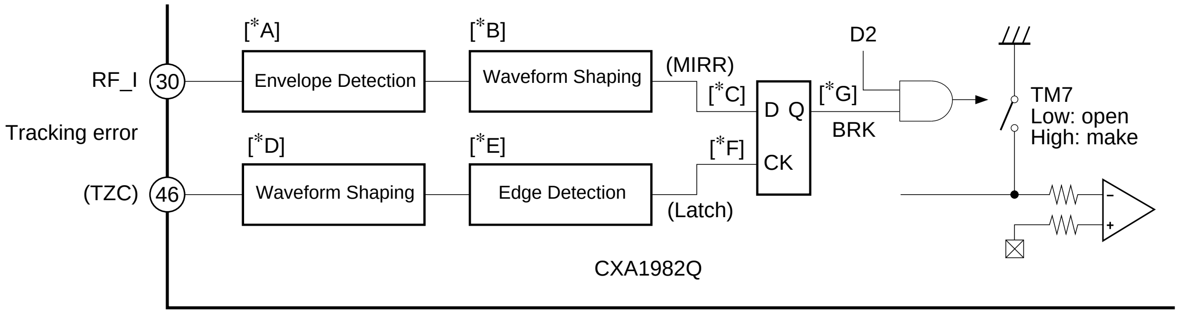


Fig. 6. TMI movement during braking operation

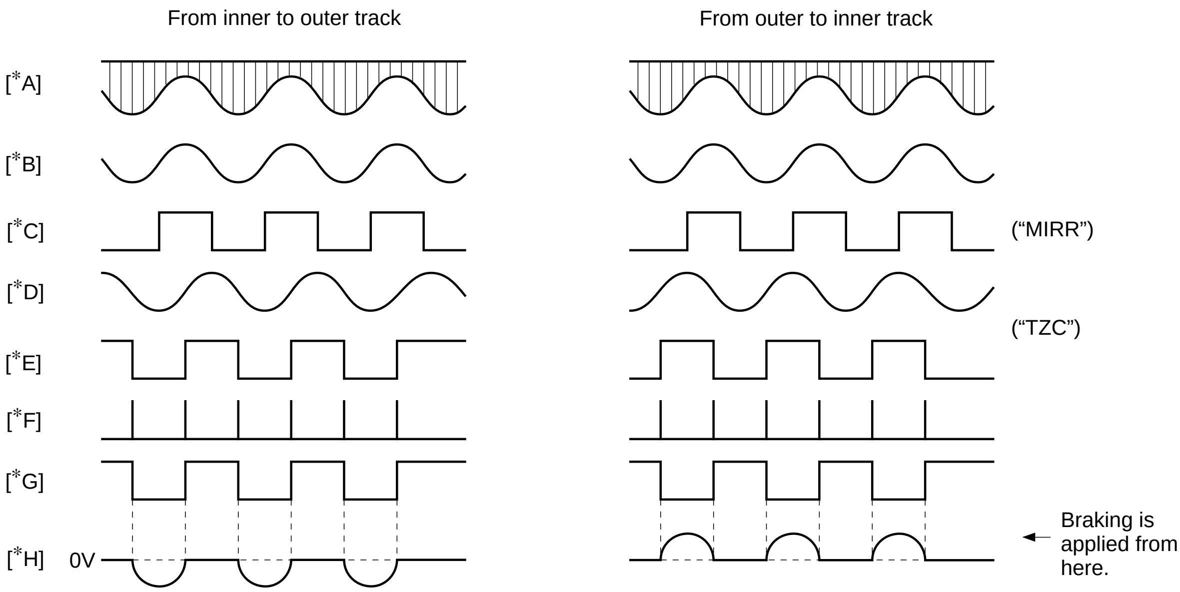


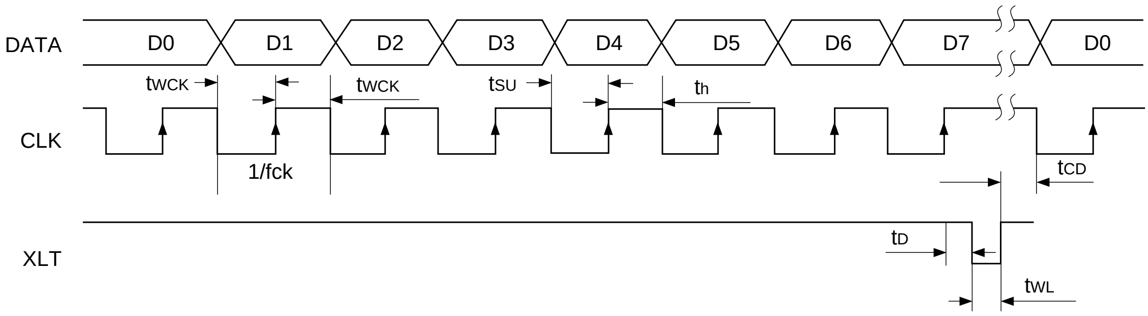
Fig. 7. Internal waveform

3. $2X (“TZC” at SENS pin (Pin 24))

These commands deal with turning the tracking servo and sled servo ON/OFF, and creating the jump pulse and fast forward pulse during access operations.

D7	D6	D5	D4	D3 D2	D1 D0
0	0	1	0	Tracking control 00: OFF 01: Servo ON 10: F-JUMP 11: R-JUMP ↓ TM1, TM3, TM4	Sled control 00: OFF 01: Servo ON 10: F-FAST FORWARD 11: R-FAST FORWARD ↓ TM2, TM5, TM6

CPU Serial Interface Timing Chart



(Vcc = 3.0V)

Item	Symbol	Min.	Type.	Max.	Unit
Clock frequency	fck			1	MHz
Clock pulse width	fwck	500			ns
Setup time	tsu	500			ns
Hold time	th	500			ns
Delay time	tD	500			ns
Latch pulse width	tWL	1000			ns
Data transfer interval	tCD	1000			ns

System Control

Item	ADRESS	DATA				SENS output
	D7 D6 D5 D4	D3	D2	D1	D0	
Focus Control	0 0 0 0	FS4 Focus ON = 1, OFF = 0	DEFECT (FS3) Disable = 1 Enable = 0	FS2 Search ON = 1, OFF = 0	FS1 Search Up = 1, Down = 0	FZC
Tracking Control	0 0 0 1	TG1, TG2 ON = 1, OFF = 0	Brake ON = 1, OFF = 0	Sled Kick + 2	Sled Kick + 1	DEFECT
Tracking Mode	0 0 1 0	Tracking Mode *1		Sled Mode *2		TZC
Select	0 0 1 1	Prohibited				—

*1 TRACKING MODE

	D3	D2
OFF	0	0
ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

*2 SLED MODE

	D1	D0
OFF	0	0
ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

Serial Data Truth Table

Serial Data	Hex	Functions			
FOCUS CONTROL		FS = 4321			
		FS4	DEFECT	FS2	FS1
0 0 0 0 0 0 0 0	$00	0	E	0	0
0 0 0 0 0 0 0 1	$01	0	E	0	1
0 0 0 0 0 0 1 0	$02	0	E	1	0
0 0 0 0 0 0 1 1	$03	0	E	1	1
0 0 0 0 0 1 0 0	$04	0	D	0	0
0 0 0 0 0 1 0 1	$05	0	D	0	1
0 0 0 0 0 1 1 0	$06	0	D	1	0
0 0 0 0 0 1 1 1	$07	0	D	1	1
0 0 0 0 1 0 0 0	$08	1	E	0	0
0 0 0 0 1 0 0 1	$09	1	E	0	1
0 0 0 0 1 0 1 0	$0A	1	E	1	0
0 0 0 0 1 0 1 1	$0B	1	E	1	1
0 0 0 0 1 1 0 0	$0C	1	D	0	0
0 0 0 0 1 1 0 1	$0D	1	D	0	1
0 0 0 0 1 1 1 0	$0E	1	D	1	0
0 0 0 0 1 1 1 1	$0F	1	D	1	1

DEFECT
E: enable
D: disable

TRACKING MODE	Hex	TM = 6 5 4 3 2 1
0 0 1 0 0 0 0 0	$20	0 0 0 0 0 0
0 0 1 0 0 0 0 1	$21	0 0 0 0 1 0
0 0 1 0 0 0 1 0	$22	0 1 0 0 0 0
0 0 1 0 0 0 1 1	$23	1 0 0 0 0 0
0 0 1 0 0 1 0 0	$24	0 0 0 0 0 1
0 0 1 0 0 1 0 1	$25	0 0 0 0 1 1
0 0 1 0 0 1 1 0	$26	0 1 0 0 0 1
0 0 1 0 0 1 1 1	$27	1 0 0 0 0 1
0 0 1 0 1 0 0 0	$28	0 0 0 1 0 0
0 0 1 0 1 0 0 1	$29	0 0 0 1 1 0
0 0 1 0 1 0 1 0	$2A	0 1 0 1 0 0
0 0 1 0 1 0 1 1	$2B	1 0 0 1 0 0
0 0 1 0 1 1 0 0	$2C	0 0 1 0 0 0
0 0 1 0 1 1 0 1	$2D	0 0 1 0 1 0
0 0 1 0 1 1 1 0	$2E	0 1 1 0 0 0
0 0 1 0 1 1 1 1	$2F	1 0 1 0 0 0

Initial State (resetting state)

Item	ADDRESS				DATA				HEXADECIMAL
	D7	D6	D5	D4	D3	D2	D1	D0	
Focus Control	0	0	0	0	0	0	0	0	$00
Tracking Control	0	0	0	1	0	0	0	0	$10
Tracking Mode	0	0	1	0	0	0	0	0	$20
Select	0	0	1	1	0	1	1	1	$37
					1	0	0	0	$38

The above data means the following operation modes.

Focus Control	Focus off, Defect enable, Focus Search off, Focus Search down
Tracking Control	TG1 – TG2 off, Brake off, Sled Kick + 2 off, Sled Kick + 1 off
Tracking Mode	Tracking off, Sled off

Notes on Operation

1. FSET pin
   The FSET pin determines the fc for the focus and tracking high-frequency phase compensation.

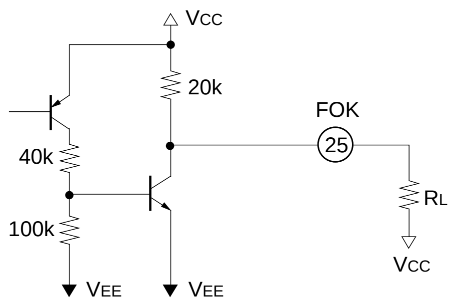
2. ISET pin
   ISET current = 1.27V/R
   = Focus search current
   = Tracking jump current
   = Sled kick current ($1X: PS1 = PS0 = 0) $\times \frac{1}{2}$
   Use the setting resistance within the range of 120kΩ to 240kΩ. If the resistance value is out of this range, the oscillation may be occurred in the ISET block.

3. FE (focus error)/TE (tracking error) gain changing method
   1) High gain: Resistance between FE pins (pins 6 and 7) 100kΩ → Large
      Resistance between TE pins (pins 12 and 13) 100kΩ → Large
   2) Low gain: A signal, whose resistance is divided between Pins 1 and 2, is input to FE.
      The external variable resistor of TEO pin is used for TE.
      The anti-shock circuit always operates in the CXA1982Q so that TG1 and TG2 (address 1 : D3) should be set to 1 for tracking adjustment to prevent this effect.
      When the anti-shock function is not used, Pin 45 (ATSC) should be fixed to VC.

4. Input voltage at Pins 19 to 22 of the microcomputer interface should be as follows:
   V_{IH} $V_{CC} \times$ 90% or more
   V_{IL} $V_{CC} \times$ 10% or less

5. Focus OK circuit
   1) Refer to the "Description of Operation" for the time constant setting of the focus OK amplifier LPF and the mirror amplifier HPF.
   2) The equivalent circuit of the output pin (FOK) is as shown below.

The FOK and comparator output are as follows:
Output voltage High: $V_{FOKH} \approx$ near V_{CC}
Output voltage Low: $V_{FOKL} \approx$ Vsat (NPN)



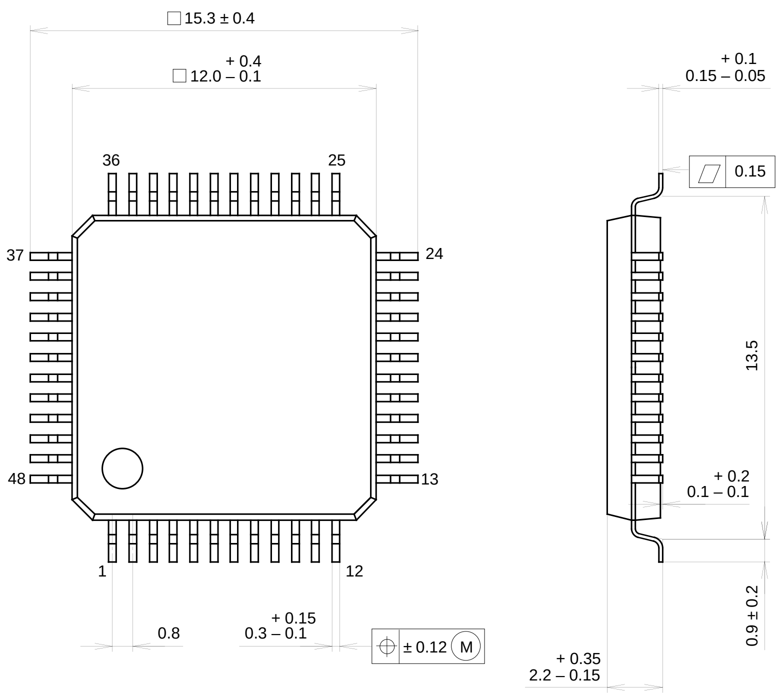
6. Sled amplifier
The sled amplifier may oscillate when used by the buffer amplifier. Use with a gain of approximately 20dB.

Sled/Tracking internal phase compensation and reference design material

	Item	SD	Measurement pin	Conditions	Typ.	Unit
FCS	1.2kHz gain	08	6	C_{FLB} = 0.1µF C_{FGD} = 0.1µF	21.5	dB
	1.2kHz phase	08			63	deg
TRK	1.2kHz gain	25	13	C_{TGU} = 0.1µF	13	dB
	1.2kHz phase	25			–125	deg
	2.7kHz gain	25→13			26.5	dB
	2.7kHz phase	25→13			–130	deg

Package Outline Unit: mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g