SONY

CXA2101Q

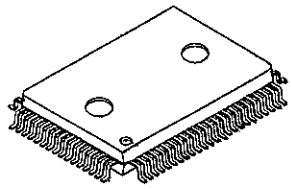
Multi-Component Processor (Base Band Video Signal Processor IC)

Description

The CXA2101Q is a bipolar IC which integrates the following functions on a single chip: base band signal processing, RGB signal processing, and video switching for 4 systems (including HV sync signal processing) using YCbCr inputs.

It was developed for multiscan TVs, and enables high-end TV systems to be configured.

80 pin QFP (Plastic)



Features

- I^2C bus compatible
- Multiscan supported
- Normal, PAL-FF, HD-TV supported
- On-chip video switching for 4 systems
- On-chip automatic sync signal identification circuit (with fixed mode)
- On-chip sync separation circuit (HD supported)
- On-chip CbCr input offset adjustment circuit
- On-chip LTI, CTI circuits
- On-chip AKB system
- YCbCr input for 1 system, external YCbCr input for 1 system
- Analog RGB input for 2 systems
- Analog RGB1 forced OFF mode supported

Absolute Maximum Ratings

• Supply voltage	Vcc	12	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	PD	2	W

(When mounted on single-layer circuit board with dimensions of 76mm × 114mm × 1.6thick)

Recommended Operating Conditions

Supply voltage	Vcc	8.5 to 9.5	V

Applications

- Multiscan TVs
- LCD projector TVs

Structure

Bipolar silicon monolithic IC

Supply voltage

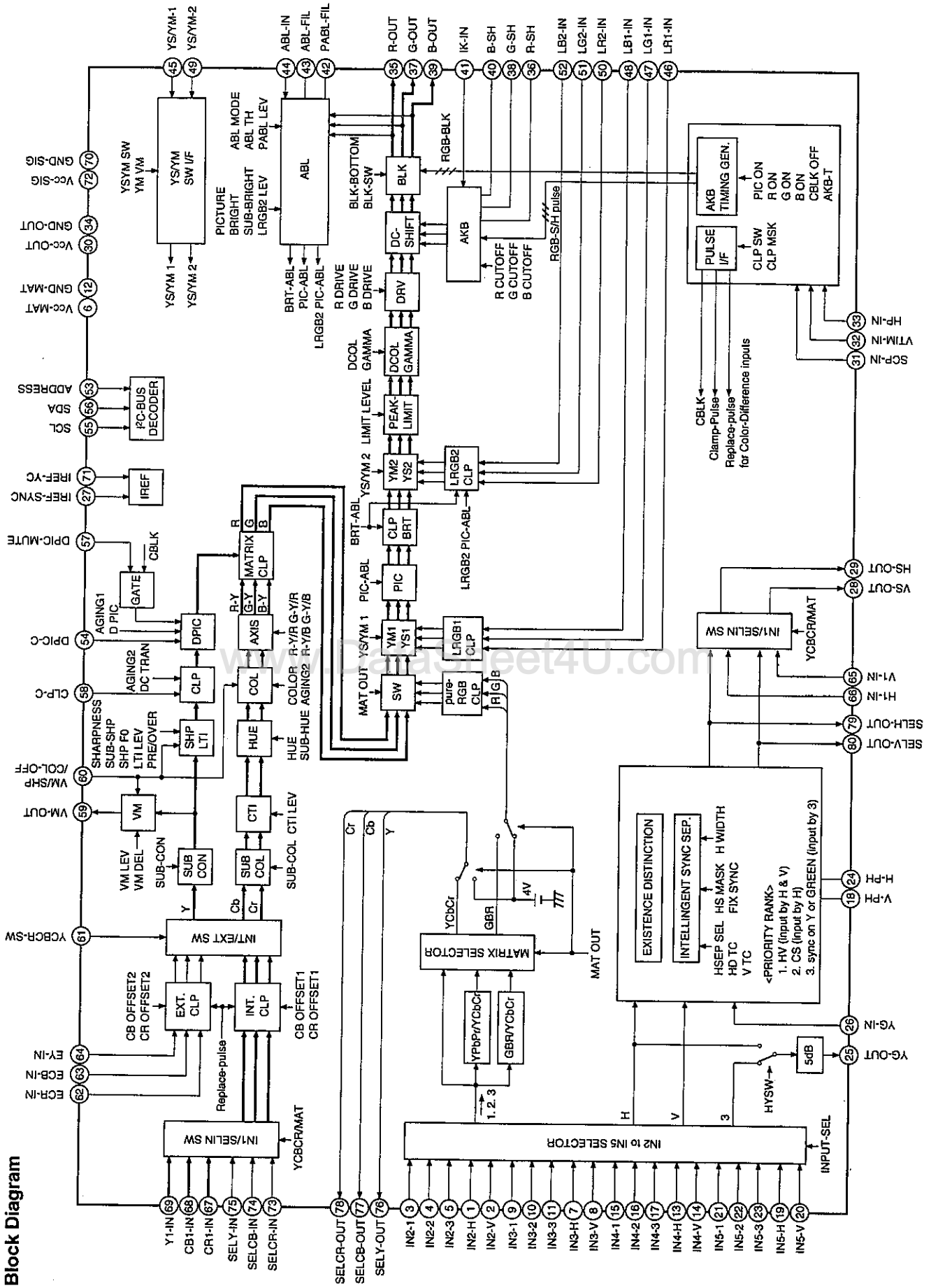
9V

Power consumption

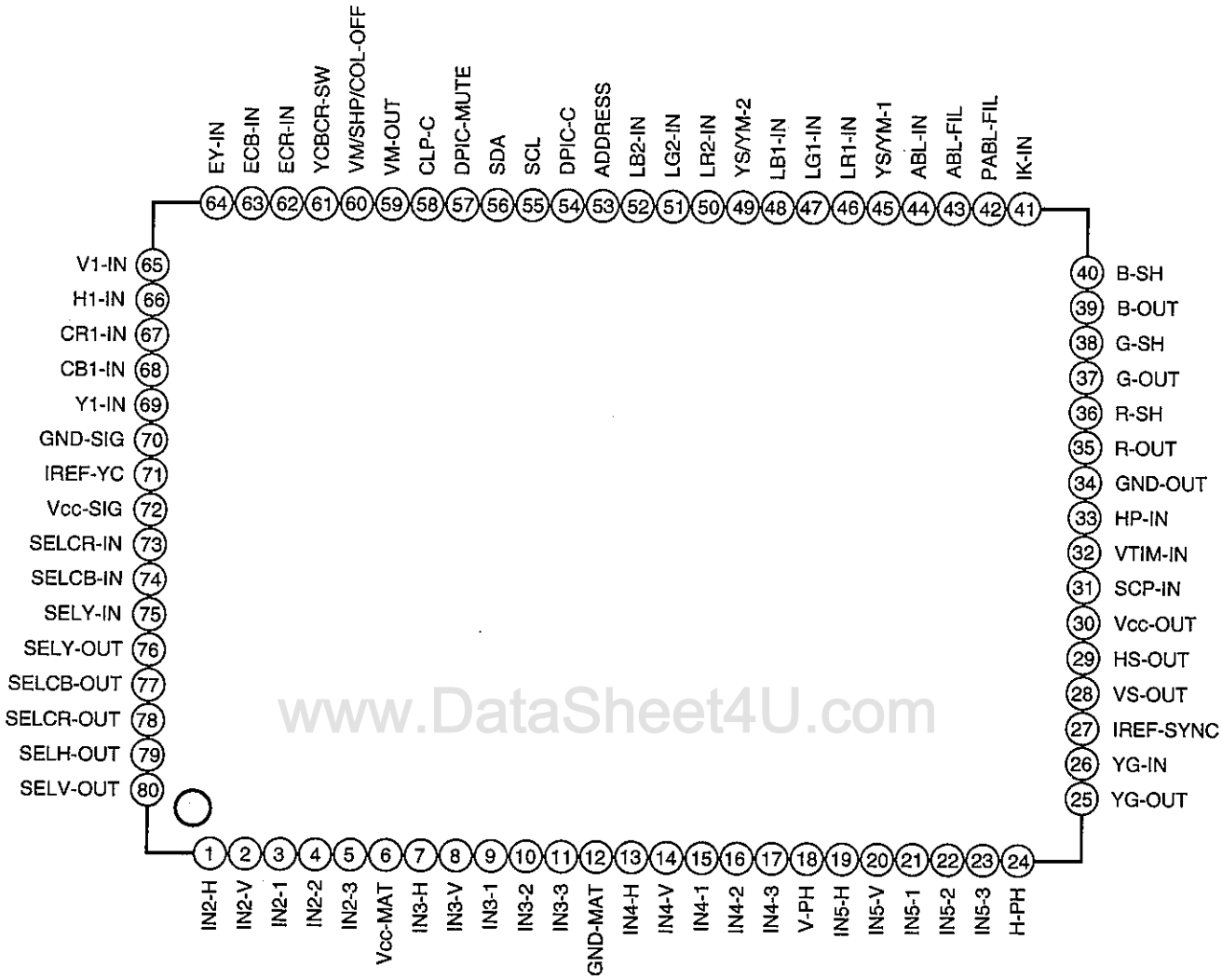
1.15W

E97718A83-PS

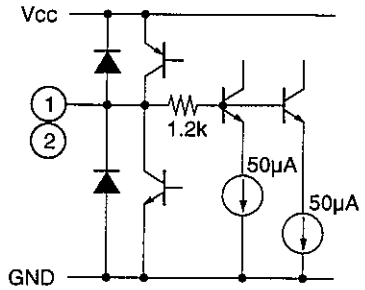
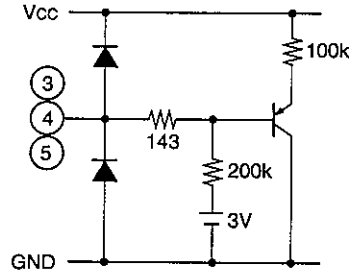
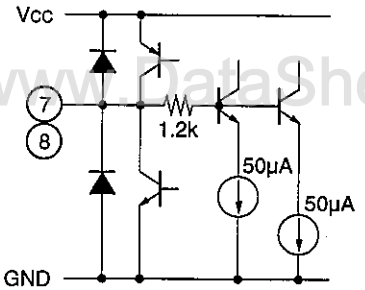
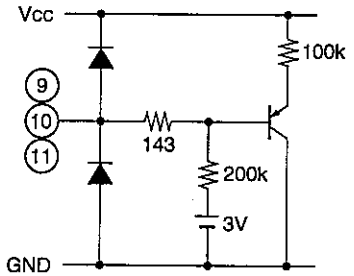
Block Diagram



Pin Configuration



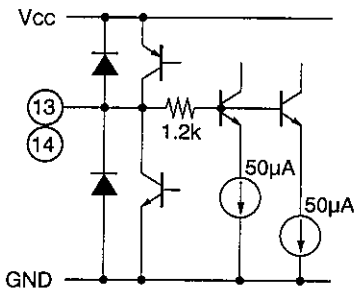
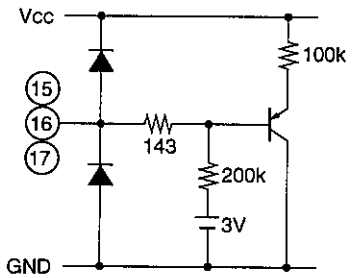
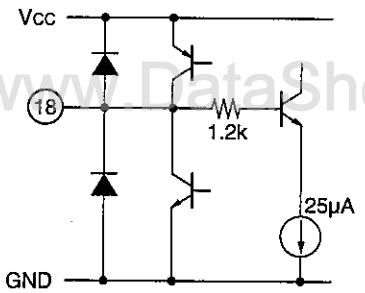
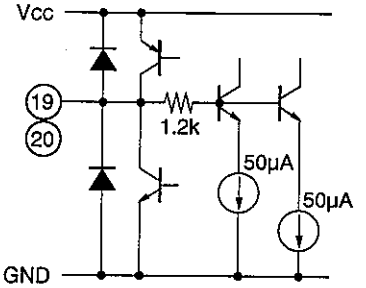
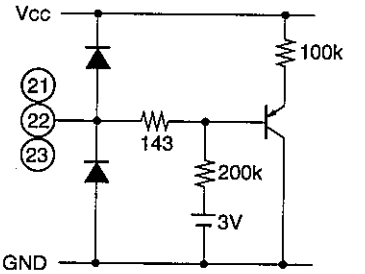
Pin Description

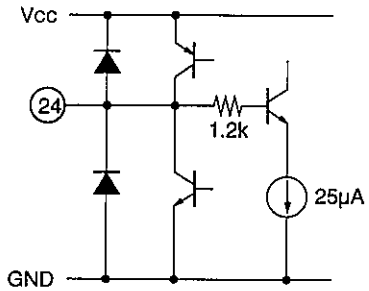
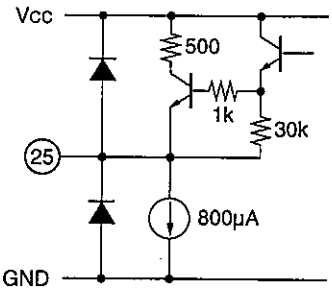
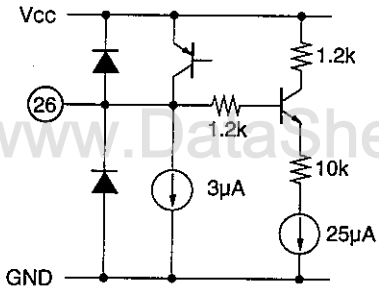
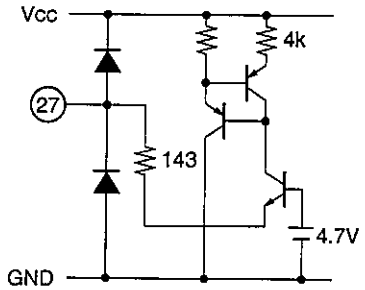
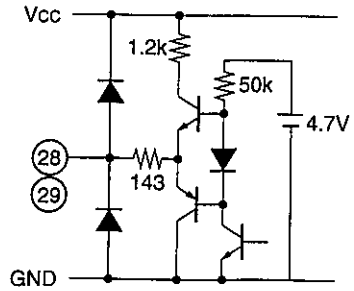
Pin No.	Symbol	Equivalent circuit	Description
1 2	IN2-H IN2-V		IN2-H: Separate H sync or CS input. IN2-V: Separate V sync signal input. Input the signals through a clamping capacitor. The bottom level is clamped to 2.5V. Both positive and negative polarities are supported. Input the signals at the level shown below. $0.5Vp\text{-}p \leq \frac{IN2\text{-}H}{IN2\text{-}V} \leq 5Vp\text{-}p$
3 4 5	IN2-1 IN2-2 IN2-3		IN2 system signal inputs. Input the signals through a capacitor. The pin voltage is biased to 3V. Refer to the input pin correspondence table. Set the Y input level to 0.7Vp-p and color difference input level to 0.7Vp-p using 100% color bar signals. In the case of sync on Y and sync on Green, input the signal at a sync level of 0.3Vp-p.
6	Vcc-MAT		Selector system and sync processing system power supply.
7 8	IN3-H IN3-V		IN3-H: Separate H sync or CS input. IN3-V: Separate V sync signal input. Input the signals through a capacitor. The bottom level is clamped to 2.5V. Both positive and negative polarities are supported. Input the signals at the level shown below. $0.5Vp\text{-}p \leq \frac{IN3\text{-}H}{IN3\text{-}V} \leq 5Vp\text{-}p$
9 10 11	IN3-1 IN3-2 IN3-3		IN3 system signal inputs. Input the signals through a capacitor. The pin voltage is biased to 3V. Refer to the input pin correspondence table. Set the Y input level to 0.7Vp-p and color difference input level to 0.7Vp-p using 100% color bar signals. In the case of sync on Y and sync on Green, input the signal at a sync level of 0.3Vp-p.

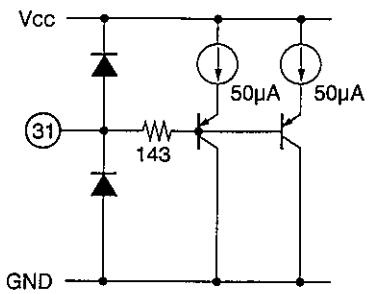
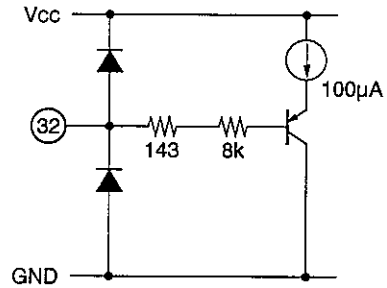
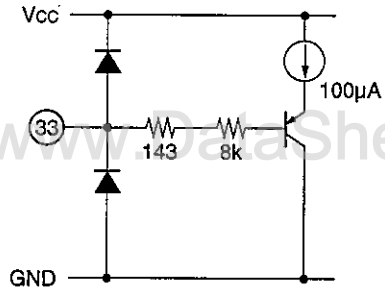
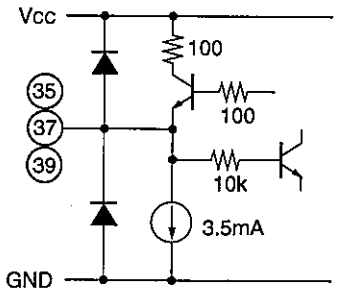
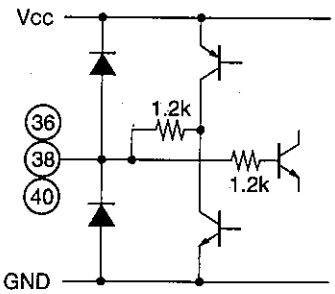
Input Pin Correspondence Table (by input signal)

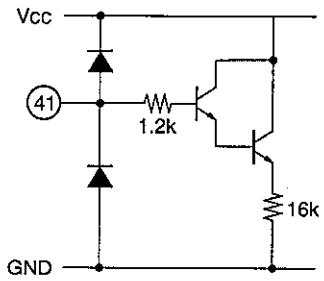
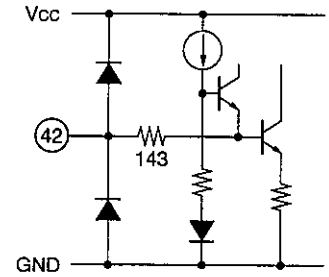
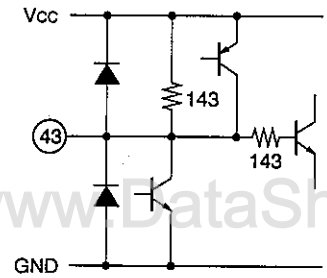
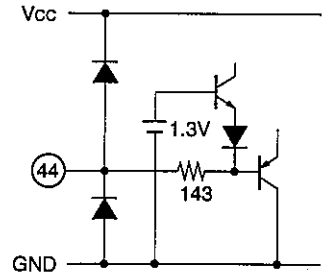
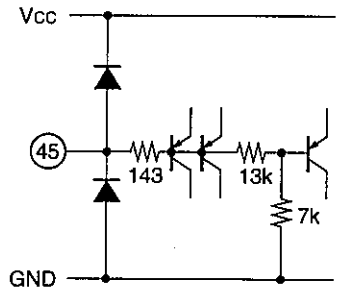
Normal	HD	Primary color	IN2			IN3			IN4			IN5		
			1	2	3	1	2	3	1	2	3	1	2	3
Y	Y_{HD}	G	×	×	O	×	×	O	×	×	O	×	×	O
Cb	Pb	B	×	O	×	×	O	×	×	O	×	×	O	×
Cr	Pr	R	O	×	×	O	×	×	O	×	×	O	×	×

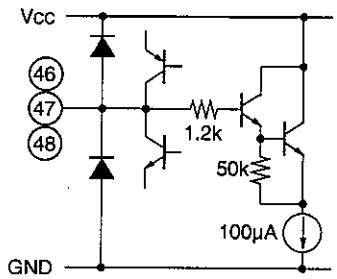
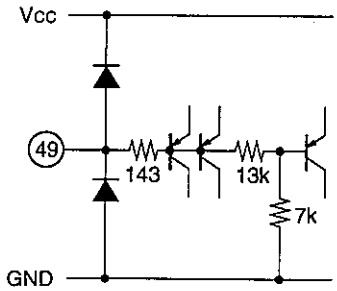
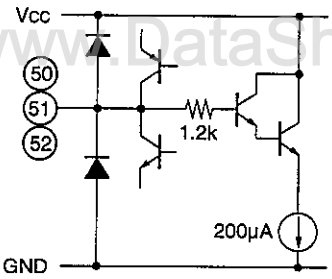
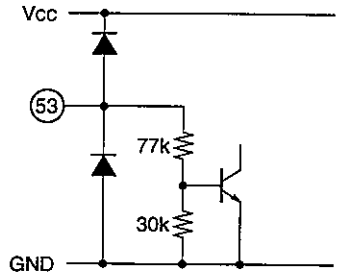
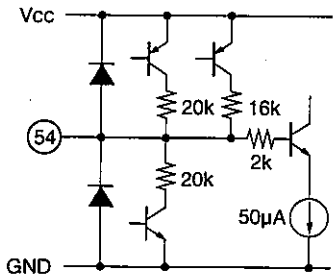
O = Input enabled; × = input disabled

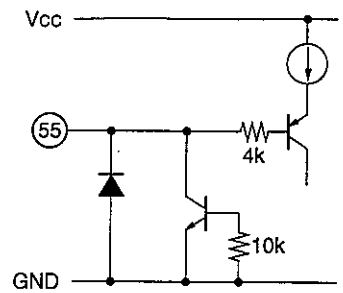
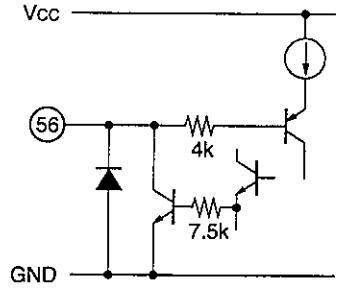
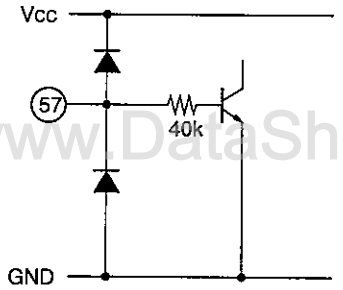
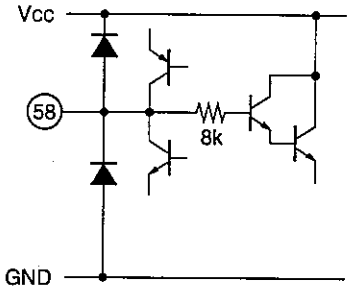
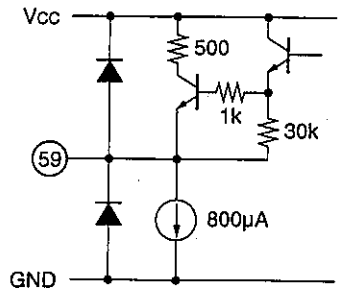
Pin No.	Symbol	Equivalent circuit	Description
12	GND-MAT		GND for selector block and sync processing block.
13	IN4-H		IN4-H: Separate H sync or CS input. IN4-V: Separate V sync signal input. Input the signals through a clamping capacitor. The bottom level is clamped to 2.5V. Both positive and negative polarities are supported. Input the signals at the level shown below. $0.5Vp\text{-}p \leq \frac{IN4\text{-}H}{IN4\text{-}V} \leq 5Vp\text{-}p$
14	IN4-V		
15 16 17	IN4-1 IN4-2 IN4-3		IN4 system signal inputs. Input the signals through a capacitor. The pin voltage is biased to 3V. Refer to the input pin correspondence table. Set the Y input level to 0.7Vp-p and color difference input level to 0.7Vp-p using 100% color bar signals. In the case of sync on Y and sync on Green, input the signal at a sync level of 0.3Vp-p.
18	V-PH		Capacitor connection for holding V sync peak.
19	IN5-H		IN5-H: Separate H sync or CS input. IN5-V: Separate V sync signal input. Input the signals through a clamping capacitor. The bottom level is clamped to 2.5V. Both positive and negative polarities are supported. Input the signals at the level shown below. $0.5Vp\text{-}p \leq \frac{IN5\text{-}H}{IN5\text{-}V} \leq 5Vp\text{-}p$
20	IN5-V		
21 22 23	IN5-1 IN5-2 IN5-3		IN5 system signal inputs. Input the signals through a capacitor. The pin voltage is biased to 3V. Refer to the input pin correspondence table. Set the Y input level to 0.7Vp-p and color difference input level to 0.7Vp-p using 100% color bar signals. In the case of sync on Y and sync on Green, input the signal at a sync level of 0.3Vp-p.

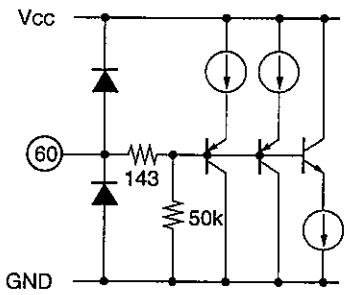
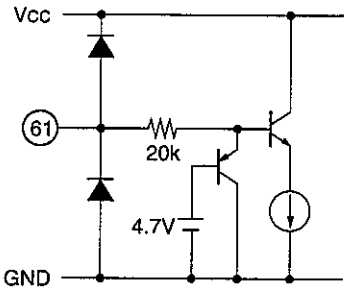
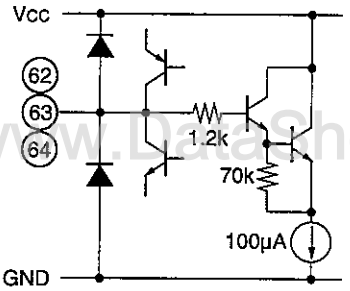
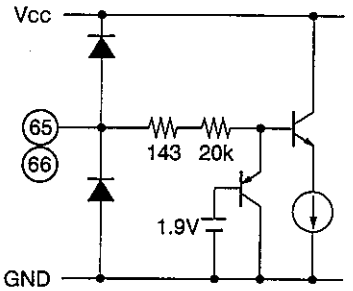
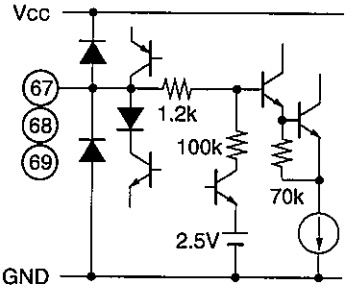
Pin No.	Symbol	Equivalent circuit	Description
24	H-PH		Capacitor connection for holding H sync peak.
25	YG-OUT		Composite video signal output for sync separation. The signal selected by I²C bus "HYSW" is amplified to 5dB and output.
26	YG-IN		Composite video signal input for sync separation. Normally, the signal output at Pin 25 is input through a clamping capacitor. The sync tip is clamped to 2.5V. Input the signal at a sync level of 0.5 to 0.6Vp-p.
27	IREF-SYNC		For setting the reference current inside the IC (mainly, sync signal processing system). Connect to GND via the 47kΩ resistor (such as a metal film resistor) with an error of less than 1%. The pin voltage is approximately 4.6V.
28 29	VS-OUT HS-OUT		Either IN1 system HV or IN2 to IN5 system selector output HV signals are selected by I²C bus "YCBCR/MAT" and output with a positive polarity. $V_{OH} \geq 3.5V$ $V_{OL} \leq 0.6V$
30	Vcc-OUT		RGB system power supply.

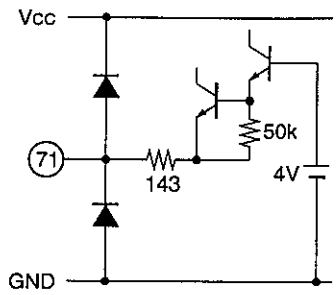
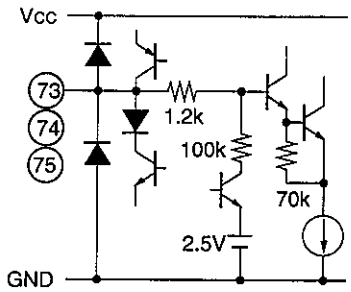
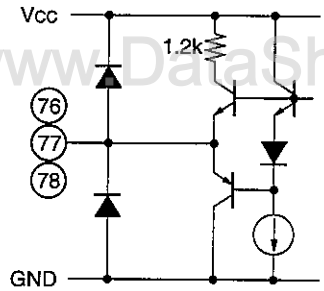
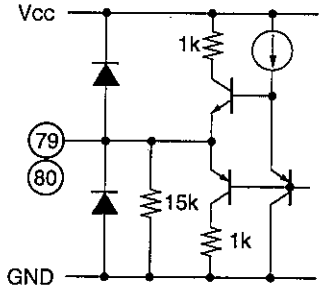
Pin No.	Symbol	Equivalent circuit	Description
31	SCP-IN		Sand castle pulse input. Used for AKB reference pulse generation and RGBOUT blanking. The input SCP definition is given on page 30. CLAMP ON $V_{IH} \geq 4V$ OFF $V_{IL} \leq 3V$ Composite BLK ON $V_{IH} \geq 2V$ OFF $V_{IL} \leq 1V$
32	VTIM-IN		V timing pulse input. Used to generate AKB reference pulses in the V compression mode (I^2C bus "AKB-T=1"). Ground the pin when it is not going to be used. $V_{IH} \geq 3.5V$ $V_{IL} \leq 1.5V$
33	HP-IN		H pulse input. Used to generate AKB reference pulses in the V compression mode (I^2C bus "AKB-T=1"). Also used to generate replacement pulses for the color difference input clamping circuit. Ground the pin when it is not going to be used. $V_{IH} \geq 3.5V$ $V_{IL} \leq 1.5V$
34	GND-OUT		RGB system ground.
35 37 39	R-OUT G-OUT B-OUT		RGB signal outputs. Signals are output at 2.6Vp-p when 100 IRE white signals are input (only when the I^2C bus has been set to the data on page 16).
36 38 40	R-SH G-SH B-SH		Sample and hold for AKB of RGB. These connect the capacitors to GND. When AKB is not used, the RGB DC level can be set by applying DC to each pin.

Pin No.	Symbol	Equivalent circuit	Description
41	IK-IN		The reference pulse is returned to this pin. Cathode current Ik of the CRT is converted into a voltage and input to the pin through a capacitor. It is clamped to 3.4V at the V retrace timing of the V blanking portion.
42	PABL-FIL		Peak hold for peak ABL. This pin connects a capacitor and resistor to GND to configure a low-pass filter.
43	ABL-FIL		This pin connects a capacitor to configure a low-pass filter for the ABL control signals.
44	ABL-IN		ABL control signal input. It operates as an average value type. The ABLIN threshold voltage can be varied by I²C bus "ABL-TH".
45	YS/YM-1		YM1/YS1 control signal input. Ternary inputs are supported. The pin also serves to set VM off when YM or YS has reached the respective value. The mode in which VM is not set off by YM is established when I²C bus "YM-VM = 1" has been set. <YS1SW> YS1: ON $V_{IH} \geq 3V$ This selects LRGB1. YS1: OFF $V_{IL} \leq 1.5V$ This selects the internal RGB signals. <YM1SW> YM1: ON $V_{IH} \geq 1.1V$ This sets the internal RGB signals to –9.5dB. YM1: OFF $V_{IL} \leq 0.3V$ The internal RGB signals pass through at 0dB.

Pin No.	Symbol	Equivalent circuit	Description
46 47 48	LR1-IN LG1-IN LB1-IN		Analog RGB1 signal inputs. The 0.7Vp-p 100 IRE (no sync) signal is input through a capacitor. The pedestal is clamped to 4.9V.
49	YS/YM-2		YM2/YS2 control signal input. Ternary inputs are supported. The pin also serves to set VM off when YM or YS has reached the respective value. The mode in which VM is not set off by YM is established when I²C bus "YM-VM = 1" has been set. <YS2SW> YS2: ON $V_{IH} \geq 3V$ This selects LRGB2. YS2: OFF $V_{IL} \leq 1.5V$ This selects the internal RGB signals. <YM2SW> YM2: ON $V_{IH} \geq 1.1V$ This sets the internal RGB signals to –9.5dB. YM2: OFF $V_{IL} \leq 0.3V$ The internal RGB signals pass through at 0dB.
50 51 52	LR2-IN LG2-IN LB2-IN		Analog RGB2 signal inputs. The 0.7Vp-p 100 IRE (no sync) signal is input through a capacitor. The pedestal is clamped to 4.6V (I²C bus "LRGB2-LEVEL = F").
53	ADDRESS		I²C bus slave address setting. 86h: $V_{IH} \geq 3.5V$ 84h: $V_{IL} \leq 1.5V$
54	DPIC-C		This connects a capacitor to GND for detecting black in the dynamic picture (black expansion).

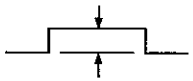
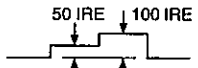
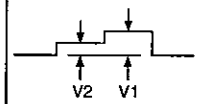
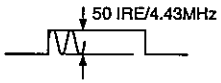
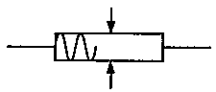
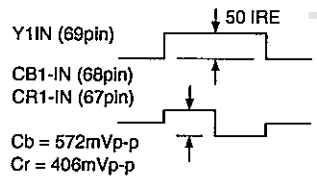
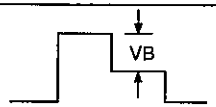
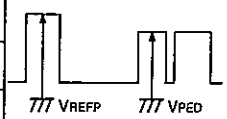
Pin No.	Symbol	Equivalent circuit	Description
55	SCL		Input for SCL (Serial Clock) complying with I²C bus standard. $V_{IH} \geq 3V$ $V_{IL} \leq 1.5V$
56	SDA		Input for SDA (Serial Data) complying with I²C bus standard. $V_{IH} \geq 3V$ $V_{IL} \leq 1.5V$ $V_{OL} \leq 0.6V$
57	DPIC-MUTE		Muting of the dynamic picture (black expansion) can be controlled by this pin. MUTE: ON $V_{IH} \geq 1V$ MUTE: OFF $V_{IL} \leq 0.4V$
58	CLP-C		Y system clamping capacitor connecting pin. Also used as a pin to connect the capacitor which sets the DC transmission rate.
59	VM-OUT		VM output. The differential waveforms of the Y signal are output with a positive polarity. Their amplitude and phase can be adjusted by the I²C bus.

Pin No.	Symbol	Equivalent circuit	Description
60	VM/SHP/ COL-OFF		For turning off the VM, sharpness and color. Ternary inputs are supported. COL: OFF $V_{IH} \geq 4.3V$ ON $V_{IL} \leq 3V$ VM/SHP: OFF $V_{IH} \geq 2.8V$ ON $V_{IL} \leq 1.4V$
61	YCBCR-SW		This pin switches the signal which has been input to the INT/EXT switch. The external input is selected when it is high. EXT: ON $V_{IH} \geq 2V$ EXT: OFF $V_{IL} \leq 1V$
62 63 64	ECR-IN ECB-IN EY-IN		External YCbCr inputs. 0.7Vp-p 100 IRE signals (but only with 100% color bars for CbCr) are supplied for YCbCr together through a capacitor. In the case of sync on Y, reduce the sync level to 0.3Vp-p. The pedestal is clamped to 4.9V.
65 66	V1-IN H1-IN		HV inputs for IN1 system. Input the signals with a negative polarity. $V_{IH} \geq 3V$ $V_{IL} \leq 1V$
67 68 69	CR1-IN CB1-IN Y1-IN		YCbCr inputs of IN1 system. 0.7Vp-p 100 IRE signals (but only with 100% color bars for CbCr) are supplied for YCbCr together through a capacitor. In the case of sync on Y, reduce the sync level to 0.3Vp-p. The pedestal is clamped to 4.9V.
70	GND-SIG		GND for Y color difference signal processing system.

Pin No.	Symbol	Equivalent circuit	Description
71	IREF-YC		For setting the reference current inside the IC (mainly, Y color difference signal processing system). Connect to GND via the 22kΩ resistor (such as a metal film resistor) with an error of less than 1%. The pin voltage is approximately 2.6V.
72	Vcc-SIG		Power supply for Y color difference signal processing system.
73 74 75	SELCR-IN SELCB-IN SELY-IN		Input the selector output YCbCr (Pins 76, 77, 78) signals through a clamping capacitor. Signals are input at a 0.7Vp-p 100 IRE level (but only with 100% color bars for CbCr). The pedestal is clamped to 4.9V.
76 77 78	SELY-OUT SELCB-OUT SELCR-OUT		IN2 to IN5 selector outputs. YCbCr-converted signals are output. These pins can be connected to an external processor, etc. Signals are output at a level equivalent to 0dB compared with the IN2 to IN5 input level. The conversion types are shown on the pages with the description of operation. Select these signals with I²C bus "MAT-OUT."
79 80	SELH-OUT SELV-OUT		IN2 to IN5 selector HV outputs. $V_{OH} \geq 2.8V$ $V_{OL} \leq 0.4V$

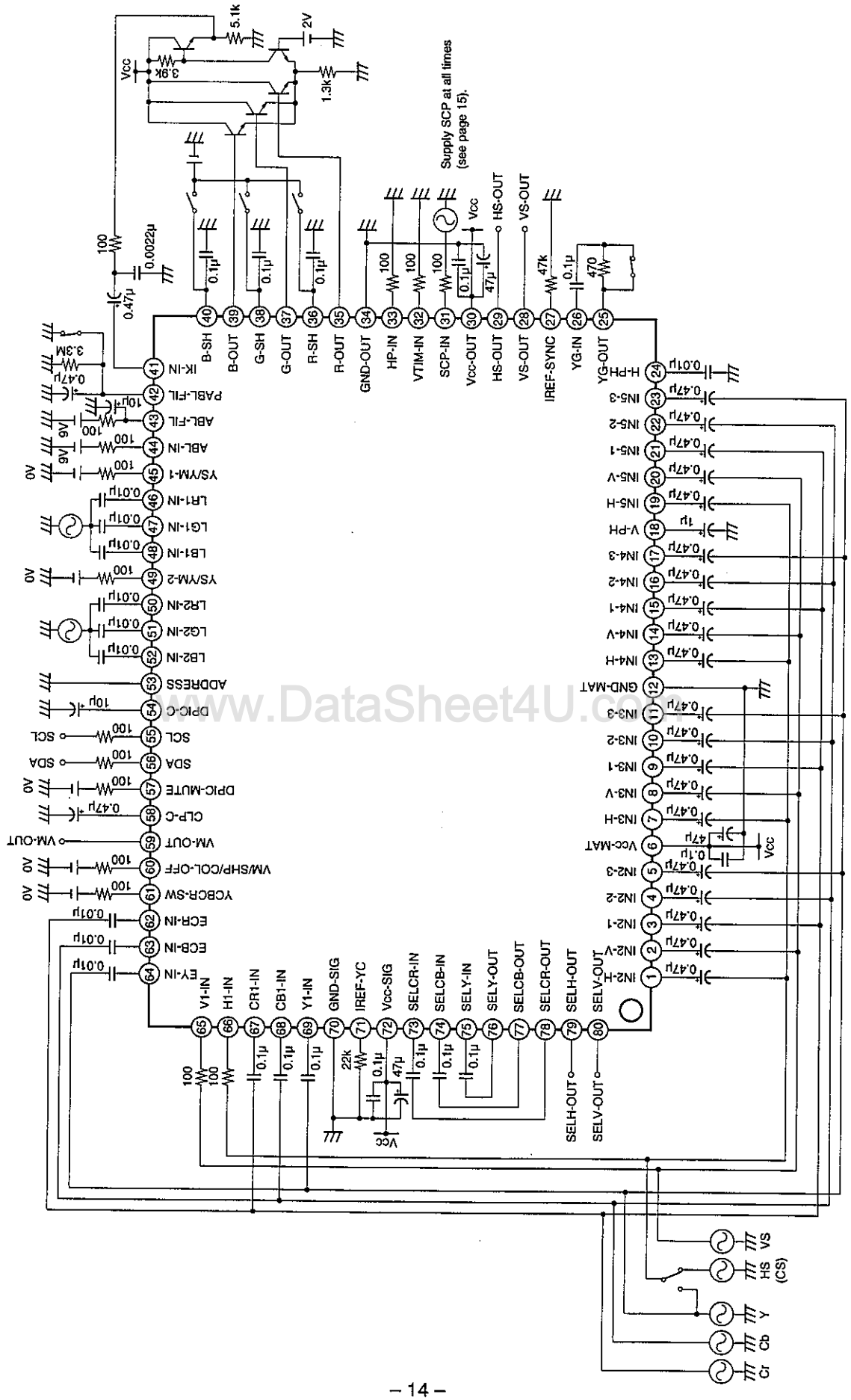
Electrical Characteristics

- Ta = 25°C, Vcc-MAT = Vcc-OUT = Vcc-SIG = 9V, GND-MAT = GND-MAT = GND-OUT = GND-SIG = 0V
- Measures the following after setting the I²C bus register as shown in "I²C BUS Register Initial Settings."

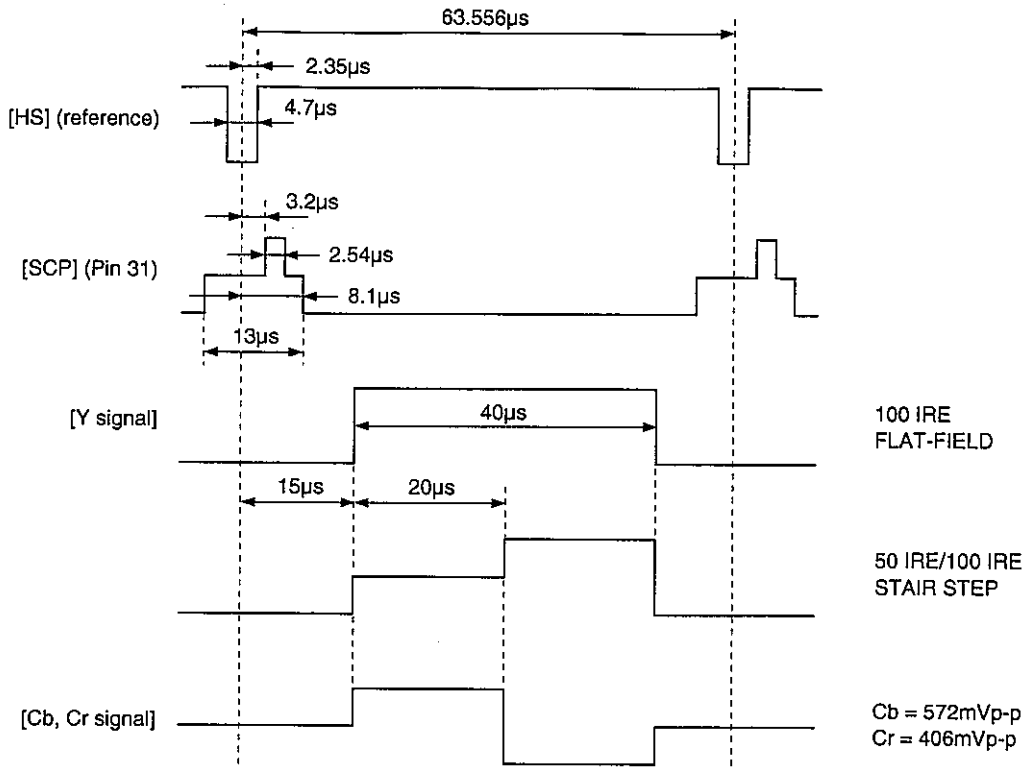
No.	Item	Symbol	Measurement conditions	Measurement pins	Measurement contents	Min.	Typ.	Max.	Unit
1	Video switch system current consumption	Icc-MAT		6	Measure the pin inflow current.	18	28	34	mA
2	RGB system current consumption	Icc-OUT		30		32	50	61	mA
3	Y color difference system current consumption	Icc-SIG		72		29	45	55	mA
4	RGB output	VRGB	 100 IRE signal input to Y1-IN (Pin 69)	35, 37, 39	Measure the output level.	2	2.6	3.1	Vp-p
5	RGB linearity	VLIN	 Staircase wave input to Y1-IN (Pin 69)	35, 37, 39	 $V_{LIN} = \frac{V1}{V2 \times 2} \times 100$	95	102	109	%
6	EY-IN gain	GEY	100 IRE signal input to EY-IN (Pin 64) YCBCR-SW (Pin 61) = 5V	37	Ratio of output level to VRGB	−1.5	−0.5	0.2	dB
7	LRGB1 gain	GL1	100 IRE signal input to LG1-IN (Pin 47) YS/YM-1 (Pin 45) = 5V	37		−1.7	−0.1	1.5	dB
8	LRGB2 gain	GL2	100 IRE signal input to LG2-IN (Pin 51) YS/YM-2 (Pin 49) = 5V	37		−2.5	−1	1	dB
9	IN2-3 gain	GSEL	100 IRE signal input to IN2-3 (Pin 5)	76	Ratio of output level to input level	−0.3	−0.1	0	dB
10	VM output	VVM	 Sine wave input to Y1-IN (Pin 64)	59	 Measure the VMOUT level.	1.6	2	2.4	Vp-p
11	HUE center	θB		39	 $\theta_B = \tan^{-1} \frac{\text{VB level with Cr input}}{\text{VB level with Cb input}}$	−4	2	8	deg.
12	BRIGHT center R channel	VBRT-R		35	 $V_{BRT} = V_{PED} - V_{REFP}$	−380	−260	−150	mV
13	BRIGHT center G channel	VBRT-G		37		−320	−240	−160	mV
14	BRIGHT center B channel	VBRT-B		39		−380	−260	−150	mV

Electrical Characteristics Measurement Circuit

Signal sources ⏦ are all GND unless otherwise specified in the Measurement conditions column of the Electrical Characteristics.



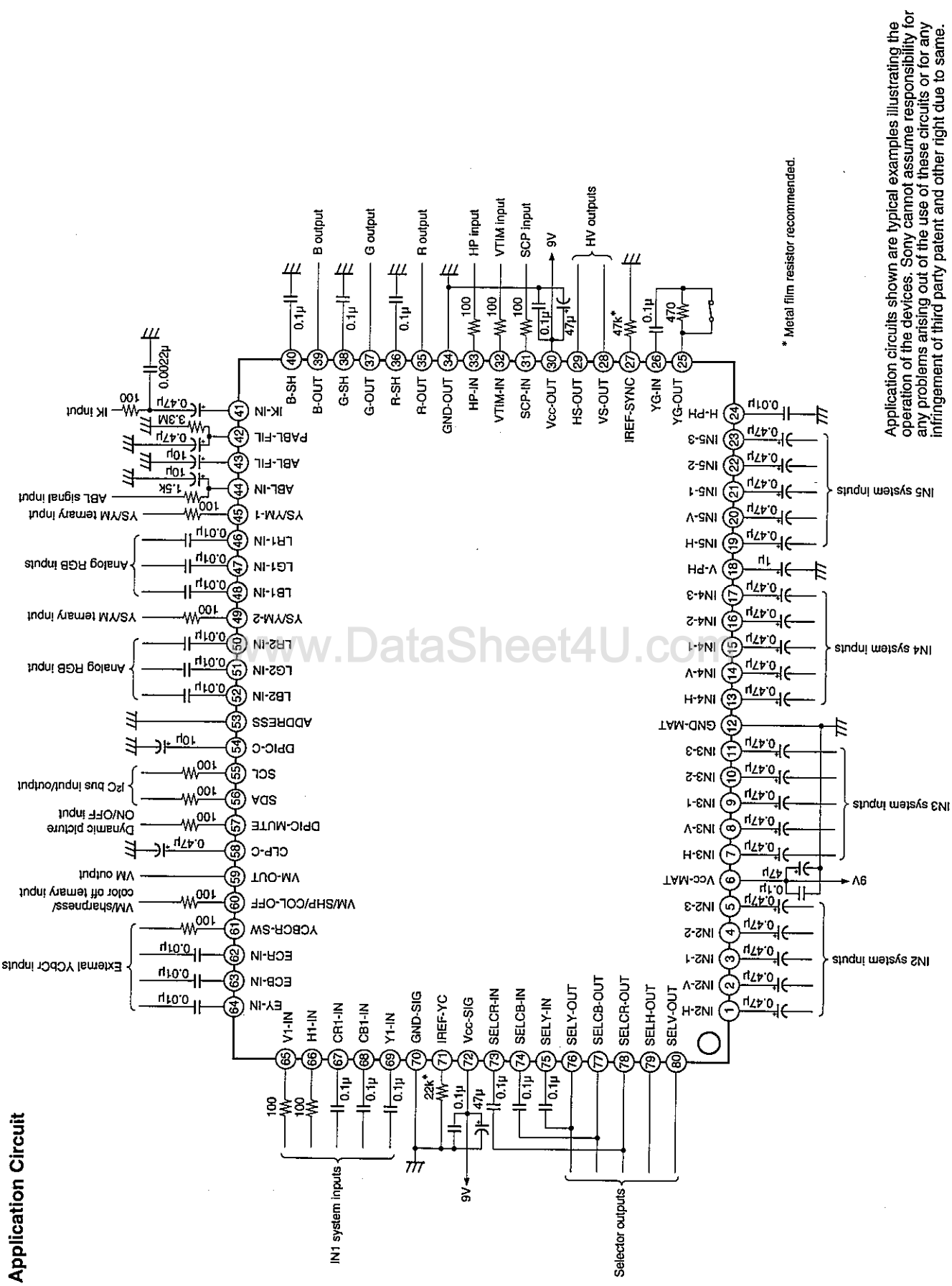
Electrical Characteristics Measurement Input Signals



Electrical Characteristics Measurement Conditions "I²C BUS Register Initial Settings"

Register name	No. of bits	Setting value	Description	Register name	No. of bits	Setting value	Description
PICON	1	1	Picture mute off	B-CUTOFF	6	1Fh	Center
RON	1	1	R output on	SUB-BRIGHT	6	1Fh	Center
GON	1	1	G output on	HSEP-SEL	1	0	Forced slice
BON	1	1	B output on	FIX-SYNC	2	0	Automatic identification
CBLKOFF	1	0	CBLK and AKB both on	V-TC	2	3	Maximum
AKB-T	1	0	Normal	H-WIDTH	2	0	THROUGH mode
BLKSW	1	0	Regular mode	HD-TC	1	1	Time constant other than HD-TV system
INPUT-SEL	2	0	IN2 system selected	HS-MASK	1	1	Added
MAT-OUT	2	0	THROUGH1 mode selected	CR-OFFSET 1	4	7h	Center
YCbCr/MAT	1	0	IN1 system selected	CB-OFFSET 1	4	7h	Center
HYSW	1	0	3 selected from IN2 to IN5	CR-OFFSET 2	4	7h	Center
PICTURE	6	3Fh	Maximum value	CB-OFFSET 2	4	7h	Center
LIMIT-LEVEL	2	0	Off	SUB-CON	4	7h	Center
HUE	6	1Fh	Center	SUB-COL	4	7h	Center
SYSTEM	2	0	Normal	SUB-HUE	4	7h	Center
COLOR	6	1Fh	Center	CTI-LEVEL	2	0	Off
AGING1	1	0	Off	R-Y/R	4	6h	NTSC-JPN
AGING2	1	0	Off	R-Y/B	4	Ch	NTSC-JPN
BRIGHT	6	1Fh	Center	G-Y/R	4	Ah	NTSC-JPN
YMYS1SW	1	0	Valid	G-Y/B	4	5h	NTSC-JPN
YM-VM	1	0	No muting of VM by YM	LRCB2-LEVEL	4	Fh	Maximum
SHARPNESS	6	1Fh	Center	GAMMA	4	0h	Off
R-DRIVE	6	26h	Center	PABL-LEVEL	4	Fh	Maximum
D-COL	1	0	Off	BLK-BOTTOM	4	0h	Minimum
G-DRIVE	6	26h	Center	SUB-SHP	2	0	Minimum
CLP-SW	1	1	SCP CLP only used	SHP-F0	2	0	Minimum
B-DRIVE	6	26h	Center	PRE/OVER	2	0	1 : 1
CLP-MSK	2	0	Normal	LTI-LEVEL	2	0	Off
R-CUTOFF	6	1Fh	Center	VM-LEV	2	3	Maximum
ABL-MODE	2	0	Picture-only mode	VM-DEL	2	3	Maximum
G-CUTOFF	6	1Fh	Center	DC-TRAN	2	0	100%
ABL-TH	2	0	Minimum	D-PIC	2	0	Off

Application Circuit



Definition of I²C BUS Registers

Slave Addresses

Slave Receiver 84h: ADDRESS (Pin 53) = Low, 86h: ADDRESS (Pin 53) = High
Slave Transmitte 85h: ADDRESS (Pin 53) = Low, 87h: ADDRESS (Pin 53) = High

Register Table

"*": Undefined

Control Register

Sub Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
xxx00000	0h	PICON	RON	GON	BON	CBLKOFF	AKB-T	BLKSW	0
xxx00001	1h	INPUT-SEL		MAT-OUT		YCbCr/MAT	HYSW	*	*
xxx00010	2h	PICTURE						LIMIT-LEVEL	
xxx00011	3h	HUE						SYSTEM	
xxx00100	4h	COLOR						AGING1	AGING2
xxx00101	5h	BRIGHT						YSYM1SW	YM-VM
xxx00110	6h	SHARPNESS						*	*
xxx00111	7h	R-DRIVE						D-COL	*
xxx01000	8h	G-DRIVE						CLPSW	*
xxx01001	9h	B-DRIVE						CLP-MSK	
xxx01010	Ah	R-CUTOFF						ABL-MODE	
xxx01011	Bh	G-CUTOFF						ABL-TH	
xxx01100	Ch	B-CUTOFF						*	*
xxx01101	Dh	SUB-BRIGHT						HSEP-SEL	*
xxx01110	Eh	FIX-SYNC		V-TC		H-WIDTH		HD-TC	HS-MASK
xxx01111	Fh	CR-OFFSET 1				CB-OFFSET 1			
xxx10000	10h	CR OFFSET 2				CB OFFSET 2			
xxx10001	11h	SUB-CON				SUB-COL			
xxx10010	12h	SUB-HUE				CTI-LEVEL		*	*
xxx10011	13h	R-Y/R				R-Y/B			
xxx10100	14h	G-Y/R				G-Y/B			
xxx10101	15h	LRGB2-LEVEL				GAMMA			
xxx10110	16h	PABL-LEVEL				BLK-BOTTOM			
xxx10111	17h	SUB-SHP		SHP-F0		PRE/OVER		LTI-LEVEL	
xxx11000	18h	VM-LEV		VM-DEL		DC-TRAN		D-PIC	

Status Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	1	1	1	1	EH	EV	IK

Description of Registers

PICON (1) : ON/OFF switch for RGB outputs including reference pulse
(Set to OFF mode at power-on)
0 = RGB output OFF (all blanking mode)
1 = RGB output ON

RON (1) : ON/OFF switch for R channel video output excluding reference pulse
(Valid when PICON = 1; set to OFF mode at power-on)
0 = R channel video output OFF (blanking mode, REF-P only output)
1 = R channel video output ON

GON (1) : ON/OFF switch for G channel video output excluding reference pulse
(Valid when PICON = 1; set to OFF mode at power-on)
0 = G channel video output OFF (blanking mode, REF-P only output)
1 = G channel video output ON

BON (1) : ON/OFF switch for B channel video output excluding reference pulse
(Valid when PICON = 1; set to OFF mode at power-on)
0 = B channel video output OFF (blanking mode, REF-P only output)
1 = B channel video output ON

CBLKOFF (1) : ON/OFF switch for H, V blanking of RGB output (set to ON mode at power-on)
AKB system is set to the OFF mode at the same time as the blanking is set off.
0 = CBLK ON; AKB ON
1 = CBLK OFF; AKB OFF
The pedestal potential when AKB is OFF can be set by the voltage applied to the R-SH, G-SH and B-SH pins for R, G, B, respectively.

AKB-T (1) : Selection of timing pulse which generates reference pulse
(Set to NORMAL mode at power-on)
0 = NORMAL mode (reference pulse generated by SCP input only)
1 = V compression mode (reference pulse generated from VTIM-IN, HP-IN)

BLKSW (1) : Selection of H, V blanking system for RGB-OUT
(Set to 0 at power-on.)
0 = Normal blanking mode (blanking up to $V_{CE\ (SAT)}$ level)
1 = Blanking at value set by BLK-BOTTOM
(Refer to the description of the BLK-BOTTOM register.)

INPUT-SEL (2) : Selection of four system inputs: IN2, IN3, IN4 and IN5
0 = IN2 selected
1 = IN3 selected
2 = IN4 selected
3 = IN5 selected

MAT-OUT (2) : Selection of type matrix conversion; selected signal is output from Pins 76, 77 and 78. A DC voltage of approximately 4V is output only for 3 of these modes.
0 = THROUGH1 (when YCbCr is input)
1 = Matrix conversion of YPbPr to YCbCr signal
2 = Matrix conversion of GBR to YCbCr signal
3 = THROUGH2 (GBR is input directly to internal RGB system)

YCbCr/MAT (1) : Selection of IN1 system signal or SELIN system signal for signal sent to Y color difference processing system. H and V sync signals are simultaneously selected and output.
0 = IN1 system input selected
1 = SELIN system input selected

HYSW (1) : Switch for switching signal output to YG-OUT pin
0 = For a sync on Y, sync on Green input
1 = For a composite sync input

PICTURE (6) : Picture gain control; valid for input signals except for LRGB2.
0h = –16dB
3Fh = 0dB

LIMIT-LEVEL (2) : Limiter to cope with excessively high inputs.
0 = OFF
1 = 104 IRE
2 = 113 IRE
3 = 122 IRE

HUE (6) : Hue control
0h = –33° Flesh color appears red.
1Fh = CENTER
3Fh = +33° Flesh color appears green.

SYSTEM (2) : Signal frequency band switching; select the band in accordance with the TV system.
0 = NORMAL
1 = FF
2 = HD
3 = FIX-HD (setting which gives greater importance to frequency response than 2)

COLOR (6) : Color gain control
0h = Color OFF
1Fh = 0dB
3Fh = +6.2dB

AGING1 (1) : White output aging mode ON/OFF switch
74 IRE flat signal is output from Y system
0 = OFF
1 = ON

AGING2 (1) : All black output aging mode ON/OFF switch
Input signals are cut off inside the Y/color difference signal processing system. As a result, the signals which were input to the RGB system are output.
0 = OFF
1 = ON

BRIGHT (6) : Main brightness control
Output DC bias setting for RGBOUT
0h = –13 IRE
1Fh = CENTER
3Fh = +13 IRE

YSYM1SW (1) : On/off switching for YS/YM-1 input pin (Pin 45)
0 = On
1 = Off

YM-VM (1) : Mute function ON/OFF switch for VM-OUT (Pin 59) in YM ON block
Setting takes effect for both YS/YM-1 (Pin 45) and YS/YM-2 (Pin 49)
0 = OFF: no muting
1 = ON: muting

SHARPNESS (6) : Sharpness gain control (when SYSTEM = 0, SUB-SHP = 0, SHP-F0 = 1)
0h = –12dB
1Fh = 0dB
3Fh = +6dB

R-DRIVE (6) : R channel drive gain control
0h = –4.2dB
29h = 0dB
3Fh = +2.1dB

D-COL (1) : Dynamic color ON/OFF switch
0 = OFF
1 = ON

G-DRIVE (6) : G channel drive gain control
0h = –4.2dB
29h = 0dB
3Fh = +2.1dB

CLPSW (1) : Switch for selecting replacement pulse for color difference input pin offset control
0 = Pulse generated inside IC (replaced in period extending from rise of pulse which is input to HP-IN to the fall of pulse in 1)
1 = Clamping pulse which has been separated from SCP

B-DRIVE (6) : B channel drive gain control
0h = –4.2dB
29h = 0dB
3Fh = +2.1dB

CLP-MSK (2) : Switching of clamping pulse width in various ways (refer to description of H-WIDTH register)
Gating at one of the SCP CLP pulse widths listed below.
0 = CLP, in its original form, serves as clamping pulse.
1 = Gating at SELH-OUT side of register "H-WIDTH"
2 = Gating at clamping pulse generation block side of register "H-WIDTH"
3 = Prohibited

R-CUTOFF (6) : R channel cut-off control
(Level control of IKIN (Pin 41) R channel reference pulse)
0h = –9.1dB
1Fh = 0dB
3Fh = +4.4dB

ABL-MODE (2) : Switching of ABL mode
0 = Picture ABL-only mode
1 = Picture/brightness ABL mode: Low
2 = Picture/brightness ABL mode: Medium
3 = Picture/brightness ABL mode: High

G-CUTOFF (6) : G channel cut-off control
(Level control of IKIN (Pin 41) G channel reference pulse)
0h = –9.1dB
1Fh = 0dB
3Fh = +4.4dB

ABL-TH (2) : Adjustment of threshold voltage for ABL-IN (Pin 44) input
0 = 1.3V
3 = 3.3V

B-CUTOFF (6) : B channel cut-off control
(Level control of IKIN (Pin 41) B channel reference pulse)
0h = –9.1dB
1Fh = 0dB
3Fh = +4.4dB

SUB-BRIGHT (6) : Sub-brightness control
Setting for output DC bias of RGBOUT
0h = –13 IRE
1Fh = CENTER
3Fh = +13 IRE

HSEP-SEL (1) : Sync separation system setting (valid for YG-IN (Pin 26) input)
0 = Forced slice at sync tip + 0.15V level
1 = Charging/discharging for duty cycle

FIX-SYNC (2) : Switch for setting sync identification circuit operation mode to auto or fixed.
0 = Automatic identification (with priority sequence)
1 = Independent H, V sync signals used
2 = Composite sync input used
3 = Sync on Y, sync on Green input used

V-TC (2) : Setting for V sync separation time constant
0 = 6µs
1 = 8µs
2 = 12µs
3 = 18µs

H-WIDTH (2) : Setting of output pulse width to HS-OUT and clamping pulse generation block.
When the pulse width of the input sync signal is wider than the pulse width in each data, the wider of the two pulses is output.

SELH-OUT	Clamping pulse generation block
0 = THRUGH	0 = 1.4µs
1 = 1.4µs	1 = 1.4µs
2 = 1.7µs	2 = 1.7µs
3 = 3.7µs	3 = 3.7µs

HHD-TC (1) : Setting of H sync separation time constant for YG-IN (Pin 26) input
0 = Time constant for input complying with HD-TV standard
1 = Time constant for input complying with any other HD-TV standard

HS-MASK (1) : Setting for whether H sync is to be added in V sync at HS-OUT (Pin 29) and SELH-OUT (Pin 79)
0 = Not Added
1 = Added

CR OFFSET 1 (4) : For canceling the offset between CrCb of IN1 and SELIN systems
0h = –14mV
7h = 0mV
Fh = +15mV
*These variable range is DC variation amount of respective input pins.

CB OFFSET 1 (4) : For canceling the offset between CrCb of IN1 and SELIN systems
0h = –14mV
7h = 0mV
Fh = +15mV
*These variable range is DC variation amount of respective input pins.

CR OFFSET 2 (4) : For canceling the offset between CrCb of EXT system
0h = –14mV
7h = 0mV
Fh = +15mV
*These variable range is DC variation amount of respective input pins.

CB OFFSET 2 (4) : For canceling the offset between CrCb of EXT system
0h = –14mV
7h = 0mV
Fh = +15mV
*These variable range is DC variation amount of respective input pins.

SUB-CON (4) : Contrast gain control (Y system level adjustment)
0h = –1.9dB
7h = 0dB
Fh = +1.7dB

SUB-COL (4) : Color gain control
0h = –2.1dB
7h = 0dB
Fh = +1.8dB

SUB-HUE (4) : Hue center control
0h = –8° Flesh color appears red.
8h = CENTER
Fh = +8° Flesh color appears green.

CTI-LEVEL (2) : Color difference signal edge enhancement setting
0 = OFF
1 = Low
2 = Medium
3 = High

R-Y/R (4) : R-Y axis +(R-Y) component setting
0h = Maximum
Fh = Minimum

R-Y/B (4) : R-Y axis –(B-Y) component setting
0h = Maximum
Fh = Minimum

G-Y/R (4) : G-Y axis –(R-Y) component setting
0h = Maximum
Fh = Minimum

G-Y/B (4) : G-Y axis –(B-Y) component setting
0h = Maximum
Fh = Minimum
Detection axis standard values

	R-Y/R	R-Y/B	G-Y/R	G-Y/B
NTSC-JAPAN	6h	Ch	Ah	5h
NTSC-USA	7h	2h	8h	Bh
PAL/SECAM	Dh	Fh	8h	4h

LRGB2-LEVEL (4) : LRGB2 system picture level control
0h = –5dB
Fh = 0dB

GAMMA (4) : Control of gamma correction amount
0h = OFF
Fh = MAX (output increased by 15 IRE at input 40 IRE point)

PABL-LEVEL (4) : Setting of level detection DC at RGB-OUT of PEAK-ABL
0h = Level detection DC: 4.9V
Fh = Level detection DC: 6.8V

BLK-BOTTOM (4) : RGB-OUT bottom limiter level control (valid when BLKSW = 1)
The limiter level is replaced with the reference DC for each H in RGB system, and it is defined by the drop voltage from that DC; it is not dependent on DC level control setting made by BRIGHT, etc. This limiter functions for all video signals. For further details, refer to the description of operation.
0h = Limiter level: –1.7V
Fh = Limiter level: –1.3V

SUB-SHP (2) : Sharpness center control (when SYSTEM = 0, SHARPNESS = 1F, SHP-F0 = 1)
0 = 0dB
3 = +4dB

SHP-F0 (2) : Sharpness f_0 setting (automatically set to f_0 best suited to each system)

	NORMAL (SYSTEM = 0)	FF (SYSTEM = 1)	HD (SYSTEM = 2)	FIX-HD (SYSTEM = 3)
0 =	3.1MHz	6.1MHz	9.1MHz	9.1MHz
3 =	4.9MHz	9.5MHz	14.3MHz	14.3MHz

PRE/OVER (2) : Preshoot to overshoot ratio setting
0 = PRE : OVER 1 : 1
3 = PRE : OVER 2 : 1

LTI-LEVEL (2) : Luminance signal edge enhancement setting
0 = OFF
1 = Low
2 = Medium
3 = High

VM-LEV (2) : VM-OUT level control
0 = OFF
1 = Low
2 = Medium
3 = High

VM-DEL (2) : VM-OUT phase control; defined by difference in phase from R-OUT
0 = Short
3 = Long

DC-TRAN (2) : Y system DC transmission ratio setting
0 = 100%
1 = 77%
* These variable range is the case when SCP clamp pulse duty is 4%.

D-PIC (2) : Dynamic picture (black expansion) control
0 = OFF
1 = Low: inflection point 30 IRE
2 = Medium: inflection point 35 IRE
3 = High: inflection point 40 IRE

Status Register

EH (1) : Availability of independent H input pins in input system selected by INPUT-SEL
0 = Not available
1 = Available

EV (1) : Availability of independent V input pins in input system selected by INPUT-SEL
0 = Not available
1 = Available

IK (1) : AKB loop operation status (REF-P on cathode current Ik detected)
0 = All REF-P for RGB within stability domain
1 = Small and unstable REF-P
Note: Due to the nature of the circuit operation, "0" is returned at power-on.
This is to be ignored by the microcomputer for 2 seconds after power-on.

Description of Operation

1. Programmable matrix selector

This IC contains video switching circuits for 4 systems, and they are selected by INPUT-SEL (I^2C bus). YCbCr, HD YPbPr, GBR and the respective HV sync signals can be supplied as the input of each system.
As the multiscan compatible range, signals can be input at a horizontal scanning frequency from 15kHz to 60kHz. The selected signals are output to SEL-OUT (Pins 76, 77, 79 and 80), and they can be connected to the external processor, etc. When the signals are to be input again to the IC, they are supplied through the clamp capacitor to the SEL-IN (Pins 62, 63 and 64) system.
Both positive and negative polarities are supported by the HV sync signal input.

Select MAT-OUT (I^2C bus) as follows in accordance with the input signals.
- When the YCbCr signals are input, select the THROUGH1 mode.
- When the YPbPr and GBR signals are input, select the mode which converts them into YCbCr signals.
- When the GBR signals are input, they can be output directly to the internal RGB system signal processing. A DC voltage of approximately 4V is output to SEL-OUT at this time.

The matrix conversion formulas are shown below.

[MAT OUT = 1: Y_{HD} PbPr → YCbCr]
$Y = Y_{HD} + 0.0938Pb + 0.196Pr$
$Cb = 0.564\ (1.762Pb - 0.196Pr)$
$Cr = 0.713\ (-0.0938Pb + 1.379Pr)$

[MAT OUT = 2: GBR → YCbCr]
$Y = 0.299R + 0.587G + 0.114B$
$Cb = 0.564\ (-0.299R - 0.587G + 0.886B)$
$Cr = 0.713\ (0.701R - 0.587G - 0.114B)$

The HV sync signal processing system will now be described.
First, whether the selected sync signals have been input from the H and V pins is identified, and the results are sent as EH and EV to the status register as the existence status data. Meanwhile, the H and V signals pass through the polarity identification circuit where their polarities are aligned, and then they are input to the priority level circuit.
When the composite sync (CS) signal is to be input, input it to the H input pin in each input system. After the signals have passed through the polarity identification circuit, the V sync signal is separated, and it enters the priority level circuit.
When sync on Y or sync on Green signal is to be input, input it to Pin 3 in each input system.
After passing through HYSW, the signal is amplified by 5dB and output to YG-OUT (Pin 25). The output is then returned to YG-IN (Pin 26) through the sync tip clamp capacitor, the sync signal is separated, and it enters the priority level circuit. By setting HYSW (I^2C bus) to 1, this route can be used also when the CS signal is input.
In this way, the respective sync signals are input to the priority level circuit, and the sync signals to be output in the EH and EV status are determined.

The priority levels are shown below. When designing a TV set, ensure that one of the following 3 conditions applies.
1. When both HV signals are present at the HV pins, give top priority to the selection of these signals.
   → EH = 1; EV = 1
2. When the CS signal is present at the H pin and no input signal is present at the V pin, the CS signal is selected.
   → EH = 1; EV = 0
3. When the Y or Green is present at Pin 3 and no input signal is present at the HV pin, the Y or Green signal is selected.
   → EH = 0; EV = 0

When the HV output is determined, the pulse width of the H sync signal is adjusted by H WIDTH (I^2C bus), and the H sync signal is output along with the V sync signal to SEL-OUT. HS-OUT and VS-OUT (Pins 28 and 29) are provided to enable these sync signals and the HV input signals (Pins 65 and 66) of the IN1 system to be selected by YCBCR/MAT (I^2C bus) and output.

2. YCbCr switching circuit

In the IN1/SELIN switching circuit, the inputs of the IN1 system (Pins 67, 68 and 69) and SELIN system (Pins 76, 77 and 78) are switched by YCBCR/MAT (I^2C bus).
In the INT/EXT switching circuit, the IN1/SEL switching circuit output and EXTIN (Pins 62, 63, and 64) system input are switched by YCBCR-SW (Pin 61).
In the respective color difference input circuits for INT and EXT, adjustment is enabled by CB OFFSET 1, CR OFFSET 1 (I^2C bus), etc. in order to reduce the color leakage resulting from DC offset between CbCr under no-input conditions. The register is made effective by a factory setting.

3. Y system signal processing

The Y signal passes through the sub-contrast control, sharpness control, LTI (luminance transient improvement), clamp, DC transmission ratio compensation and black expansion circuits, and is output to MATRIX/CLP.

fo for the sharpness, LTI, VM, etc. is set to the optimum value for each TV system (normal, FF, HD) by SYSTEM (I^2C bus). It can be set to any value by the I^2C bus when various effects are to be changed.
The differential waveform of the Y signal is output to VM-OUT (Pin 59). The VM-OUT phase is about 60ns ahead of the R-OUT signal phase, and it can be finely adjusted by VMDEL (I^2C bus). VM-OUT can be muted by the YS/YM-1, YS/YM-2 and VM/SHP/C-OFF pins.
The sharpness can be turned off simultaneously at the VM/SHP/C-OFF pin. Refer to the Pin Description.
LTI provides aperture correction by creating compensation signals in the rise and fall parts of the color difference signals and by adding these signals to the original signals.
This IC comes with aging modes. The AGING1 mode (all white output) and AGING2 mode (all black output) can be set by the I^2C bus. When PURE-RGB (from the matrix selector), LRGB1 and LRGB2 have been selected, the aging mode is canceled since the output of these inputs takes priority.

4. Color difference (CbCr) system signal processing

Color difference signals CbCr pass through the sub-color control, CTI (chrominance transient improvement), hue control, color control and detection axis setting circuits, and are output to MATRIX/CLP.

fo for CTI is set to the optimum value for each TV system (normal, FF, HD) by SYSTEM (I^2C bus). CTI provides aperture correction by creating compensation signals in the rise and fall parts of the color difference signals and by adding these signals to the original signals.
In the color gain control amplifier, the color off mode is fully established when the COLOR (I^2C bus) data is set to 00h. The color can also be turned off at VM/SHP/C-OFF (Pin 60). Refer to the Pin Description.
Next, in the detection axis setting circuit, the R-Y axis and G-Y axis components are set by fixing the B-Y axis. After conversion into the respective color difference signals, the signals are input to the MATRIX/CLP circuit along with the Y signal to form the RGB primary colors.

5. RGB system signal processing

The RGB signals are output through the pure RGB switching, YMYS1, picture control, clamp, brightness control, YMYS2, peak limiter, dynamic color, gamma correction, drive control and cutoff control circuits.

In the pure RGB switching circuit, the matrix selector output can be input directly to the RGB system when RGB signals are supplied. Set MAT OUT (I^2C bus) to data 3.
In YM1YS1, whether the main signals are to be toned down (YM) to 1/3 or switched (YS) to the analog RGB1 signals is set. Input the control signal to YS/YM-1 (Pin 45). Refer to the Pin Description.
Next, the signals pass through the picture control, clamp and brightness control circuits, and the signal level and DC level are adjusted by the picture and brightness controls on which the ABL control voltage is superimposed.
ABL operates as an average-value type.
Although similar to YS1YM1, YS2YM2 enables the level of the analog RGB2 input signals to be adjusted by LRGB2 LEV (I^2C bus).
The peak limiter operates in tandem with the brightness control: in other words, it functions only for the signal level (100 IRE). After passing through the dynamic color, gamma correction and drive control (separate adjustment possible for RGB) circuits, the signals are subject to cutoff control by the AKB system, and then output to the buffer.
The dynamic color circuit increases the color temperature of the picture when 75% of the R signal level is lower than that for G or B. The color temperature is varied up to a maximum of R : G : B = 0.97 : 1 : 1.05.
The IC contains a peak ABL circuit for suppressing excessive brightness: The peak level of the RGB output signals is detected inside the IC and sent to the ABL circuit. Refer to the section on PABL LEV in the description of the registers for details on the detection value. As for the feedback time constant for the actual signals, configure a low-pass filter and attach it externally to PABL-FIL (Pin 42).
At the output stage, the bottom limiter voltage can be set by BLK-BOTTOM (I^2C bus). Limiter ON/OFF can be set by BLK-SW (I^2C bus). The HV blanking level is approximately 0.1V when the limiter is set OFF. The limiter voltage is replaced with the reference DC in each H by the RGB system and defined by the drop voltage from that DC. The "reference DC" refers to the output DC level of REF-P for AKB. This means that the limiter voltage is linked to the AKB status or, in other words, to the RGB-SH pin voltage. It does not depend on the settings of the DC level control based on BRIGHT, etc. It functions for all the video signals.

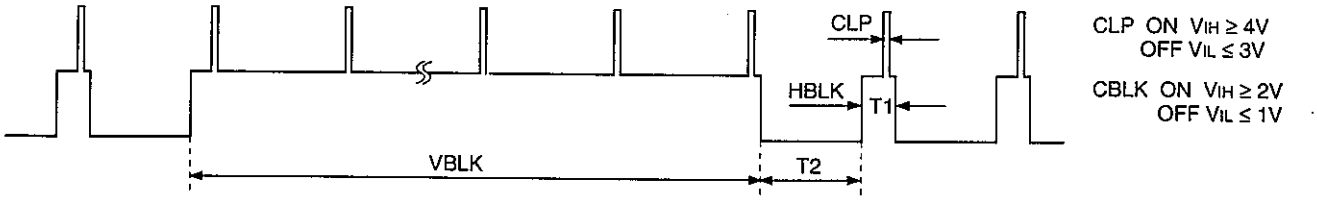
The AKB system (auto cutoff function) automates the white balance (black balance) adjustment by forming a loop between this IC and the CRT. The aging of the CRT can be compensated for by forming this loop. This system functions using RGB-DRIVE, which adjusts the gain between the RGB outputs by I^2C bus, and RGB-CUTOFF, which adjusts the DC level.
The operation of the auto cutoff function is described next. (Refer to Fig. 1 showing the timing charts of the REF-P output.)

- The RGB signals are shifted by 1H in sequence from R to G and from G to B at the top of the picture (overscanning area), and the reference pulse (REF-P) for auto cutoff appears at a level of 8 IRE. Reference pulses equivalent to 1H are output from the RGBOUT pin to the latter part of the vertical blanking period.
- These output reference pulses are detected as cathode current Ik which is then input to IKIN (Pin 41) after it has been converted into a voltage.
- The voltage input to IKIN is compared with the reference voltage inside the IC, and the current generated by the difference between the two voltages is sampled by the capacitor connected to the RGB-SH (Pins 40, 38 and 36) during the REF-P period. The current is held outside the REF-P period.
- The DC level of RGBOUT varies in accordance with the voltage of the RGB-SH pins. This is repeated in each V period until the level is made equal to the reference voltage. The RGB signals each have the reference voltage which is varied using the CUTOFF control of the I^2C bus.

When this IC is used in an LCD projector, etc., it is possible to set a mode in which HV blanking is turned off. The HV blanking and AKB system control circuits are turned off by setting the CBLK-OFF (I^2C bus) data to 1. In this mode, the RGB-OUT DC level can be adjusted by applying the voltage directly to the RGB-SH (Pins 40, 38 and 36).

6. Pulse interface

The sand-castle pulse is input to SCP-IN (Pin 31).
SCP is a ternary pulse which combines CBLK and CLP.
In this IC, input SCP using the pulse width shown in the figure below.
CLP and CBLK are used by each block as the clamp pulse and composite blanking pulse, respectively.
CBLK is input to the AKB timing generator, and is required to generate REF-P.

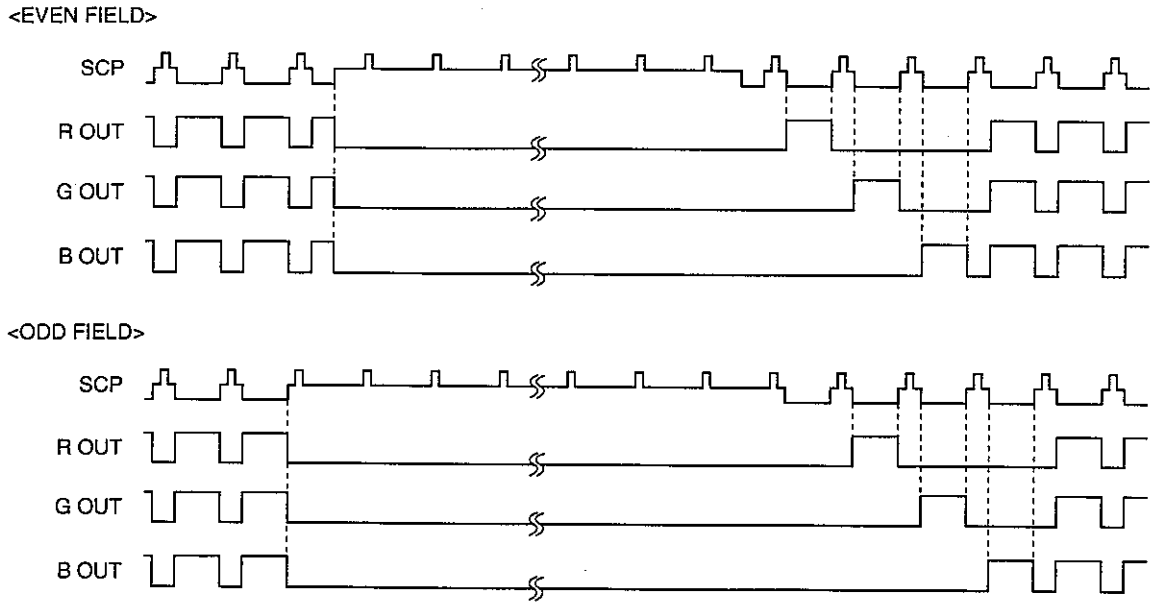


- HBLK width: T1 ≤ 25µs
- From VBLK end to next HBLK: T2 ≥ 9µs

The V-timing pulse is input to VTIM-IN (Pin 32).
This pulse is used as the vertical blanking pulse in the V compression mode (AKB-T (I^2C bus) = 1). It is input to the AKB timing generator, and is required to generate REF-P.

H-pulse is input to HP-IN (Pin 33).
This pulse is used as the horizontal blanking pulse in the V compression mode (AKB-T (I^2C bus) = 1). It is input to the AKB timing generator, and is required to generate REF-P.
When offset control is to be provided for the color difference input, the job of replacing the pulse with the DC but only for a certain period is performed, and it is used in the replacement pulse generation block. Refer to Fig. 2.

Normal: AKB-T = 0 (I^2C bus)



V compression mode: AKB-T = 1 (I^2C bus)

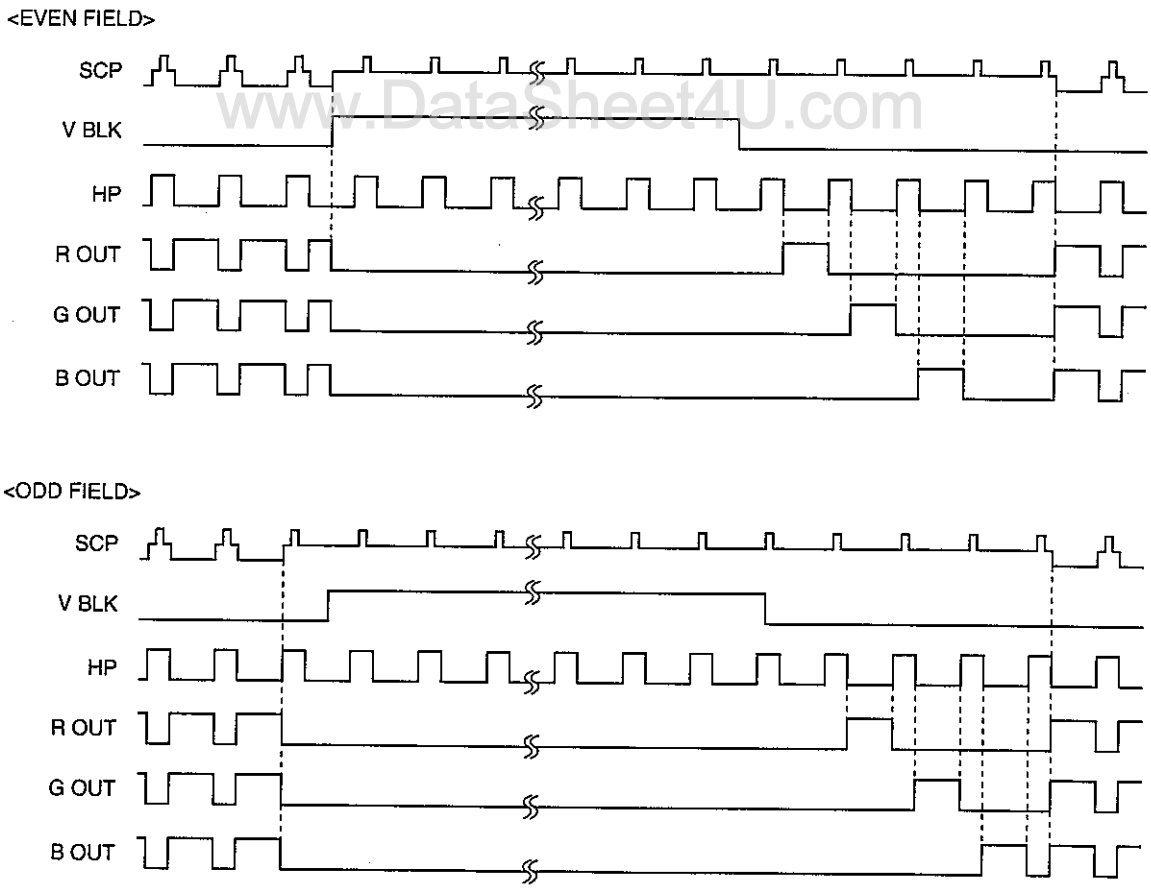


Fig. 1. AKB timing charts

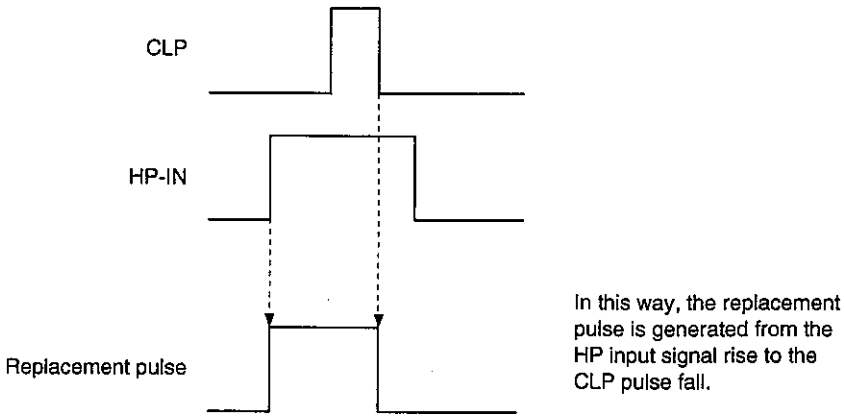


Fig. 2. Replacement timing pulse for adjusting color difference input offset

Notes on Operation

- Since the RGB signals which are output from the CXA2101Q are DC direct connected, the board pattern must be designed with consideration given to minimizing interference from around the power supply and GND. It is best to use a solid earth rather than separating the GND patterns for each pin. Design the power supply to achieve an impedance as low as possible. Locate the bypass capacitor between the power supply and GND as close to the pins as possible.
  It is also recommended that a buffer be connected to RGBOUT as near to this IC as possible.

- Input the waveforms to SCP-IN (Pin 31) with the pulse widths (T1, T2) mentioned in the description of operation regardless of the scanning frequency. This is to prevent the AKB timing generator from malfunctioning.

- Input the Y, Cb, Cr, H and V signals at a sufficiently low impedance. This is particularly important for inputs to the pins which are clamped (refer to the Pin Description).

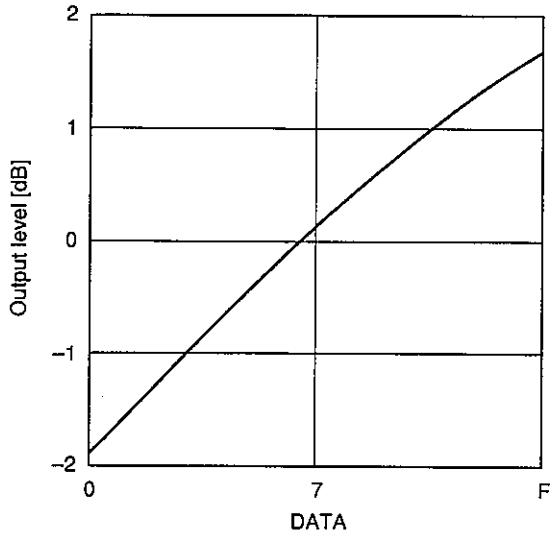
- Use resistors (such as metal film resistors) with an error of less than 1% as the resistors which are connected to IREF-SYNC (Pin 27) and IREF-YC (Pin 71).

- Processing of unused pins
  Open: Pins 1 to 5, 7 to 11, 13 to 17, 19 to 23, 26, 45 and 49
  Connect to GND: Pins 32, 33, 41 and 61
  Connect to Vcc: Pins 46 to 48, 50 to 52, 62 to 64

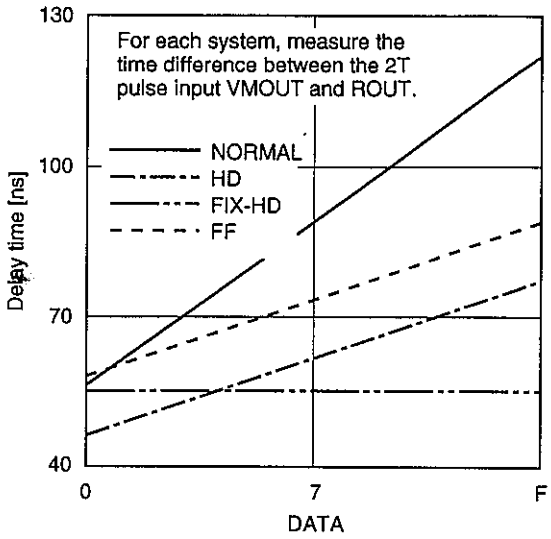
Alternatively, the input pins for clamping (refer to the Pin Description) can be connected to GND via a capacitor.

Curve Data (The I²C bus data conforms to the Electrical Characteristics Measurement Conditions on page 16.)

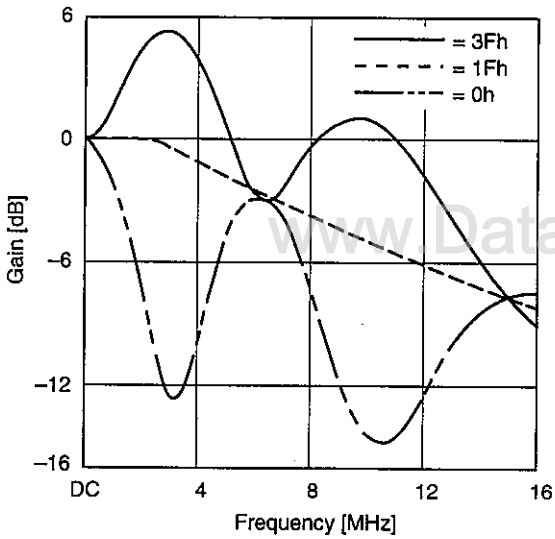
SUB-CONT



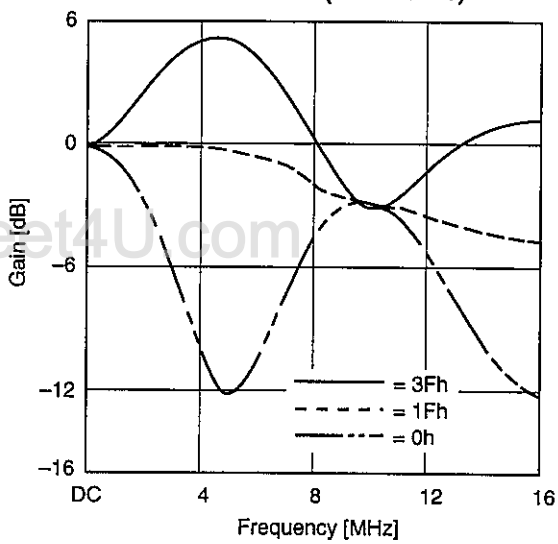
VM-DL



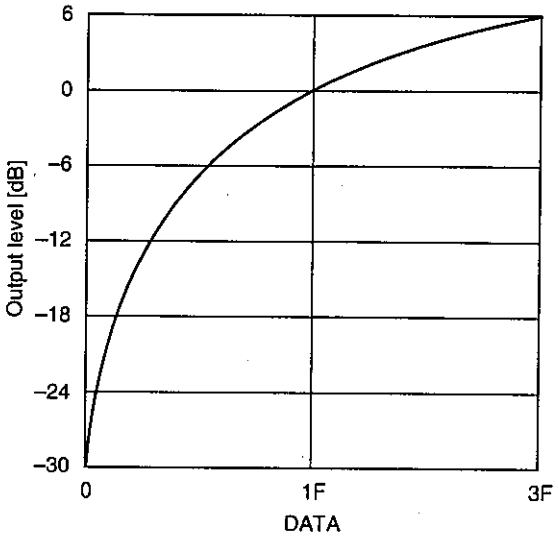
SHARPNESS (SHP-F0 = 0)



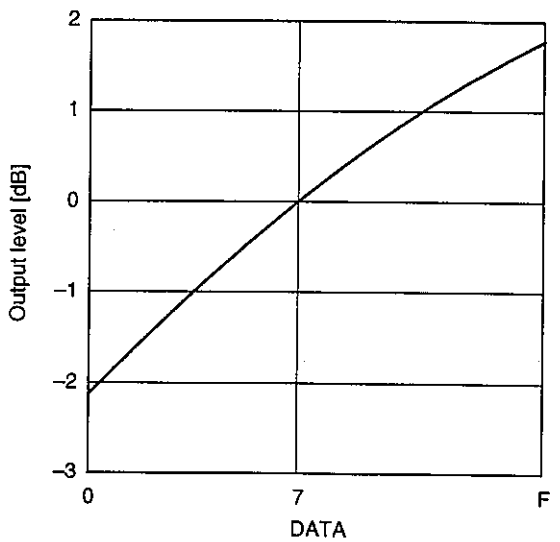
SHARPNESS (SHP-F0 = 3)



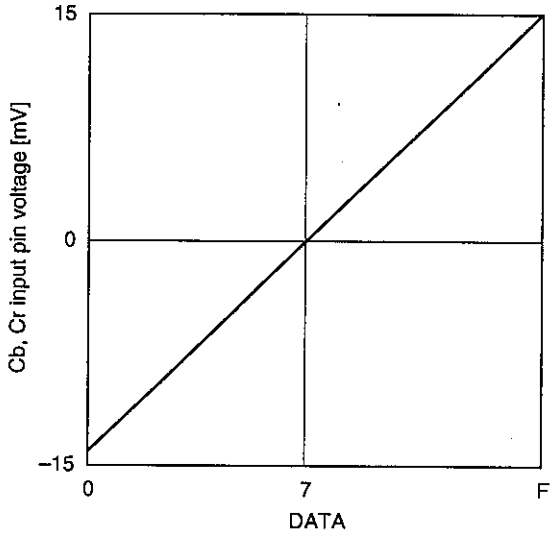
COLOR



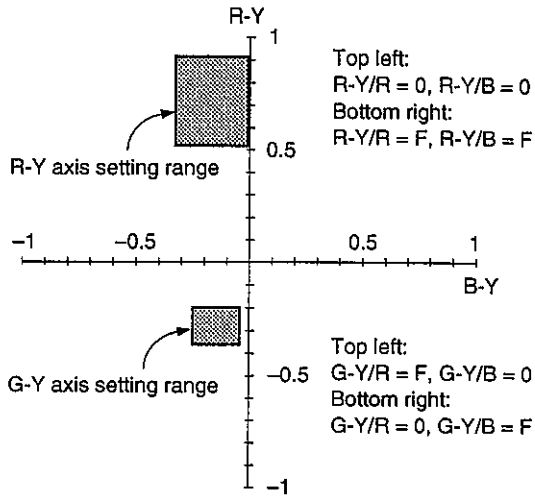
SUB-COL



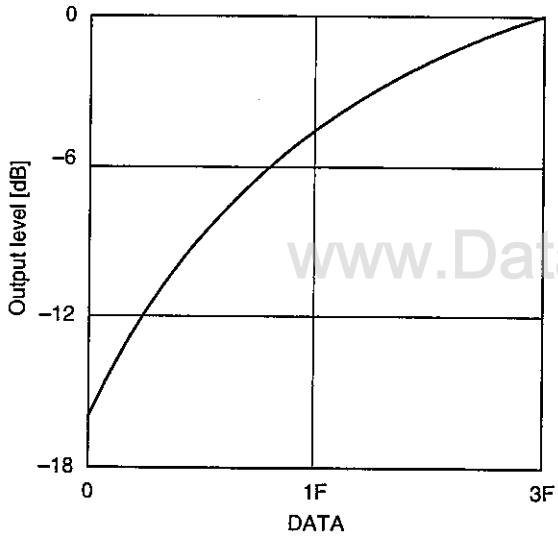
CB, CR OFFSET



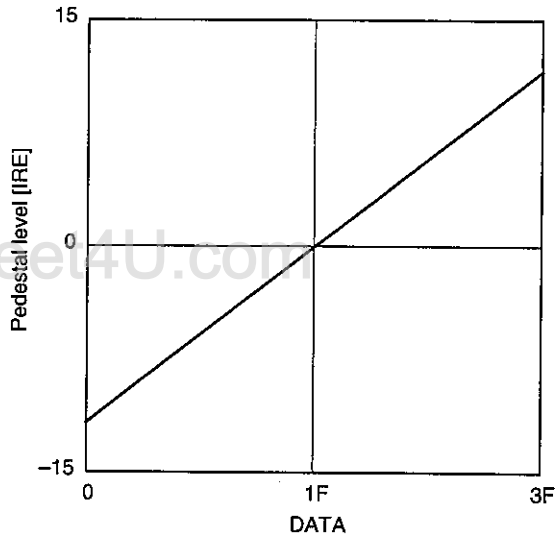
Detection axis adjustment



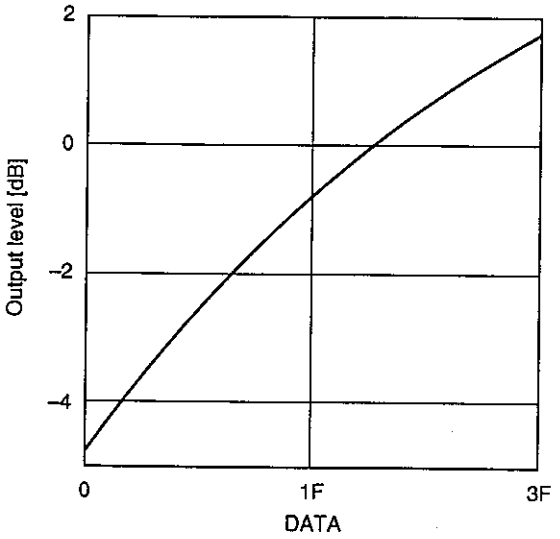
PICTURE



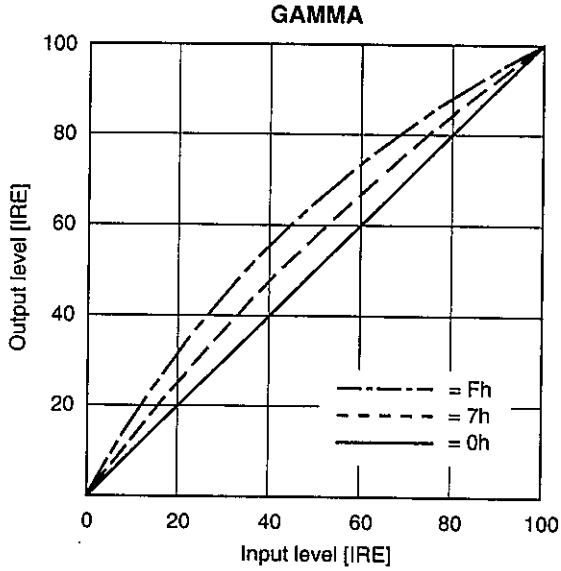
BRIGHT



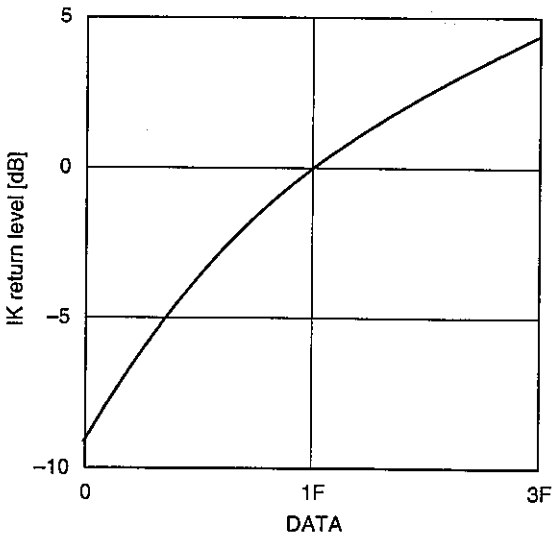
DRIVE



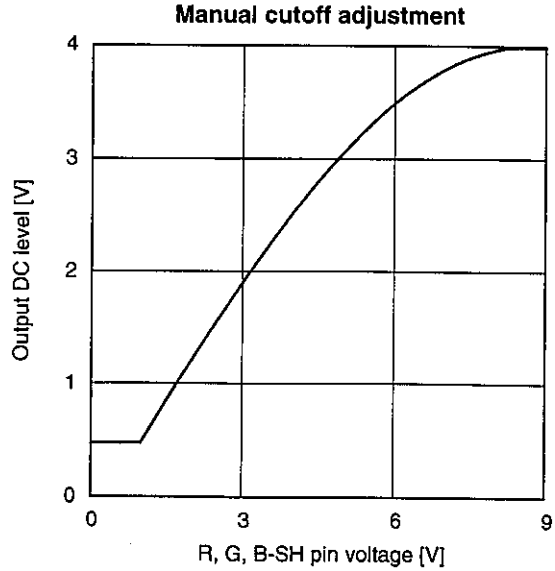
GAMMA



CUTOFF

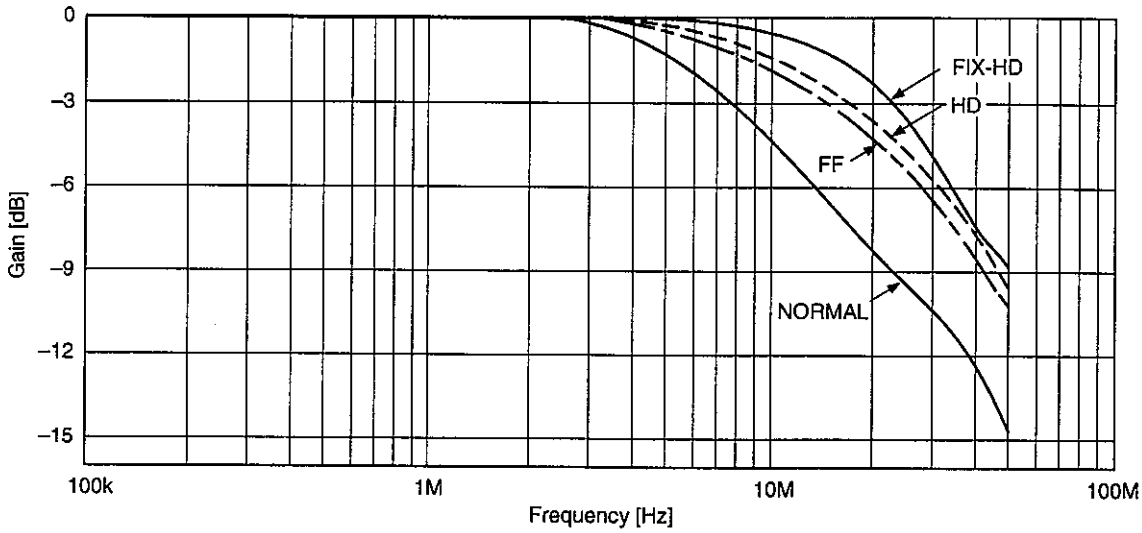


Manual cutoff adjustment

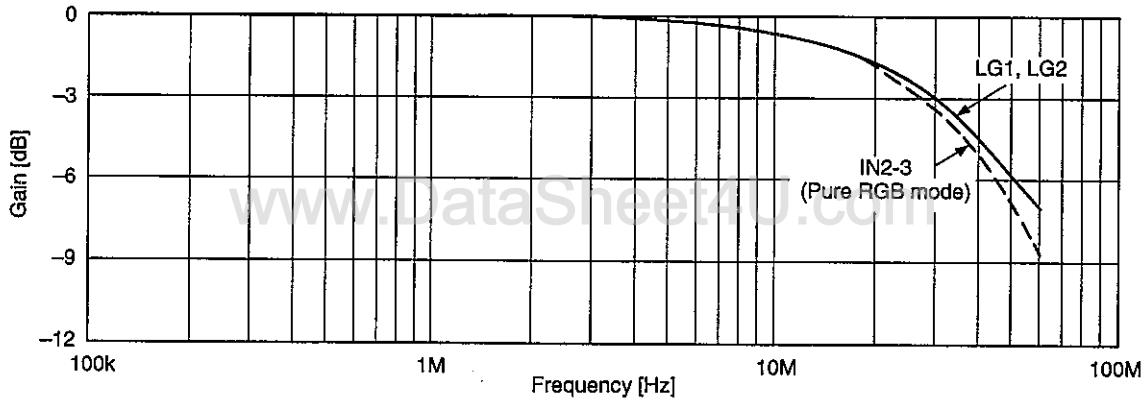


Frequency Response

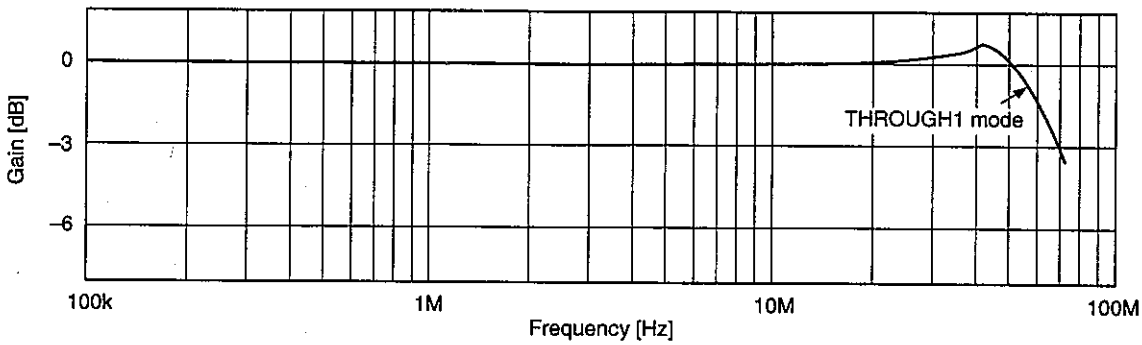
GOUT output versus Y1-IN input frequency response



GOUT output versus LG1, LG2 and IN2-3 input frequency response



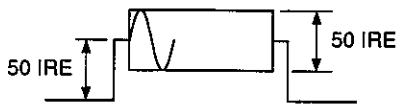
SELY-OUT output versus IN2-3 input frequency response



[Frequency response measurement conditions]

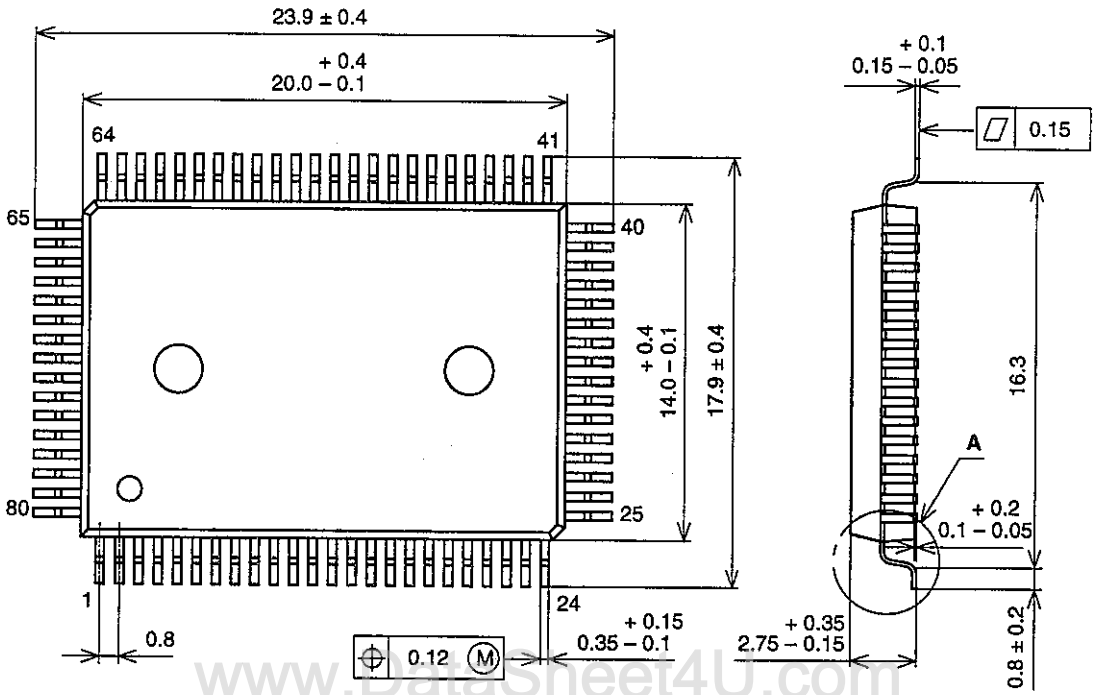
I²C bus: conforms to the Electrical Characteristics Measurement Conditions (on page 16.)

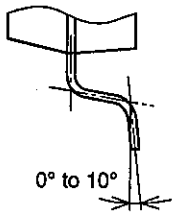
Input signal:



Package Outline Unit: mm

80PIN QFP (PLASTIC)





DETAIL A

SONY CODE	QFP-80P-L01
EIAJ CODE	*QFP080-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g