



Dual-SP3T (SP3Tx2) SOI Antenna Switch

CXA2947GC

Description

The CXA2947 is Rx power SP3Tx2 antenna switch for balanced signal switching application.

The CXA2947 has a 1.8 V CMOS compatible decoder.

The SONY Silicon On Insulator (SOI) technology is used for low insertion loss.

Features

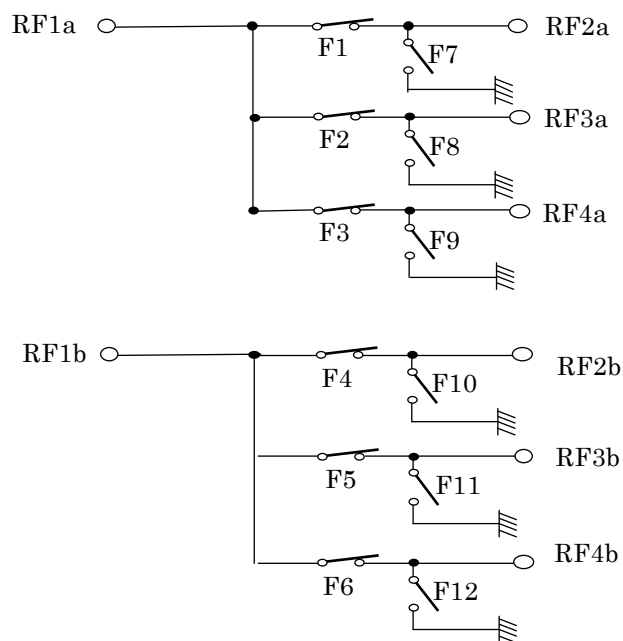
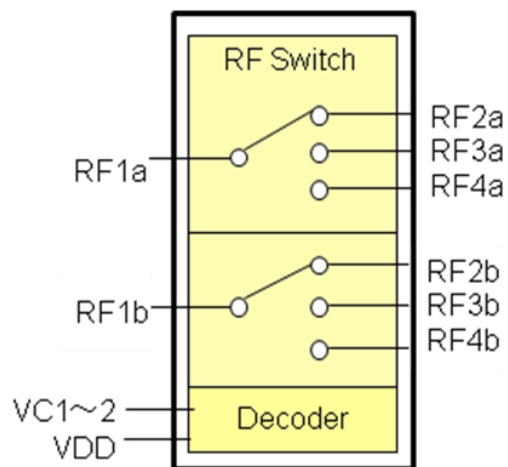
- ◆Low Insertion loss : 0.30 dB (typ.) @800 MHz
 0.35 dB (typ.) @2 GHz
 0.40 dB (typ.) @2.7 GHz
- ◆No DC Blocking Capacitors (except sourcing DC bias)
- ◆Solder Bump Bare Die(SBBD) : Bump Pitch = 0.4 mm
- ◆Small Flip-Chip Size : 1.5 mm x 1.5 mm x 0.35 mm Typ.
- ◆Lead-Free and RoHS compliant

Structure

SOI CMOS MMIC

This IC is ESD sensitive device. Special handling precautions are required

Block Diagram of Dual-SP3T SOI Antenna Switch

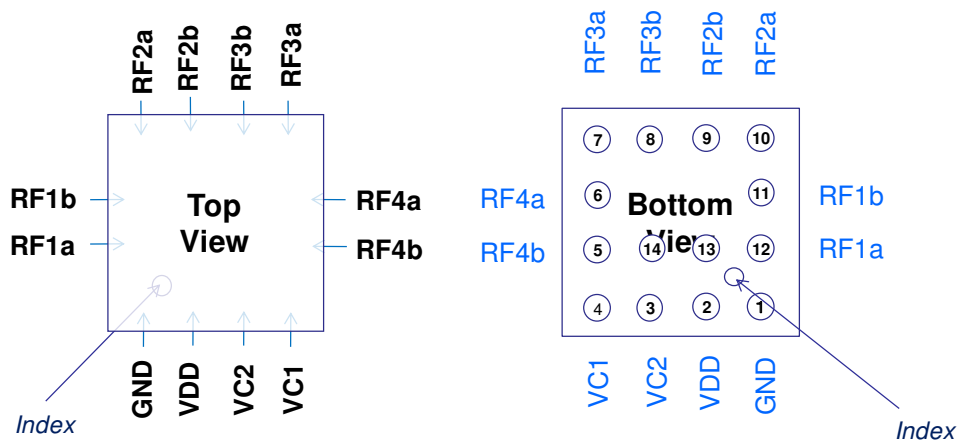


Truth Table

State	Active Path	VC State		Switch State											
		1	2	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12
1	RF1a-RF2a、 RF1b-RF2b	H	L	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON
2	RF1a-RF3a、 RF1b-RF3b	L	L	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	ON	ON	OFF	ON
3	RF1a-RF4a、 RF1b-RF4b	L	H	OFF	OFF	ON	OFF	OFF	ON	ON	ON	OFF	ON	ON	OFF

Pin Configuration

Chip Size : 1.5 x 1.5 mm (0.4 mm pitch, $\Phi 200 \mu\text{m}$)



No.	Name
1	GND
2	VDD
3	VC2
4	VC1
5	RF4b
6	RF4a
7	RF3a
8	RF3b
9	RF2b
10	RF2a
11	RF1b
12	RF1a
13	GND
14	GND

Absolute Maximum Ratings

◆ Supply voltage	V_{DD}	4	V	($T_a = 25\text{ }^{\circ}\text{C}$)
◆ Control voltage	VC	4	V	($T_a = 25\text{ }^{\circ}\text{C}$)
◆ Maximum input		25	dBm	($T_a = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 2.5$ to 3.3 V)
◆ Operating temperature	T_{opr}	-35 to +90	$^{\circ}\text{C}$	
◆ Storage temperature	T_{stg}	-65 to +150	$^{\circ}\text{C}$	

DC Bias Condition

(Ta = 25 °C)

Parameter	Min.	Typ.	Max.	Unit
VDD	2.5	2.8	3.3	V
VC(H)	1.3	1.8	3.3	V
VC(L)	0	-	0.45	V

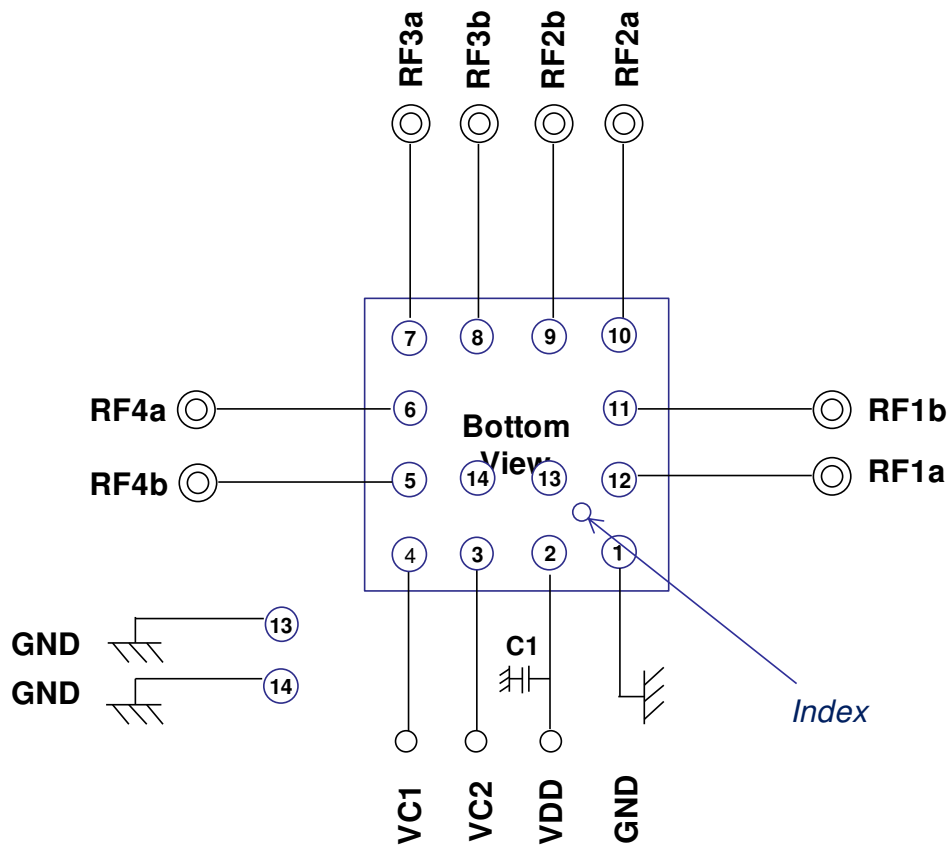
Electrical Characteristics

(VDD = 2.5 V, Ta = 25 °C)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL	RF1a - RF2a	*1	-	0.30	0.40	dB
			*2	-	0.35	0.50	
			*3	-	0.40	0.55	
		RF1a - RF3a	*1	-	0.30	0.40	
			*2	-	0.35	0.50	
			*3	-	0.40	0.55	
		RF1a - RF4a	*1	-	0.30	0.40	
			*2	-	0.35	0.50	
			*3	-	0.40	0.55	
		RF1b - RF2b	*1	-	0.30	0.40	
			*2	-	0.40	0.55	
			*3	-	0.45	0.60	
		RF1b - RF3b	*1	-	0.30	0.40	
			*2	-	0.40	0.55	
			*3	-	0.45	0.60	
		RF1b - RF4b	*1	-	0.30	0.40	
			*2	-	0.40	0.55	
			*3	-	0.50	0.65	
Isolation	ISO	RF1a/b - RF2a/b	*1	32	37	-	dB
			*2	24	29	-	
			*3	23	27	-	
		RF1a/b - RF3a/b	*1	35	44	-	
			*2	26	31	-	
			*3	23	28	-	
		RF1a/b - RF4a/b	*1	35	44	-	
			*2	28	33	-	
			*3	24	29	-	
VSWR	VSWR	All Ports in Active Paths	734 to 2170 MHz	-	1.20	1.40	-
			2500 to 2690 MHz	-	1.30	1.50	
Switching Time	Ts		50 % Ctl to 90 % RF	-	2	5	μs
Control Current	Ictl		Vctl = 1.80 V	-	0.01	1	μA
Supply Current	Idd		Vdd = 2.60 V	-	14	30	μA

Electrical Characteristics are measured with all RF ports terminated in 50 Ohms.

- * 1 freq = 734 to 960 MHz
- * 2 freq = 1805 to 2170 MHz
- * 3 freq = 2620 to 2690 MHz
- * 4 Measured with the recommended circuit

Recommended Circuit


*1: No DC blocking capacitors are required on all RF ports.

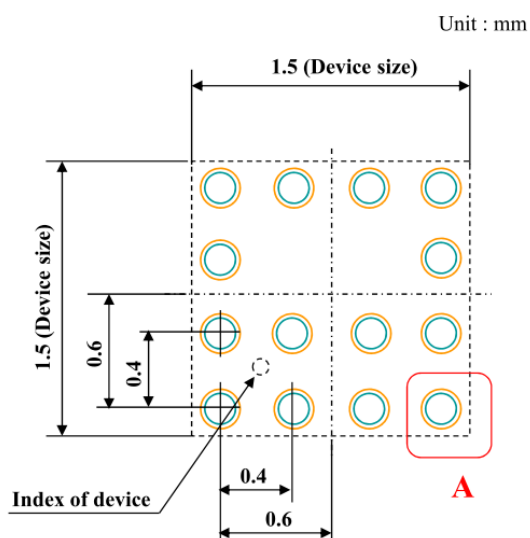
*2: DC levels of all RF ports are GND.

*4: C1 (100 pF) is recommended on VDD pin for Decoupling Capacitor.

Solder Bump Foot Print (Macro) *Reference

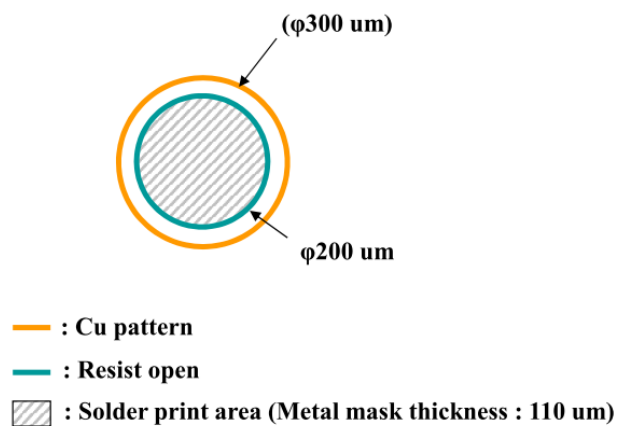
Device specification

- Device size : 1.5 mm × 1.5 mm × t 0.35 mm
- Pin counts : 14 Pin
- Solder Bump height : 0.15 mm
- Solder Bump ball size : $\phi 0.2$ mm
- Solder Bump pitch : 0.4 mm

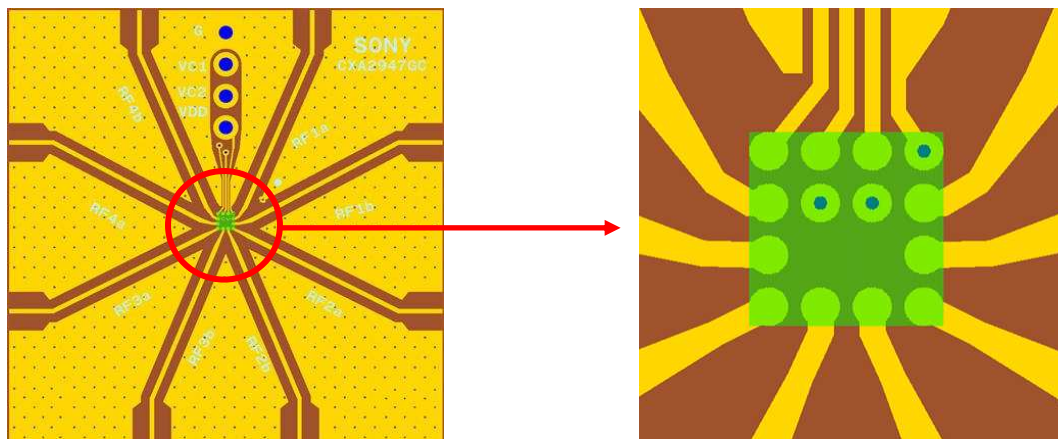


Detail - A

- Land size (Resist Open area) : $\phi 200$ μm
- Cu pattern size : ($\phi 300$ μm)



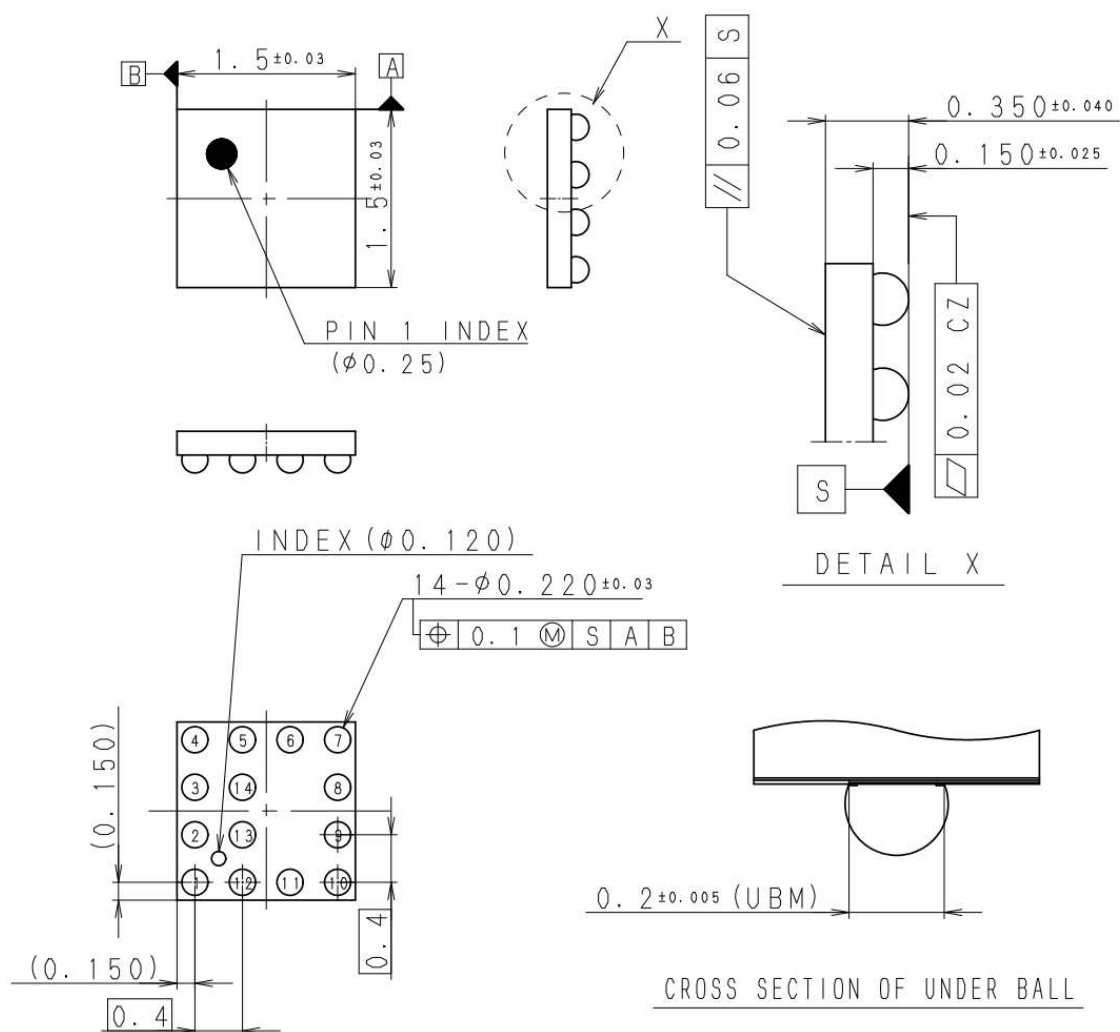
Recommended PCB Layout



- Device Area
- Via
- Metal Pattern

Package Outline

14 PIN XFLGA



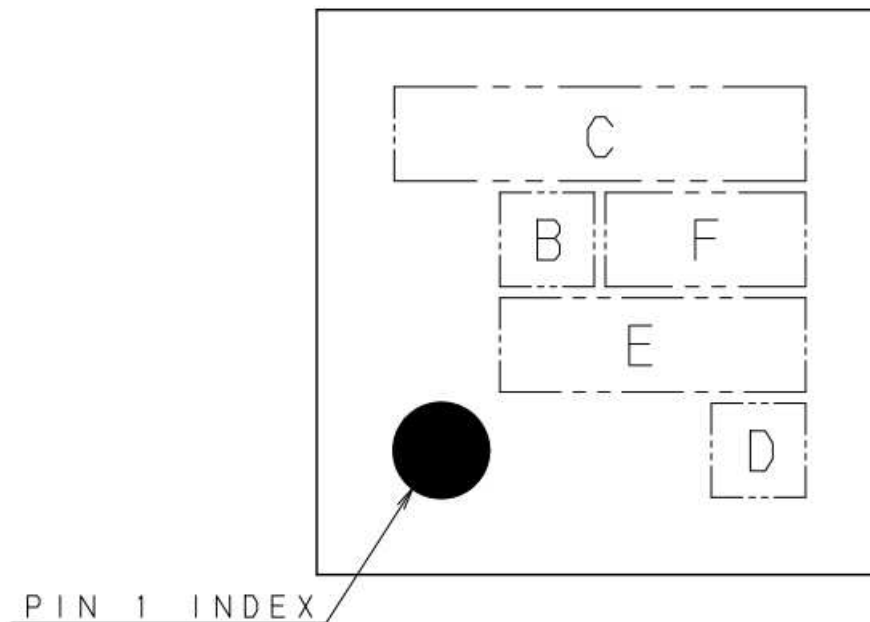
PACKAGE STRUCTURE

SONY CODE	XFLGA-14S-432
JEITA CODE	S-XFLGA14-1.5x1.5-0.4
JEDEC CODE	—

PACKAGE MATERIAL	Si SUBSTRATE
TERMINAL MATERIAL	Sn-3.0Ag-0.5Cu
PACKAGE MASS	0.0014g

PART No.	AP-2000-14LGAS2	Rev. 0
ISSUED	12.12.18	REVISED
PRODUCTION LINE	COMPILING DIV.	SONY SEMICONDUCTOR.
REMARKS	PKG CORD:GX-14-CAS	

Marking



MARKING C: 2947

注1) C部は製品名 (Max 4 文字) を配置する。
(4 文字を超える場合は製品名省略標示規定に従う。)

2) B部は製造年 (1 文字) を配置する。

3) D部は組立場所記号 (1 文字) を配置する。

4) E部は通し記号 (MAX 3 文字) を配置する。

5) F部は製造週 (MAX 2 文字) を配置する。

< INSTRUCTIONS >

1) TYPE NO. (MAX 4 CHARACTERS) IN SECTION C.
(FOR MORE THAN 4 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)

2) MANUFACTURING YEAR (1 CHARACTER) IN SECTION B.

3) ASSEMBLY LOCATION CODE (1 CHARACTER) IN SECTION D.

4) SERIAL CODE (MAX 3 CHARACTERS) IN SECTION E.

5) MANUFACTURING WEEK (MAX 2 CHARACTERS) IN SECTION F.

Moisture Sensitivity

Moisture Sensitivity Level for this part is MSL = 1

Note: The MSL of this product contains the following storage conditions (Taping).

Storage period

(With or without opening moisture-proof packing)

⇒The storage time limit shall be 1 year or less under storage environment
conditions of temperature 30 °C or less and humidity 85 %RH or less.

*This device is unnecessary management of moisture sensitivity.

However, we will assume 1 year for the convenience of seal strength of the taping product.

Avoid storage in locations exposed to direct sunlight, locations where corrosive gases are generated, or dusty locations.

Note

Sony reserves the right to change products and specifications without prior notice.

This information does not convey any license by any implication or otherwise under any patents or other right.

Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits