SONY

CXA3002N

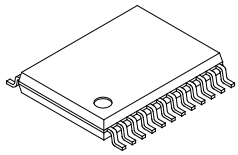
TX Gain Control Amplifier

For the availability of this product, please contact the sales office.

Description

CXA3002N is a TX gain control amplifier for CDMA cellular mobile phone.

24 pin SSOP (Plastic)



Features

- Wide gain control range
- Linear gain slope
- High output IP_3 Typ. +9dBm at Gain = 35dB
- Power save function included

Absolute Maximum Ratings

• Supply voltage	V_{CC}	6	V
• Operating temperature	Topr	–40 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	420	mW
• Supply voltage range		–0.3 to 6	V
• Logic input voltage		–0.3 to V_{CC} +0.3	V
• Signal input voltage		–0.3 to V_{CC} +0.3	V
• Differential signal input voltage		0 to 2.5	V

Operating Conditions

Supply voltage		3.1 to 3.8	V

Applications

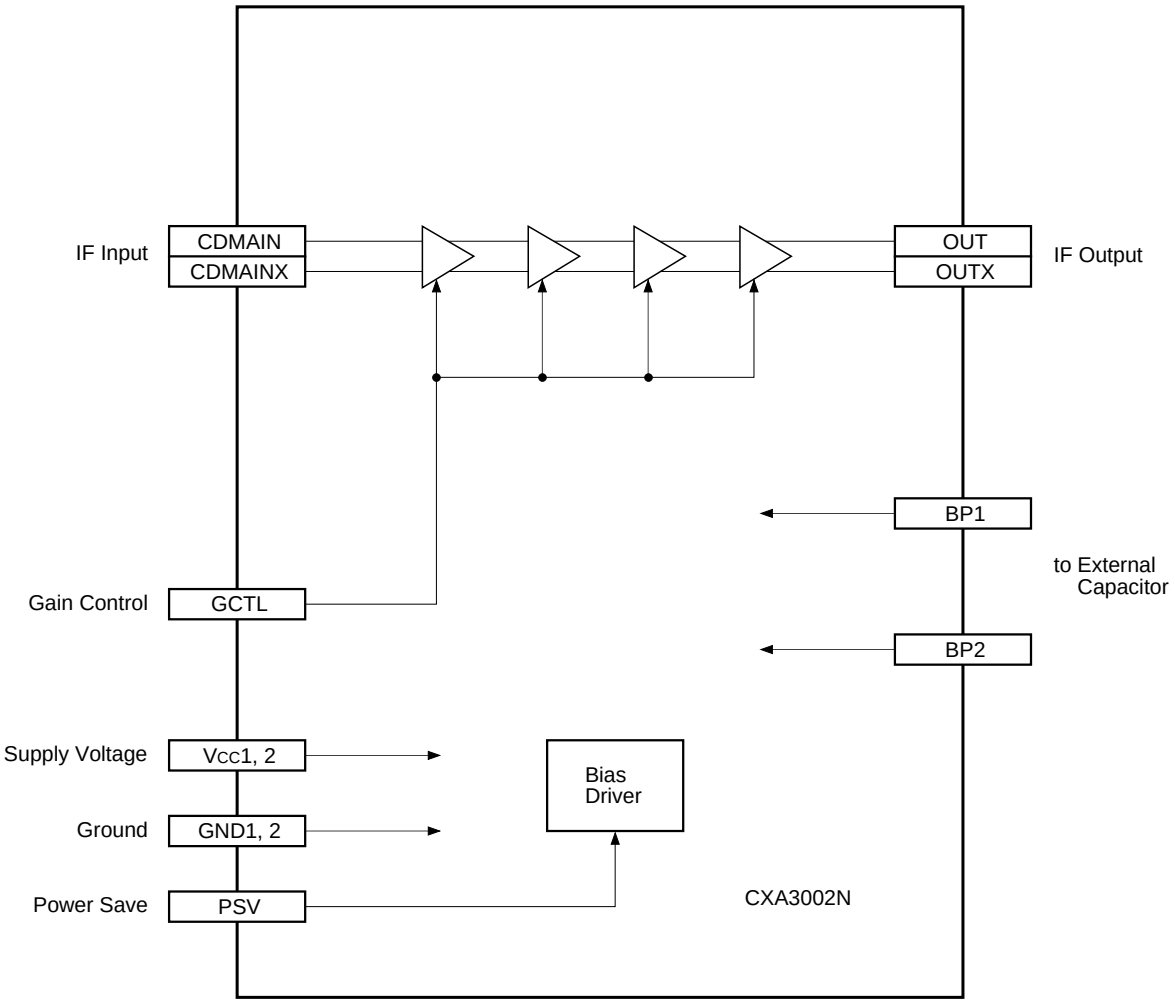
- CDMA cellular mobile phone
- CDMA & AMPS cellular phone

Structure

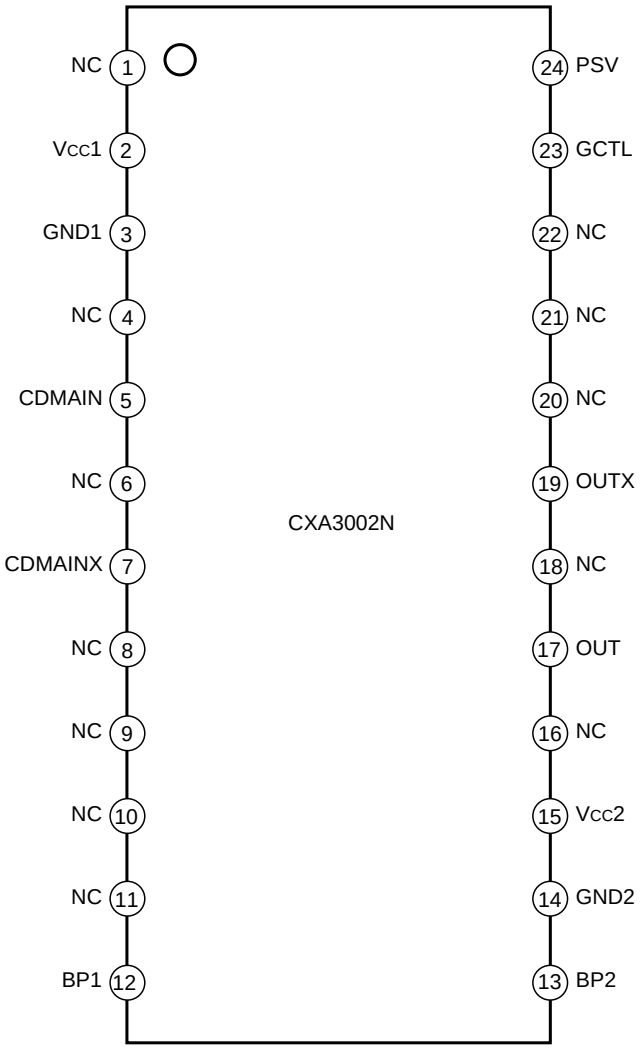
Bipolar sillicon monolithic IC

E95712-PP

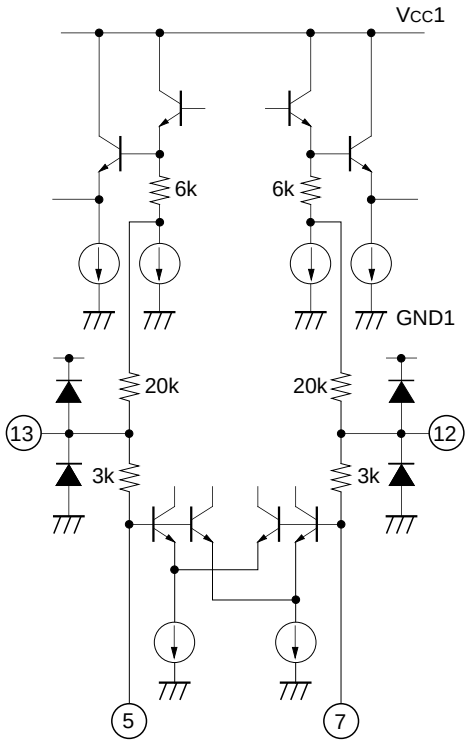
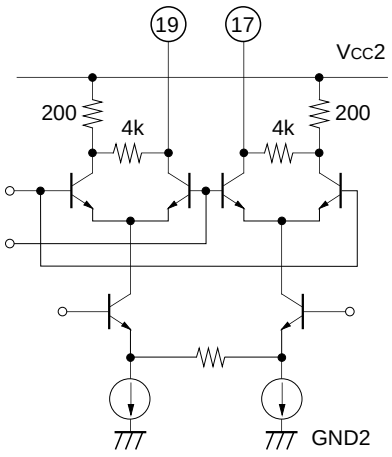
Block Diagram

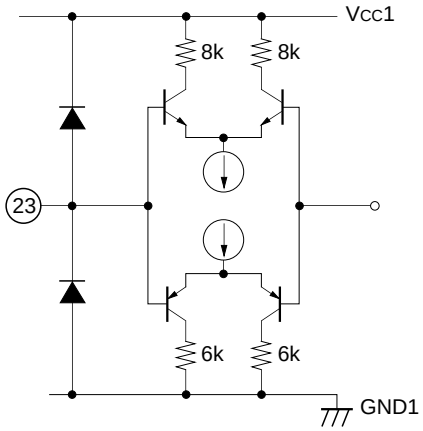
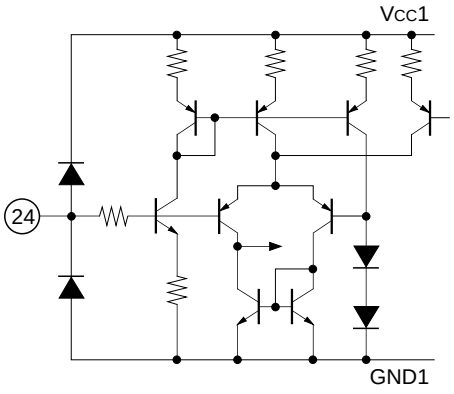


Pin Configuration



Pin Description

Pin No.	Symbol	Pin voltage Typ. (V)	Equivalent circuit	Description
1	N.C.			No connection.
2	Vcc1	3.6		Positive power supply.
3	GND1	0		Ground.
4	N.C.			No connection.
5	CDMAIN	1.9		Differential input pin for CDMA transmit IF signal.
7	CDMAINX	1.9		
6 8 9 10 11	N.C.			No connection.
12	BP1	1.9		Connected to GND with capacitor 0.01µF.
13	BP2	1.9		
14	GND2	0		Ground for output stage.
15	Vcc2	3.6		Positive power supply for output stage.
16	N.C.			No connection.
17	OUT			Differential output pins for transmit IF signal. Open collector output.
19	OUTX			

Pin No.	Symbol	Pin voltage Typ. (V)	Equivalent circuit	Description
18 20 21 22	N.C.			No connection.
23	GCTL			Gain control pin with a ripple filter.
24	PSV			Power save function pin. High: Active Low: Power save

Electrical Characteristics

DC characteristics

(V_{CC} = 3.6V, Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current Consumption 1	$I_{CC}1$	Gain = MAX., Pin 2	4.1	5.7	7.3	mA
Current Consumption 2	$I_{CC}2$	Gain = MAX., Pin 15	3.2	4.4	5.6	
Current Consumption 3	$I_{CC}3$	Gain = MAX., Pin 17 + Pin 19	5	7	9	
Current Consumption 4	$I_{CC}4$	Gain = MIN., Pin 2	4.2	5.8	7.4	
Current Consumption 5	$I_{CC}5$	Gain = MIN., Pin15	8.0	11.1	14.2	
Current Consumption 6	$I_{CC}6$	Gain = MIN., Pin 17 + Pin 19	0.2	0.3	0.4	
Current Consumption 7	$I_{CC}7$	V_{PSV} = 0.5V, Pin 2			1	µA
Current Consumption 8	$I_{CC}8$	V_{PSV} = 0.5V, Pin 15			1	
Current Consumption 9	$I_{CC}9$	V_{PSV} = 0.5V, Pin 17 + Pin 19			1	
Input current pin 23H	$I_{GCTL\ H}$	V_{GCTL} = 3V			10	
Input current pin 23L	$I_{GCTL\ L}$	V_{GCTL} = 0.5V	–10			
Input current pin 24H	I_{PSVH}	V_{PSV} = 3V			10	
Input current pin 24L	I_{PSVL}	V_{PSV} = 0.5V	–10			
PSV high voltage	V_{PSH}	Pin 24	3			V
PSV low voltage	V_{PSL}				0.5	

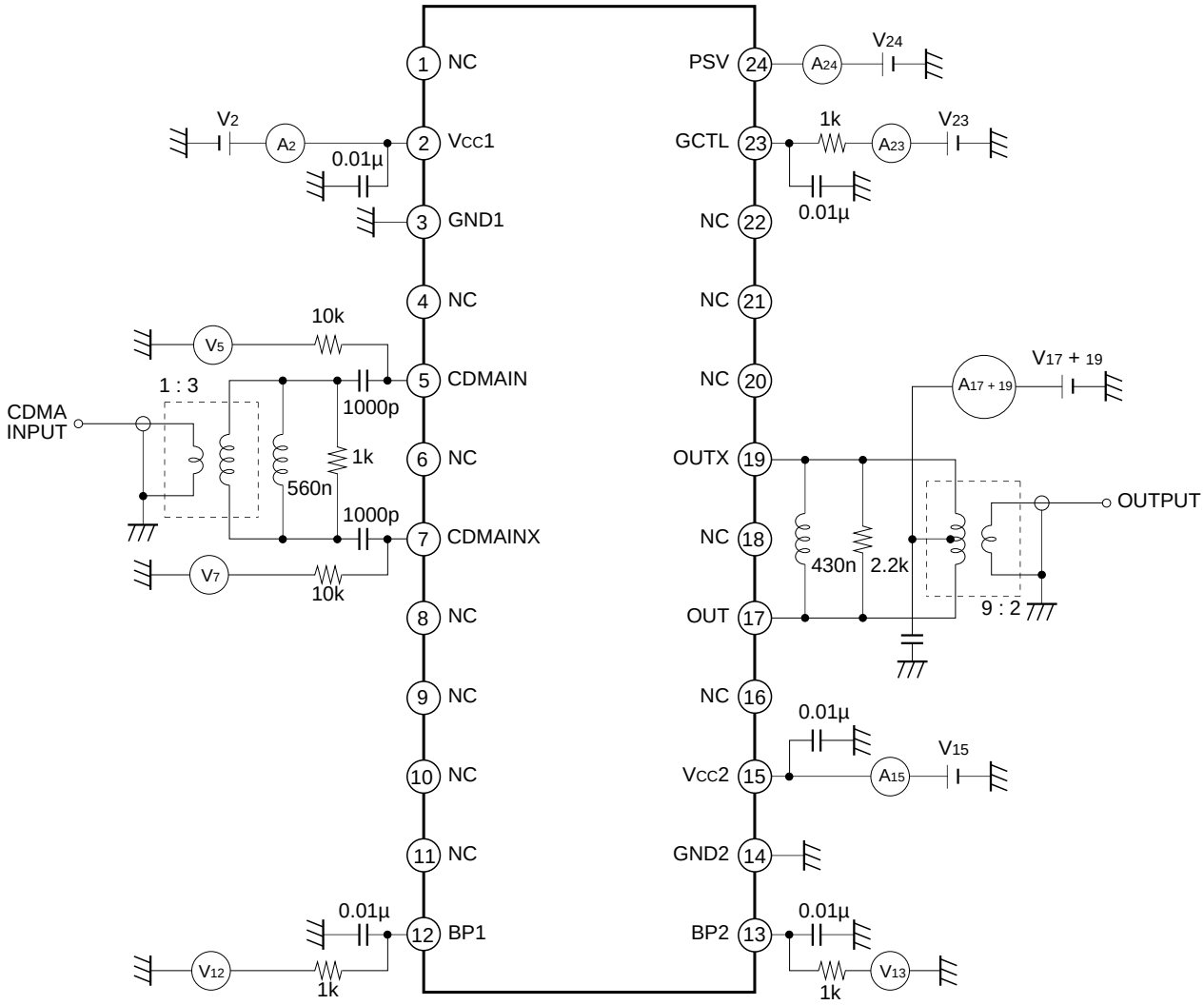
AC characteristics

(V_{CC} = 3.6V, Ta = 25°C)

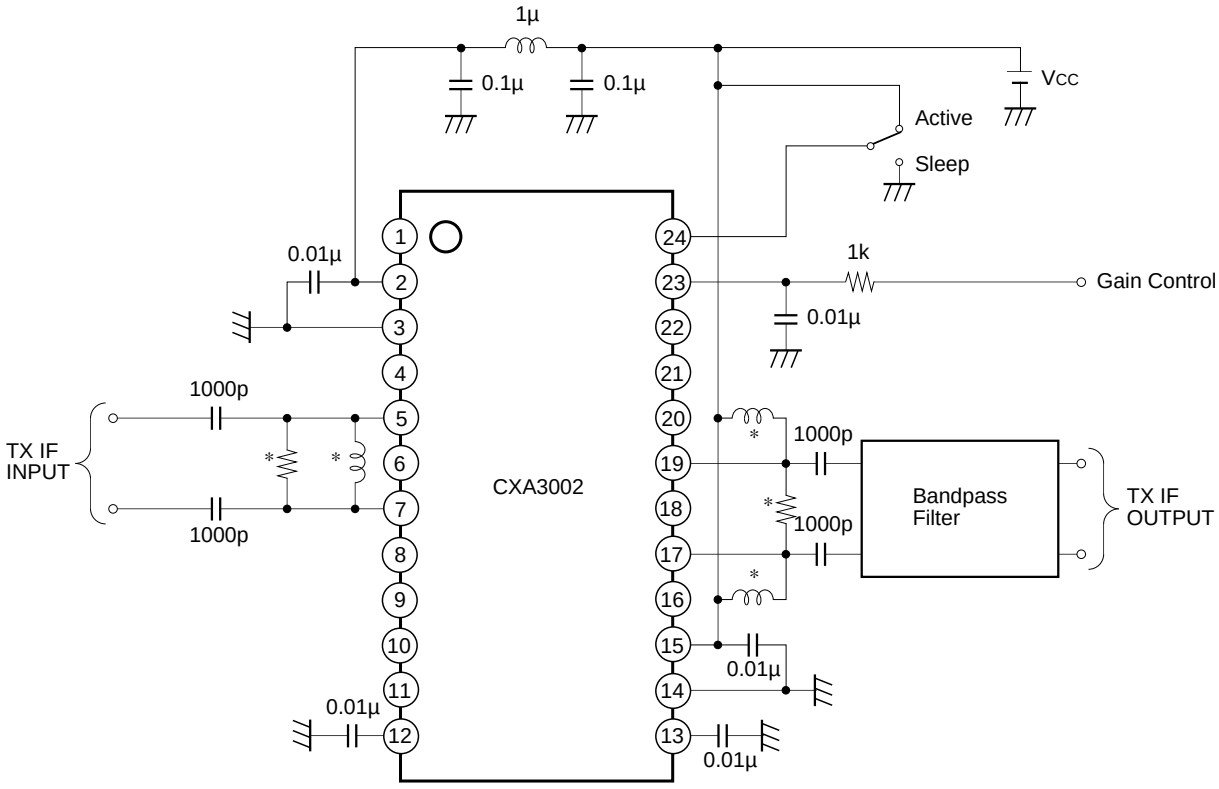
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating frequency range	F_R		10		200	MHz
Gain MAX.	$G_{2.7}$	V_{GCTL} = 2.7V	38.5	42.5		dB
Gain center	$G_{1.5}$	V_{GCTL} = 1.5V	–10	–5	0	
Gain MIN.	$G_{0.3}$	V_{GCTL} = 0.3V		–58	–52	
Gain slope	G_{CLIN}	V_{GCTL} = 1 to 2V	58	61	64	dB/V
Input level 3rd order intercept point	IIP_3	G = 35dB* F_1 = 131.38MHz F_2 = 132.38MHz Measure to 130.38MHz	–30	–26		dBm
Noise Figure	NF	G = 35dB* Used 1MHz BPF Measure to 130.38MHz		10	14	dB

* Adjust GCTL voltage, and set the overall gain to 35dB.

Measurement Circuit



Application Circuit



* Must be adjusting values to result a best impedance matching between BPF filter and this IC.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Design Reference Values

Single ended measurement (V_{CC} = 3.6V, Ta = 25°C)

Item	Symbol	Conditions	Typ.	Unit
Input resistance	R_{IN}	f = 130.38MHz, V_{GCTL} = 1.5V	1.9	kΩ
Input capacitance	C_{IN}		4	pF
Output resistance	R_{OUT}		1.6	kΩ
Output capacitance	C_{OUT}		5	pF

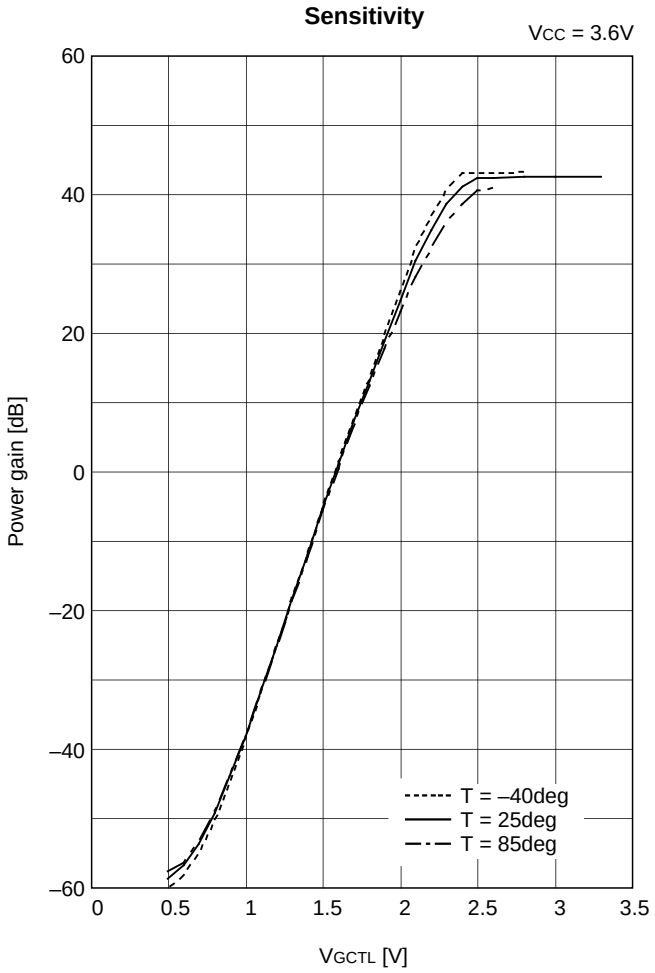
Notes on Operation

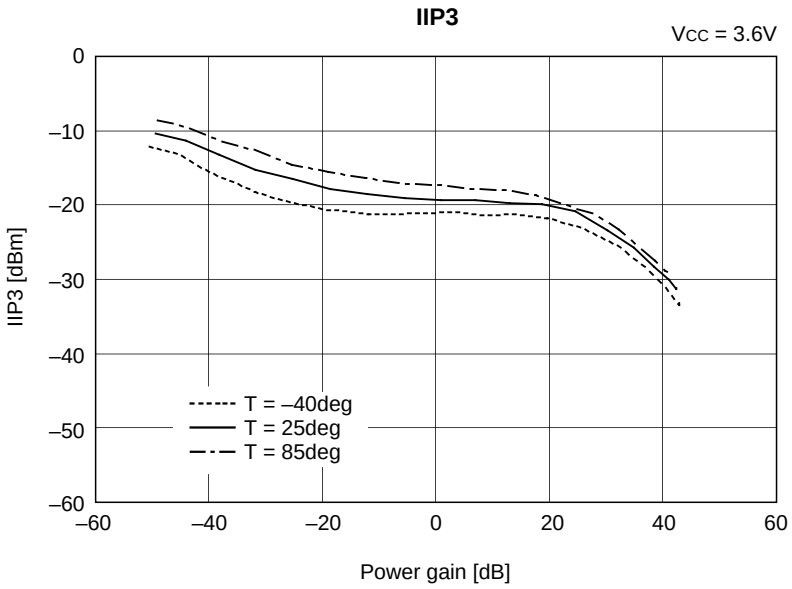
1) This IC is a wideband amplifier with wide gain control range. Separate Pin 3 (GND1) and Pin 14 (GND2) to prevent interference between input and output. Furthermore, the decoupling capacitors between Pins 2 and 3, Pins 14 and 15 should be as close to the IC as possible.

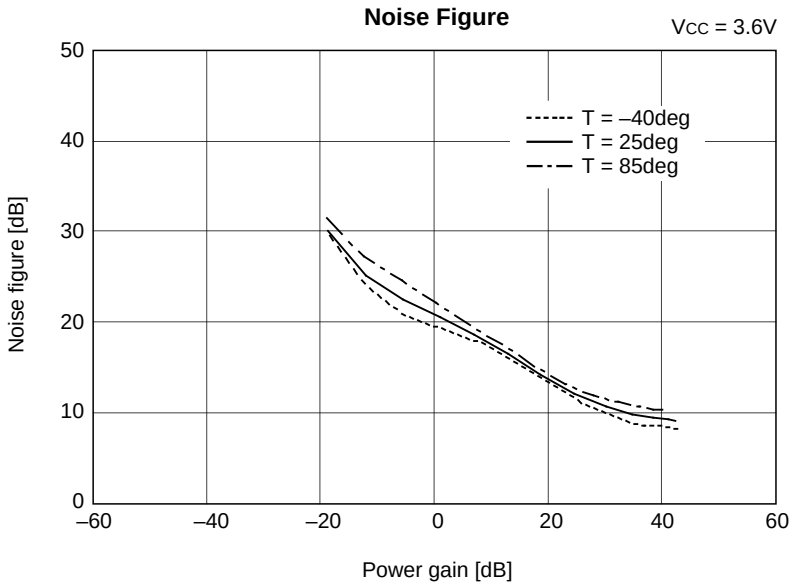
2) This IC assumes the excellent characteristics when the differential input impedance between Pins 5 and 7 is 500Ω, and the differential output impedance between Pins 17 and 19 is 1kΩ. Refer to the Measurement Circuit for the external element settings, etc.

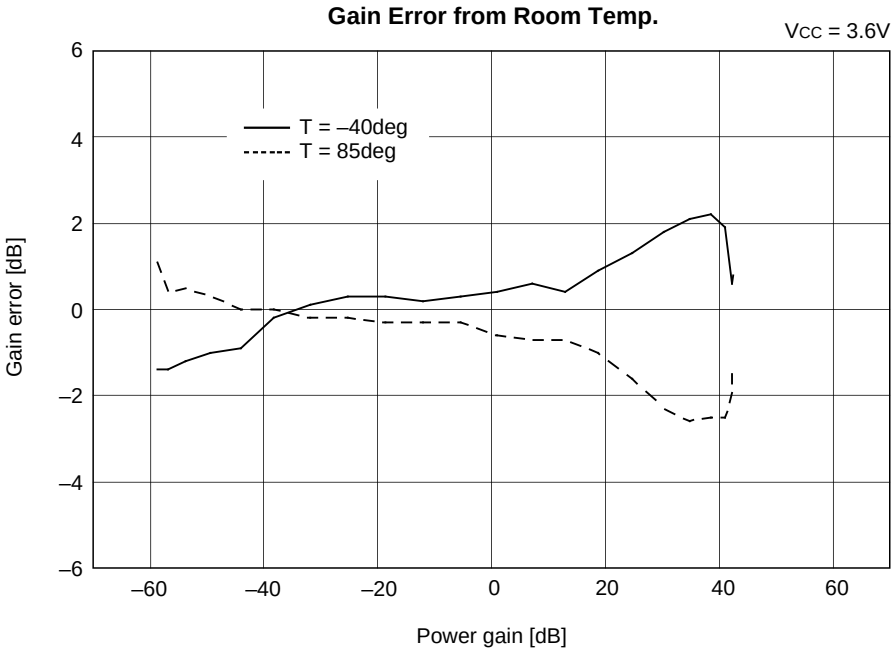
3) Connect the capacitors, which are connected to Pins 12 and 13, to Pin 14 (GND2).

4) Pay attention to handling this IC because its electrostatic discharge strength is weak.


Sensitivity
VCC = 3.6V
Power gain [dB]
60
40
20
0
–20
–40
–60
0
0.5
1
1.5
2
2.5
3
3.5
VGCTL [V]
T = –40deg
T = 25deg
T = 85deg

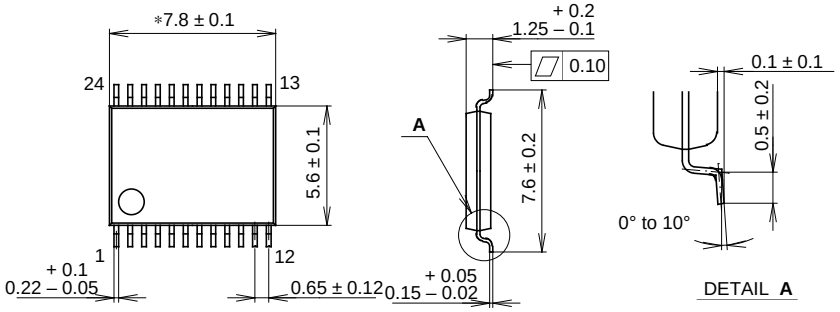

IIP3
VCC = 3.6V
IIP3 [dBm]
0
–10
–20
–30
–40
–50
–60
–60
–40
–20
0
20
40
60
Power gain [dB]
T = –40deg
T = 25deg
T = 85deg


Noise Figure
VCC = 3.6V
T = –40deg
T = 25deg
T = 85deg
Noise figure [dB]
50
40
30
20
10
0
–60
–40
–20
0
20
40
60
Power gain [dB]


Gain Error from Room Temp.
VCC = 3.6V
T = –40deg
T = 85deg
Gain error [dB]
6
4
2
0
–2
–4
–6
–60
–40
–20
0
20
40
60
Power gain [dB]

Package Outline Unit: mm

24PIN SSOP (PLASTIC) 275mil



NOTE : ∗NOT INCLUDE MOLD FINS.

PACKAGE STRUCTURE

SONY CODE	SSOP-24P-L01
EIAJ CODE	A SIMILAR TO SSOP024-P-0300
JEDEC CODE	———

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	———