SONY

CXA3314ER

6GHz PLL

Description

The CXA3314ER is a general-purpose PLL IC which directly frequency divides RF up to 6GHz in combination with an external VCO and loop.

Features

- Low current consumption: 9mA (typ. at V_{CC} = 3V)
- Low voltage operation: 2.7 to 3.3V
- Small package: 24-pin VQFN (plastic)
- Supports sleep mode: 10µA (max. at V_{CC} = 3V)
- Data setting by a 3-wire interface
- Reference frequency divider
  Reference counter: 15 bits (3 to 32767)
- Comparison frequency divider
  Fixed frequency division: 4
  Swallow counter: 5 bits (0 to 31)
  Main counter: 13 bits (3 to 8191)
  Comparison frequency division value: 4 × (992 to 262143)
- Built-in charge pump circuit with high-speed pull-in and normal modes
- Lock signal output function

Applications

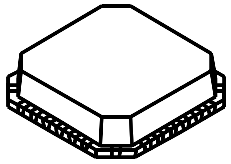
This IC is ideal for the synthesizers of microwave communications equipment up to 6GHz and general-purpose PLL synthesizers such as in high-speed, high frequency measurement equipment.

- ETC (ITS) related
- VCO modules
- Wireless LAN communications
- High-speed, high frequency measurement equipment

Structure

Bipolar silicon monolithic IC

24 pin VQFN (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	3.6	V
• Operating temperature	Topr	–30 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	900	mW

Operating Condition

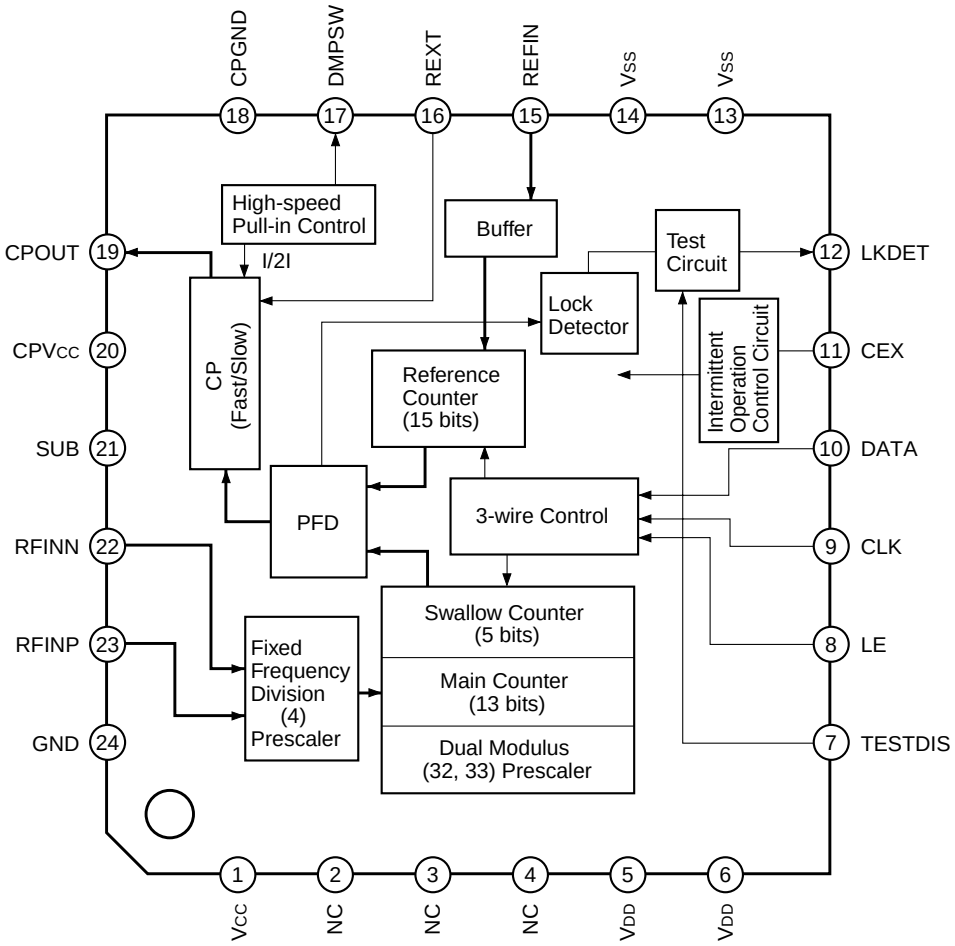
Supply voltage	V_{CC}	2.7 to 3.3	V

Note on ESD strength

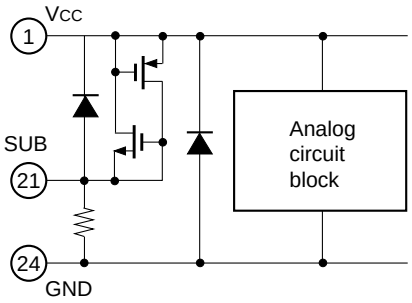
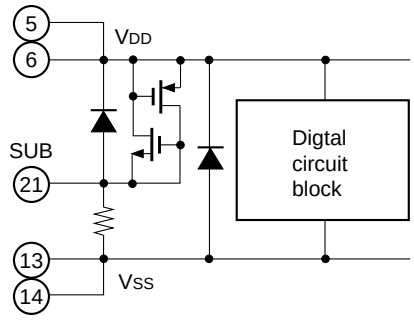
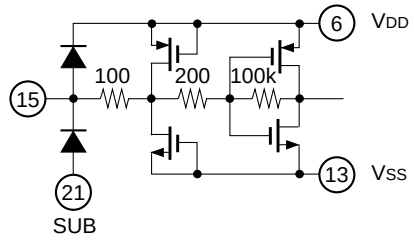
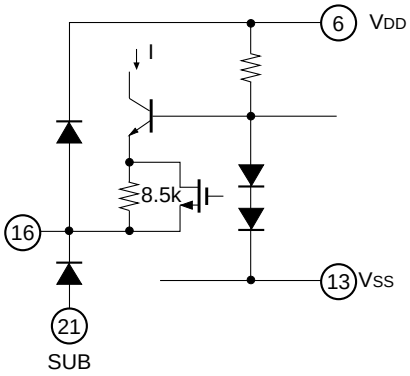
This product has a low ESD strength to ensure the high frequency characteristics.
Sony semiconductor devices are classified into ESD strength ranks from A to E based on ESD test results according to Sony original criteria.
These ESD ranks are set for each test, and indicate the ESD risk for each breakdown model.

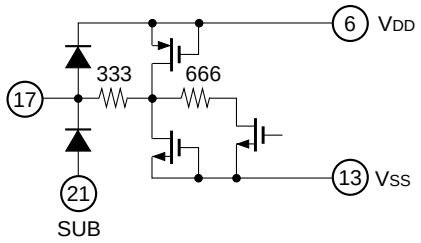
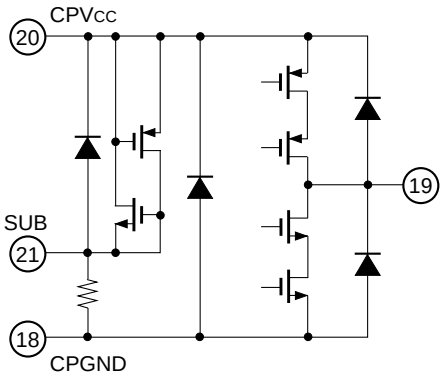
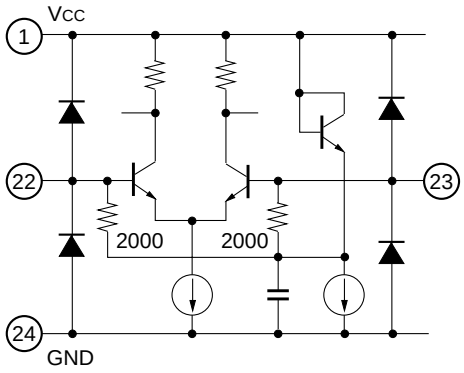
E00782E2Z-PS

Block Diagram and Pin Configuration

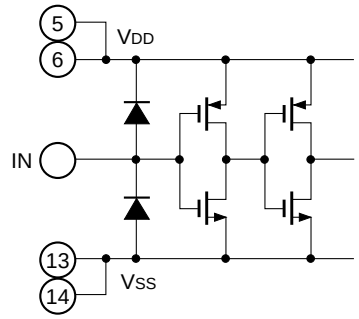
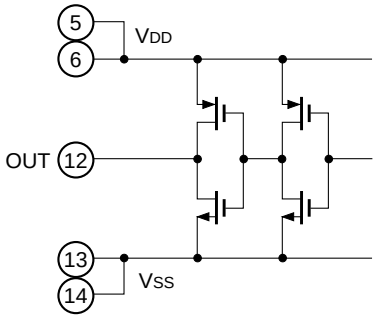


Pin Description

Pin No.	Symbol	Standard DC voltage [V]	Equivalent circuit	Description
1	V_{CC}	3		Power supply.
21	SUB	0		Substrate. Connect to GND normally.
24	GND	0		Ground.
2, 3, 4	NC	—		No connected.
5, 6	V_{DD}	3		Power supply for output stage.
13, 14	V_{SS}	0		Ground.
15	REFIN	1/2V_{CC}		Reference frequency signal input.
16	REXT	0.15		Internal reference current setting. Connect to GND via a external resistor (1.8kΩ). Icp = I × 6.7 I ≈ I_{Rext} Icp: Charge pump current I: Internal reference current I_{Rext}: External resistor current Internal charge pump current switching.

Pin No.	Symbol	Standard DC voltage [V]	Equivalent circuit	Description
17	DMPSW	—		Connect to the loop filter via a resistor.
18	CPGND	0		Ground for the charge pump output.
19	CPOUT	—		Charge pump output.
20	CPVCC	3		Power supply for the charge pump output.
22	RFINN	Vcc – 0.9		VCO signal input.
23	RFINP	Vcc – 0.9		

Pin Description

Pin No.	Symbol	I/O	Equivalent circuit	Description
7	TESTDIS	I		Test mode switch pin. High: Active Low: Test mode
8	LE	I		Latch input.
9	CLK	I		Clock input.
10	DATA	I		Data input.
11	CEX	I		Power save function pins. High: Power save Low: Active
12	LKDET	O		Lock detection signal output. •Active mode High: Lock Low: Unlock •Test mode Refer to “2. Test mode setting” on page 12.

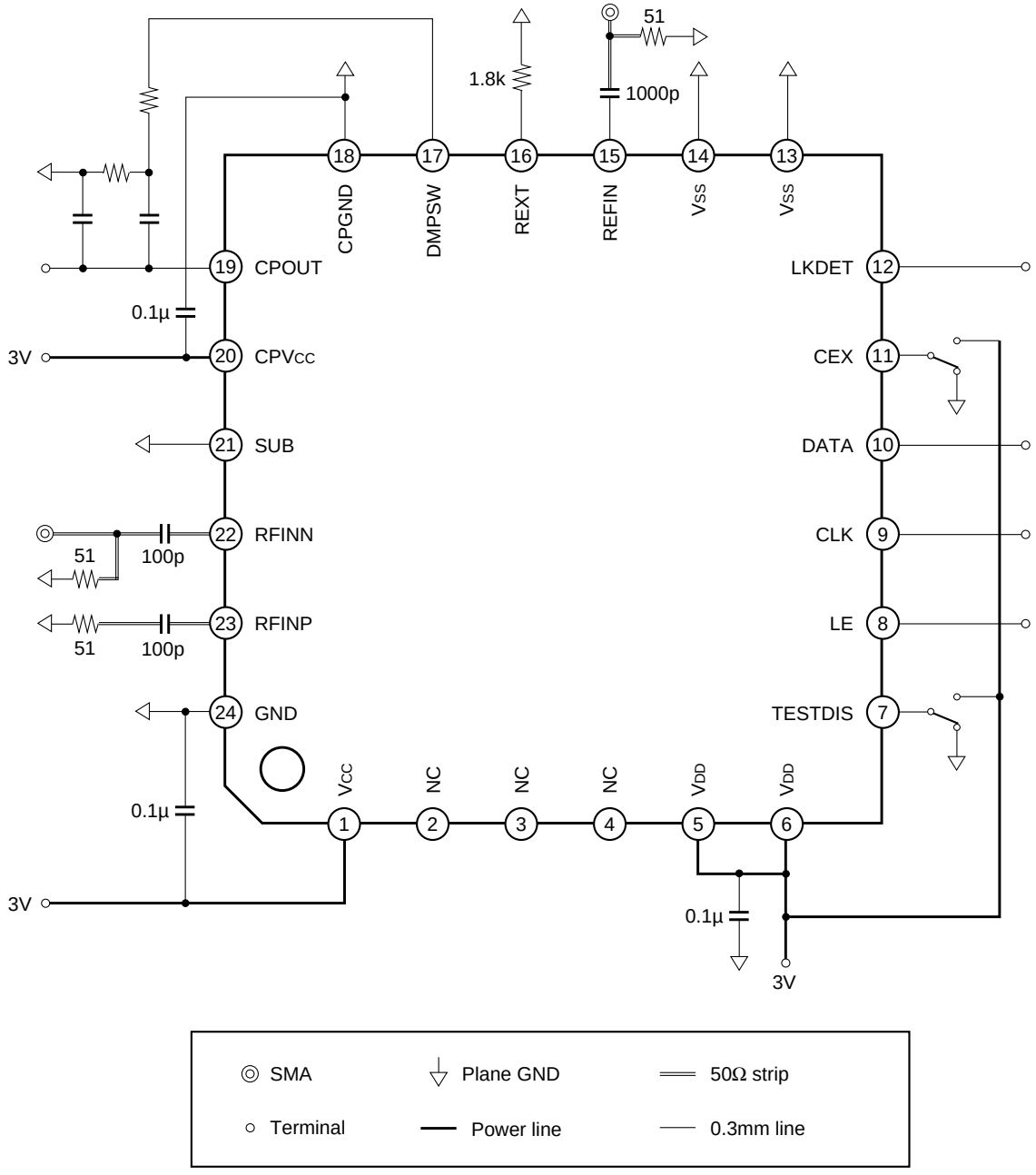
Electrical Characteristics (V_{CC} = 3V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	ICC	Current flowing to Pins 1, 6 and 20 during operation (Pin 11 (CEX): 0)		9	14	mA
Current consumption (in sleep mode)	ICC (PS)	Current flowing to Pins 1, 6 and 20 in sleep mode (Pin 11 (CEX): High)			10	µA
Operating frequency	F-RF	V-RF = –10dBm	2		6	GHz
Input level	V-RF	F-RF = 5.845GHz	–12		+10	dBm
Reference input operating frequency	F-REF	V-REF = 0.2Vp-p	10		30	MHz
Reference input level	V-REF	F-REF = 10MHz	0.2		2.0	Vp-p

Design Reference Values

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
CEX DATA CLK LE	High input voltage	V_{IH}	—	V_{CC} – 0.2		V_{CC}	V
	High input current	I_{IH}	—	–1		+1	µA
	Low input voltage	V_{IL}	—	0		GND + 0.2	V
	Low input current	I_{IL}	—	–1		+1	µA
REFIN input resistance		R_{IREF}	DC resistance value		100		kΩ
RFINN input resistance		R_{IRF}	DC resistance value		2000		Ω
Pin 17 input resistance		ON	DC resistance value		3000		Ω

Electrical Characteristics Measurement Circuit and Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

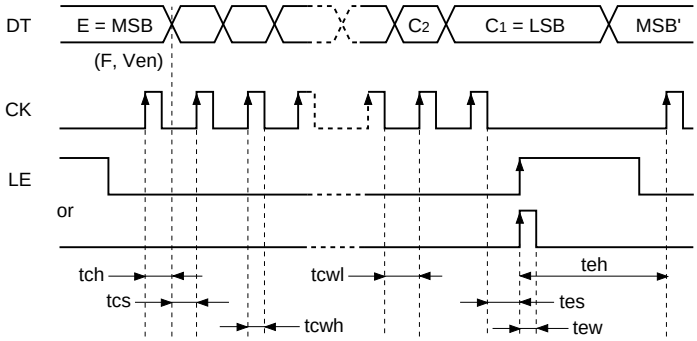
The CXA3314ER can make the following operation settings using the three DT, CK and LE signals.

Item	Item number
Counter frequency division value and pull-in mode settings	1
Reference counter (R counter) frequency division value setting	1-1
Swallow counter and main counter (N counter) frequency division value settings	1-2
Pull-in mode setting	1-3
Initialization	1-4
Test mode	1-5
Test mode setting	2
Standby mode setting	3

1. Counter frequency division value and pull-in mode setting method

The CXA3314ER sets data using the three DT, CK and LE signals. At this time, serial data is input as described below.

21-bit serial data is loaded via DT in order from the MSB at the rising edge of CK. After 21 bits have been input, the data is actually set at the rising edge of LE.



However, as mentioned above, if the counter overlaps with the preset timing of the frequency division value, there is the risk that an incorrect preset value may be preset in the counter. Therefore, the frequency division value should be set in sync with the counter output so as to avoid the preset timing. That is to say, the counter frequency division value is set after waiting for up to one cycle of the previous comparison cycle. Therefore, CK input is prohibited for the previous comparison cycle (Tcmp) after LE.

The AC characteristics are as follows.

Symbol	Item	Min.	Unit
tcs	Data to clock setup time	50	ns
tch	Data to clock hold time	10	ns
tcwh	Clock pulse width high	50	ns
tcwl	Clock pulse width low	50	ns
tew	Load enable pulse width	50	ns
tes	Clock to load enable setup time	50	ns
teh	Clock load enable hold time	Tcmp	ns

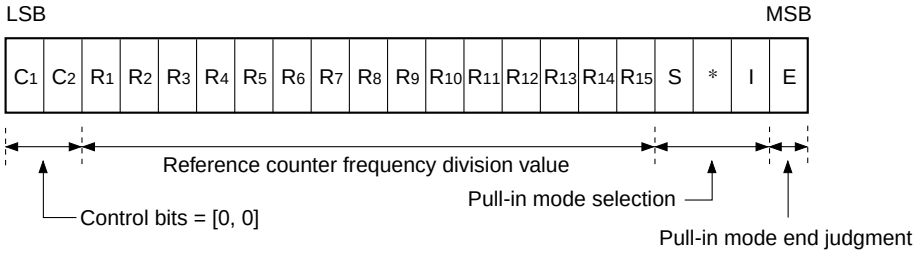
Tcmp: Previous comparison cycle

The final two bits of the serial input are the control bits (C_1, C_2), and the setting item is selected according to these values. The setting items corresponding to the control bit values are as follows.

C_1	C_2	Setting item
0	0	R counter frequency division value setting, pull-in mode setting
1	0	N counter frequency division value setting, pull-in start/end
1	1	Initialization
0	1	Test mode setting

1-1. Reference counter (R counter) frequency division value setting

When the control bits [C_1, C_2] = [0, 0], the 15 bits (R_{15} to R_1) of the serially input 21 bits are set as the reference counter frequency division value R. The value input as the frequency division value must satisfy the condition $3 \leq R \leq 32767$.
In addition, (S, I, E) of the upper 4 bits are set simultaneously with the R value as the pull-in mode. The serial input format is as follows.



* Always set to "0".

15-bit reference counter frequency division value R ($3 \leq R \leq 32767$)

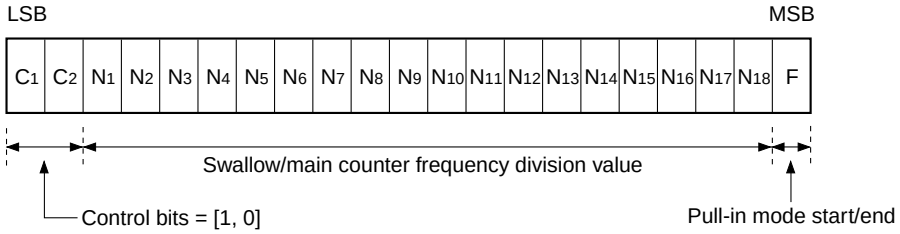
R	R_{15}	R_{14}	R_{13}	R_{12}	R_{11}	R_{10}	R_9	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

1-2. Swallow counter and main counter (N counter) frequency division value setting

The N counter is comprised of a 5-bit swallow counter and a 13-bit main counter. When the control bits [C_1, C_2] = [1, 0], the 18 bits (N_{18} to N_1) of the serially input 21 bits are set as the N counter frequency division value N = 32 × M + S. The values input as the frequency division values must satisfy the conditions 0 ≤ S ≤ 31 and S ≤ M ≤ 8191. Adding the condition that the N value be a continuous value, the optional setting range is 992 ≤ N ≤ 262143.

Note that in the CXA3314ER, the input to the N counter is the fixed 1/4 frequency division of the VCO output. Therefore, care must be taken as VCO frequency/comparison frequency (VCK) = 4 × N.

In addition, the uppermost bit (F) is set simultaneously with the N value as the pull-in start/end bit. The serial input format is as follows.



5-bit swallow counter frequency division value S (0 ≤ S ≤ 31, S ≤ M)

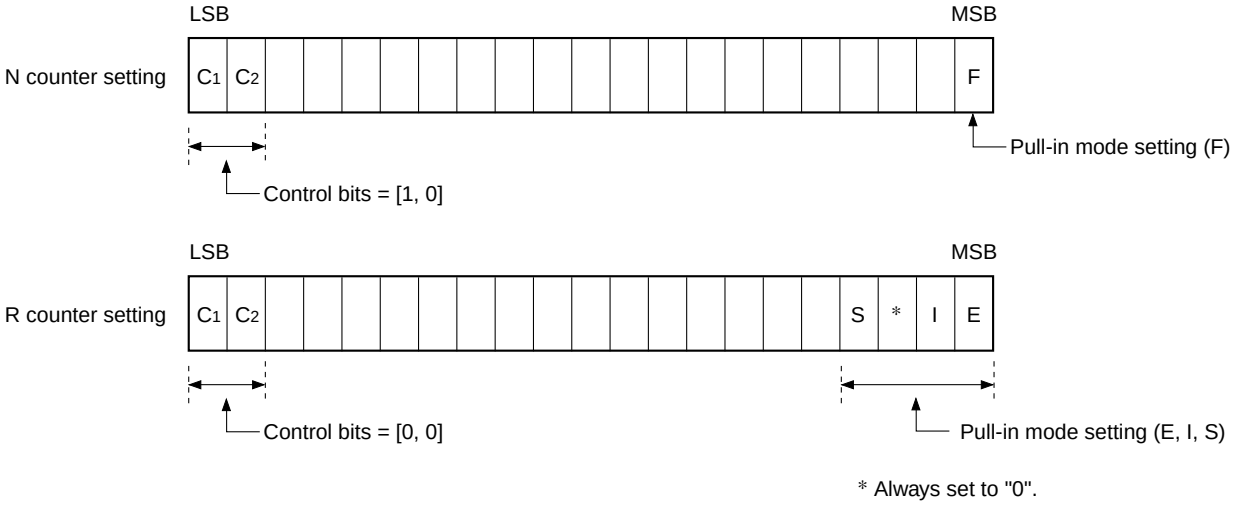
S	N_5	N_4	N_3	N_2	N_1
0	0	0	0	0	0
1	0	0	0	0	1
:	:	:	:	:	:
31	1	1	1	1	1

13-bit main counter frequency division value M (3 ≤ M ≤ 8191)

M	N_{18}	N_{17}	N_{16}	N_{15}	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	N_7	N_6
3	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	1	0	0
:	:	:	:	:	:	:	:	:	:	:	:	:	:
8191	1	1	1	1	1	1	1	1	1	1	1	1	1

1-3. Pull-in mode setting

The uppermost bit (F) set simultaneously with the N value and (S, I, E) of the upper 4 bits set simultaneously with the R value are used for various settings in pull-in mode.



The meaning of each bit is as follows.

F: Pull-in mode start/end flag
Pull-in mode is activated and the lock detector is cleared when the F flag is set to "1".
Pull-in mode ends when the F flag is set to "0".

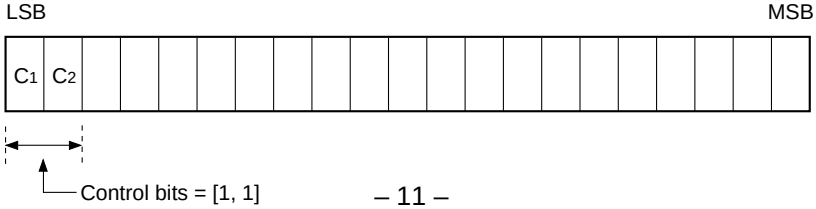
E: Pull-in mode end judgment flag
Pull-in mode automatically ends when the E flag is "1" and lock is detected.
When the E flag is "0", pull-in mode continues until the F flag is set to "0".

IS: Pull-in mode flags
These flags select the high-speed pull-in method used in pull-in mode.
The various methods are active at the following timings.

Loop filter saturation reset	When the S flag is "1".
CP current doubled	When the I flag is "1".
Damping resistance value halved	When either of the S or I flags is "1".

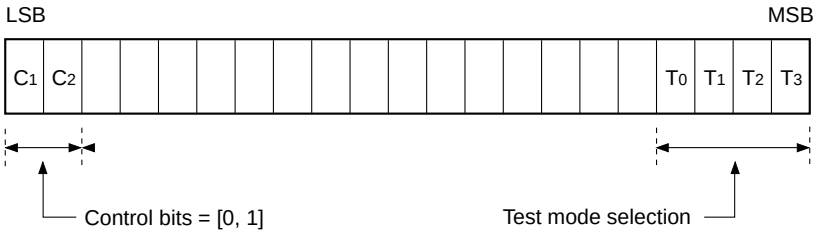
1-4. Initialization

When the control bits [C_1, C_2] = [1, 1], the counter frequency division value and pull-in mode setting bits are initialized and set to R = 40, N = 5795, F = 1, SI = 11, and E = 1. The serial input format is as follows.



1-5. Test mode

When the control bits [C_1, C_2] = [0, 1], the test command is set. The serial input format is as follows. Test mode operation is described in detail in the following section.



2. Test mode setting

Switching between normal operation mode and test mode is controlled by the TESTDIS pin. Normal operation mode results when TESTDIS is “1”, and test mode when “0”.
In test mode, the mode settings can also be controlled by 3-wire interface input. The input format is the same as that described above. Note that the settings are valid only while TESTDIS is “0”. When TESTDIS is “1”, T_0, T_1, T_2 and T_3 are all initialized to “0”.
The test mode operations set by the setting bits are shown in the table below.

T_0	T_1	T_2	T_3	
x	x	x	0	Frequency division error detection flag function off
x	x	x	1	Frequency division error detection flag function on; output to LKDET pin
0	0	x	0	$\overline{\text{RCK}}$ signal output to LKDET pin
1	0	x	0	$\overline{\text{VCK}}$ signal output to LKDET pin
0	1	x	0	$\overline{\text{MOD}}$ signal output to LKDET pin
1	1	x	0	Pull-in ON/OFF signal output to LKDET pin

x: don’t care

3. Standby mode setting

Standby operation is controlled by the CEX pin. Normal operation mode results when CEX is “0”, and standby mode when “1”.
In standby mode, the R counter, N counter, PFD and lock detector are all cleared, and the CP output is maintained at high impedance. In addition, the counter frequency division value setting and pull-in mode setting are saved.

Loop Filter Constant Settings

The loop filter constant calculation method is shown below.

Parameter definitions

N: Counter frequency division value*1
K_{VCO}: VCO sensitivity (rad/s/V) *2
ωn: Natural angular frequency (rad/s)
fn: Natural frequency (Hz)
K_{PD}: Charge pump gain (A/rad) *3
ξ: Damping factor*4
LUT: Lock-up time (s)

$$\omega n = \sqrt{\frac{K_{PD} \times K_{VCO}}{N \times C}} = 2\pi fn$$

$$fn = \frac{\omega n}{2\pi} = \frac{1}{\frac{LUT}{2.5}} \quad (\therefore LUT = \frac{5\pi}{\omega n})$$

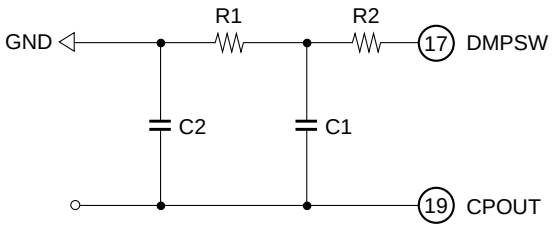
$$R = \frac{2 \times \xi}{\omega n \times C}$$

*1 Frequency division value N = (VCO oscillation frequency) ÷ (Comparison frequency)

*2 The K_{VCO} unit is normally expressed as MHz/V, but here it is multiplied by 2π to adjust the dimensions and expressed as rad/s/V.

*3 The charge pump is a current output type. Here, the current capacitance is divided by 2π to adjust the dimensions and expressed as A/rad. Note that the charge pump current capacitance of this IC is approximately 300µA in normal mode and approximately 600µA in CP current doubled mode (REXT = 1.8kΩ).

*4 $\xi = \sqrt{0.5} \approx 0.7$ (typ.)

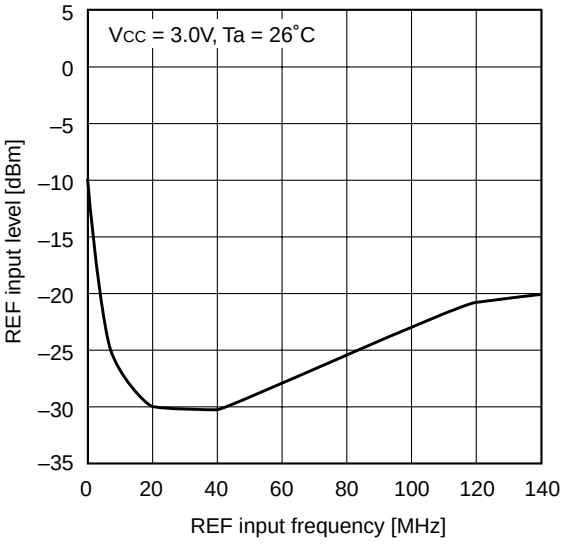


Loop filter

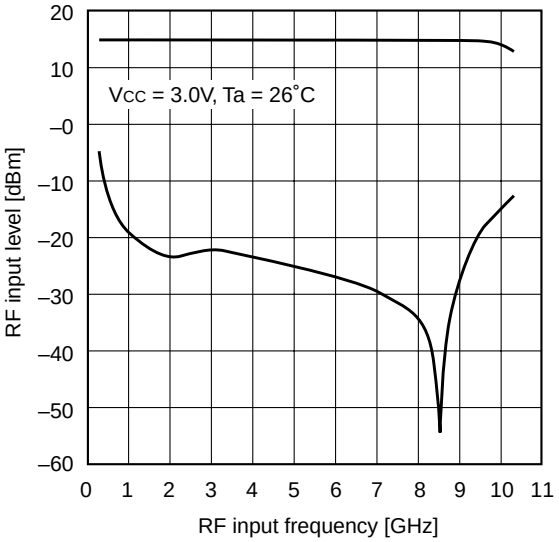
- Set C1 and R1 to the C and R values obtained by the formula above.
- C2 is generally set to 1/10 the value of C1.
- Set R2 so that the composite resistance of R1//R2 is the R value obtained by the formula above when the charge pump current value is doubled. (See *3.)

Example of Representative Characteristics

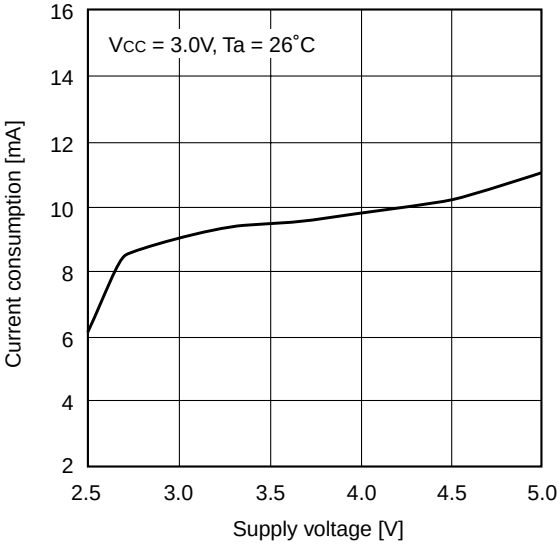
REFIN input sensitivity characteristics



RFIN input sensitivity characteristics



Current consumption

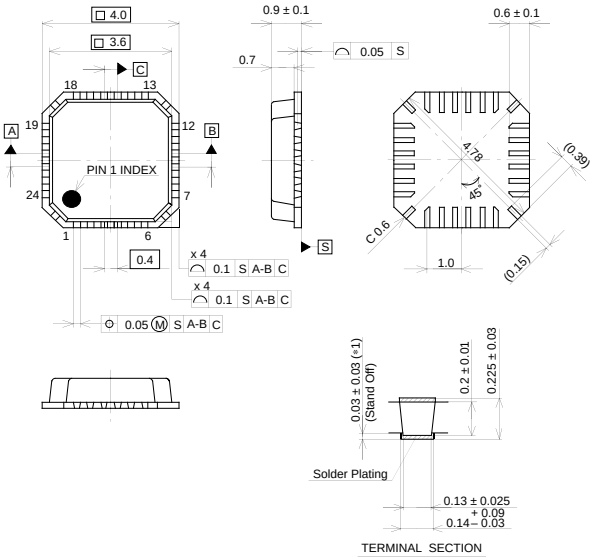


• **Example of 3-wire Serial Data Settings**

R value	N value	
0 000 000 000 000 000 011 00		R = 3
0 000 111 111 111 111 100 00		R = 32764
	0 000 000 001 111 100 000 01	N = 992
	0 001 100 001 101 010 000 01	N = 50000
	0 111 111 111 111 111 111 01	N = 262143
110 0 000 000	000 000 000 01	Reset
0 000 000 001	010 010 000 11	Initialize
0 000 000 000 001 100 100 00	0 000 000 000 011 111 010 01	R = 100, N = 250
0 000 000 000 001 100 100 00	0 000 000 100 111 000 100 01	R = 100, N = 2500
1 100 000 000 001 100 100 00	↓	R = 100, E = 1, I = 1, N = 2500
1 001 000 000 001 100 100 00	↓	R = 100, E = 1, S = 1, N = 2500
0 101 000 000 001 100 100 00	1 000 000 100 111 000 100 01	R = 100, I, S = 1, N = 2500, F = 1
MSB LSB	MSB LSB	

Package Outline Unit: mm

24PIN VQFN(PLASTIC)

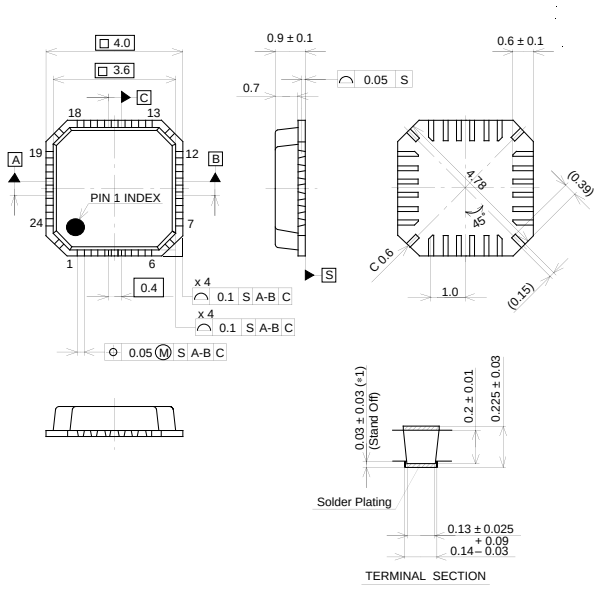


PACKAGE STRUCTURE

SONY CODE	VQFN-24P-03
EIAJ CODE	————
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g

24PIN VQFN(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	VQFN-24P-03
EIAJ CODE	————
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm