

Analog Signal Processor TX-IF IC for W-CDMA Cellular Phones *Preliminary***Description**

The CXA3329ER is an analog signal processor TX-IF IC for the W-CDMA cellular phones. This IC contains voltage-controlled gain control amplifier and quadrature modulator.

Features

- Gain control amplifier with a linear and wide gain variable range
- I-Q quadrature modulator
- Power saving switch
- Low voltage operation (2.7 to 3.3V)
- Small package (24-pin VQFN)

Applications

Analog signal processor TX-IF IC for the W-CDMA cellular phones

Structure

Bipolar silicon monolithic IC

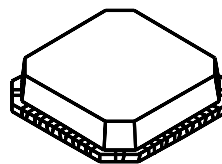
Absolute Maximum Ratings

- | | | | |
|-------------------------|-----------|--------------|----|
| • Supply voltage | V_{CC} | -0.3 to +5.5 | V |
| • Operating temperature | T_{opr} | -55 to +125 | °C |
| • Storage temperature | T_{stg} | -65 to +150 | °C |

Recommended Operating Conditions

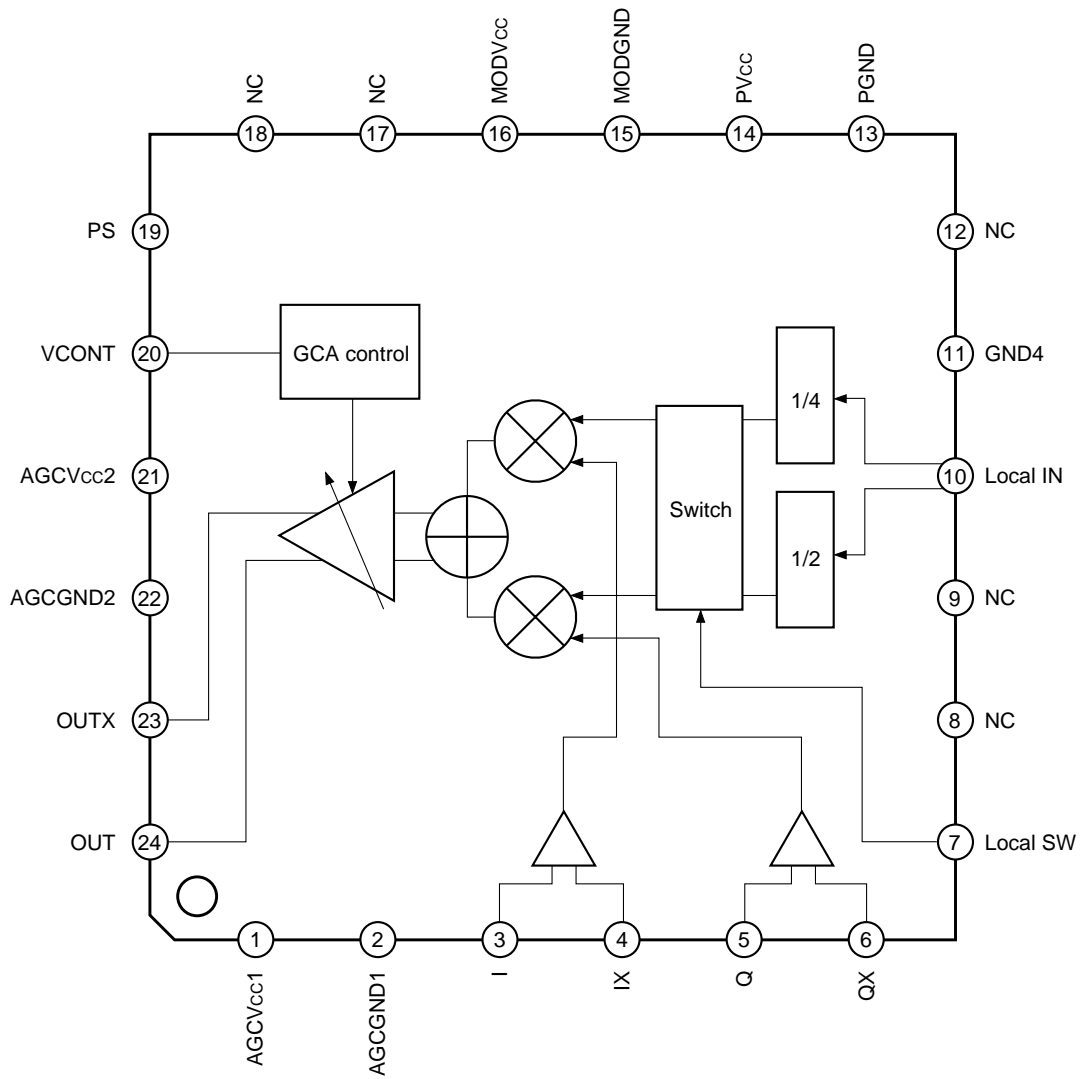
- | | | | |
|-------------------------|----------|------------|----|
| • Supply voltage | V_{CC} | 2.7 to 3.3 | V |
| • Operating temperature | T_a | -25 to +85 | °C |

24 pin VQFN (Plastic)



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram



Pin Description

Pin No.	Symbol	Typical pin voltage [V]	Equivalent circuit	Description
1	AGCVcc1	2.85		Positive power supply.
2	AGCGND1	0		Ground.
3, 4 5, 6	I, IX Q, QX	1.425		I, Q inputs. Applies a bias voltage from the external source.
7	Local SW	—		Frequency division value selection. High: 1/4 frequency division Low: 1/2 frequency division Open: Low
8, 9	NC	—		No connection.
10	Local IN	—		Local input.
11	GND4	0		Ground.
12	NC	—		No connection.
13	PGND	0		Ground.
14	PVcc	2.85		Positive power supply.
15	MODGND	0		Ground.
16	MODVcc	2.85		Positive power supply.

Pin No.	Symbol	Typical pin voltage [V]	Equivalent circuit	Description
17, 18	NC	—		No connection.
19	PS	—		Power saving mode switch input. High: Active mode Low: Power saving mode
20	VCONT	—		Gain control voltage input.
21	AGCVcc2	2.85		Positive power supply.
22	AGCGND2	0		Ground.
23 24	OUTX OUT	—		IF signal differential output.

Input Conditions for Each Pin

Pin No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
3, 4, 5, 6	I/Q bias voltage	VBIQ		1.35	1.425	1.65	V
3, 4, 5, 6	I/Q input voltage	VIQ	Differential input	—	0.4	1	Vp-p
3, 4, 5, 6	I/Q band width	BW _{IQ}		—	—	5	MHz
7	Local switch voltage-High	V _{LSH}		2.5		V _{CC}	V
7	Local switch voltage-Low	V _{LSL}		0		0.8	V
10	Local frequency	f _{LO}		—	760	—	MHz
10	Local input level	LO		-18	-15	-12	dBm
19	PS voltage-High	V _{PSH}		2.0		V _{CC}	V
19	PS voltage-Low	V _{PSL}		0		0.8	V
20	Control voltage range	V _{CN}		0		V _{CC}	V

Electrical Characteristics

Item	Symbol	Conditions	Measurement point	Min.	Typ.	Max.	Unit
DC Characteristics							
Current consumption 1	I _{max}	VCONT = 2.85V	A		24		mA
Current consumption 2	I _{min}	VCONT = 0V	A		17		
Power saving current	I _{ps}	PS = low (in power saving mode)	A	—	—	5	μA
AC Characteristics							
Output IP3	OIP3	Note1	B	8.5			dBm
Output power 1	P _{O1}	VCONT = 2.3V, differential output, f = 380MHz	B	-19	-15	-11	dBm
Output power 2	P _{O2}	VCONT = 0.3V, differential output, f = 380MHz	B	-83	-77	-73	
Gain control range	G _{cr}	VCONT = 0.3 to 2.3V, f = 380MHz	B	54	62	70	dB
Output noise power 1	N _{O1}	VCONT = 1.8V, I/Q inputs are no signal.	B	—	—	-147	dBm/ Hz
I, Q residual sideband product	I _{mg}	Suppression ratio of desired signal (f = 380 + 1) MHz and image signal (f = 380 - 1) MHz	B	—	—	-25	dBc
Carrier leak	CL	Ratio of desired signal (f = 380 + 1) MHz and local leak (f = 380) MHz	B	—	—	-18	
Input I/Q phase error	I _{QPE}	Input signal I/Q phase difference -90° when the output signal I/Q phase difference is 90°.	B	-3	0	3	deg
Input I/Q gain error	I _{QGE}	I/Q input signal level difference when the output signal I/Q levels are the same.	B	-2.5	0	2.5	dB

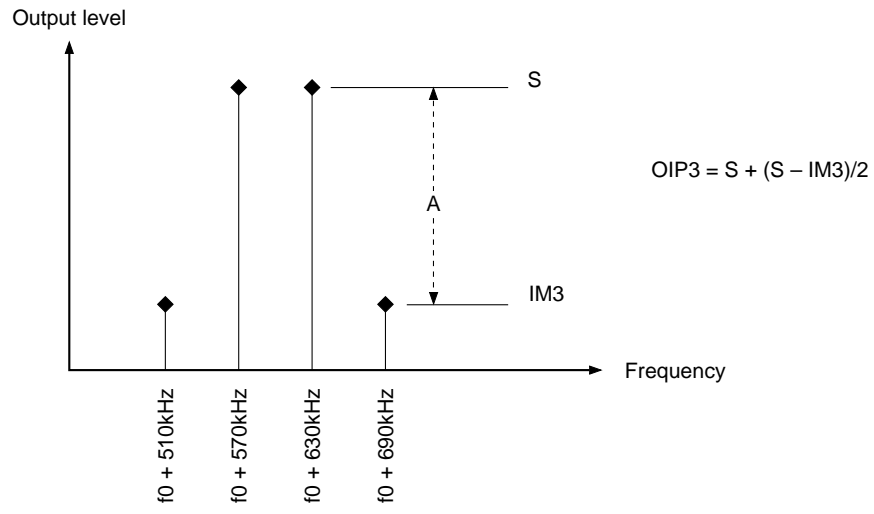
- Unless otherwise specified, the I/Q baseband input signals and local input signal use the conditions shown in the Electrical Characteristics Measurement Circuit and the control voltage and power saving pins are set to VCONT = 2.3V, PS = high.

The local switching pin is left open (1/2 frequency division).

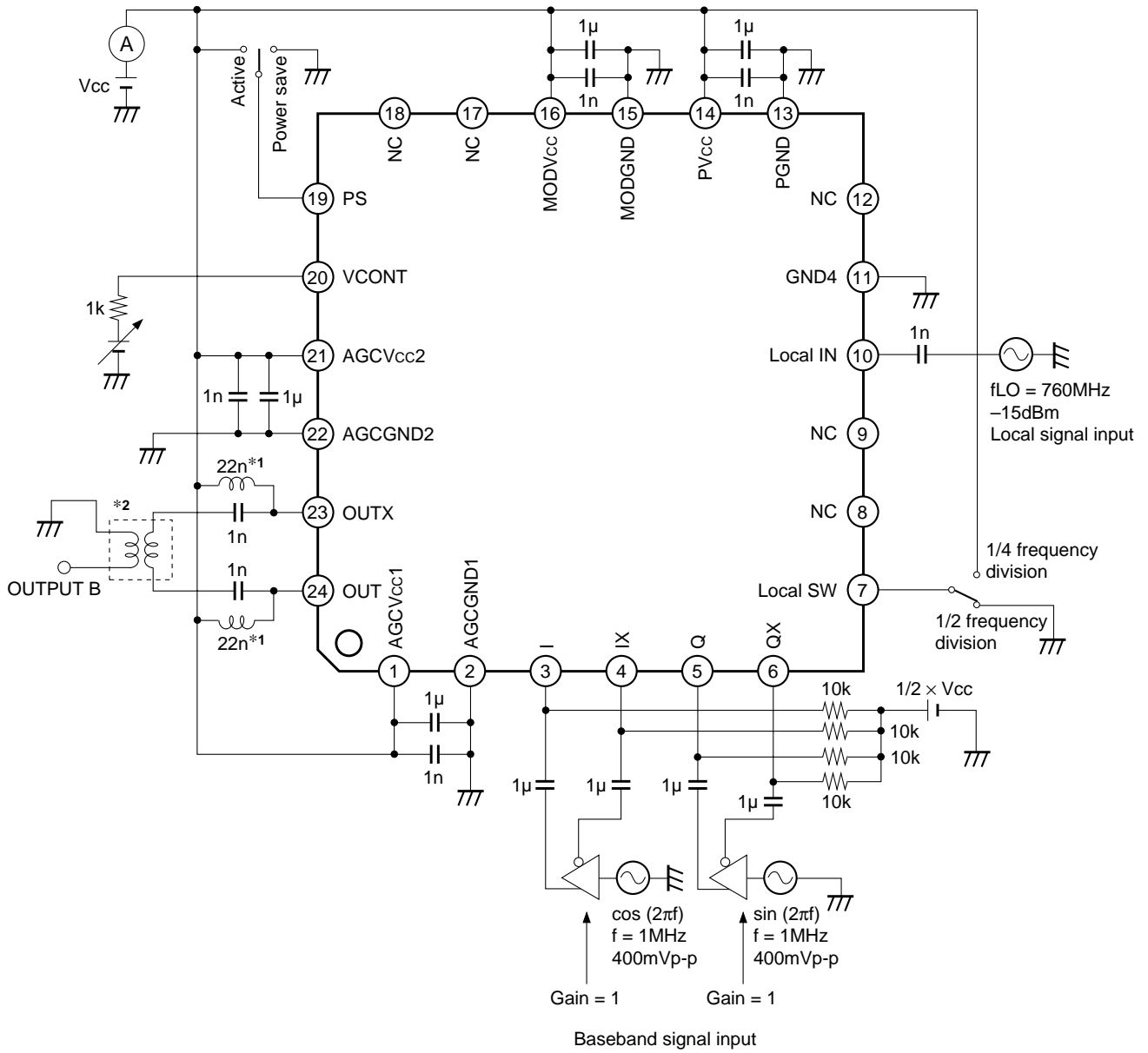
- IF output impedance is 1kΩ.
- Values measured with a Sony evaluation board.

Note1) Set the control voltage so that the output power becomes -15dBm under the conditions shown in the Electrical Characteristics Measurement Circuit. Input the two tone signals of 570kHz, 200mVp-p and 630kHz, 200mVp-p to I-IX; and also input to Q-QX the two tone signals whose phases are deviated by 90 degrees from those signals.

The ratio of the desired component and the 3rd order harmonic component of the outputs resulted from the above is measured, and the power level that is made by adding the half ratio to the desired component power level is labeled as the output IP3. See the figure on the next page.

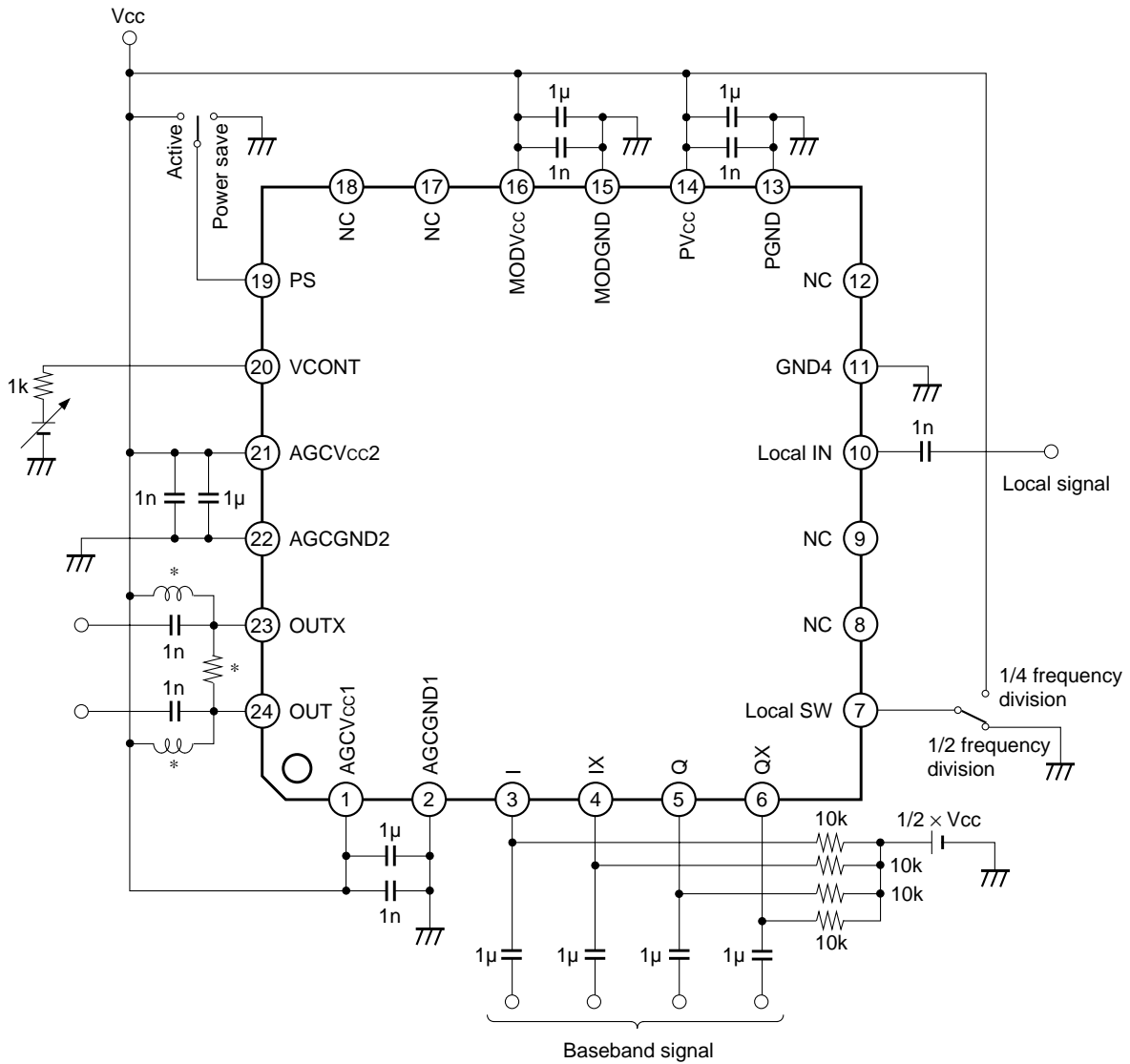


Electrical Characteristics Measurement Circuit



*1 Murata, Inc. LQN21A22NJ (K) 04
 *2 TOKO, Inc. B5FL 616DS-1135

Application Circuit



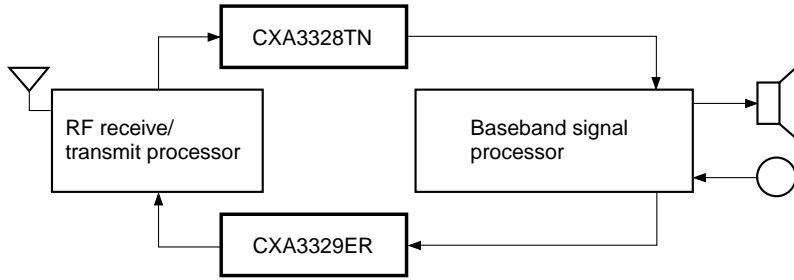
* Adjust these values so that the impedance matching with this IC is optimum.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

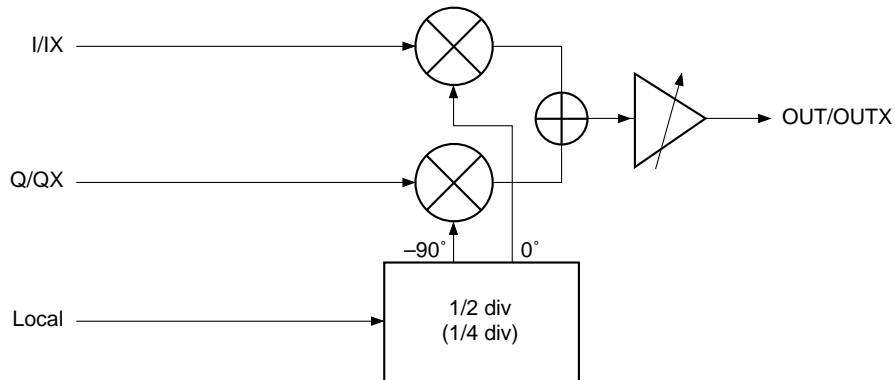
1. Outline of operation

This IC performs the signal processing between the analog transmit baseband processor block and the analog transmit RF processor block of the cellular phone. The figure below shows the general circuit block diagram for the portable cellular phones using this IC. The input for this IC is connected to the baseband signal processor block; the output is connected to the analog RF processor block.



2. IC Internal Signal Flow

Two baseband-processed signals I, Q and the local signal are input to this IC as shown in the figure below. The local signal is 1/2-frequency divided, and that signal becomes the quadrature I/Q local signal. The baseband I/Q signals are input to the quadrature modulator, and baseband processing to IF upconversion is performed with the quadrature local signals. The signal is input to the gain control amplifier, and output after the gain controlled to the necessary level.



Notes on Operation

1. Baseband signal I/Q input

Pins 3 to 6, where the baseband signal is input, do not have a determined voltage internally on the IC. Therefore, a bias voltage equivalent to $1/2V_{cc}$ should be applied externally.

2. IF signal output

The IF signal outputs, OUT/OUTX, are differential outputs. The output impedance should be $1k\Omega$ including the external resistance with differential. Also, it is necessary to connect the inductor to eliminate the parasitic capacitance in the IC.

3. Notes on power supplies

The CXA3329ER is designed to operate by a 2.85V stabilized power supply to allow use with the battery driven portable phones. Using the multiple voltage regulators throughout the phone is recommended to minimize the power supply noise in the CXA3329ER power supply unit. The recommended power supply range for the CXA3329ER is from 2.7V to 3.3V. Decouple the power supplies around the CXA3329ER using $1\mu F$ capacitor for each V_{cc} pin. Locate this capacitor as close to the pins as possible to minimize the series inductance. Using an additional 1nF decoupling capacitor in parallel to the $1\mu F$ capacitor is recommended to further reduce the high frequency noise in the power supply input to the CXA3329ER.

Design Materials (Design Guarantee)

Electrical Characteristics

(V_{CC} = 2.7 to 3.8V, T_a = -25 to +85°C)

Item	Symbol	Conditions	Measurement point	Min.	Typ.	Max.	Unit
DC Characteristics							
Current consumption 1	I _{max}	V _{CONT} = 2.85V	A		24		mA
Current consumption 2	I _{min}	V _{CONT} = 0V	A		17		
Power saving current	I _{ps}	PS = low (in power saving mode)	A	—	—	5	μA
AC Characteristics							
Output IP3	OIP3	Note1 (See page 6.)	B	8.5	—	—	dBm
Output power 1	P _{O1}	V _{CONT} = 2.3V, differential output, f = 380MHz	B	-19	-15	-11	dBm
Output power 2	P _{O2}	V _{CONT} = 0.3V, differential output, f = 380MHz	B	-83	-77	-73	
Gain control range	G _{cr}	V _{CONT} = 0.3 to 2.3V, f = 380MHz	B	54	62	70	dB
Gain accuracy	G _{ct}	Difference between the output powers where T _a = -25°C, 85°C and T _a = 27°C	B	-2	0	2	dB
Gain flatness	G _{flat}	IF ± 2.5MHz	B	-0.25	0	0.25	dB
Output noise power 1	No ₁	P _o = -25dB, I/Q inputs are no signal.	B	—	—	-147	dBm/ Hz
Output noise power 2	No ₂	P _o = -65dBm, I/Q inputs are no signal.	B	—	—	-162	
I, Q residual sideband product	I _{mg}	Suppression ratio of desired signal (f = 380 + 1) MHz and image signal (f = 380 - 1) MHz	B	—	—	-25	dBc
Carrier leak	CL	Ratio of desired signal (f = 380 + 1) MHz and local leak (f = 380) MHz	B	—	—	-18	
Input I/Q phase error	I _{QPE}	Input signal I/Q phase difference -90° when the output signal I/Q phase difference is 90°.	B	-3	0	3	deg
Input I/Q gain error	I _{QGE}	I/Q input signal level difference when output signal I/Q levels are the same.	B	-2.5	0	2.5	dB
Error vector magnitude	EVM		B	—	—	3	%
Response time	T _r	Until output rise of 90% after the power is turned ON.	B	—	—	10	μs

- Unless otherwise specified, the I/Q baseband input signals and local input signal use the conditions shown in the Electrical Characteristics Measurement Circuit and the control voltage and power saving pins are set to V_{CONT} = 2.3V, PS = high.
The local switching pin is left open (1/2 frequency division).
- IF output impedance is 1kΩ.
- Values measured with a Sony evaluation board.

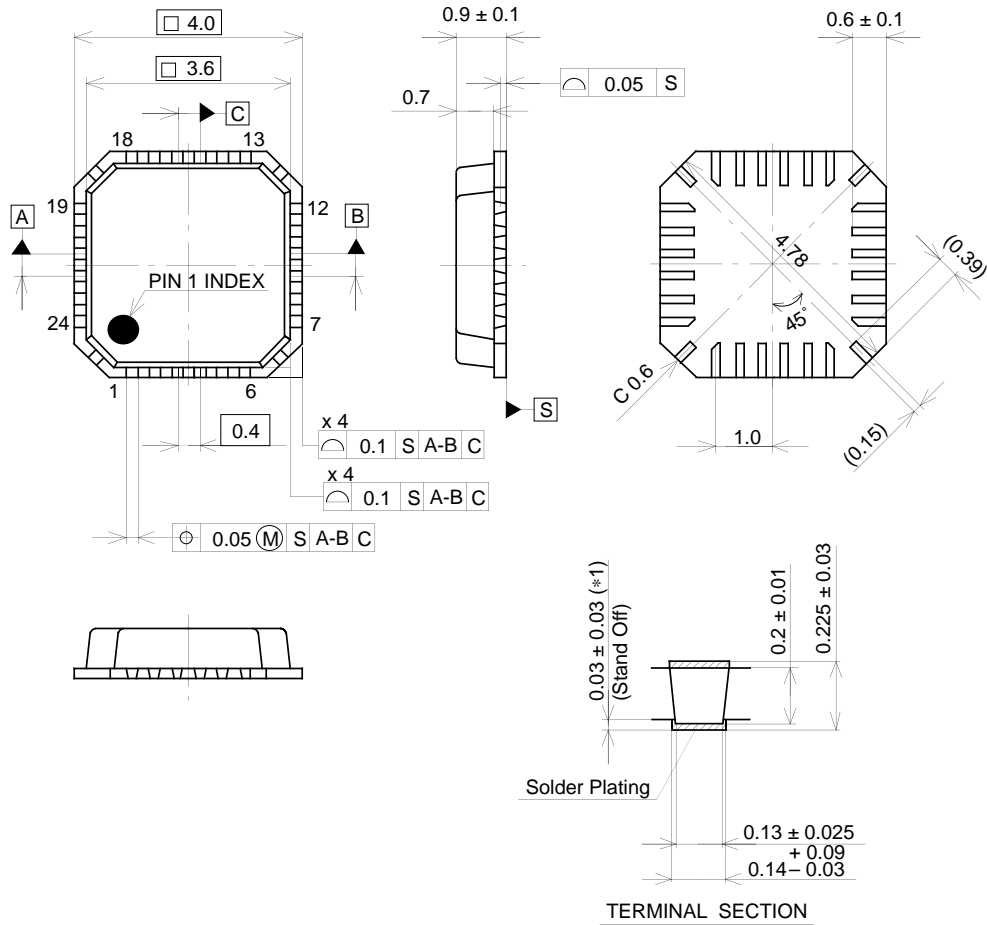
Design Materials (Design Guarantee)

Item	Symbol	Conditions	Measurement point	Min.	Typ.	Max.	Unit
Input Impedance							
I/Q input resistance	R _{IQ}	Single	3, 4, 5, 6	60	85	—	kΩ
I/Q input capacitance	C _{IQ}	Single	3, 4, 5, 6	—	—	10	pF
VCONT pin input resistance	R _{vc}		20	10	—	—	kΩ
Local IN input resistance	R _L		10	37.5	50	62.5	Ω

Package Outline

Unit: mm

24PIN VQFN(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	VQFN-24P-03
EIAJ CODE	_____
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g