SONY

Audio Driver for TV

CXA3785R

Description

The CXA3785R is an integrated audio sub-system designed for TV audio application. It has a stereo headphone amplifier, and 4 stereo amplifiers. It also integrated gain control, mute control, input selector, and voltage detectors. Each settable value is controlled through I^2C compatible interface.

Features

- ◆ 4 stereo audio amplifiers (HP, AMP1, AMP2, AMP3) with programmable gain control
- ◆ Cap less headphone amplifier
- ◆ 2 amplifiers (HP and AMP1) with 3rd order LPF for PWM input
- ◆ AMP3 with 2 stereo input multiplexer and LL/RR output
- ◆ AMP4 for Digital Media Port (DMP) with differential input
- ◆ 4 voltage detection circuits for VUNREG (un-regulated power supply voltage), REGAUD (audio amp power supply voltage), REG33 (DSP power supply voltage) and speaker output
- ◆ 3 muting circuits with external mute control and buffer transistor
- ◆ REGAUD output for supply voltage of 4 stereo audio amplifiers and DMP
- ◆ REG33 output for supply voltage of DSP and PWM output stage
- ◆ I^2C control
- ◆ Package size: 64pin LQFP (Body size: 10mm × 10mm)

E08906

Absolute Maximum Ratings

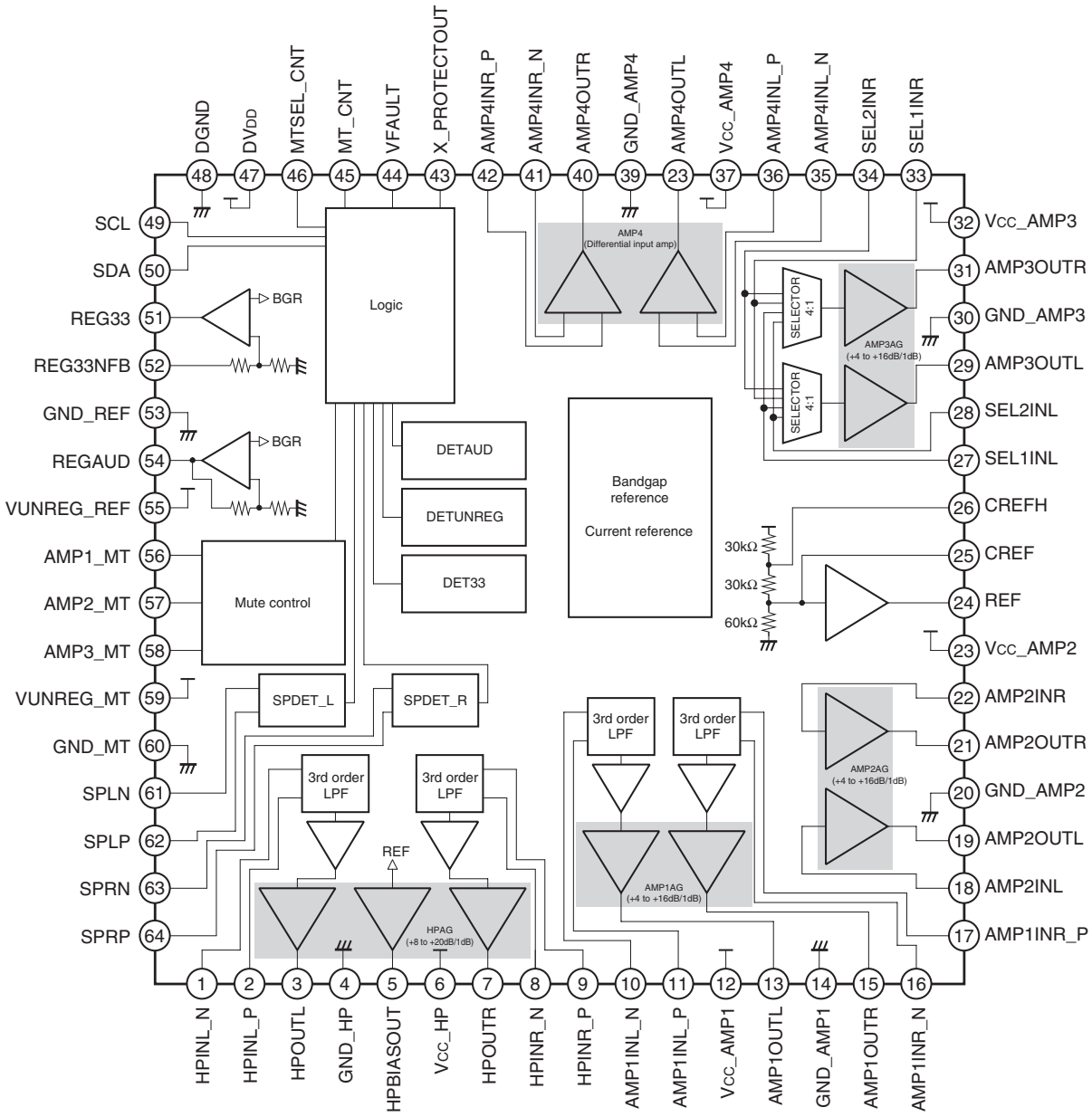
Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	24.0	V
	V_{UNREG}	24.0	V
	DV_{DD}	4.5	V
Operating temperature range	T_A	–25 to +85	˚C
Storage temperature range	Tstg	–55 to +125	˚C
Junction temperature	T_J(max)	+125	˚C
Power dissipation	P_D	(T_J(max) – T_A) / θJA*1	—
Thermal impedance	θJA	80	˚C/W
	θJC	20	˚C/W

*1 Glass fabric base epoxy two-layer board, 76mm × 114mm, t = 1.6mm

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Condition	Unit
Supply voltage	V_{CC}	8.0	12.0	13.0	V_{CC} = REGAUD	V
	V_{UNREG}	11.5	15.0	18.0	VUNREG – REGAUD ≥ 2.5V	V
	DV_{DD}	3.0	3.3	3.6		V
Operating ambient temperature	Topt	–25	—	+85		˚C

Block Diagram

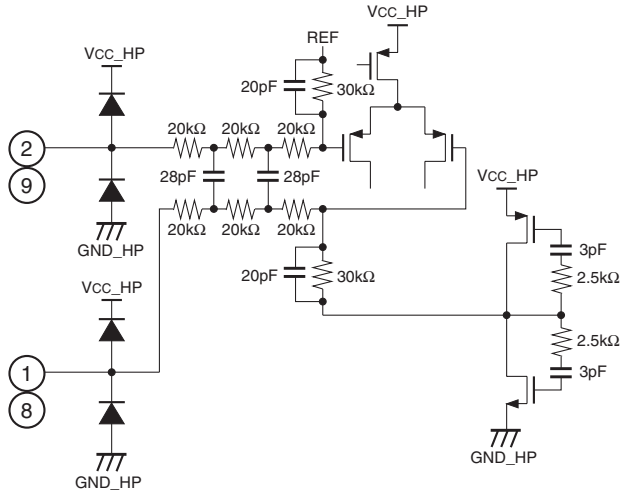
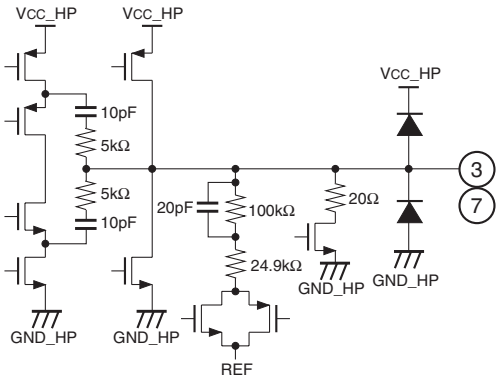
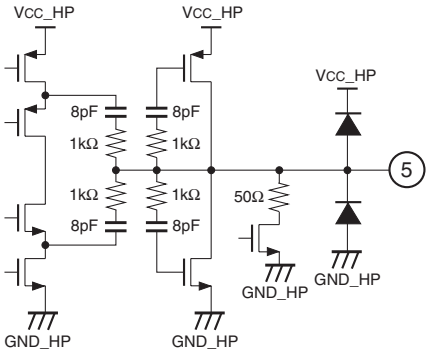


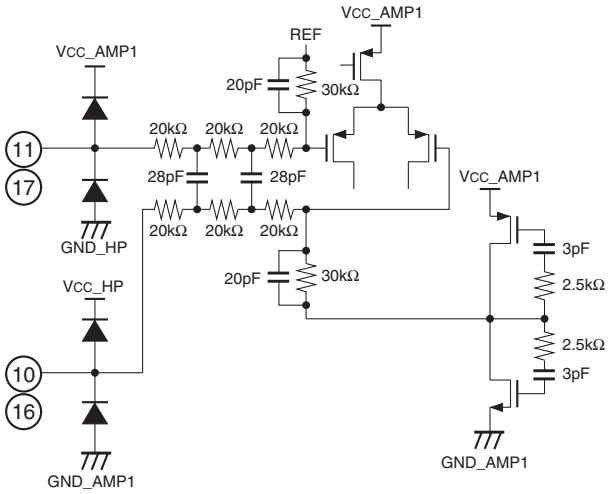
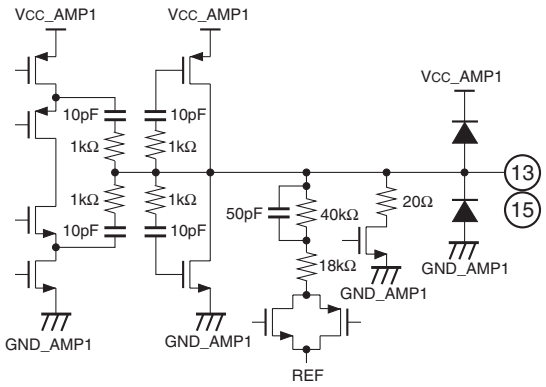
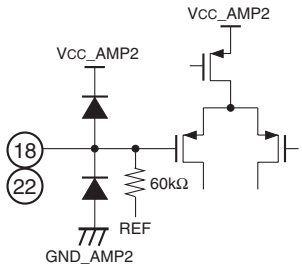
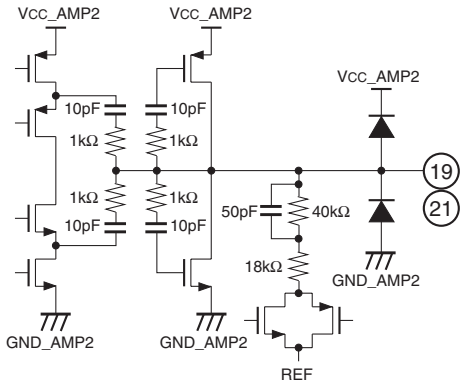
Pin Description

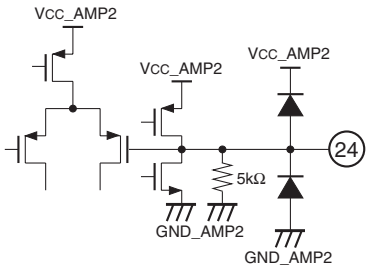
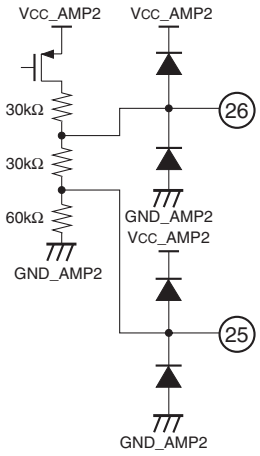
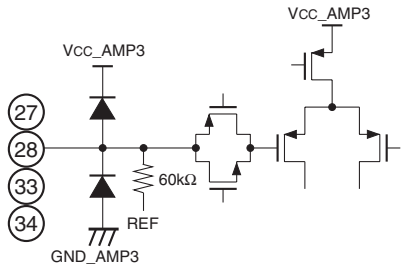
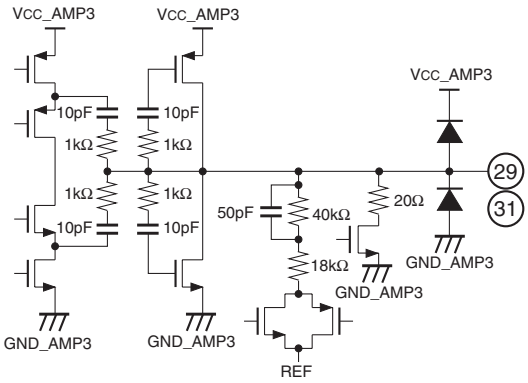
Pin No.	Pin name	Direction	Description
1	HPINL_N	I	Headphone amp Lch negative input
2	HPINL_P	I	Headphone amp Lch positive input
3	HPOUTL	O	Headphone amp Lch output
4	GND_HP	—	Headphone amp GND
5	HPBIASOUT	O	Headphone amp bias output
6	Vcc_HP	—	Headphone amp power
7	HPOUTR	O	Headphone amp Rch output
8	HPINR_N	I	Headphone amp Rch negative input
9	HPINR_P	I	Headphone amp Rch positive input
10	AMP1INL_N	I	AMP1 Lch negative input
11	AMP1INL_P	I	AMP1 Lch positive input
12	Vcc_AMP1	—	AMP1 power
13	AMP1OUTL	O	AMP1 Lch output
14	GND_AMP1	—	AMP1 GND
15	AMP1OUTR	O	AMP1 Rch output
16	AMP1INR_N	I	AMP1 Rch negative input
17	AMP1INR_P	I	AMP1 Rch positive input
18	AMP2INL	I	AMP2 Lch input
19	AMP2OUTL	O	AMP2 Lch output
20	GND_AMP2	—	AMP2 GND
21	AMP2OUTR	O	AMP2 Rch output
22	AMP2INR	I	AMP2 Rch input
23	Vcc_AMP2	—	AMP2 power
24	REF	O	All Amp reference
25	CREF	O	Reference capacitor
26	CREFH	O	“H” reference capacitor
27	SEL1INL	I	AMP3 Lch selector input 1
28	SEL2INL	I	AMP3 Lch selector input 2
29	AMP3OUTL	O	AMP3 Lch output
30	GND_AMP3	—	AMP3 GND
31	AMP3OUTR	O	AMP3 Rch output
32	Vcc_AMP3	—	AMP3 power
33	SEL1INR	I	AMP3 Rch selector input 1
34	SEL2INR	I	AMP3 Rch selector input 2
35	AMP4INL_N	I	AMP4 Lch negative input
36	AMP4INL_P	I	AMP4 Lch positive input
37	Vcc_AMP4	—	AMP4 power

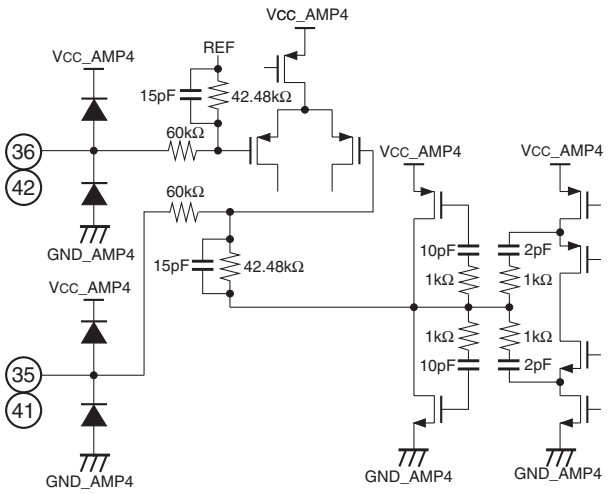
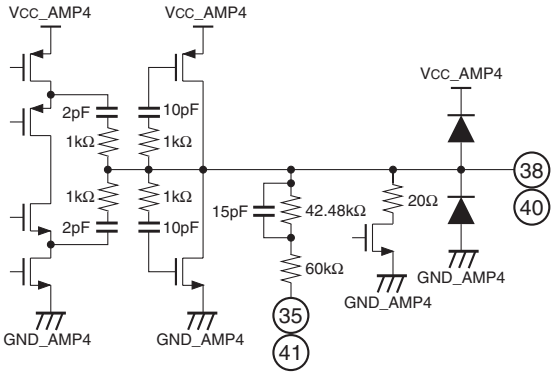
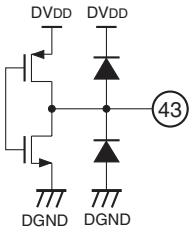
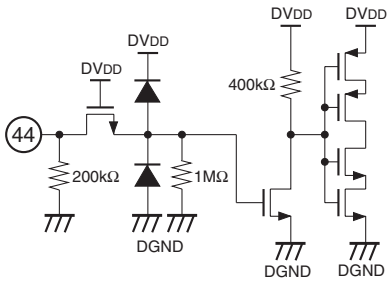
Pin No.	Pin name	Direction	Description
38	AMP4OUTL	O	AMP4 Lch output
39	GND_AMP4	—	AMP4 GND
40	AMP4OUTR	O	AMP4 Rch output
41	AMP4INR_N	I	AMP4 Rch negative input
42	AMP4INR_P	I	AMP4 Rch positive input
43	X_PROTECTOUT	O	Protect signal output
44	VFAULT	I	Fault signal input
45	MT_CNT	I	All amp mute control signal input
46	MTSEL_CNT	I	Selected amp mute control signal input
47	DV_{DD}	—	Logic power
48	DGND	—	Logic GND
49	SCL	I	I^2C clock
50	SDA	I/O	I^2C data
51	REG33	O	REG33 external FET control signal output
52	REG33NFB	O	REG33 negative feedback output
53	GND_REF	—	Reg/reference GND
54	REGAUD	O	Regulator output for audio amp
55	VUNREG_REF	—	Un-regulated power for reg/reference
56	AMP1_MT	O	AMP1 mute control signal output
57	AMP2_MT	O	AMP2 mute control signal output
58	AMP3_MT	O	AMP3 mute control signal output
59	VUNREG_MT	—	Un-regulated power for mute circuit
60	GND_MT	—	Mute circuit GND
61	SPLN	I	Speaker Lch negative input
62	SPLP	I	Speaker Lch positive input
63	SPRN	I	Speaker Rch negative input
64	SPRP	I	Speaker Rch positive input

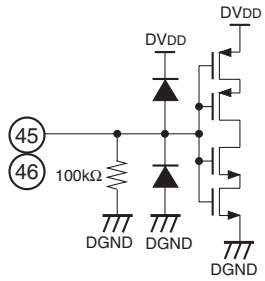
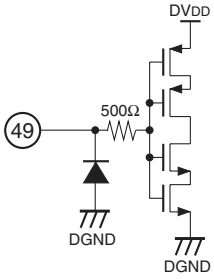
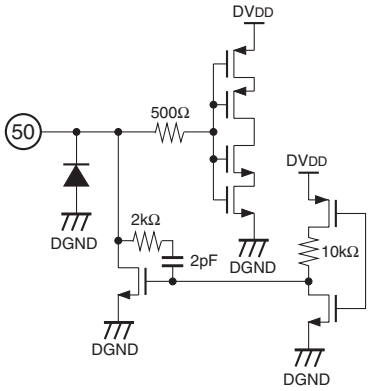
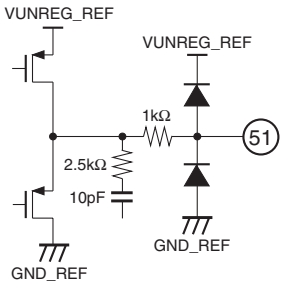
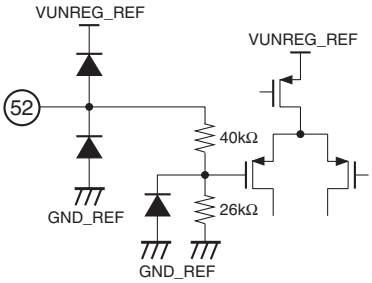
Pin Circuit

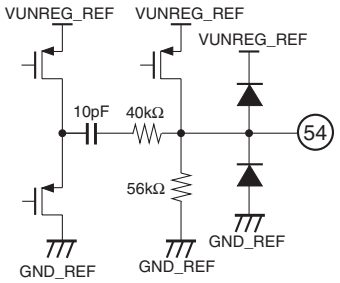
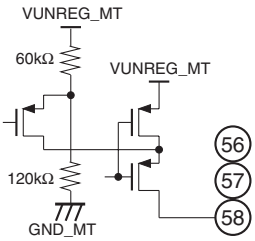
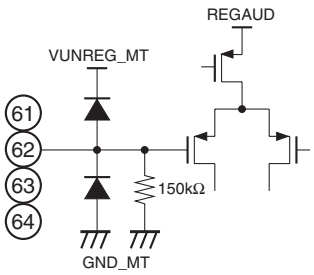
Pin	Symbol	Equivalent circuit
1 2 8 9	HPINL_N HPINL_P HPINR_N HPINR_P	
3 7	HPOUTL HPOUTR	
5	HPBIASOUT	

Pin	Symbol	Equivalent circuit
10 11 16 17	AMP1INL_N AMP1INL_P AMP1INR_N AMP1INR_P	
13 15	AMP1OUTL AMP1OUTR	
18 22	AMP2INL AMP2INR	
19 21	AMP2OUTL AMP2OUTR	

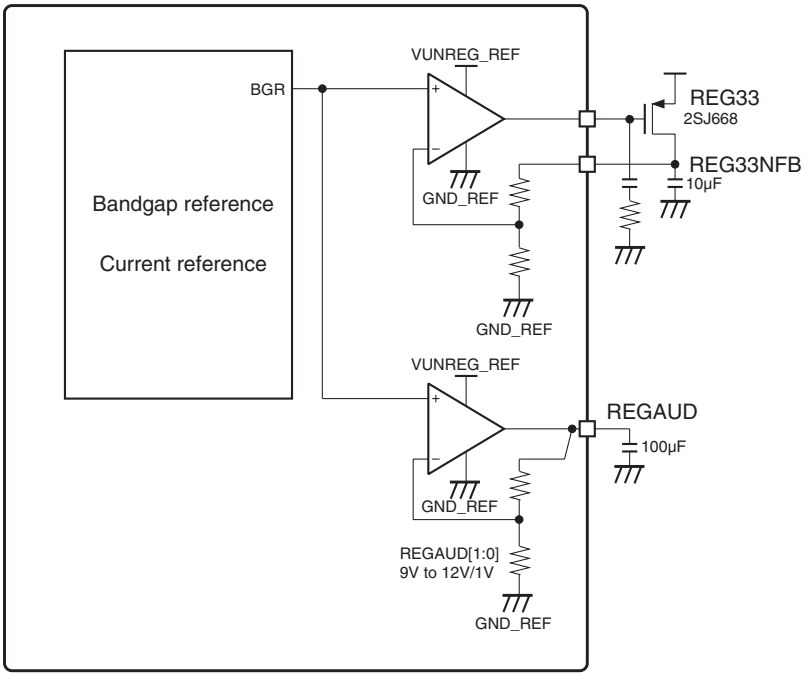
Pin	Symbol	Equivalent circuit
24	REF	
25 26	CREF CREFH	
27 28 33 34	SEL1INL SEL2INL SEL1INR SEL2INR	
29 31	AMP3OUTL AMP3OUTR	

Pin	Symbol	Equivalent circuit
35 36 41 42	AMP4INL_N AMP4INL_P AMP4INR_N AMP4INR_P	
38 40	AMP4OUTL AMP4OUTR	
43	X_PROTECTOUT	
44	VFAULT	

Pin	Symbol	Equivalent circuit
45 46	MT_CNT MTSEL_CNT	
49	SCL	
50	SDA	
51	REG33	
52	REG33NFB	

Pin	Symbol	Equivalent circuit
54	REGAUD	
56 57 58	AMP1_MT AMP2_MT AMP3_MT	
61 62 63 64	SPLN SPLP SPRN SPRP	

Block Diagram (Regulator, Reference)



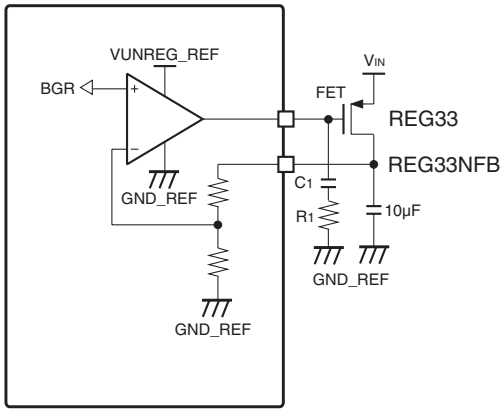
Electrical Spec. (HP Amp)

Electrical Characteristics (Regulator, Reference)

(Unless otherwise specified; Ta = 25°C, V_{CC} = REGAUD = 12.0V, V_{UNREG} = 15.0V, DV_{DD} = 3.3V, fsignal = 1kHz, measurement band width = 20 to 20kHz)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
REG33NFB output voltage	$V_{REG33NFB}$	I_{LOAD} = 1mA	3.0	3.3	3.6	V
REG33 output voltage swing	$V_{REG33SW1}$	I_{LOAD} = 1mA, REG33NFB = REG33NFB (I_{LOAD} = 1mA) + 25mV	V_{UNREG} – 2.0	V_{UNREG} – 1.0	—	V
	$V_{REG33SW2}$	I_{LOAD} = 1mA, REG33NFB = REG33NFB (I_{LOAD} = 1mA) – 25mV	—	3.0	6.0	V
REG33 sourcing current	$I_{REG33SOURCE}$	I_{LOAD} = 1mA, REG33 = 10V, REG33NFB = REG33NFB (I_{LOAD} = 1mA) + 25mV	10	20	40	μA
REG33 sinking current	$I_{REG33SINK}$	I_{LOAD} = 1mA, REG33 = 10V REG33NFB = REG33NFB (I_{LOAD} = 1mA) – 25mV	1.5	3.0	6.0	mA
REGAUD output voltage 1	V_{AUD1}	I_{LOAD} = 100mA, V_{CC} = REGAUD = 12V	11.0	12.0	13.0	V
REGAUD output voltage 2	V_{AUD2}	I_{LOAD} = 100mA, V_{CC} = REGAUD = 11V	10.0	11.0	12.0	V
REGAUD output voltage 3	V_{AUD3}	I_{LOAD} = 100mA, V_{CC} = REGAUD = 10V	9.0	10.0	11.0	V
REGAUD output voltage 4	V_{AUD4}	I_{LOAD} = 100mA, V_{CC} = REGAUD = 9V	8.0	9.0	10.0	V
REGAUD load regulation	V_{LO_AUD}	I_{LOAD} = 1m – 100mA, V_{CC} = REGAUD = 12V	—	—	0.3	V
REGAUD line regulation	V_{LI_AUD}	VUNREG = 14.5 – 18V, I_{LOAD} = 100mA V_{CC} = REGAUD = 12V	—	—	0.3	V
REGAUD PSRR	$PSRR_{AUD}$	I_{LOAD} = 100mA	40	60	—	dB
CREF output voltage	V_{CREF}		(V_{CC}/2) × 0.9	V_{CC}/2	(V_{CC}/2) × 1.1	V
CREFH output voltage	V_{CREFH}		(3 × V_{CC}/4) × 0.9	3 × V_{CC}/4	(3 × V_{CC}/4) × 1.1	V
REF output voltage	V_{REF}		(V_{CC}/2) × 0.9	V_{CC}/2	(V_{CC}/2) × 1.1	V

Design Procedure (REG33)



Regulator Compensation

The compensation network (C_1, R_1) is customizable and depends on load and MOSFET characteristics:

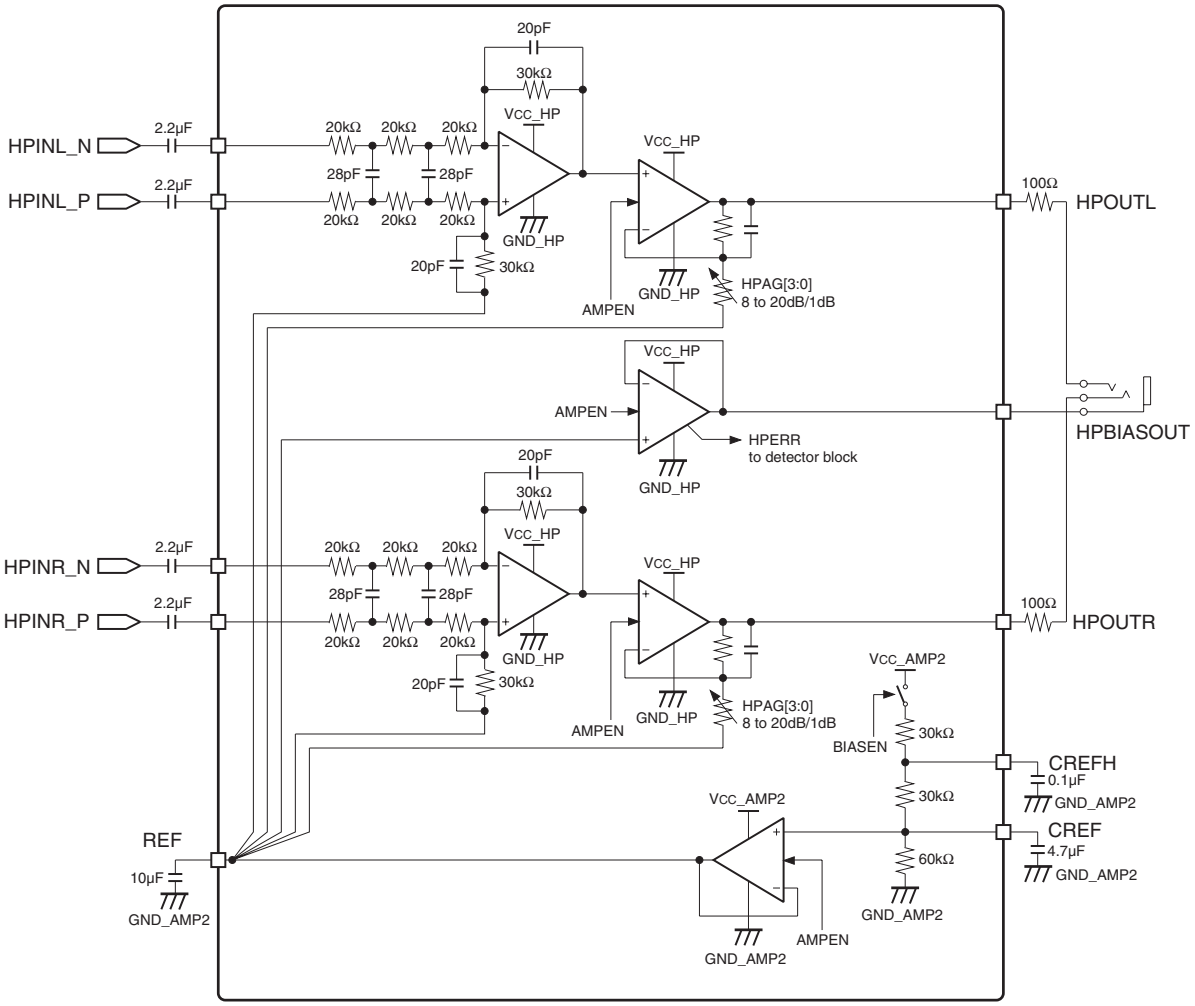
- Strength of the external p-channel MOSFET (gm), it's forward transconductance (gfs), and the gate-to-source capacitance (Cgs).
- The driver transconductance (gmdrv) of the integrated circuit driver.
- Load current range (including the minimum load): Imin to Imax

External MOSFET Selection

The selected MOSFET must have a gate threshold voltage (at the required max load) that meets the following criteria:

$$Vgs\_min < V_{IN} - V_{REG33SW2}$$

Block Diagram (HP Amp)



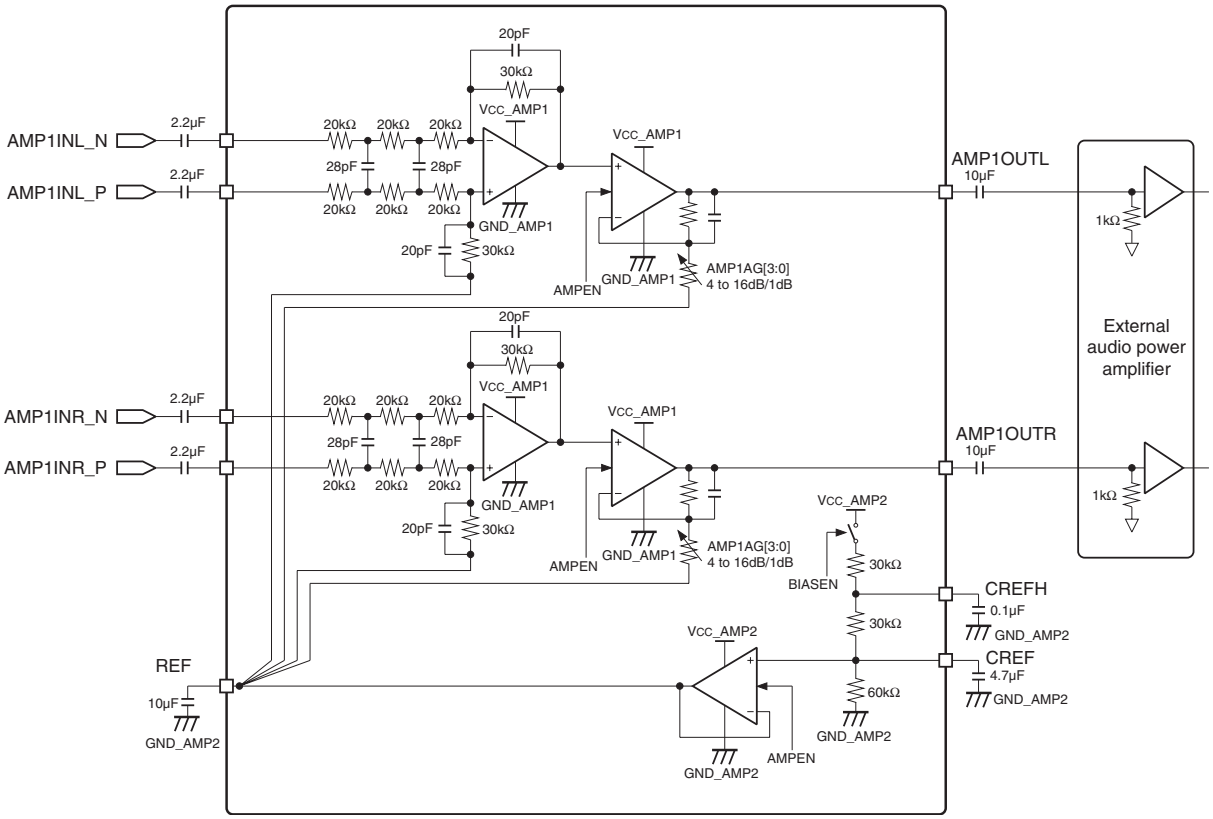
Electrical Spec. (HP Amp)

Electrical Characteristics (HP Block)

(Unless otherwise specified; Ta = 25°C, V_{CC} = REGAUD = 12.0V, V_{UNREG} = 15.0V, DV_{DD} = 3.3V, fsignal = 1kHz, measurement band width = 20 to 20kHz)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input impedance	RIN_{HP}		48.0	60.0	72.0	kΩ
Output DC voltage (HPOUT, HPBIASOUT)	$VOUT_{HP}$	Gain = 14dB, AC coupled input	(V_{CC}/2) × 0.9	V_{CC}/2	(V_{CC}/2) × 1.1	V
Gain adjustment range	$GAIN_{HP}$	fsig = 1kHz	8.0	—	20.0	dB
Gain adjustment step	STP_{HP}		0	1.0	2.0	dB
LPF cutoff frequency	LPF_{HP}	VO = 55kHz/1kHz	–5.5	–3.0	–0.5	dB
Maximum output level	VOM_{HP_1}	Gain = 14dB, THD = 1.0%, RL = 100Ω + 32Ω, V_{CC} = REGAUD = 12.0V	2.8	—	—	Vrms
	VOM_{HP_2}	Gain = 14dB, THD = 1.0%, RL = 100Ω + 32Ω, V_{CC} = REGAUD = 9.0V	2.1	—	—	
THD+N	THD_{HP}	Gain = 14dB, LPF RL = 100Ω + 32Ω, VIN = 0.1Vrms	—	0.10	0.50	%
Output noise level	VN_{HP}	Gain = 14dB, RL = 100Ω + 32Ω, Measured at RL of 32Ω	—	–92.0	–82.0	dBV
Gain error	GE_{HP}	Gain = 14dB, RL = 1kΩ	–1.0	0	1.0	dB
Channel separation	CT_{HP}	Gain = 14dB, VIN = 0.4Vrms	70.0	80.0	—	dB
Mute level	MT_{HP}	Gain = 14dB, Output level = 2.8Vrms	—	–90.0	–80.0	dB
PSRR	$PSRR_{HP}$	fsig = 1kHz	30.0	40.0	—	dB

Block Diagram (AMP1 Amp)



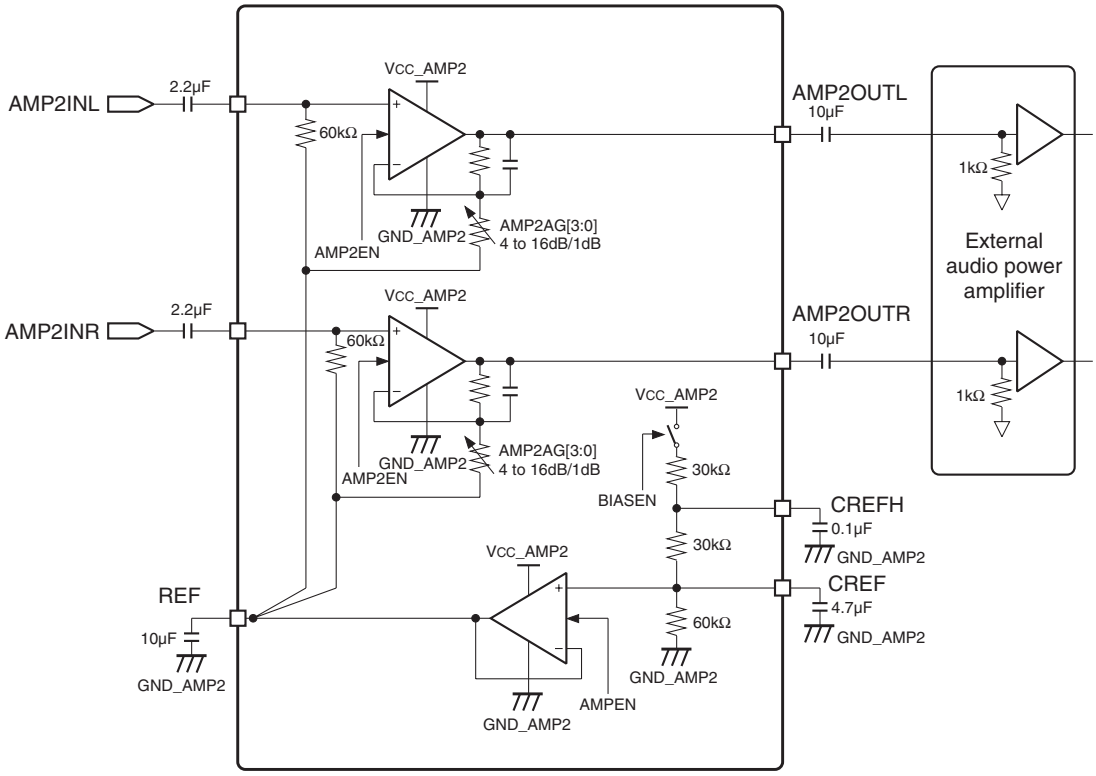
Electrical Spec. (AMP1 Amp)

Electrical Characteristics (AMP1 Block)

(Unless otherwise specified; Ta = 25°C, V_{CC} = REGAUD = 12.0V, V_{UNREG} = 15.0V, DV_{DD} = 3.3V, fsignal = 1kHz, measurement band width = 20 to 20kHz)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input impedance	RIN_{AMP1}		48.0	60.0	72.0	kΩ
Output DC voltage	$VOUT_{AMP1}$	Gain = 10dB, AC coupled input	(V_{CC}/2) × 0.9	V_{CC}/2	(V_{CC}/2) × 1.1	V
Gain adjustment range	$GAIN_{AMP1}$	fsig = 1kHz	4.0	—	16.0	dB
Gain adjustment step	STP_{AMP1}		0	1.0	2.0	dB
LPF cutoff frequency	LPF_{AMP1}	VO = 55kHz/1kHz	–5.5	–3.0	–0.5	dB
Maximum output level	VOM_{AMP1_1}	Gain = 10dB, THD = 1.0%, RL = 1kΩ V_{CC} = REGAUD = 12.0V	2.8	—	—	Vrms
	VOM_{AMP1_2}	Gain = 10dB, THD = 1.0%, RL = 1kΩ V_{CC} = REGAUD = 9.0V	2.1	—	—	
THD+N	THD_{AMP1}	Gain = 10dB, RL = 1kΩ, VIN = 0.2Vrms	—	0.01	0.10	%
Output noise level	VN_{AMP1}	Gain = 10dB, RL = 1kΩ	—	–90.0	–80.0	dBV
Gain error	GE_{AMP1}	Gain = 10dB, RL = 1kΩ	–1.0	0	1.0	dB
Channel separation	CT_{AMP1}	Gain = 10dB, VIN = 1.0Vrms	70.0	80.0	—	dB
PSRR	$PSRR_{AMP1}$	fsig = 1kHz	30.0	40.0	—	dB

Block Diagram (AMP2 Amp)



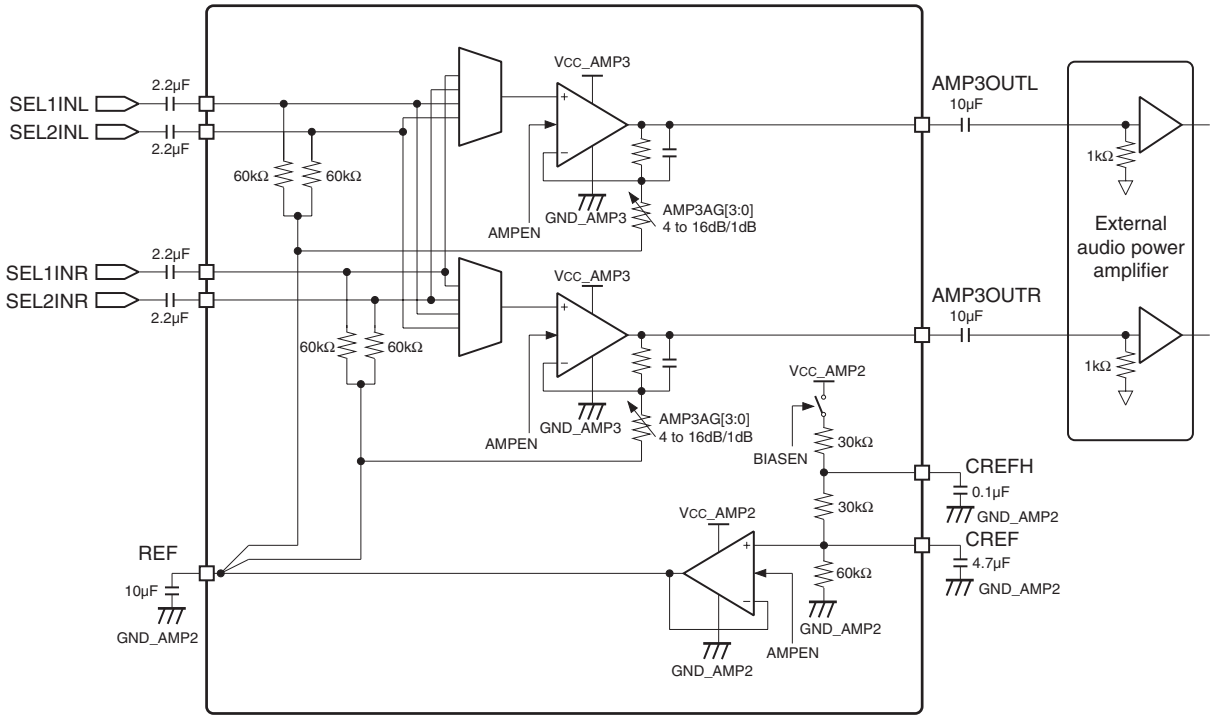
Electrical Spec. (AMP2 Amp)

Electrical Characteristics (AMP2 Block)

(Unless otherwise specified; Ta = 25°C, V_{CC} = REGAUD = 12.0V, V_{UNREG} = 15.0V, DV_{DD} = 3.3V, fsignal = 1kHz, measurement band width = 20 to 20kHz)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input impedance	RIN_{AMP2}		48.0	60.0	72.0	kΩ
Output DC voltage	$VOUT_{AMP2}$	Gain = 10dB, AC coupled input	(V_{CC}/2) × 0.9	V_{CC}/2	(V_{CC}/2) × 1.1	V
Gain adjustment range	$GAIN_{AMP2}$	fsig = 1kHz	4.0	—	16.0	dB
Gain adjustment step	STP_{AMP2}		0	1.0	2.0	dB
Maximum output level	VOM_{AMP2_1}	Gain = 10dB, THD = 1.0%, RL = 1kΩ V_{CC} = REGAUD = 12.0V	2.8	—	—	Vrms
	VOM_{AMP2_2}	Gain = 10dB, THD = 1.0%, RL = 1kΩ V_{CC} = REGAUD = 9.0V	2.1	—	—	
THD+N	THD_{AMP2}	Gain = 10dB, RL = 1kΩ, VIN = 0.2Vrms	—	0.01	0.10	%
Output noise level	VN_{AMP2}	Gain = 10dB, RL = 1kΩ	—	–95.0	–85.0	dBV
Gain error	GE_{AMP2}	Gain = 10dB, RL = 1kΩ	–1.0	0	1.0	dB
Channel separation	CT_{AMP2}	Gain = 10dB, VIN = 1.0Vrms	70.0	80.0	—	dB
PSRR	$PSRR_{AMP2}$	fsig = 1kHz	30.0	40.0	—	dB

Block Diagram (AMP3 Amp)



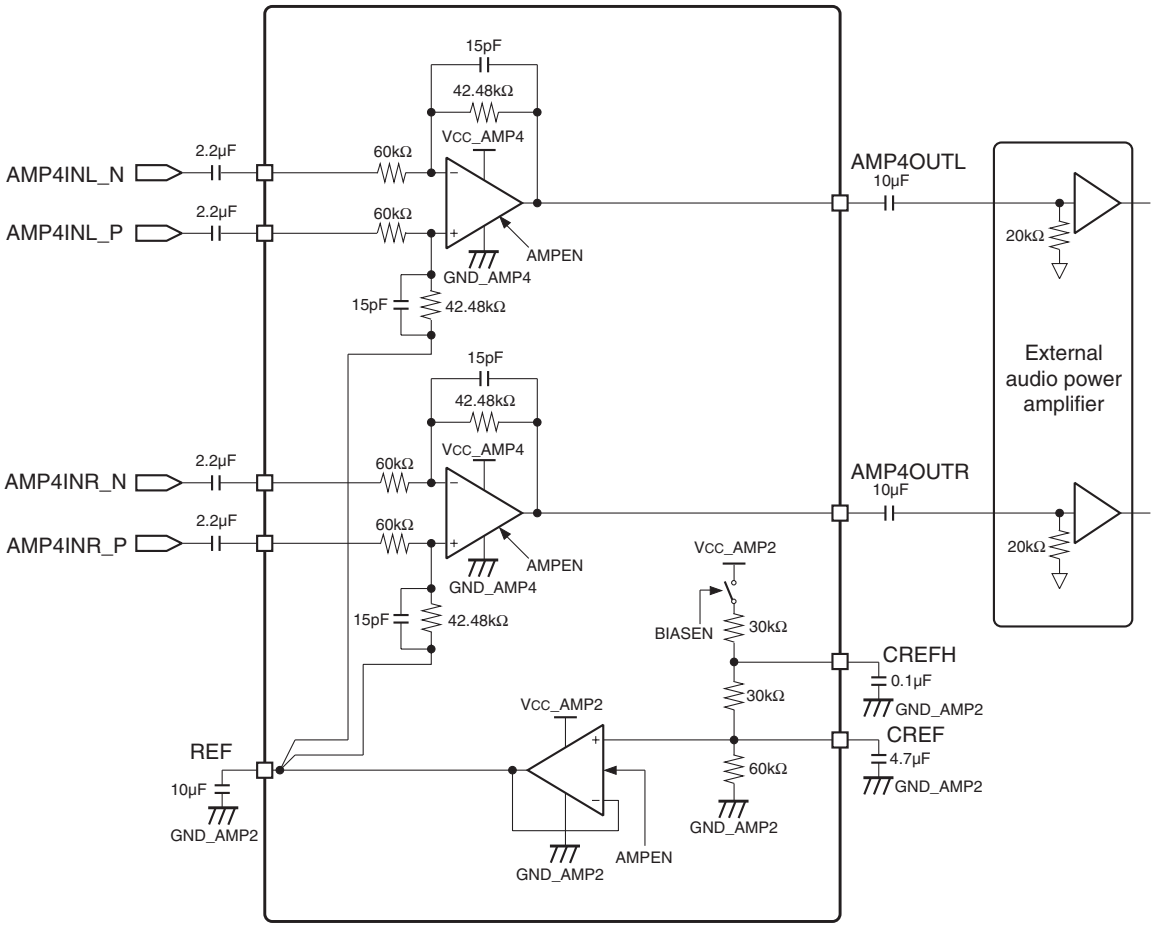
Electrical Spec. (AMP3 Amp)

Electrical Characteristics (AMP3 Block)

(Unless otherwise specified; Ta = 25°C, V_{CC} = REGAUD = 12.0V, V_{UNREG} = 15.0V, DV_{DD} = 3.3V, fsignal = 1kHz, measurement band width = 20 to 20kHz)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input impedance	RIN_{AMP3}		48.0	60.0	72.0	kΩ
Output DC voltage	$VOUT_{AMP3}$	Gain = 10dB, AC coupled input	(V_{CC}/2) × 0.9	V_{CC}/2	(V_{CC}/2) × 1.1	V
Gain adjustment range	$GAIN_{AMP3}$	fsig = 1kHz	4.0	—	16.0	dB
Gain adjustment step	STP_{AMP3}		0	1.0	2.0	dB
Maximum output level	VOM_{AMP3_1}	Gain = 10dB, THD = 1.0%, RL = 1kΩ V_{CC} = REGAUD = 12.0V	2.8	—	—	Vrms
	VOM_{AMP3_2}	Gain = 10dB, THD = 1.0%, RL = 1kΩ V_{CC} = REGAUD = 9.0V	2.1	—	—	
THD+N	THD_{AMP3}	Gain = 10dB, RL = 1kΩ, VIN = 0.2Vrms	—	0.01	0.10	%
Output noise level	VN_{AMP3}	Gain = 10dB, RL = 1kΩ	—	–95.0	–85.0	dBV
Gain error	GE_{AMP3}	Gain = 10dB, RL = 1kΩ	–1.0	0	1.0	dB
Channel separation	CT_{AMP3}	Gain = 10dB, VIN = 1.0Vrms	70.0	80.0	—	dB
PSRR	$PSRR_{AMP3}$	fsig = 1kHz	30.0	40.0	—	dB

Block Diagram (AMP4 Amp)



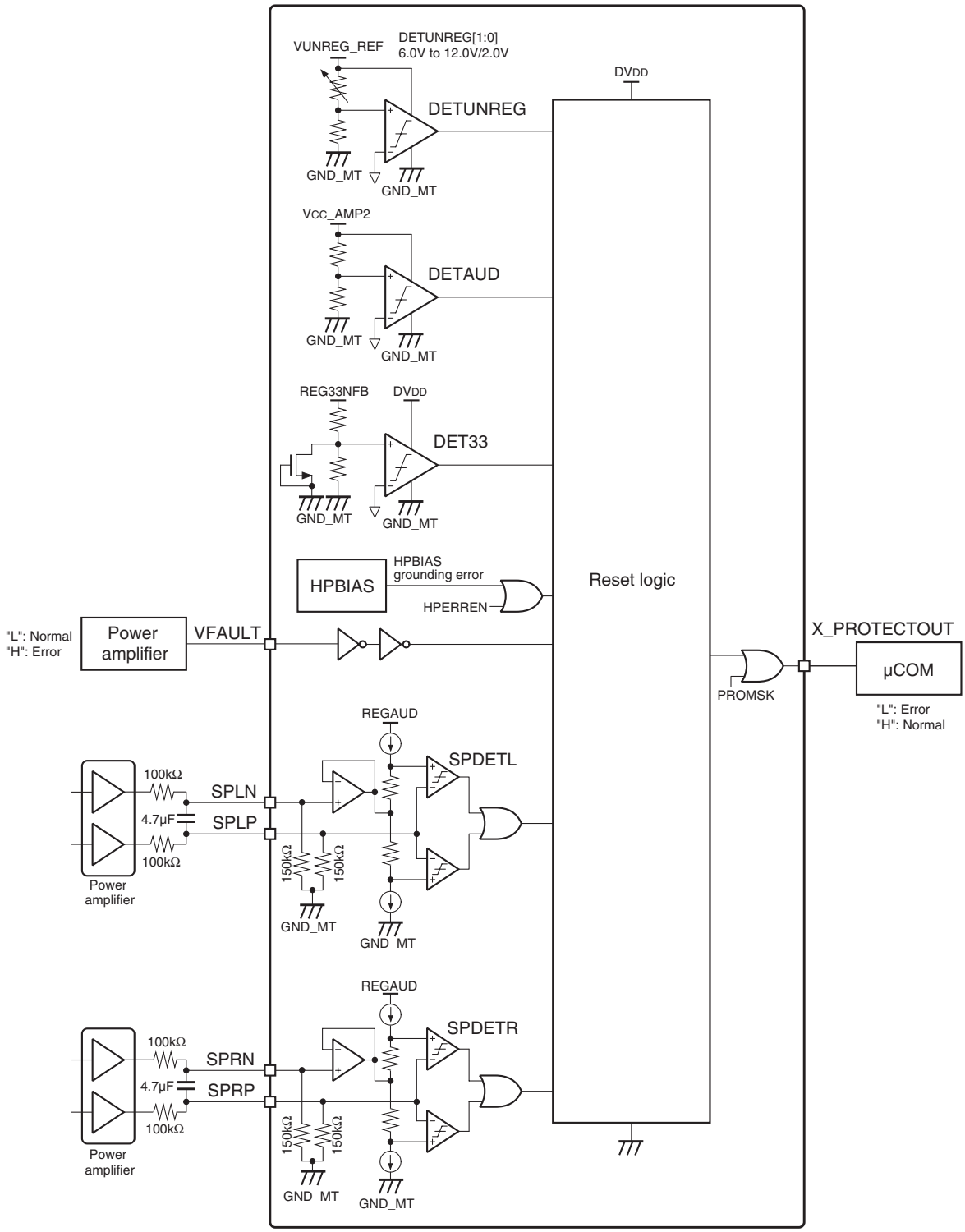
Electrical Spec. (AMP4 Amp)

Electrical Characteristics (AMP4 Block)

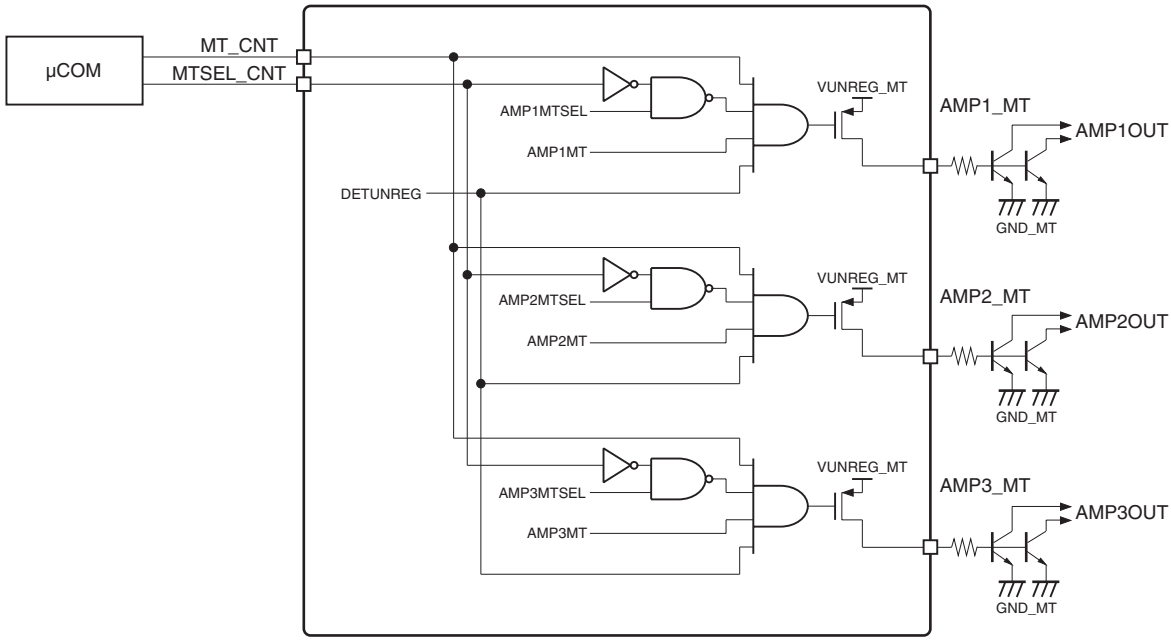
(Unless otherwise specified; Ta = 25°C, V_{CC} = REGAUD = 12.0V, V_{UNREG} = 15.0V, DV_{DD} = 3.3V, fsignal = 1kHz, measurement band width = 20 to 20kHz)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input impedance	RIN_{AMP4}		48.0	60.0	72.0	kΩ
Output DC voltage	$VOUT_{AMP4}$	AC coupled input	(V_{CC}/2) × 0.9	V_{CC}/2	(V_{CC}/2) × 1.1	V
Gain	$GAIN_{AMP4}$	Single Input, fsig = 1kHz	–4.0	–3.0	–2.0	dB
Maximum output level	VOM_{AMP4_1}	Gain = 10dB, THD = 1.0%, RL = 1kΩ V_{CC} = REGAUD = 12.0V	2.8	—	—	Vrms
	VOM_{AMP4_2}	Gain = 10dB, THD = 1.0%, RL = 1kΩ V_{CC} = REGAUD = 9.0V	2.1	—	—	
THD+N	THD_{AMP4}	RL = 20kΩ, VIN = 1.0Vrms	—	0.01	0.10	%
Output noise level	VN_{AMP4}	RL = 20kΩ	—	–95.0	–85.0	dBV
Gain error	GE_{AMP4}	RL = 20kΩ	–1.0	0	1.0	dB
Channel separation	CT_{AMP4}	VIN = 1.0Vrms	70.0	80.0	—	dB
PSRR	$PSRR_{AMP4}$	fsig = 1kHz	30.0	40.0	—	dB

Block Diagram (Detector)



Block Diagram (Mute Control)



Electrical Spec. (Detector 1)

Electrical Characteristics (Detector Block1)

(Unless otherwise specified; Ta = 25℃, V_{CC} = 12.0V, V_{UNREG} = 15.0V, DV_{DD} = 3.3V, fsignal = 1kHz, measurement band width = 20 to 20kHz)

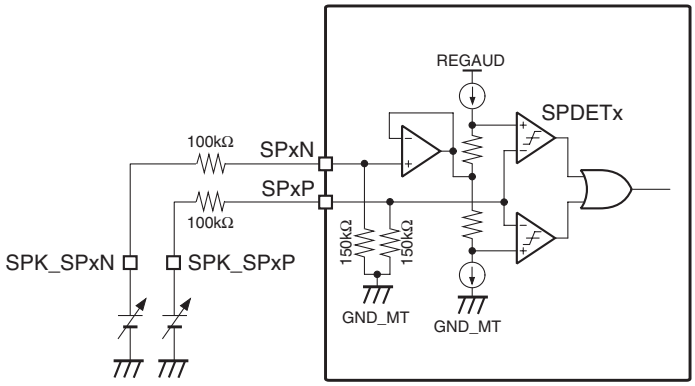
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection voltage 1_1 *1	V_{DET1_1}	VUNREG voltage detection (set: 6.0V)	4.8	6.0	6.6	V
Release voltage 1_1 *1	V_{REL1_1}		—	—	7.0	
Detection voltage 1_1	V_{DET1_1}	VUNREG voltage detection (set: 8.0V)	7.0	8.0	8.8	V
Release voltage 1_1	V_{REL1_2}		—	—	9.5	
Detection voltage 1_2	V_{DET1_3}	VUNREG voltage detection (set: 10.0V)	9.0	10.0	11.0	V
Release voltage 1_2	V_{REL1_3}		—	—	12.0	
Detection voltage 1_3	V_{DET1_4}	VUNREG voltage detection (set: 12.0V)	10.8	12.0	13.2	V
Release voltage 1_3	V_{REL1_4}		—	—	14.0	
Detection voltage 2	V_{DET2}	REGAUD voltage detection	5.4	6.0	6.6	V
Release voltage 2	V_{REL2}		—	—	7.0	
Detection voltage 3	V_{DET3}	REG33NFB voltage detection	1.44	1.60	1.76	V
Release voltage 3	V_{REL3}		—	—	1.80	
Minimum input voltage (SPP/N)	$V_{IN\_SPP/N}$	SPP/N minimum input voltage	3.0	—	—	V
Detection voltage 4_2*2,*3	V_{DET4}	Speaker out (|SPP – SPN|) voltage detection Rin = 100kΩ + 150kΩ Input voltage (SPxP/N) is over 3.0V necessary.	1.10	1.45	1.80	V
Detection voltage 5	V_{DET5}	HPBIAS voltage detection, HPERREN = “1”	1.50	2.50	3.50	V

*1 This is not tested. Therefore the characteristics is guaranteed by design.

*2 X_PROTECTOUT outputs “L” when input voltage (SPxP/N) become under 3.0V.

*3 Next page shows the measurement circuit example.

SPDET Measurement Circuit



Input pin (SPxN/P) is should be biased to over 3.0V.

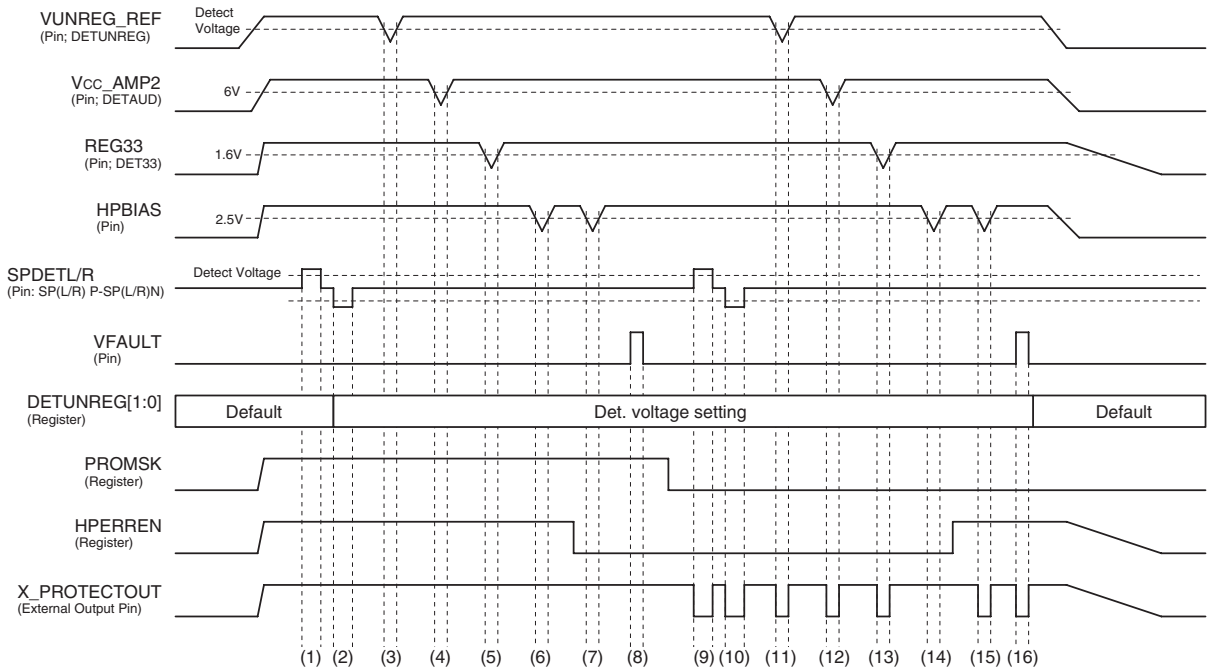
Electrical Spec. (Detector 2)

Electrical Characteristics (Detector Block2)

(Unless otherwise specified; Ta = 25℃, V_{CC} = 12.0V, V_{UNREG} = 15.0V, DV_{DD} = 3.3V, fsignal = 1kHz, measurement band width = 20 to 20kHz)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VFAULT High level input voltage	V_{FAULTH}	Input: High level	2.5	—	18.0	V
VFAULT Low level input voltage	V_{FAULTL}	Input: Low level	0	—	0.5	V
X_PROTECTOUT High level output voltage	VO_{PROH}	Output: High level, RL = 1MΩ	2.5	—	DV_{DD}	V
X_PROTECTOUT Low level output voltage	VO_{PROL}	Output: Low level, RL = 1MΩ	0	—	0.5	V
MT_CNT / MTSEL_CNT High level input voltage	VI_{MT_CNT}	Input: High level	2.5	—	DV_{DD}	V
MT_CNT / MTSEL_CNT Low level input voltage	VI_{MT_CNT}	Input: Low level	0	—	0.5	V
MT output voltage (Low: OFF)	V_{MT_L}	Rout = 10kΩ	—	0	0.5	V
MT output voltage (High: ON)	V_{MT_H}	Rout = 10kΩ	13.0	V_{UNREG}	—	V
MT output current (OFF)	IO_{MTH}	Rout = 10kΩ	—	0	3.0	μA
MT output current (ON)	IO_{MTL}	Rout = 10kΩ	1.4	1.5	—	mA

Detector Waveform

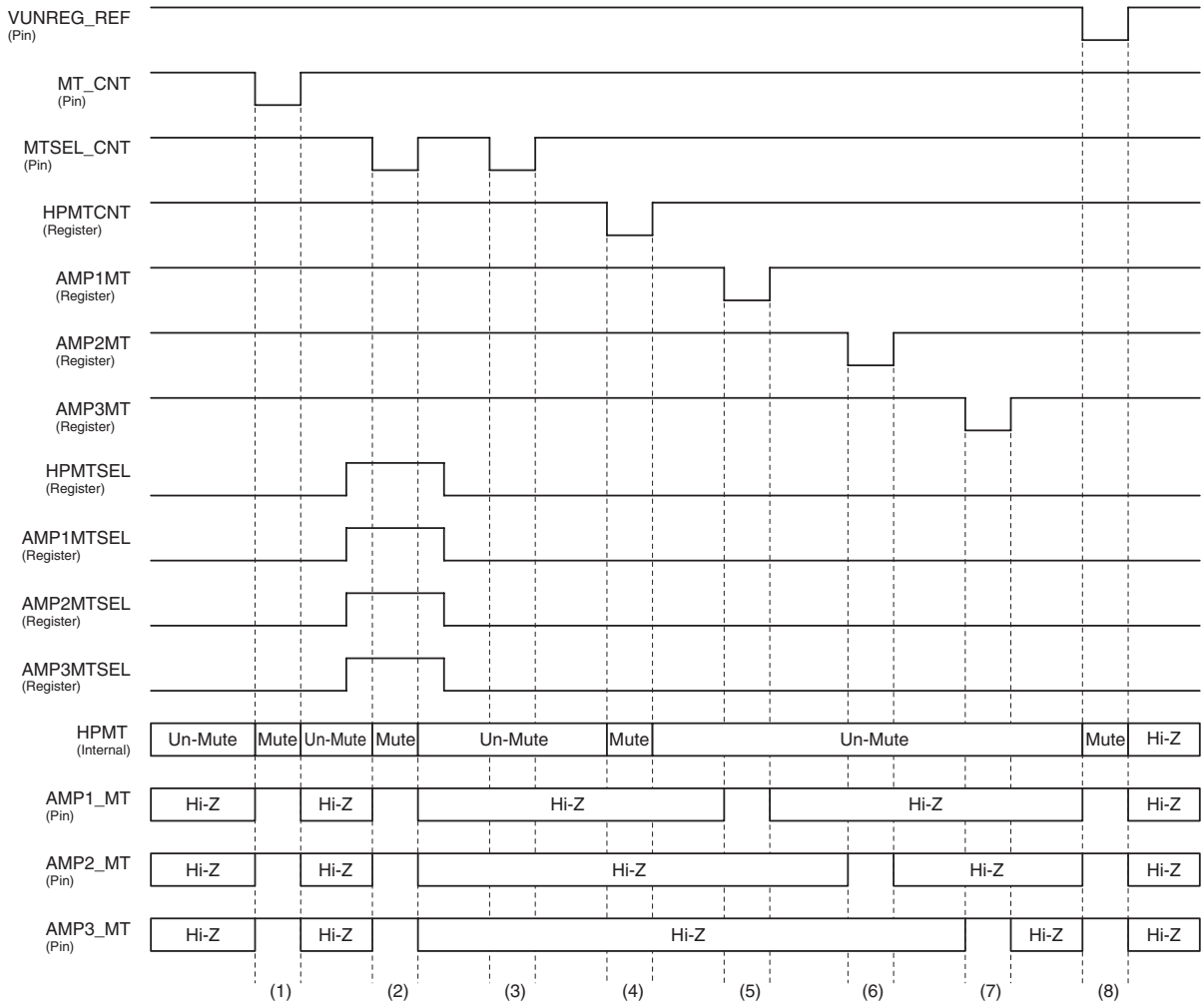


Description of Detector Waveform

(1) to (8) Despite each voltage falls below detect voltage, X_PROTECTOUT keeps "H" because PROMSK is "H".

(9) When difference voltage between SPxP and SPxN rise over detect voltage, X_PROTECTOUT is "L".
(10) Same as (9).
(11) When VUNREG_REF is falls below detect voltage, X_PROTECTOUT is "L".
(12) When VCC_AMP2 falls below the detect voltage, X_PROTECTOUT is "L".
(13) When REG33 falls below the DETAUD detect voltage, X_PROTECTOUT is "L".
(14) When HPBIAS falls below the detect voltage but HPEREN is "L", X_PROTECTOUT keeps "H".
(15) When HPBIAS falls below the detect voltage, X_PROTECTOUT is "L".
(16) When VFAULT is "H", X_PROTECTOUT is "L".

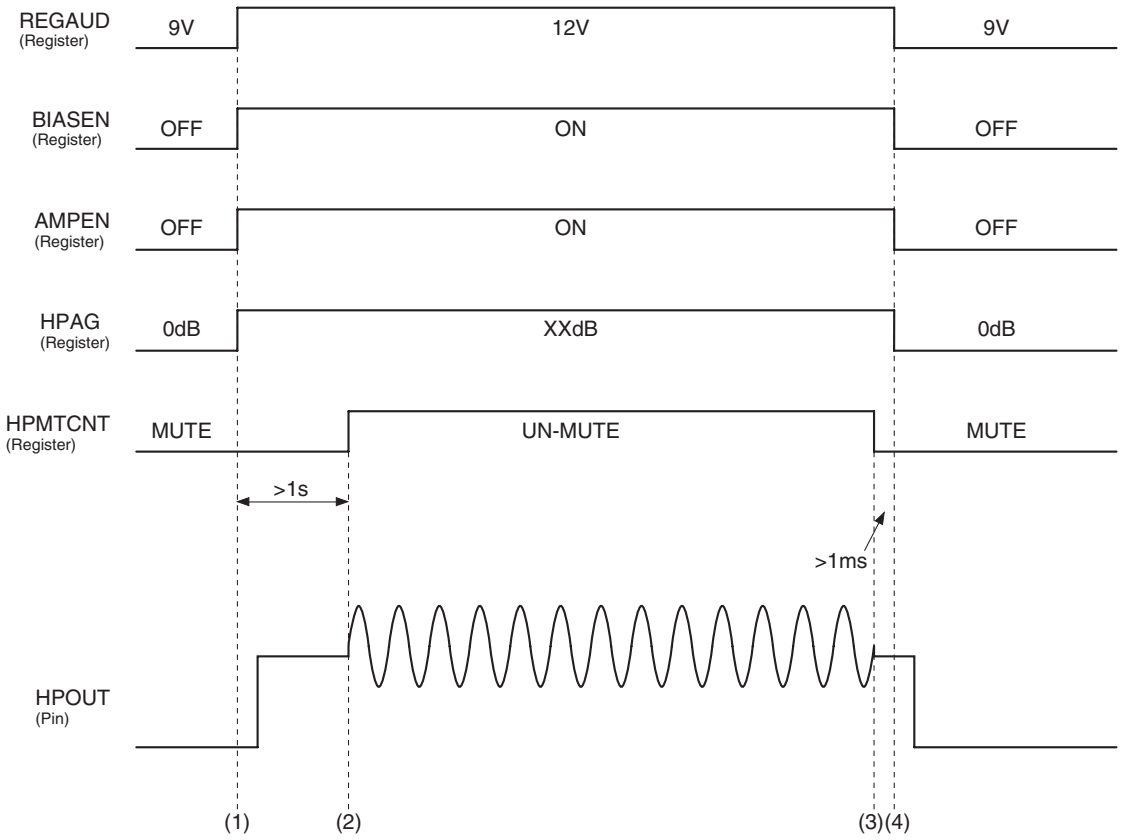
Mute Control Waveform



Description of Mute Control Waveform

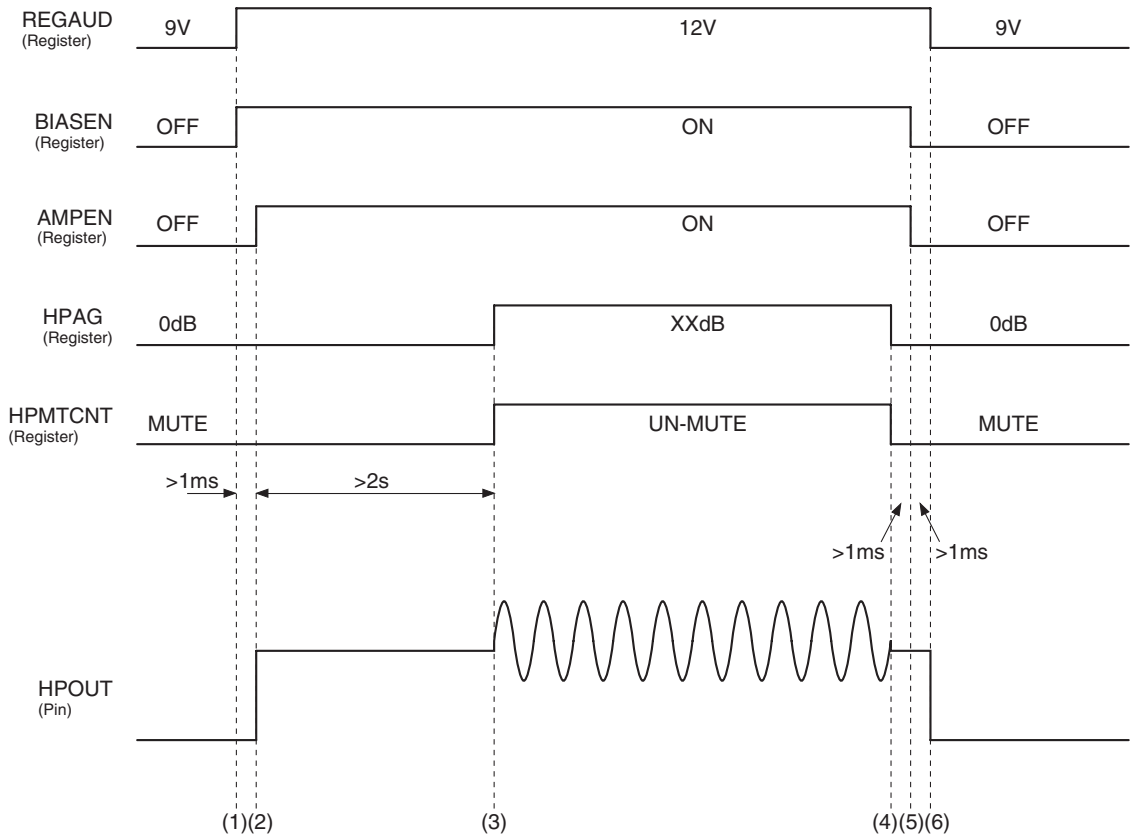
(1) When MT_CNT is "L", all amp output is muted except for AMP4.
(2) When MTSEL_CNT is "L" and XXSEL is "H", XXAMP output is muted.
(3) When MTSEL_CNT is "L" and XXSEL is "L", XXAMP keeps un-mute.
(4) When HPMTCNT is "H", HPAMP output is muted.
(5) When AMP1MTCNT is "H", AMP1AMP output is muted.
(6) When AMP2MTCNT is "H", AMP2AMP output is muted.
(7) When AMP3MTCNT is "H", AMP3AMP output is muted.
(8) When VUNREG_REF is fall below the VUNREG detector voltage, all amp output is muted except for AMP4.

Amp Sequence with Mute Transistor (HP, AMP1-3)



(1) BIASEN and AMPEN set on, REGAUD and HPAG set intended value.
(2) MTCNT should be set un-mute at least 1s after (1).
(3) When shut off the AMP, MTCNT should be set mute at first.
(4) All settings set off or set default at least 1ms after (3).

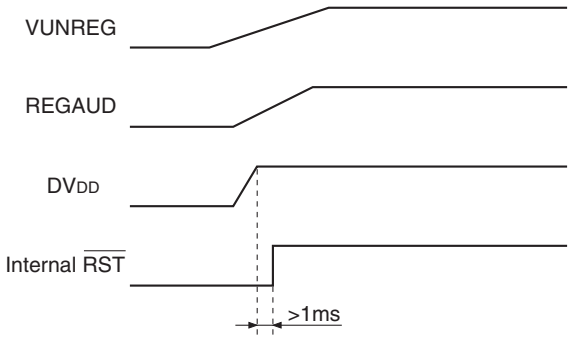
Amp Sequence without Mute Transistor (HP)



(1) REGAUD set intended value and BIASEN set on.
(2) AMPEN should be set on at least 1ms after (1).
(3) HPAG set intended value and HPMTCNT set un-mute at least 2s after (2).
(4) When shut off HPAMP, first HPAG set 0dB and HPMTCNT set mute at the same time.
(5) BIASEN and AMPEN set off at least 1ms after (4).
(6) REGAUD set default value at least 1ms after (5) if needed.

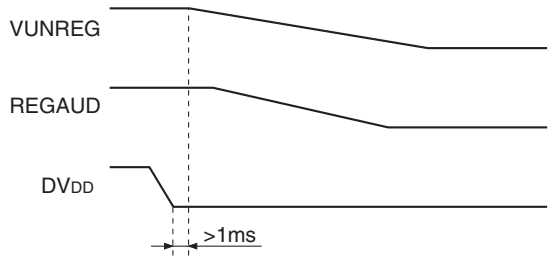
Power-On/Power-Off Sequence

Recommended Power-On Sequence



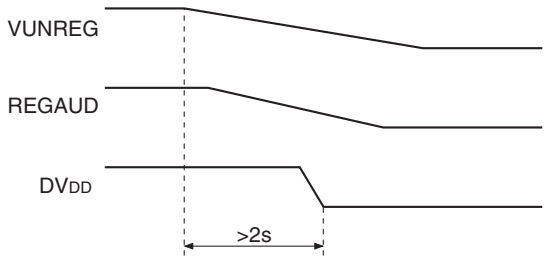
I²C should be controlled at least 1ms after DVDD is supplied.

Power-Off Sequence (with Mute Transistor)



VUNREG should be turn off at least 1ms after DVDD turn off.

Power-Off Sequence (without Mute Transistor)



DVDD should be turn off at least 2s after VUNREG turn off.

Electrical Spec. (I²C BUS Block)

Electrical Characteristics (I²C BUS Block)

(Unless otherwise specified; Ta = 25℃, V_{CC} = 12.0V, V_{UNREG} = 15.0V, DV_{DD} = 3.3V, fsignal = 1kHz, measurement band width = 20 to 20kHz)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		2.5	—	DV_{DD}	V
Low level input voltage	V_{IL}		0	—	0.5	V
High level input current	I_{IH}		—	—	10.0	μA
Low level input current	I_{IL}		—	—	10.0	μA
Low level output voltage	V_{OL}	with SDA 3mA current supplied	0	—	0.4	V
Clock frequency	f_{SCL}		0	—	400	kHz
Data change minimum waiting time	t_{BUF}		1.3	—	—	μs
Data transfer start waiting time	$t_{HD;STA}$		0.6	—	—	μs
Low level clock pulse width	t_{LOW}		1.3	—	—	μs
High level clock pulse width	t_{HIGH}		0.6	—	—	μs
Start setup waiting time	$t_{SU;STA}$		0.6	—	—	μs
Data hold time	$t_{HD;DAT}$		0	—	—	μs
Data setup time	$t_{SU;DAT}$		100	—	—	ns
Rise time	t_R		—	—	300	ns
Fall time	t_F		—	—	300	ns
Stop setup waiting time	$t_{SU;STO}$		0.6	—	—	μs

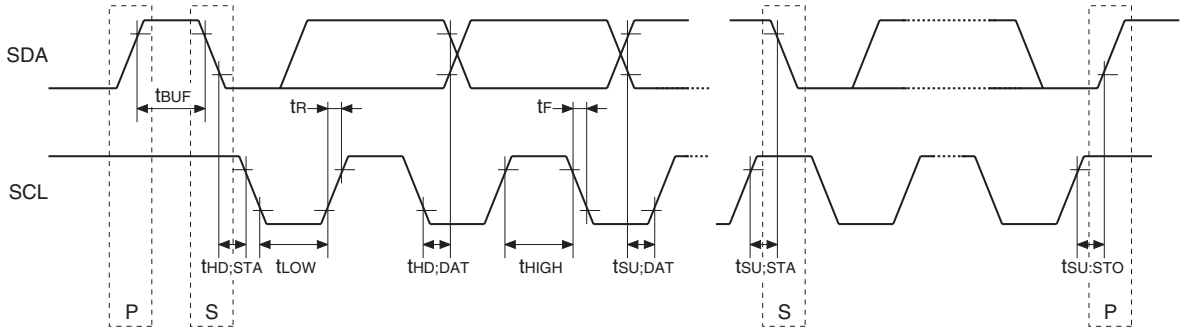
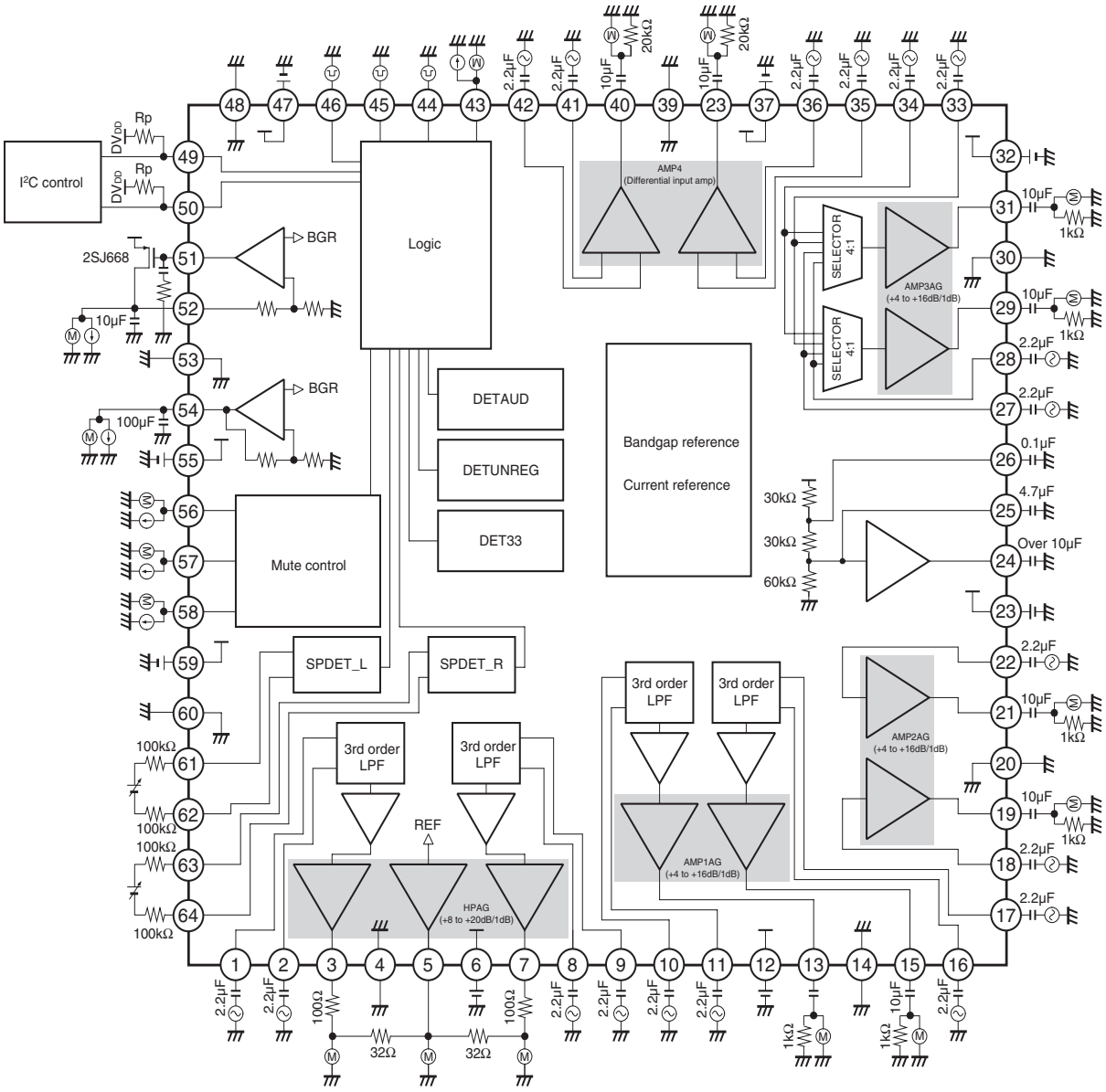


Fig. I²C BUS Control Signal Timing Chart

Measurement Circuit



I²C BUS Interface

Description

The bus protocol conforms to the I²C bus specifications, but the following restrictions are applied.

- ◆ Bus slave operation only
- ◆ Supports fast mode only
- ◆ The general call address and start byte of the slave address are not supported.
- ◆ CBUS compatibility is not supported.
- ◆ 10-bit slave addresses are not supported.
- ◆ Write mode and read mode (only 1bit: sub add “00”, S7) are supported.

Slave Address

Transmit the 7-bit slave address and the 1-bit read/write code following the START condition.
Write operation to this IC is allowed only when the input slave address and the device code match.
When the slave address dose not match the device code, an ACK (acknowledge response) is not generated and the IC dose not respond.

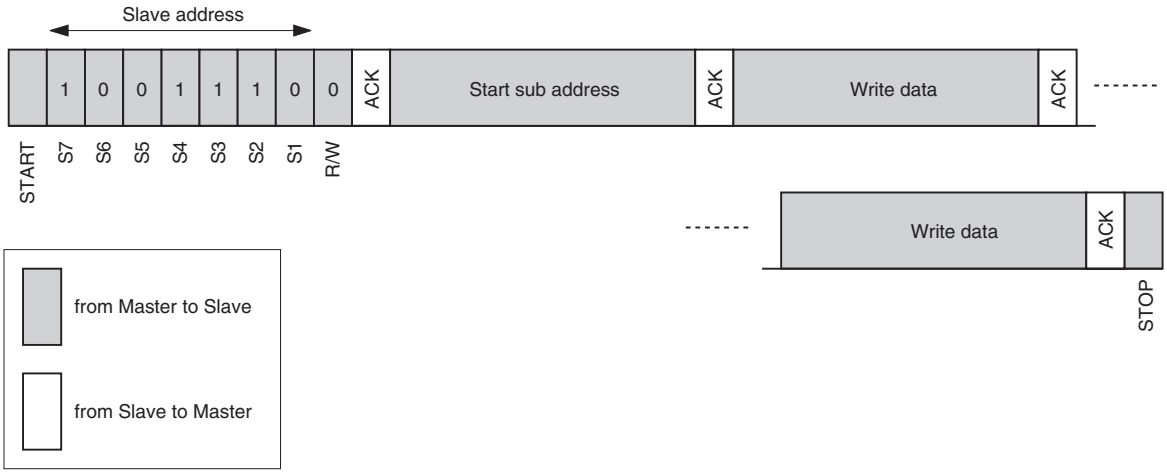
Slave Address

Slave address word (8bits)							
Device code (fixed)							R/W code (fixed)
S7	S6	S5	S4	S3	S2	S1	S0
1	0	0	1	1	1	0	0/1

Register Function (Write Register)

Write Cycle

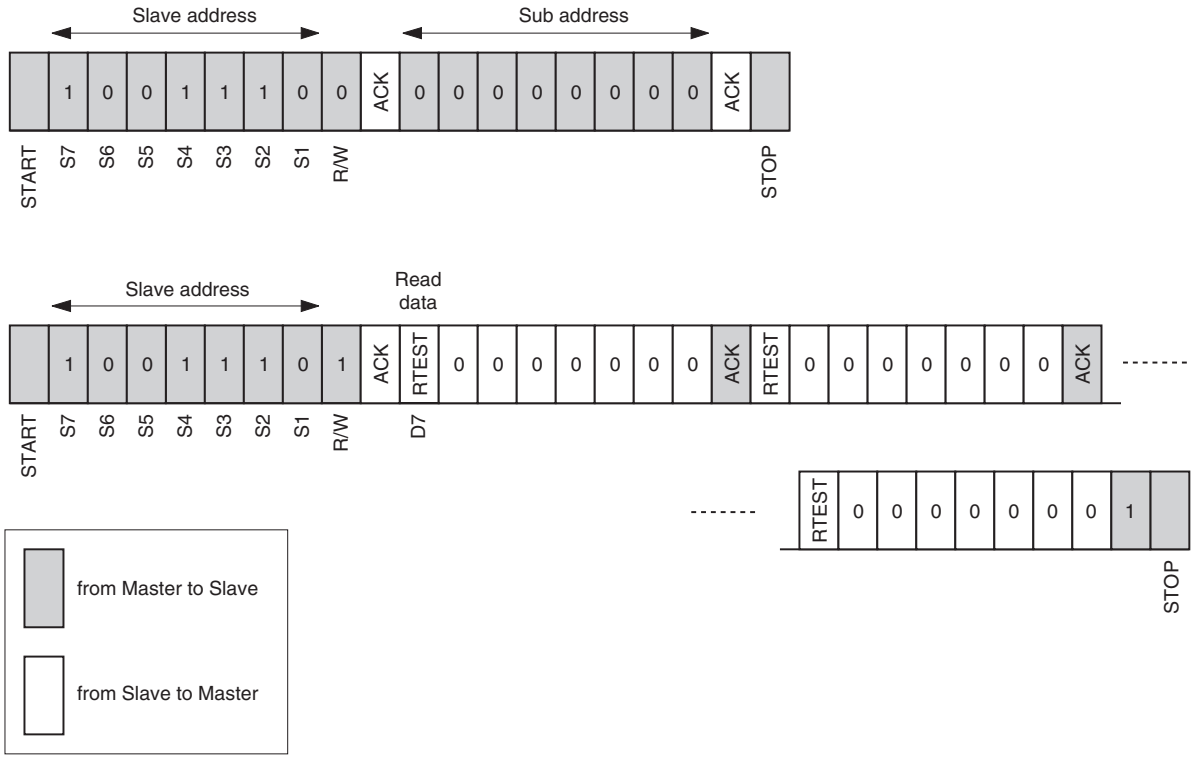
After providing slave address from master, set next transfer cycle data as write start sub address of control register to internal control register address. After that, cycle write the data providing from master to sub address indicated by control register address. Designated control register address is incremented automatically every one byte transfer completion. See the control register map for writable control register.



Register Function (Read Register)

Read Cycle

The sub address that can read is only 00hex.
To be operated read, transfer sub address (00hex) in the same procedure of write cycle. After that, re-transfer slave address from master in read mode and then the CXA3785R is in a read mode, data from sub address (00hex) accessed by control register address is returned to host.
Also, data from sub address (00hex) is returned to host continuously, until stop condition is transferred.



Register Map

Write Register

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
00	AMP ENABLE PROTECTOR READ REGISTER	RTEST	AMP2EN	PROMSK	HPERREN	HPOLPEN	REGOLPEN	BIASEN	AMPEN
R/W		R/W	W	W	W	W	W	W	W
Default		0	0	1	1	1	1	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
01	HP/AMP1 GAIN	HPAG[3:0]				AMP1AG[3:0]			
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
02	AMP2/AMP3 GAIN	AMP2AG[3:0]				AMP3AG[3:0]			
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
03	DETUNREG AMP3SEL	AMP3SEL_R[1:0]		AMP3SEL_L[1:0]		REGAUD[1:0]		DETUNREG[1:0]	
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
04	MUTE CONTROL	HPMTSEL	AMP1MTSEL	AMP2MTSEL	AMP3MTSEL	HPMTCNT	AMP1MT	AMP2MT	AMP3MT
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

Read Register

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
00	READ REGISTER	RTEST	0	0	0	0	0	0	0

Register Function (ADD: 00)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
00	AMP ENABLE PROTECTOR READ REGISTER	RTEST	AMP2EN	PROMSK	HPERREN	HPOLPEN	REGOLPEN	BIASEN	AMPEN
R/W		R/W	W	W	W	W	W	W	W
Default		0	0	1	1	1	1	0	0

D7: RTEST

Read register

D6: AMP2EN

AMP2 enable
"0" OFF (default)
"1" ON

D5: PROMSK

X_PROTECTOUT mask control
"0" Mask OFF
"1" Mask ON (default)
(X_PROTECTOUT function OFF)

D4: HPERREN

HP bias short error to VFAULT enable
"0" OFF
"1" ON (default)

D3: HPOLPEN

HP bias over load protect
"0" OFF
"1" ON (default)

D2: REGOLPEN

REGAUD over load protect
"0" OFF
"1" ON (default)

D1: BIASEN

Amp bias enable
"0" OFF (default)
"1" ON

D0: AMPEN

HPAMP, AMP1, AMP3, AMP4 enable
"0" OFF (default)
"1" ON

Register Function (ADD: 01)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
01	HP/AMP1 GAIN	HPAG[3:0]				AMP1AG[3:0]			
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

D7-4: HPAG[3:0]

HP gain control
- “0000” 0dB (default)
- “0001” 8dB
- “0010” 9dB
- “0011” 10dB
- “0100” 11dB
- “0101” 12dB
- “0110” 13dB
- “0111” 14dB
- “1000” 15dB
- “1001” 16dB
- “1010” 17dB
- “1011” 18dB
- “1100” 19dB
- “1101” 20dB
- “1110” Don’t care
- “1111” Don’t care

D3-0: AMP1AG[3:0]

AMP1 gain control
- “0000” 0dB (default)
- “0001” 4dB
- “0010” 5dB
- “0011” 6dB
- “0100” 7dB
- “0101” 8dB
- “0110” 9dB
- “0111” 10dB
- “1000” 11dB
- “1001” 12dB
- “1010” 13dB
- “1011” 14dB
- “1100” 15dB
- “1101” 16dB
- “1110” Don’t care
- “1111” Don’t care

Register Function (ADD: 02)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
02	AMP2/AMP3 GAIN	AMP2AG[3:0]				AMP3AG[3:0]			
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

D7-4: AMP2AG[3:0]

AMP2 gain control
- “0000” 0dB (default)
- “0001” 4dB
- “0010” 5dB
- “0011” 6dB
- “0100” 7dB
- “0101” 8dB
- “0110” 9dB
- “0111” 10dB
- “1000” 11dB
- “1001” 12dB
- “1010” 13dB
- “1011” 14dB
- “1100” 15dB
- “1101” 16dB
- “1110” Don’t care
- “1111” Don’t care

D3-0: AMP3AG[3:0]

AMP3 gain control
- “0000” 0dB (default)
- “0001” 4dB
- “0010” 5dB
- “0011” 6dB
- “0100” 7dB
- “0101” 8dB
- “0110” 9dB
- “0111” 10dB
- “1000” 11dB
- “1001” 12dB
- “1010” 13dB
- “1011” 14dB
- “1100” 15dB
- “1101” 16dB
- “1110” Don’t care
- “1111” Don’t care

Register Function (ADD: 03)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
03	DETUNREG AMP3SEL	AMP3SEL_R[1:0]		AMP3SEL_L[1:0]		REGAUD[1:0]		DETUNREG[1:0]	
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

D7-6: AMP3SEL_R[1:0]

AMP3 Rch selector control
- “00” SEL1INL (default)
- “01” SEL2INL
- “10” SEL1INR
- “11” SEL2INR

D5-4: AMP3SEL_L[1:0]

AMP3 Lch selector control
- “00” SEL1INL (default)
- “01” SEL2INL
- “10” SEL1INR
- “11” SEL2INR

D3-2: REGAUD[1:0]

REGAUD output voltage control
- “00” 9V (default)
- “01” 10V
- “10” 11V
- “11” 12V

D1-0: DETUNREG[1:0]

UNREG detector voltage control
- “00” 6V (default)
- “01” 8V
- “10” 10V
- “11” 12V

Register Function (ADD: 04)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
04	MUTE CONTROL	HPMTSEL	AMP1MTSEL	AMP2MTSEL	AMP3MTSEL	HPMTCNT	AMP1MT	AMP2MT	AMP3MT
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

D7: HPMTSEL

HP select mute control
“0” no select (default)
“1” select

D6: AMP1MTSEL

AMP1 select mute control
“0” no select (default)
“1” select

D5: AMP2MTSEL

AMP2 select mute control
“0” no select (default)
“1” select

D4: AMP3MTSEL

AMP3 select mute control
“0” no select (default)
“1” select

D3: HPMTCNT

HP mute control
“0” Mute (default)
“1” Un-mute

D2: AMP1MT

AMP1 mute control
“0” Mute (default)
“1” Un-mute

D1: AMP2MT

AMP2 mute control
“0” Mute (default)
“1” Un-mute

D0: AMP3MT

AMP3 mute control
“0” Mute (default)
“1” Un-mute

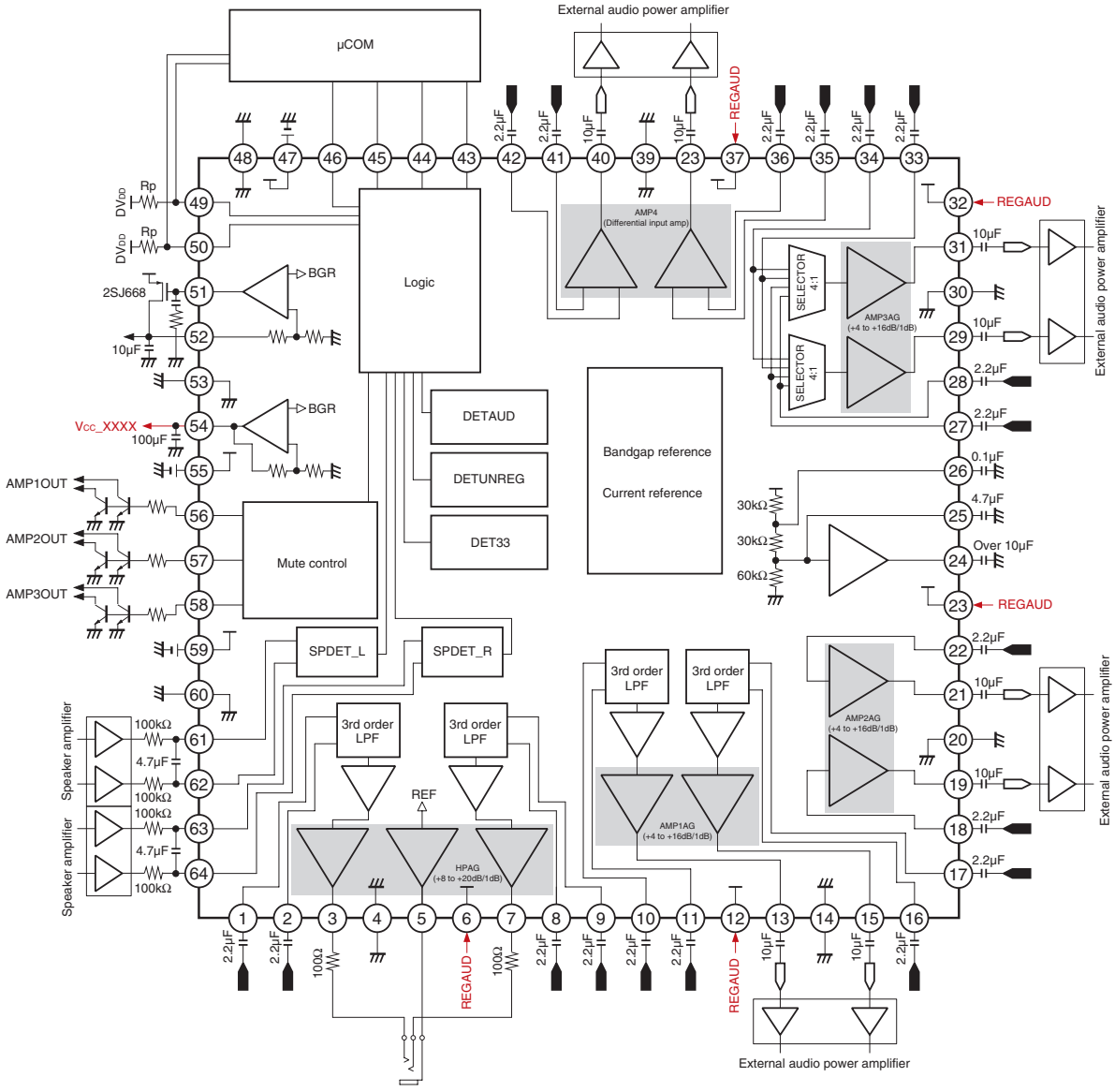
Register Function (Read Register)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
00	READ REGISTER	RTEST	0	0	0	0	0	0	0

D7: RTEST

Read register

Application Circuit

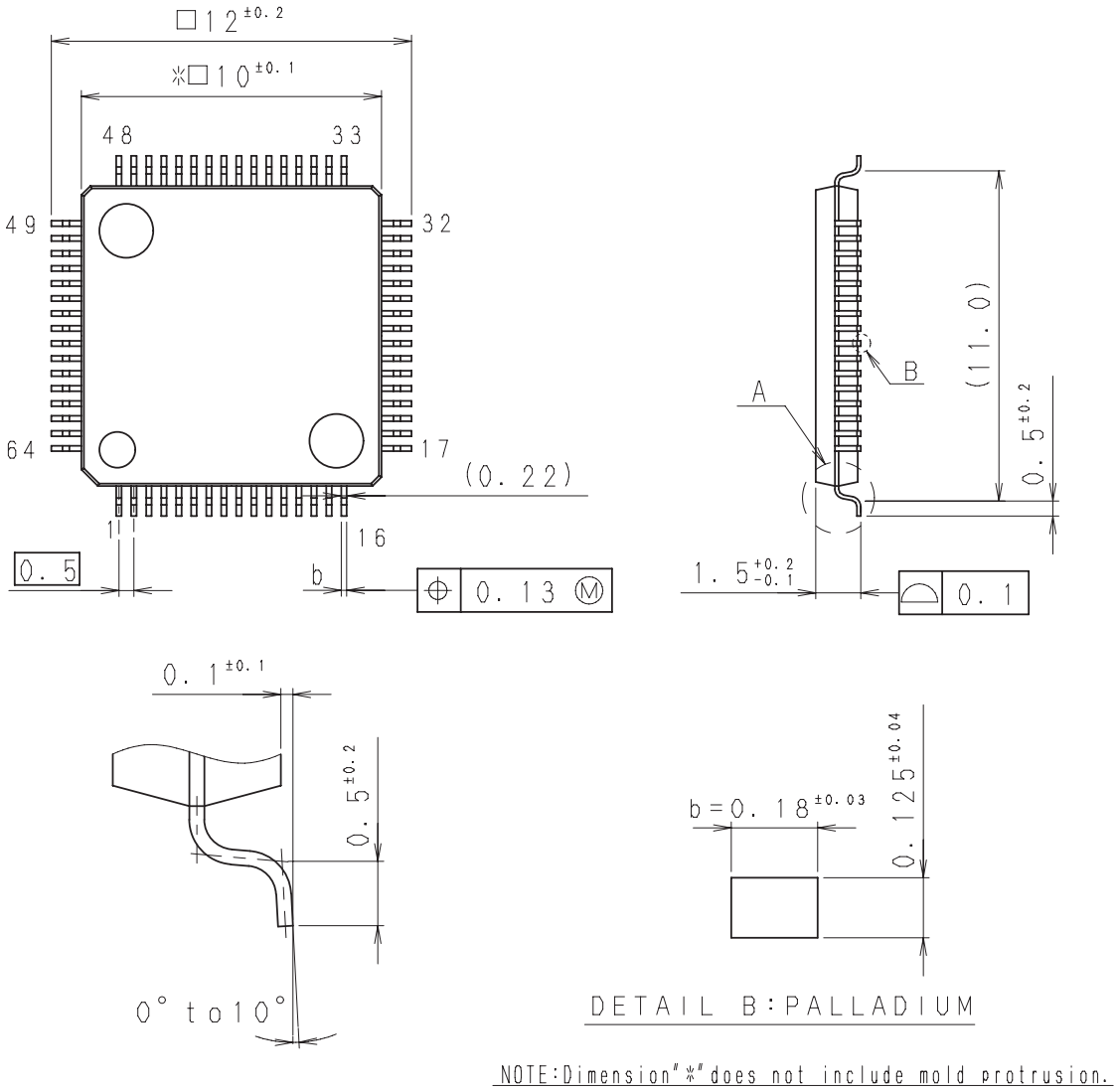


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline

(Unit: mm)

64PIN LQFP (PLASTIC)



NOTE:Dimension"※"does not include mold protrusion.

SONY CODE	LQFP-64P-L01
JEITA CODE	P-LQFP64-10X10-0.5
JEDEC CODE	————

AP-4000-64003S3 Rev.1

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.3g