

CXA3812M

Description

The CXA3812M is the current resonant controller IC and has optimum configuration to realize various power supply circuits easily and compactly.
(Applications: Power supply circuit, etc.)

Features

- ◆ Overcurrent timer latch
- ◆ Soft start function
- ◆ Minimum frequency adjustment
- ◆ Pulse overcurrent load detection
- ◆ Adjacent 2-pin short protection
- ◆ Various protection functions including overvoltage and overcurrent

Structure

BiCMOS silicon monolithic IC

Package

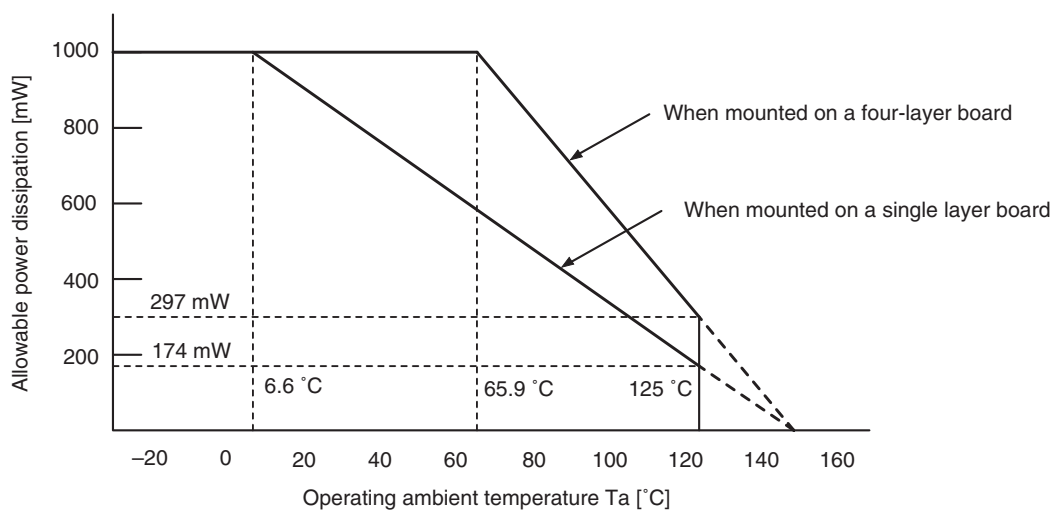
14-pin SOP

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Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Remarks
Maximum supply voltage	VCC	24.0	V	VCC
Pin voltage which operates with VCC as power supply	VCCIN	-0.3 to VCC + 0.3	V	xEN
Driver output pin voltage	VOUT	-0.3 to VCC + 0.3	V	OUTP, OUTN
Power supply pin voltage for internal circuit	VREF	-0.3 to +7.0	V	VREF
Pin voltage which operates with VREF as power supply	VREFIN	-0.3 to +7.0	V	VSENSE, OFFADJ, CS1, CS2, RT, SS, FMIN
Allowable power dissipation	P _D	*1	mW	(See the thermal derating curve.)
Operating ambient temperature range	T _{opt}	-30 to +125	°C	
Junction temperature	T _{jmax}	+150	°C	
Storage temperature range	T _{stg}	-55 to +150	°C	

*1 Allowable power dissipation reduction characteristics

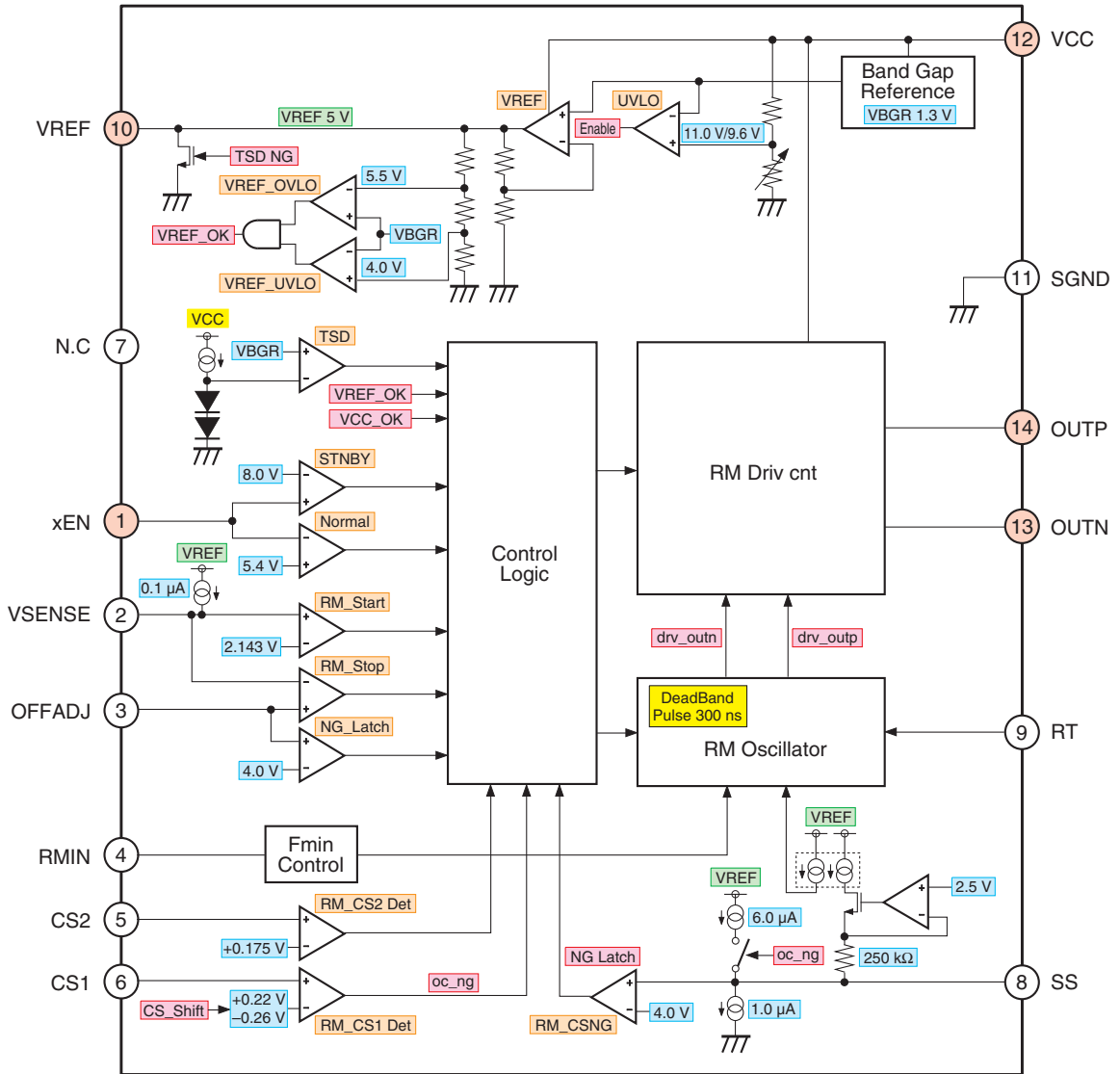


Glass fabric base epoxy board 76 mm × 114 mm t = 1.6 mm

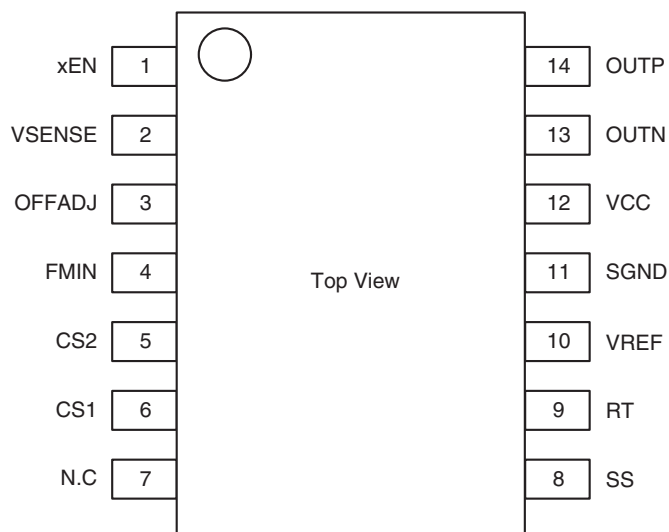
Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Remarks
Supply voltage (VCC)	VCC	12.0 to 18.0	V	
Operating ambient temperature range	T _{opt}	-25 to +85	°C	
Junction temperature	T _j	-25 to +125	°C	

Block Diagram



Pin Configuration



Pin Table

Pin No.	Symbol	Description	Connection end of protection diode
1	xEN	Mode select	VCC, SGND
2	VSENSE	Operation start voltage input	VREF, SGND
3	OFFADJ	Operation stop voltage adjustment and abnormal latch forcible input	VREF, SGND
4	FMIN	Minimum frequency adjustment	VREF, SGND
5	CS2	Overcurrent detection 2	VREF
6	CS1	Overcurrent detection 1	VREF
7	N.C	—	—
8	SS	Soft start and overcurrent timer latch	VREF, SGND
9	RT	Frequency control	VREF, SGND
10	VREF	Internal supply voltage output	VCC, SGND
11	SGND	Signal GND	—
12	VCC	Power supply input	SGND
13	OUTN	FET gate driver output for Low	—
14	OUTP	FET gate driver output for High	—

Pin Description

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit	Description
1	xEN	I	VCC to GND		Mode select (GND connection: Normal operation, VCC connection: Standby mode)
2	VSENSE	I	VREF to GND During steady state: 2.5 V		Operation start voltage input (Connect to PFC output detection resistor.)
3	OFFADJ	I	VREF to GND		Operation stop voltage adjustment and abnormal latch forcible input
4	FMIN	I	1.2 V		Minimum oscillation frequency control (Connect to minimum frequency control resistor.)
5 6	CS2 CS1	I I	VREF to -0.3 V		Overcurrent detection 2 Overcurrent detection 1 (Connect to current detection resistor.)

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit	Description
7	N.C	—	—	—	—
8	SS	I/O	VREF to GND During steady state: 2.5 V		Soft start and overcurrent timer latch (Connect to soft start capacitor.)
9	RT	I	(3.5 V)		Frequency control
10	VREF	O	5.0 V		Internal supply voltage output (Connect to photocoupler for output feedback.)
11	SGND	—	—	—	Ground
12	VCC	—	—	—	Power supply input
13	OUTN	O	VCC to GND		FET gate driver output for Low. (Connect to drive transformer.)
14	OUTP	O			

Electrical Characteristics

(Unless otherwise specified, $T_a = 27 [^{\circ}\text{C}]$, $V_{CC} = 12 [\text{V}]$, $x\text{EN} = \text{GND}$, $\text{RT} = \text{OPEN}$, $\text{R}_{\text{fmin}} = 120 \text{ k}\Omega$)

1. Current consumption (VCC pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption in standby mode	Istb	$x\text{EN} = \text{VCC}$	—	500	800	μA
Current consumption in operation mode	Iact	$x\text{EN} = \text{GND}$, $\text{VSENSE} = 2.0 \text{ V}$ * Non Switching	—	1.5	2.5	mA

2. Under Voltage Lock Out circuit (VCC pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Operation start voltage	Vact		10.2	11.0	11.8	V
Operation stop voltage	Voff		9.0	9.6	10.2	V
Hysteresis width	Vact-Voff	$\text{Vact} - \text{Voff}$	1.1	1.4	1.7	V

3. Reference voltage output circuit (VREF pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Output voltage	Vvref		4.85	5.00	5.15	V
Input stability	Vline	$\text{VCC} = 10.5 \text{ V to } 18 \text{ V}$	—	10	30	mV
Load stability	Vload	$\text{Iload} = 0.1 \text{ mA to } 5 \text{ mA}$	—	20	50	mV
Pin voltage for NG latch (for TSD)	Vvrefng	$\text{Iout} = 10 \text{ mA}$ (design guarantee)	—	0.1	0.5	V

4. xEN pin voltage detection circuit (xEN pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Detection voltage Low	Venl		5.2	—	5.6	V
Detection voltage High	Venh		7.6	—	8.4	V
Internal pull-up resistance value	Ren	$x\text{EN} = 0.1 \text{ V}$	35	50	65	$\text{k}\Omega$

5. Operation start voltage detection circuit (VSENSE pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Operation start voltage	Vstart		2.036	2.143	2.250	V
Operation stop voltage	Vstop	$\text{OFFADJ} = 1.883 \text{ V}$	1.789	1.883	1.977	V
Pin pull-up current	Ivs	$\text{VSENSE} = 0.1 \text{ V}$	0.05	0.1	0.2	μA

6. Stop voltage adjustment circuit (OFFADJ pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Latch voltage for external abnormal detection	Voffadjng		3.8	4.0	4.2	V

7. Gate Drive circuit (OUTP, OUTN pins)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Output Low voltage	Voutl	VCC = 18 V, Iout = +10 mA	—	0.05	0.1	V
Output High voltage	Vouth	VCC = 18 V, Iout = -10 mA	17.9	17.95	—	V
Rise time *1	Voutr	VCC = 18 V, CLOAD = 1000 pF	—	35	100	ns
Fall time *1	Voutf	VCC = 18 V, CLOAD = 1000 pF	—	35	100	ns

*1 Rise time and fall time use $VCC \times 0.1$ to $VCC \times 0.9$ as judgment voltages.

8. Soft start circuit (SS pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Soft start current	I _{ss}	SS = 0 V	7.5	10	12.5	μA
Clamp voltage	V _{ss}		2.3	2.5	2.7	V
Overcurrent timer latch detection voltage	V _{timerlatch}		3.8	4.0	4.2	V
Charge current for overcurrent detection	I _{occ}	CS1 = 0.3 V, SS = 3.0 V	3.2	5.0	6.8	μA

9. Frequency control circuit (RT pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Maximum oscillation frequency	F _{max}	I _{rt} = 2 mA, R _{fmin} = 39 kΩ	800	—	—	kHz
Deadband width	T _{db}		270	300	330	ns
Clamp frequency magnification during soft start	F _{clamp}	f ₀ /f ₄ (f ₀ : RM_SS = 0 V, f ₄ : RM_SS = open) R _{fmin} = 390 kΩ	3.5	4.0	4.5	times

10. Minimum frequency adjustment circuit (FMIN pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Setting frequency 1	F _{min1}	R _{fmin} = 390 kΩ	-3 %	46.1	+3 %	kHz
Setting frequency 2	F _{min2}	R _{fmin} = 120 kΩ	-4 %	96.7	+4 %	kHz
Setting frequency 3	F _{min3}	R _{fmin} = 39 kΩ	-5 %	144.1	+5 %	kHz
Pin low current detection	LC _{det}		0.85	1.25	1.65	μA

11. Overcurrent detection circuit 1 (CS1 pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Positive side detection	Vcs1p	When RM_OUTP = High	0.209	0.220	0.231	V
Negative side detection	Vcs1n	When RM_OUTN = High	-0.295	-0.260	-0.235	V
Detection delay time	Tcsdly	CS to DRV RM_CS = -0.3 V \leftrightarrow 0.3 V (Rectangular wave input)	100	150	200	ns
Detection mask time	Tcsmask	RM_CS = 0.3 V	384	480	576	ns
Overcurrent detection voltage ratio for +B drop	Rrmocp	VSENSE < 2.143 V	10	15	20	%

12. Overcurrent detection circuit 2 (CS2 pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Continuous load detection voltage	Vcs2	When RM_OUTP = High	0.158	0.175	0.193	V
Detection mask time	Tcsmask	RM_CS = 0.3 V	384	480	576	ns
Continuous load detection time	Tcs2	(When the time corresponds to 2.1 s \times 5 times)		(10)		s

Note) ◆ Shipping inspection is performed at room temperature. (The design is guaranteed with respect to temperature fluctuation.)

- ◆ The notation “ \pm ” of applied current shown in the measurement conditions indicates that “-” is outflow current from the IC and “+” is inflow current to it.

13. List of Electrical Characteristics

Item	Specification ratings (Ta = 27 °C)			Design guarantee ratings (Ta = -25 to +85 °C) (*1)			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (VCC pin)							
Current consumption in standby current	—	500	800	—	500	800	μA
Current consumption in operation mode	—	1.5	2.5	—	1.5	2.5	mA
Low voltage misoperation prevention circuit (VCC pin)							
Operation start voltage	10.2	11	11.8	10.2	11	11.8	V
Operation stop voltage	9	9.6	10.2	9	9.6	10.2	V
Hysteresis width	1.1	1.4	1.7	1.1	1.4	1.7	V
Reference voltage output (VREF pin)							
Output voltage	4.85	5	5.15	4.85	5	5.15	V
Input stability	—	10	30	0	10	30.5 (*2)	mV
Load stability	—	20	50	—	20	50	mV
Pin voltage for NG latch (When TSD)	—	0.1	0.5	—	0.1	0.5	V
Mode select circuit (xEN pin)							
Detection voltage Low	5.2	—	5.6	5.2	—	5.6	V
Detection voltage High	7.6	—	8.4	7.6	—	8.4	V
Internal pull-up resistor value	35	50	65	35	50	65	kΩ
Operation start voltage detection circuit (VSENSE pin)							
Operation start voltage	2.036	2.143	2.250	2.036	2.143	2.250	V
Operation stop voltage	1.789	1.883	1.977	1.789	1.883	1.977	V
Pin pull-up current	0.05	0.1	0.2	0.05	0.1	0.2	μA
Stop voltage adjustment circuit (OFFADJ pin)							
Latch voltage for external abnormal detection	3.8	4	4.2	3.8	4	4.2	V
Output circuit (OUTP, OUTN pins)							
Output Low voltage	—	0.05	0.1	—	0.05	0.1	V
Output High voltage	17.9	17.95	—	17.9	17.95	—	V
Rise time	—	35	100	—	35	100	ns
Fall time	—	35	100	—	35	100	ns
Soft start circuit (SS pin)							
Soft start current 1	7.5	10	12.5	7.5	10	12.5	μA
Soft start current 2	4.69	6.25	7.81	4.69	6.25	7.81	μA
Clamp voltage	2.3	2.5	2.7	2.3	2.5	2.7	V
Overcurrent timer latch detection voltage	3.8	4	4.2	3.8	4	4.2	V
Charge current for overcurrent detection	3.2	5.0	6.8	3.2	5.0	6.8	μA

Item	Specification ratings (Ta = 27 °C)			Design guarantee ratings (Ta = -25 to +85 °C) (*1)			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency control circuit (RT pin)							
Maximum oscillation frequency	800	—	—	800	—	—	kHz
Deadband width	270	300	330	270	300	330	ns
Clamp frequency magnification during soft start	3.5	4.0	4.5	3.5	4.0	4.5	times
Minimum frequency adjustment circuit (FMIN pin)							
Setting frequency 1	-3.0 %	46.1	+3.0 %	-3.8 % (*2)	46.1	+3.0 % (*2)	kHz
Setting frequency 2	-4.0 %	96.7	+4.0 %	-4.7 % (*2)	96.7	+4.0 % (*2)	kHz
Setting frequency 3	-5.0 %	144.1	+5.0 %	-5.6 % (*2)	144.1	+5.0 % (*2)	kHz
Constant current detection threshold value	0.85	1.25	1.65	0.85	1.25	1.65	μA
Overcurrent circuit (CS1 pin)							
Positive side detection	0.209	0.220	0.231	0.209	0.220	0.231	V
Negative side detection	-0.295	-0.260	-0.235	-0.295	-0.260	-0.235	V
Overcurrent detection voltage ratio for +B drop	10	15	20	10	15	20	%
Detection delay time	100	150	200	100	150	200	ns
Detection mask time	384	480	576	384	480	576	ns
Overcurrent detection circuit (CS2 pin)							
Continuous load detection voltage	0.158	0.175	0.193	0.158	0.175	0.193	V
Detection mask time	384	480	576	384	480	576	ns
Continuous load detection time		(10)			(10)		s

*1 Ratings are design guarantee values within this temperature range.

*2 Specification values at room temperature may not be satisfied because of temperature dependence.

Detailed Description of Each Block

1. Misdetection Prevention Circuit

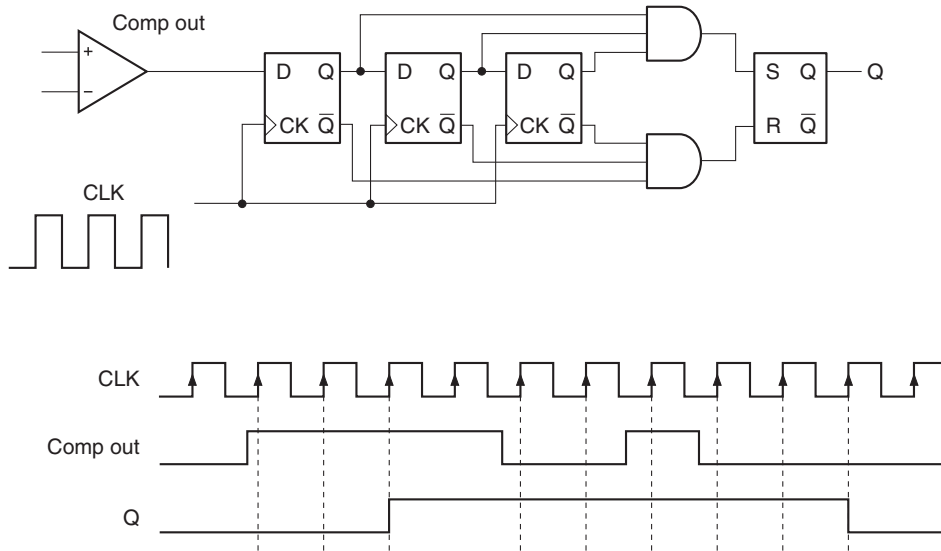


Fig. 1. Equivalent Circuit of 1 ms × 3 times-Sampling Chatter Filter

Fig. 1 above shows the equivalent circuit of 1 ms × 3 times-sampling chatter filter. When CLK has a 1 ms cycle, Comp out is monitored at the rising edge of every 1 ms, and the output Q is defined when it reaches three times. The other chatter filters also operate using a similar circuit.

The clocks used for each setup time are generated by frequency dividing the 1 MHz clock. The setup time variance of the 1 ms × 3 times chatter filter in the example above is as follows. Variance of 2 ms < setup time < 3 ms occurs due to the Comp out inversion timing. In addition, taking into account the basic clock 1 kHz variance, the 1 ms (1024 μs) clock has variance of 0.972 ms to 1.075 ms (±5 %), so at the maximum variance the setup time variance is 1.944 ms < setup time < 3.225 ms.

Setup time of misdetection prevention counter (when the basic clock of 1 MHz has no variance) used for this IC is shown below.

- ◆ Corresponds to 32 μs × 3 times 64 μs to 96 μs
- ◆ Corresponds to 128 μs × 5 times 512 μs to 640 μs
- ◆ Corresponds to 1 ms × 3 times 2 ms to 3 ms (Converted by 1 ms for 1.024 ms)
- ◆ Corresponds to 1 ms × 5 times 4 ms to 5 ms
- ◆ Corresponds to 8 ms × 6 times 40 ms to 48 ms (Converted by 16 ms for 16.4 ms)
- ◆ Corresponds to 2.1 s × 3 times 4.2 s to 6.3 s (Converted by 2.1 s for 2.097 s)
- ◆ Corresponds to 2.1 s × 5 times 8.4 s to 10.5 s

2. xEN Pin Voltage Detection Circuit

Normal sequence mode and standby mode can be set in accordance with the xEN pin input voltage.

Normal sequence mode can be set by short-circuiting the xEN pin to GND, and standby mode can be set by short-circuiting the xEN pin to VCC or leaving the pin open.

Note that this IC has a test mode for minimum frequency setting. The output pin can be forcibly operated by setting the xEN pin voltage to the voltage shown below.

$$5.6 \text{ V} < \text{xEN pin voltage} < 7.6 \text{ V}$$

In addition, the mode transition setup times when the xEN pin voltage is switched are as follows. Transition to test mode can be enabled only in standby mode.

- ◆ Normal sequence mode ⇒ Standby mode : 32 μs \times 3 times
- ◆ Standby mode ⇒ Normal sequence mode : 32 μs \times 3 times
- ◆ Standby mode ⇒ Test mode : 1 ms \times 3 times
- ◆ Test mode ⇒ Standby mode : 1 ms \times 3 times

3. Operation Start Voltage Detection Circuit

Fig. 2 shows the equivalent circuit for VSENSE pin.

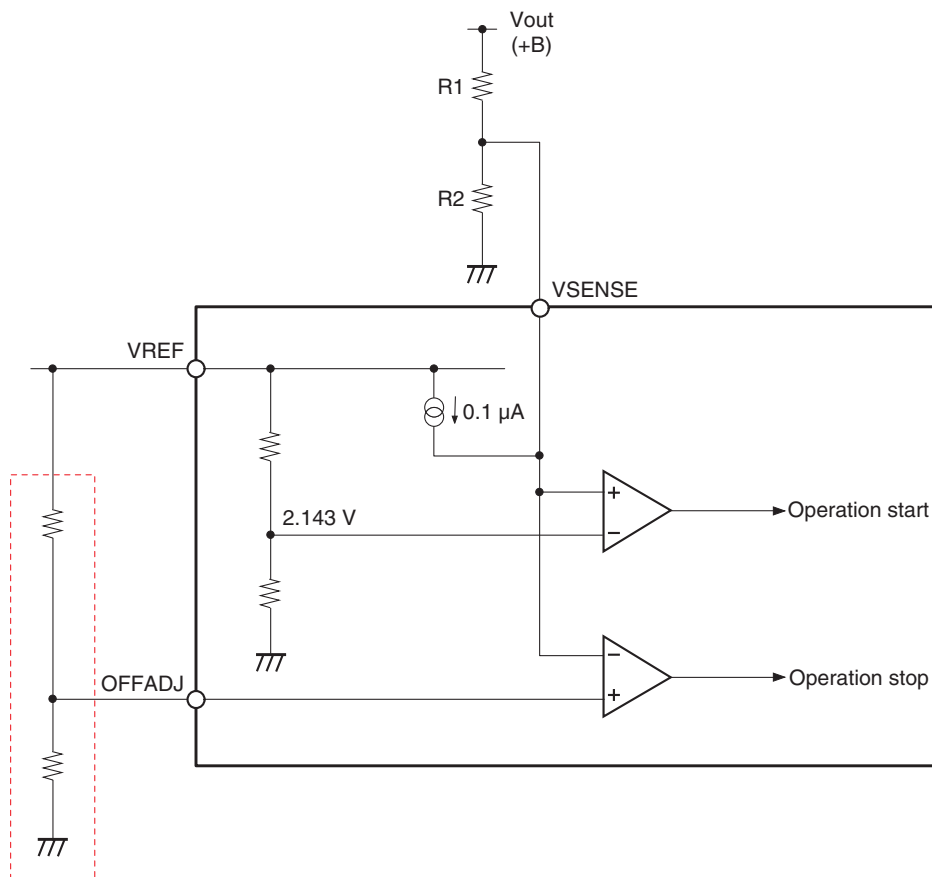


Fig. 2. Equivalent Circuit for Operation Start Voltage Detection Block

The VSENSE pin controls the operation start/stop.

- ◆ Operation start voltage
Controller operation starts when $V_{SENSE} > 2.143 \text{ V}$ is detected, corresponding to $8 \text{ ms} \times 6$ times.
- ◆ Operation stop voltage
Controller operation stops when $V_{SENSE} < OFFADJ$ is detected, corresponding to $1 \text{ ms} \times 5$ times.

The circuit connected to this pin operates at all time after the power-on reset is released. Even if a High signal is input to the xEN pin, the circuit operates, the $8 \text{ ms} \times 6$ times chatter filter also operates. If a Low signal is input to the xEN pin after condition where the VSENSE pin voltage is 2.143 V or more is counted up, the operation starts immediately.

4. Oscillator Block

4-1. Oscillator circuit

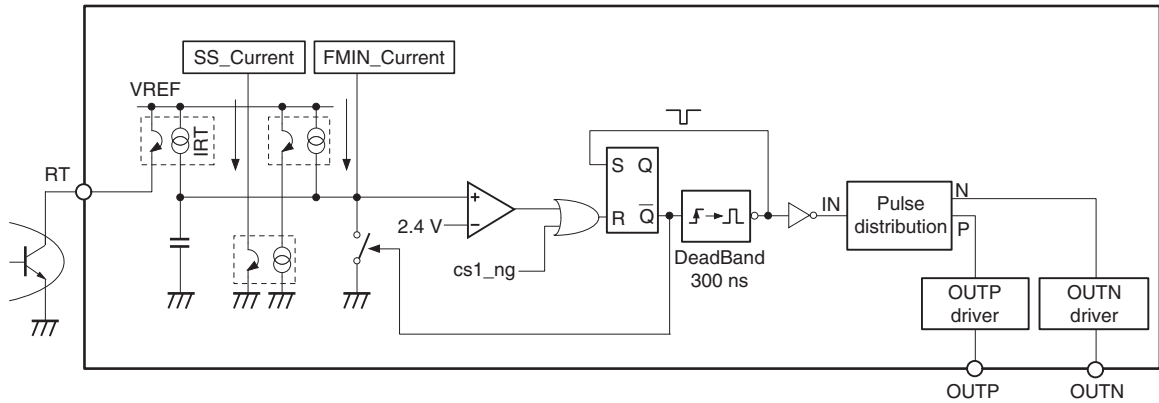


Fig. 3. Oscillator Equivalent Circuit

Fig. 3 shows the equivalent circuit for oscillator circuit. Outputs of some current mirror circuits are connected to internal timing capacitor, discharge switch, and positive input of comparator. The resonant oscillation frequency is determined by the current led from the RM_RT pin, the current from the minimum frequency setting circuit, and the current from the soft start circuit. The deadband width is fixed internally to 300 ns. The Fig. 4 graph shows the resonant oscillation frequency response at a minimum frequency setting of 46.1 kHz, relative to the current led from the RM_RT pin.

Resonant oscillation frequency
When Rfmin = 390 kΩ connected (46.1 kHz setting)

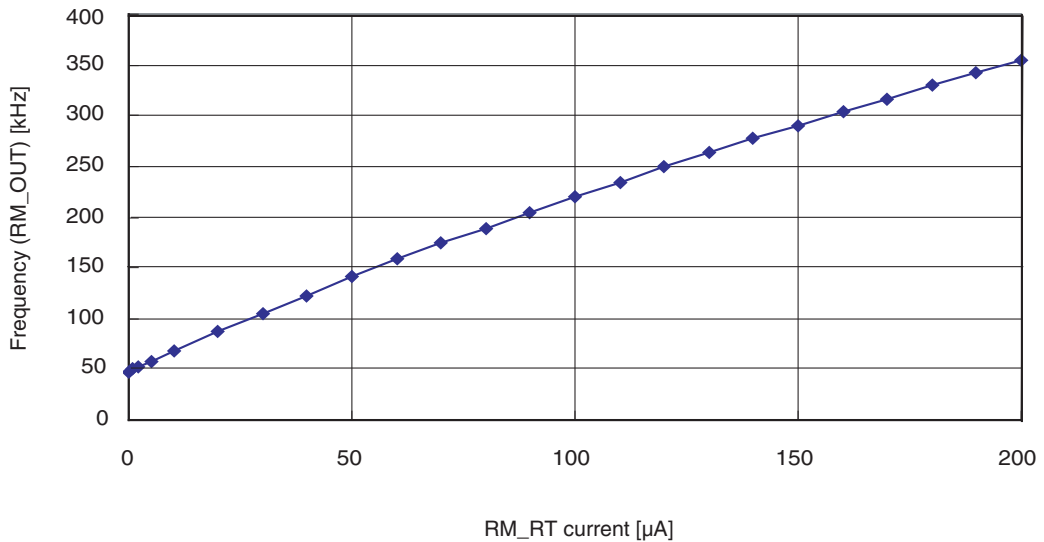


Fig.4. Resonant Oscillation Frequency

4-2. Minimum Frequency Setting Circuit

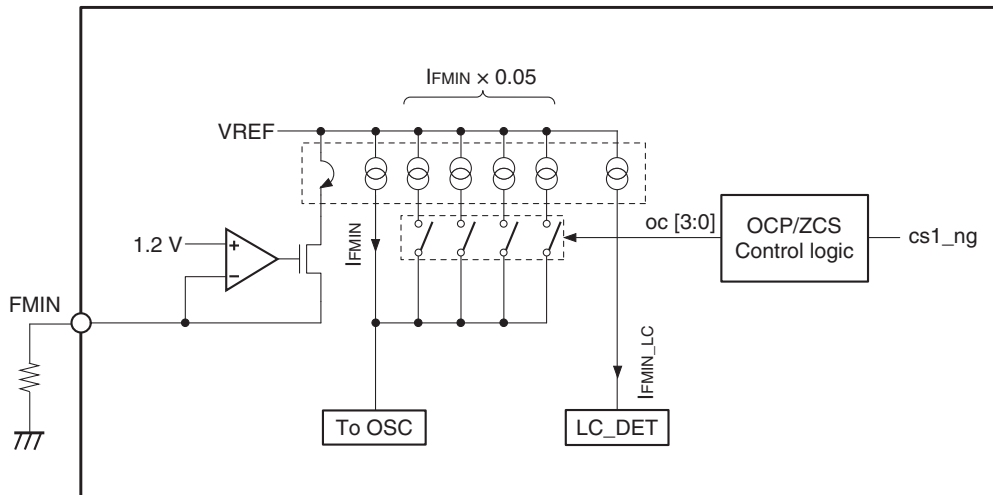


Fig. 5. Equivalent Circuit for Minimum Frequency Control Block

Fig. 5 shows the equivalent circuit for minimum frequency control block. The minimum resonant frequency can be set by externally connecting a resistor to the RM_FMIN pin. The Fig. 6 graph shows the minimum frequency response relative to the external resistor value.

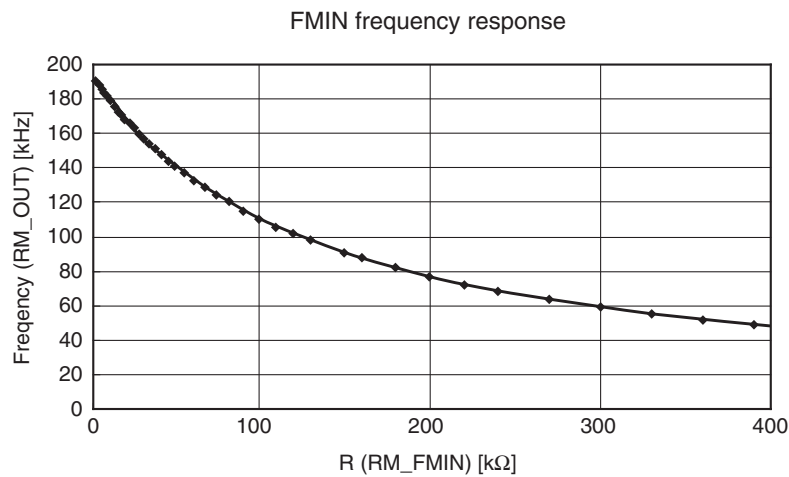


Fig. 6. Minimum Oscillation Frequency Setting

The minimum oscillation frequency decreases when the RM_FMIN pin is left open or the current led from the pin decreases. IC latch operation forcibly results when the current led from the pin is detected as being continuously 1.25 μA or less (LC_DET) for 6 s (2.1 s × 3 times). This pin voltage becomes 925 kΩ by converting to a resistance value connected to the pin. Connect a resistor of 700 kΩ or less to the RM_FMIN pin, considering a margin to the IC variance.

4-3. Soft Start Circuit

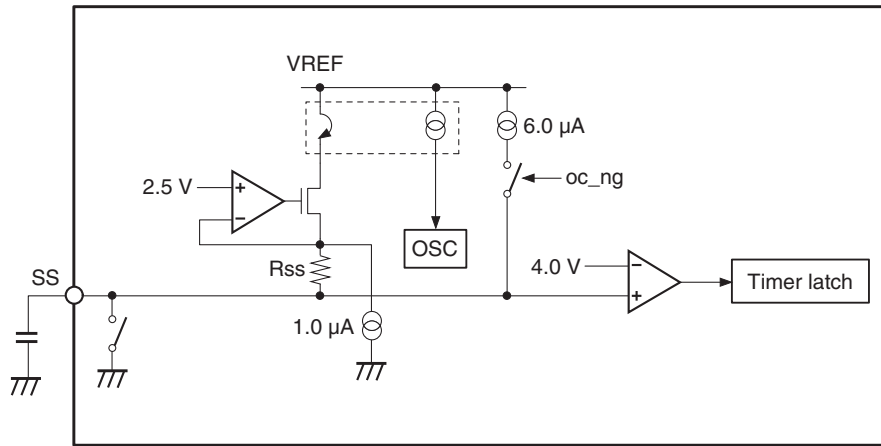


Fig. 7. Equivalent Circuit for Soft Start Control Block

Fig. 7 shows the equivalent circuit for soft start block.

The soft start circuit feeds back the current, determined by the internal 2.5 V output, the IC internal resistance (R_{ss}), and the external capacitor, to the oscillator of the resonant controller. This enables to start oscillation from a high frequency during resonant start-up. The R_{ss} value is 400 k Ω in active standby mode and 250 k Ω in high-speed startup mode.

In addition, the maximum frequency during soft start is limited to 4 times (max.) the minimum frequency determined by the RM_FMIN pin external resistor.

Note that the frequency other than during soft start is not limited to 4 times the minimum frequency. In these cases the frequency is controlled according to the current led from the RM_RT pin.

The Fig. 8 graph shows the resonant oscillation frequency response during soft start.

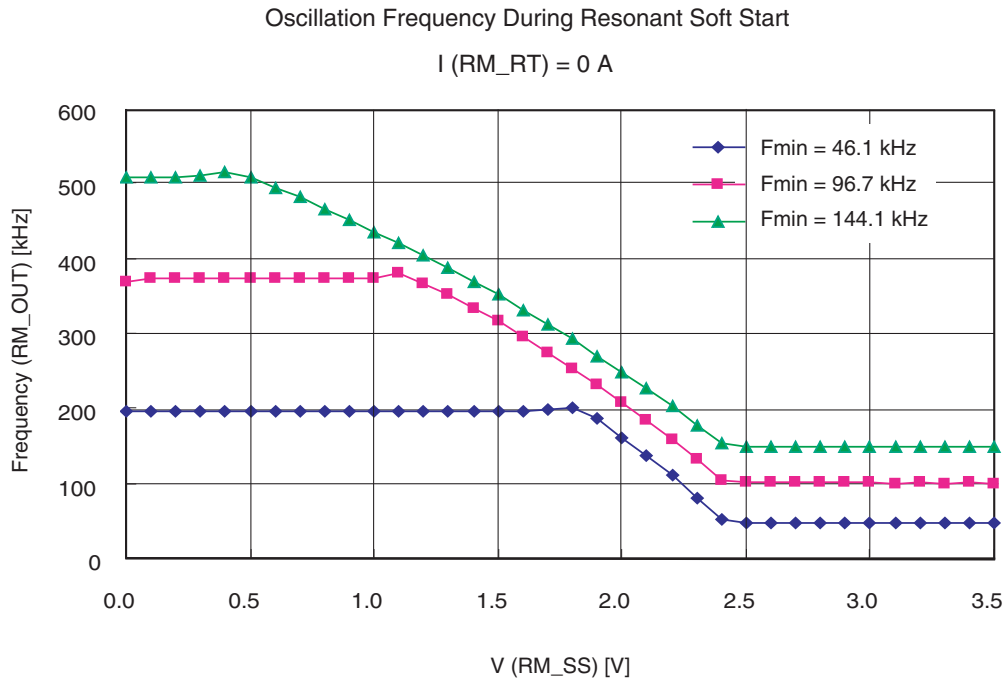


Fig. 8. Oscillation Frequency During Soft Start

5. Overcurrent Detection Circuit

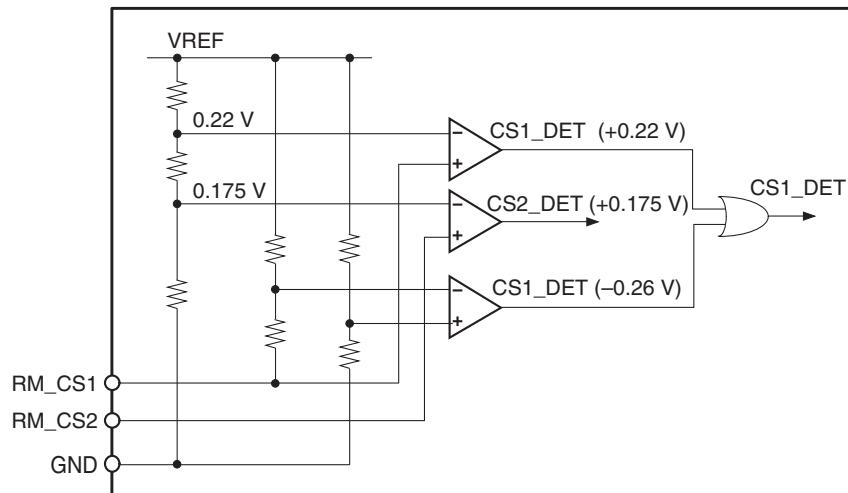


Fig. 9. Equivalent Circuit for Overcurrent Detection Block

Fig. 9 shows the equivalent circuit for resonant overcurrent detection block.

The voltage between the RM_CS and GND pins is monitored, and overcurrents in both the positive (+0.22 V) and negative (-0.26 V) directions are detected according to RM_OUTP and RM_OUTN pin operation. When the PFC output voltage lowers ($PFC_VSENSE < 2.143$ V), the resonant overcurrent threshold voltage is switched to 1.15 times that in normal state both for positive and negative directions; +0.253 V for positive direction and -0.299 V for negative direction.

Operation in overcurrent detection mode is as shown in Fig. 10. When an overcurrent is detected, regardless of positive or negative direction, the output pulse is forcibly turned off by pulse-by-pulse control. In addition, when an overcurrent is detected, the minimum oscillation frequency is controlled to 1.2 times the setting value. Thereafter, the minimum oscillation frequency limit changes in the order of 1.2 times \Rightarrow 1.15 times \Rightarrow 1.1 times \Rightarrow 1.05 times \Rightarrow 1.0 times the setting value with each deadband pulse, and control is performed to return to the original setting frequency with each pulse (4 steps). The minimum oscillation frequency is controlled to 1.2 times the setting value in this manner each time an overcurrent is detected again during the frequency limit period.

In addition, in overcurrent detection mode, the capacitor connected to the RM_SS pin is charged by approximately 5.0 μ A, and when the RM_SS pin voltage reaches 4.0 V (128μ s \times 5 times), the IC is NG latched and the output goes off (both the RM_OUTP and RM_OUTN pins output Low). (Timer latch operation) Approximately 1.0 μ A is constantly discharged from the RM_SS pin to the inside of the IC, so when the overcurrent is canceled partway, the RM_SS pin is discharged until the clamp voltage is reached.

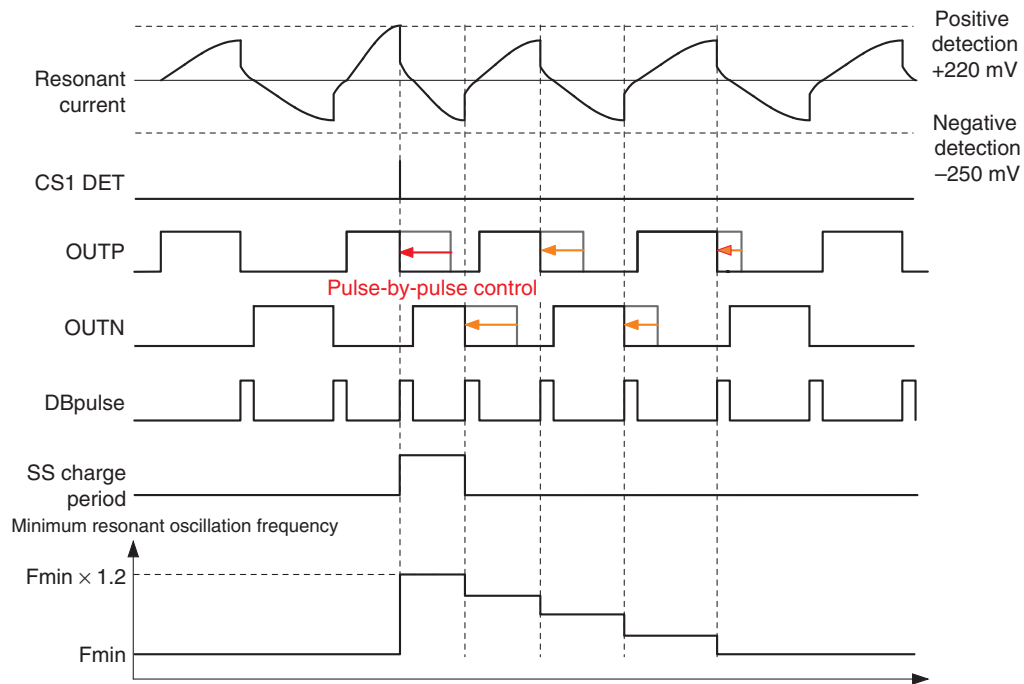


Fig. 10. Operating Waveform in Overcurrent Detection Mode

Fig. 9 also shows the circuit which monitors the voltage between RM_CS2 and GND pins and detects the continuous pulse overcurrent (CS2_DET: +0.175 V detection). Operation in continuous overcurrent detection mode differs from the operation shown in Fig. 10, and instead normal operation continues. When CS2 overcurrent detection continues for approximately 10 s (set up by $2.1 \text{ s} \times 5$ times), NG latch results and the IC forcibly stopped. When CS2 overcurrent is not detected for even one cycle during the approximately 10 s count, the counter is reset. Then, when an overcurrent is detected again, the 10 s counter starts from zero.

6.Operation Stop Voltage Detection Block

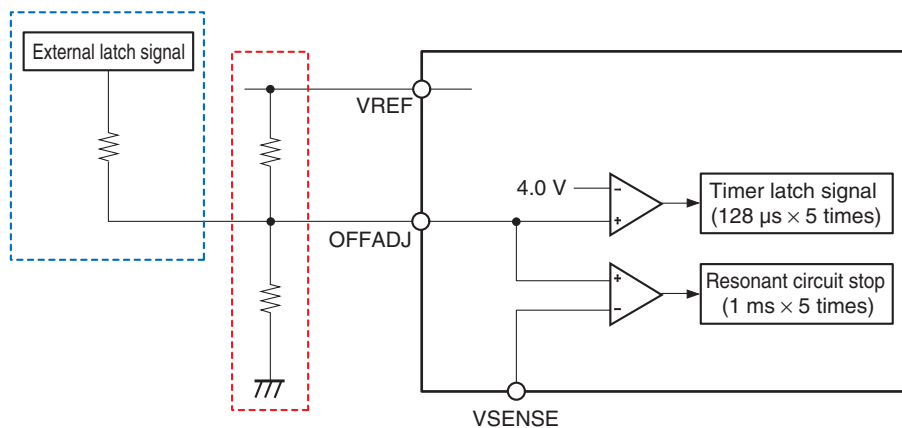


Fig. 11 OFFADJ Pin Internal Equivalent Circuit

Fig. 11 shows the OFFADJ pin internal equivalent circuit.

The operation stop voltage is determined by the OFFADJ pin setting voltage. When the VSENSE pin is set to the voltage lower than the OFFADJ pin voltage, the operation stops. The OFFADJ pin voltage can be set to an arbitrary value by adding the circuit enclosed by the red dotted line shown in Fig. 11.

This pin has an abnormal latch detection function that activates at 4.0 V or more, so the IC can be forcibly set to latch operation using the secondary overvoltage detection or other signal by externally adding the circuit enclosed by the blue dotted line in Fig. 11.

7. NG Latch Operation

◆ CS1 overcurrent timer latch

When $CS1 > 0.22\text{ V}$ or $CS1 < -0.25\text{ V}$ is detected, the RM_SS pin is charged by a charging current of $1.25\text{ }\mu\text{A}$. Latch operation results after $SS > 4.0\text{ V}$ is detected and set up by $128\text{ }\mu\text{s} \times 5$ times.

◆ CS2 continuous overcurrent latch

Latch operation results after $CS2 > 0.175\text{ V}$ is detected continuously and set up by $2.1\text{ s} \times 5$ times.

◆ TSD (IC overheat) latch

Latch operation results immediately after a chip temperature of approximately $140\text{ }^\circ\text{C}$ is detected.

◆ OFFADJ latch

Latch operation results after $OFFADJ > 4.0\text{ V}$ is detected and set up by $128\text{ }\mu\text{s} \times 5$ times.

◆ Other latch

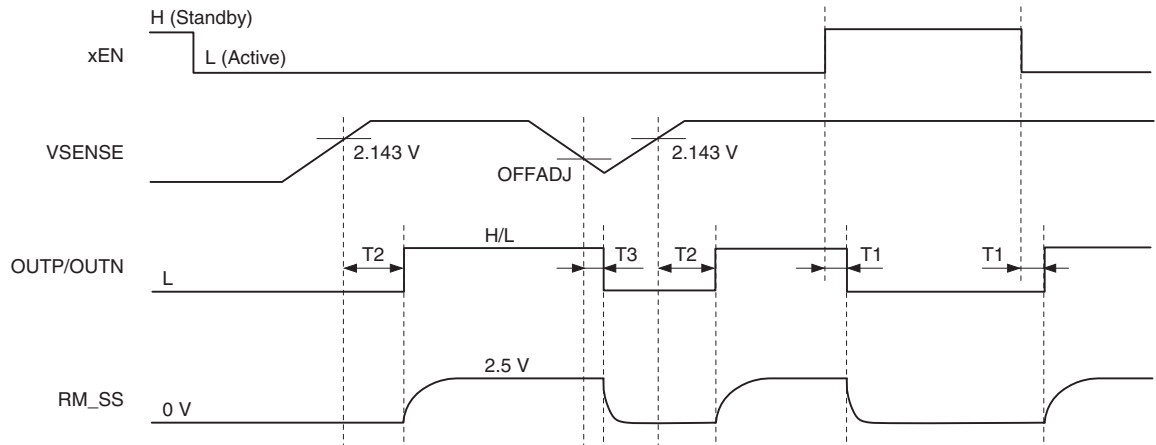
Latch operation results after any of the following operations are detected and set up by $2.1\text{ s} \times 3$ times.

- ◆ VREF_OVLO detection: 5.5 V or more
- ◆ FMIN pin low current: $125\text{ }\mu\text{A}$ or less

Circuit operation stops after NG latch, but the VREF pin continues to output High. NG latch is canceled by transitioning to standby mode.

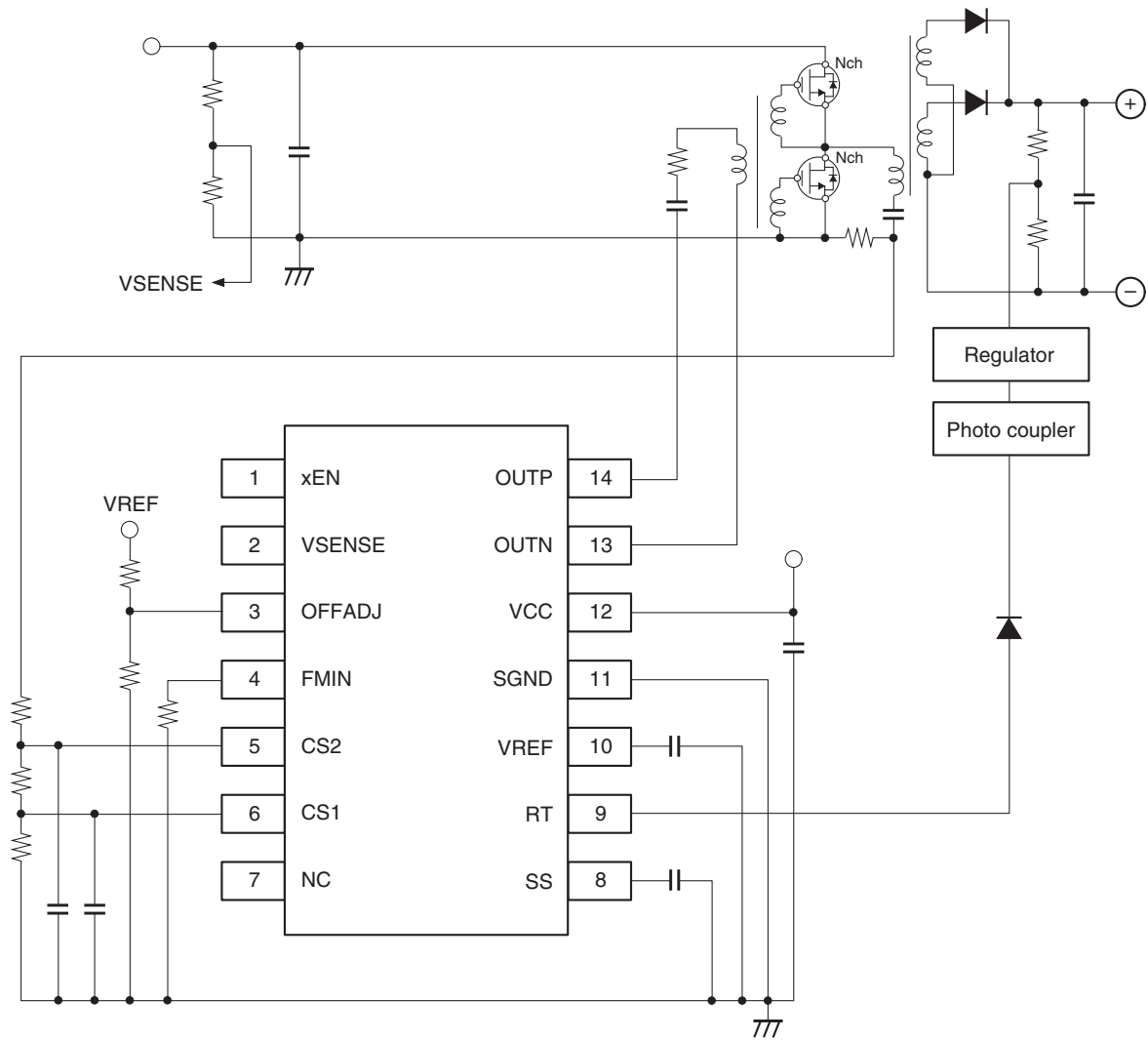
However, during TSD latch the VREF pin outputs Low, and the TSD latch state is canceled only by turning the IC power off and on again, or by detecting VCC UVLO ($VCC < 9.6\text{ V}$).

Timing Chart



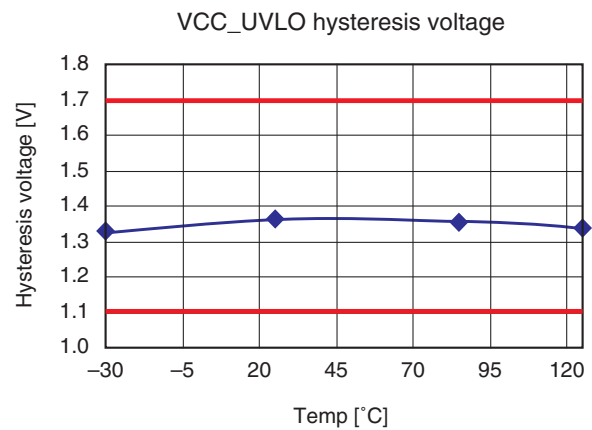
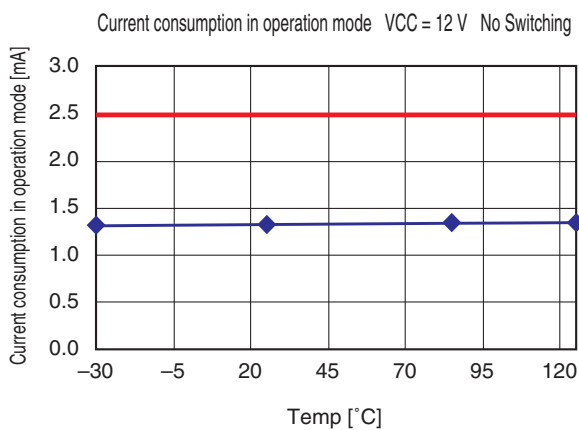
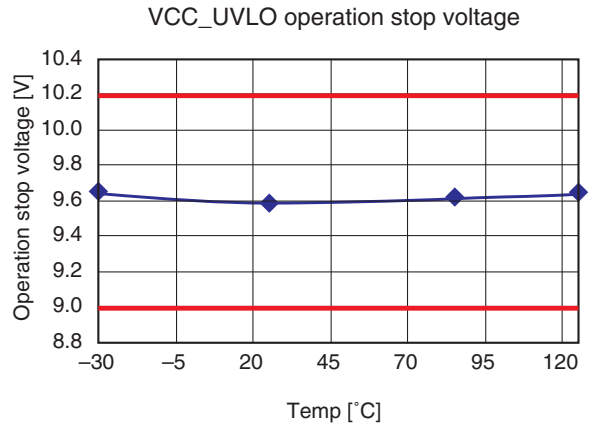
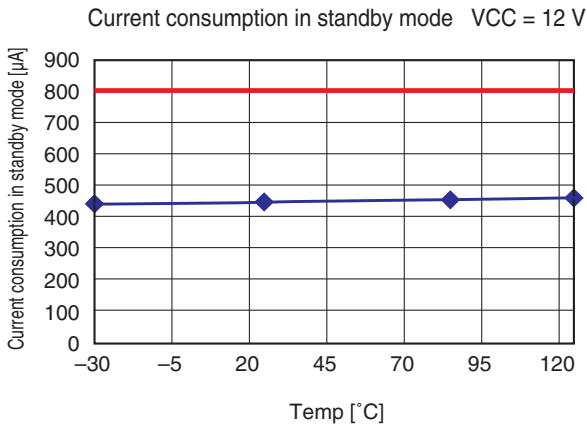
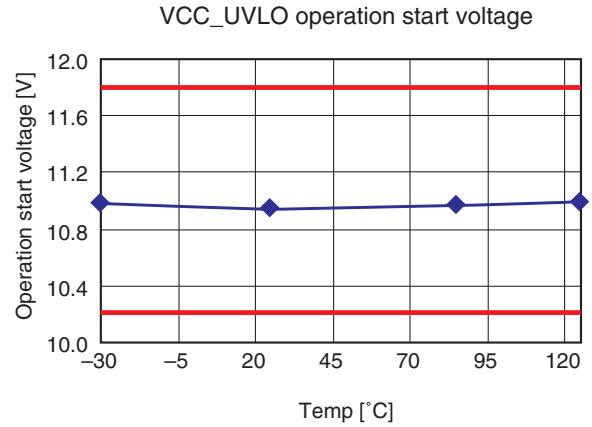
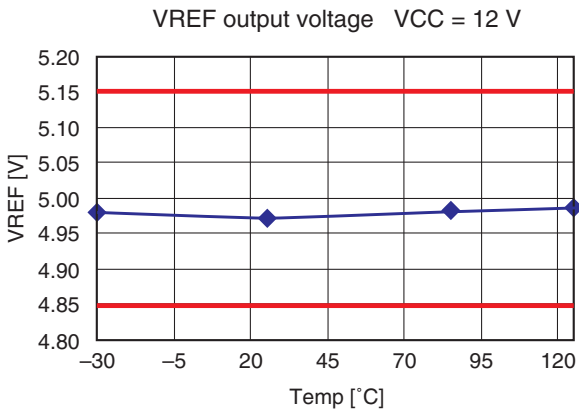
T1: Corresponds to $32 \mu\text{s} \times 3$ times
 T2: Corresponds to $8 \text{ ms} \times 6$ times
 T3: Corresponds to $1 \text{ ms} \times 5$ times

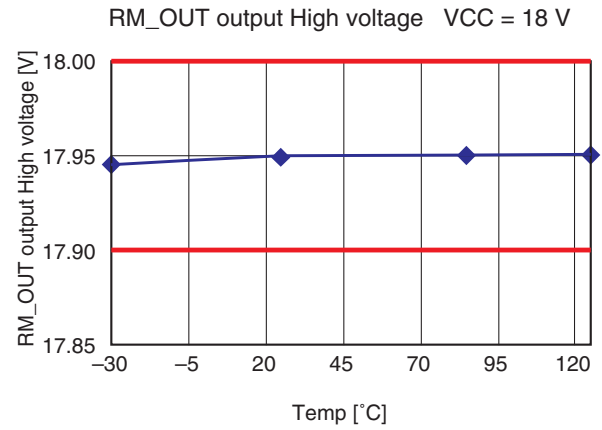
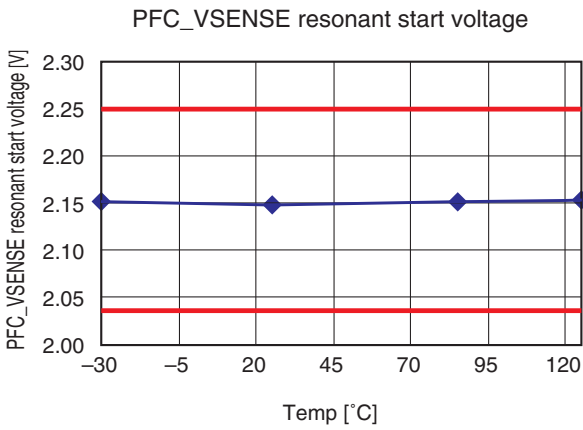
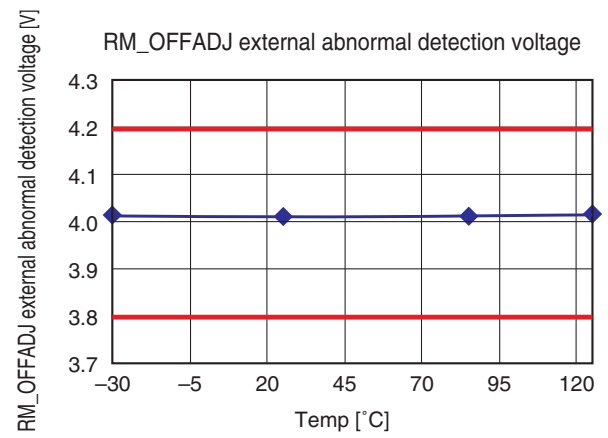
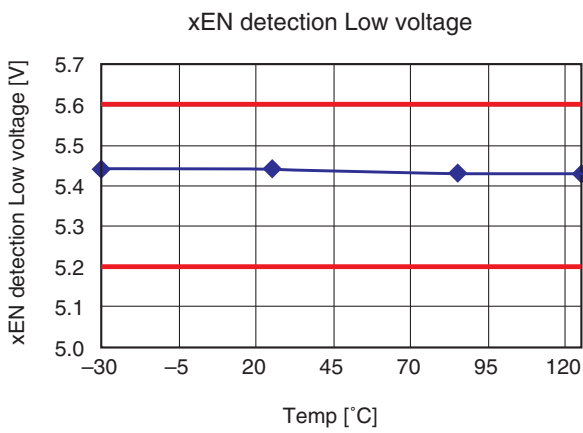
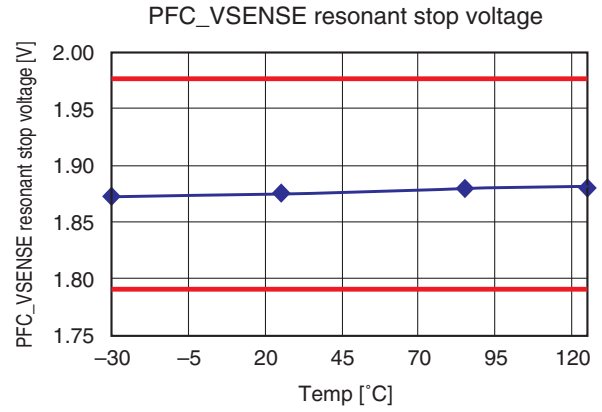
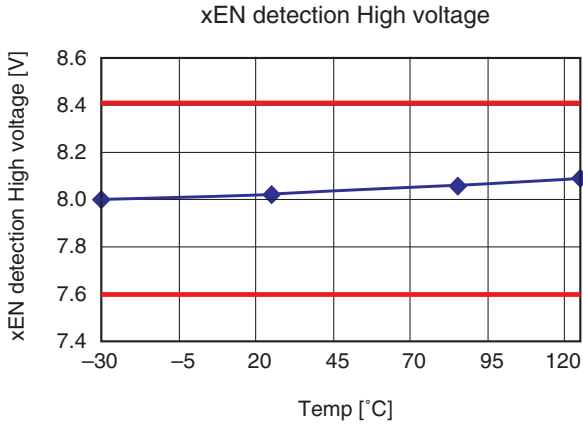
Application Circuit

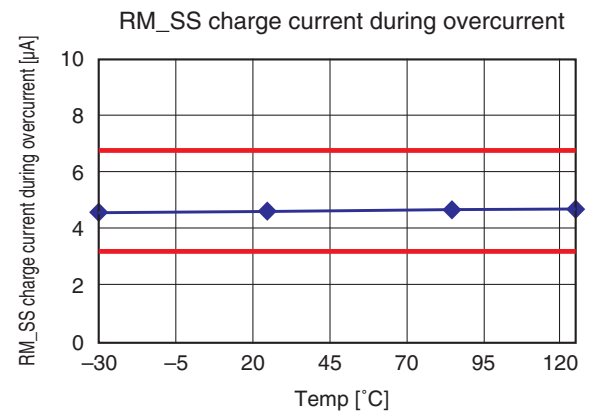
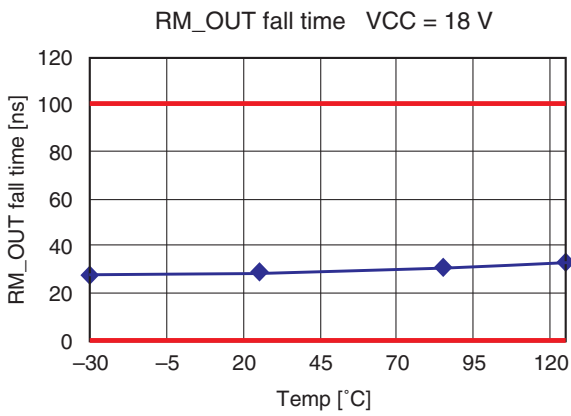
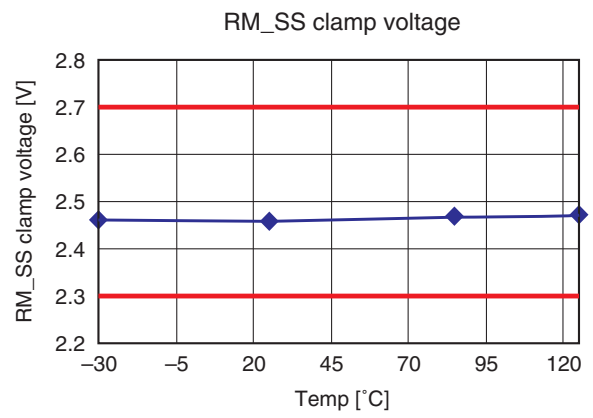
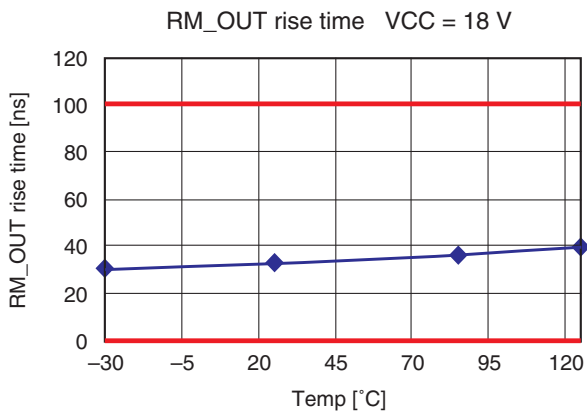
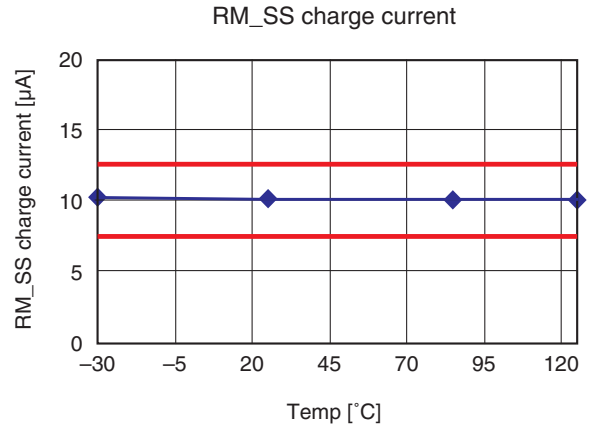
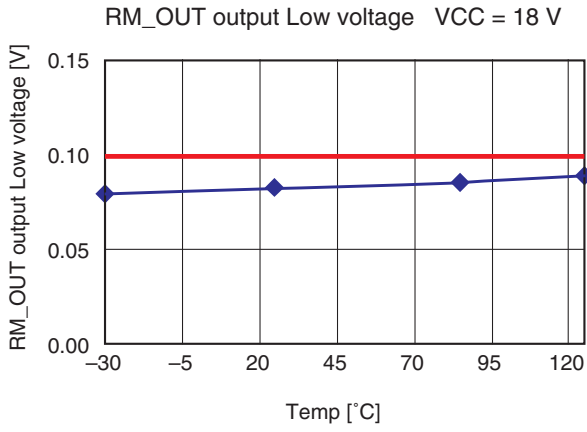


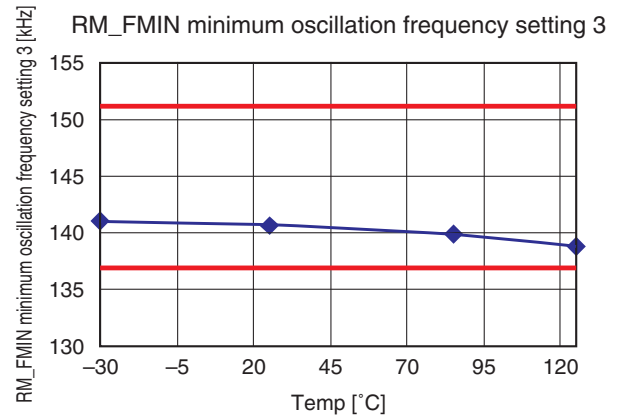
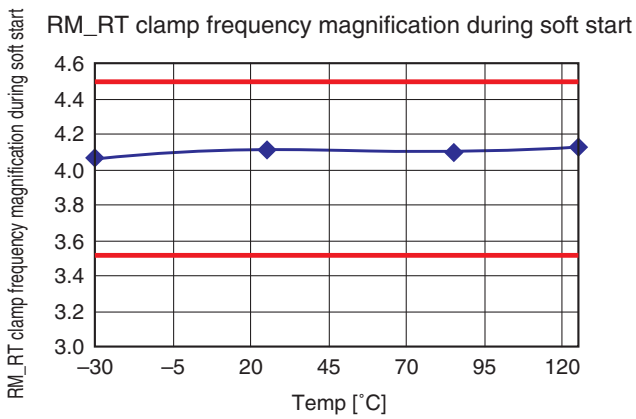
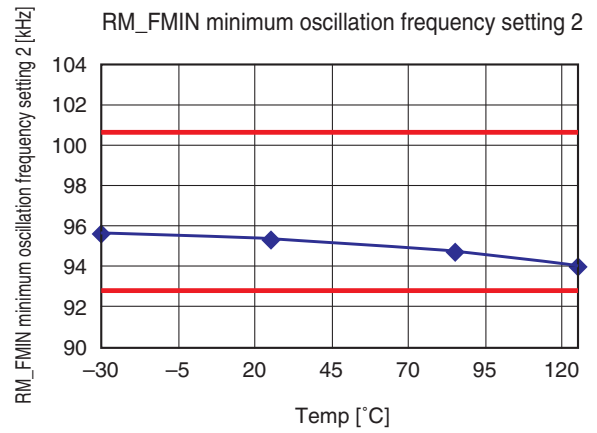
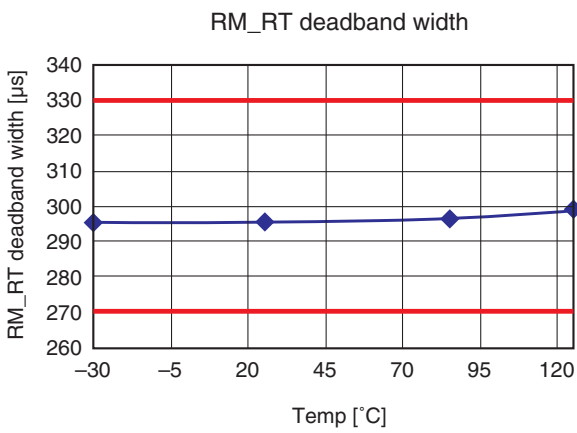
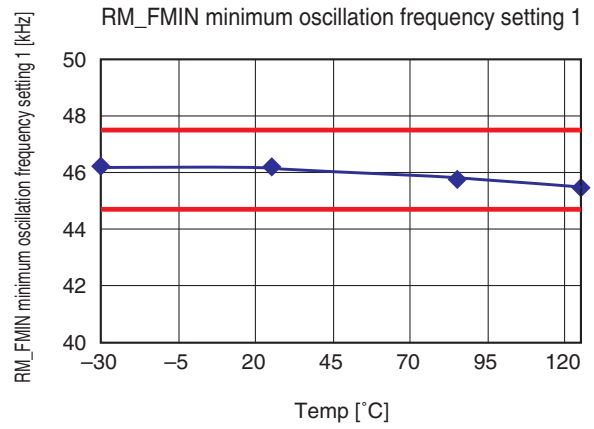
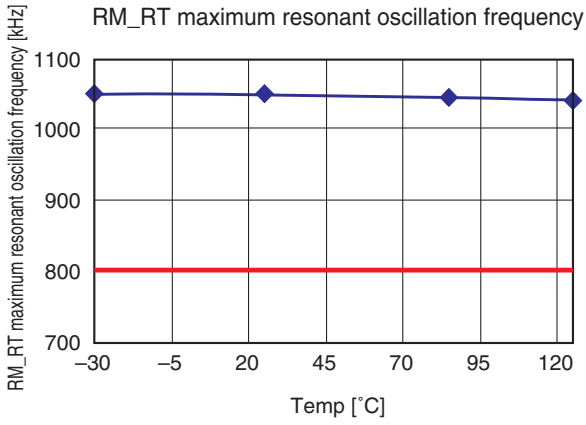
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

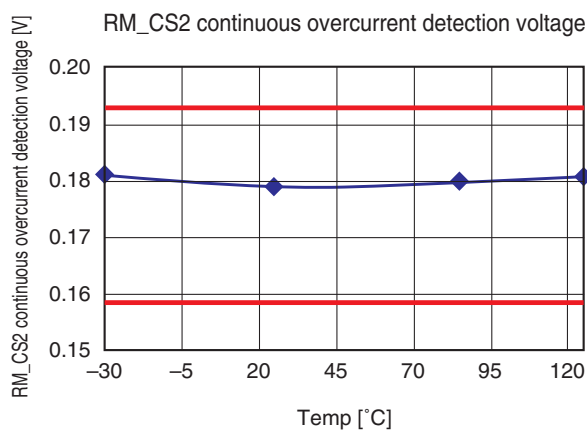
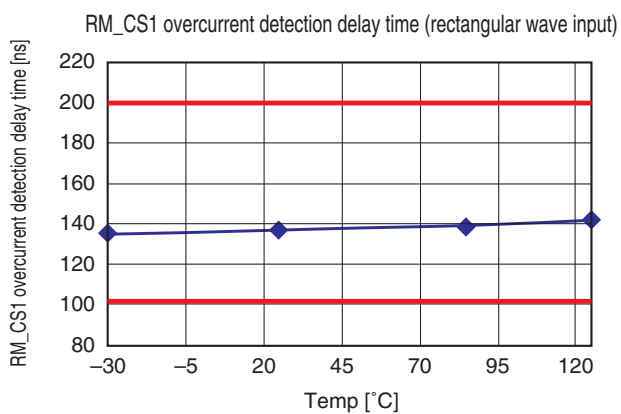
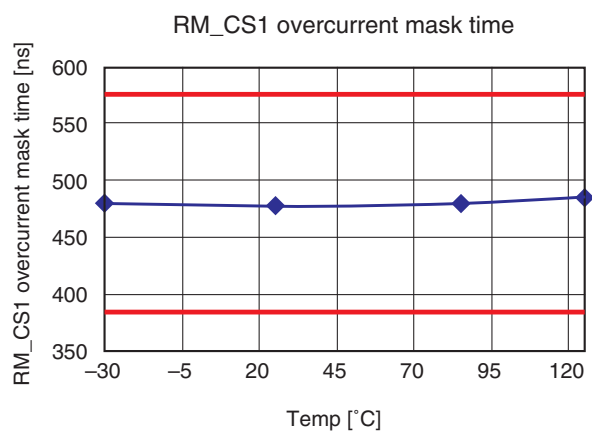
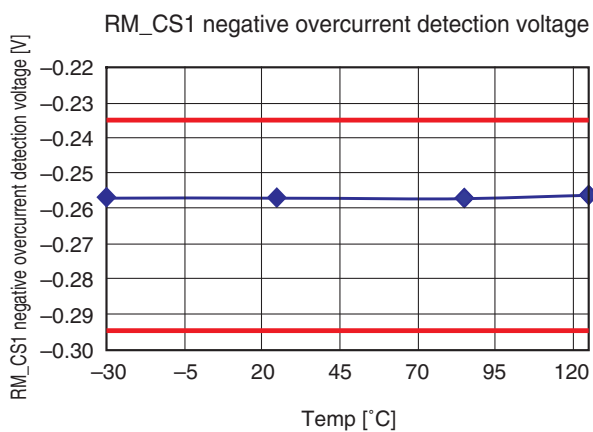
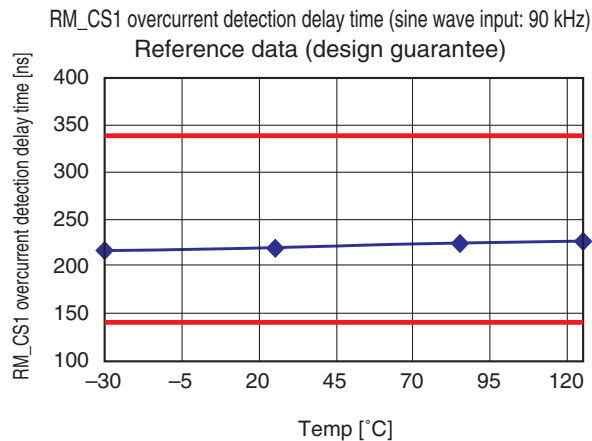
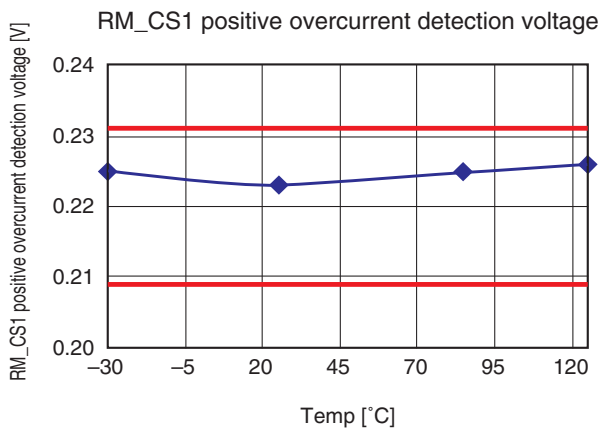
Example of Representative Characteristics

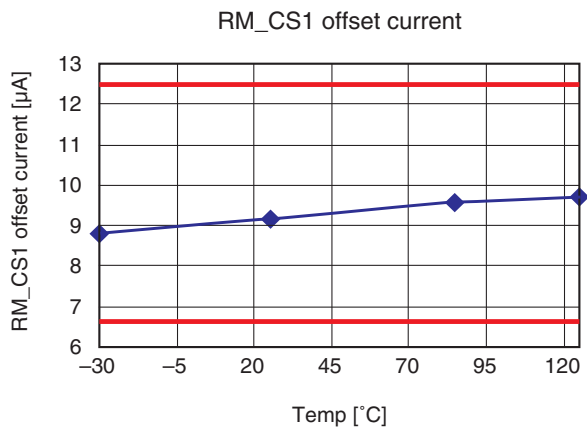










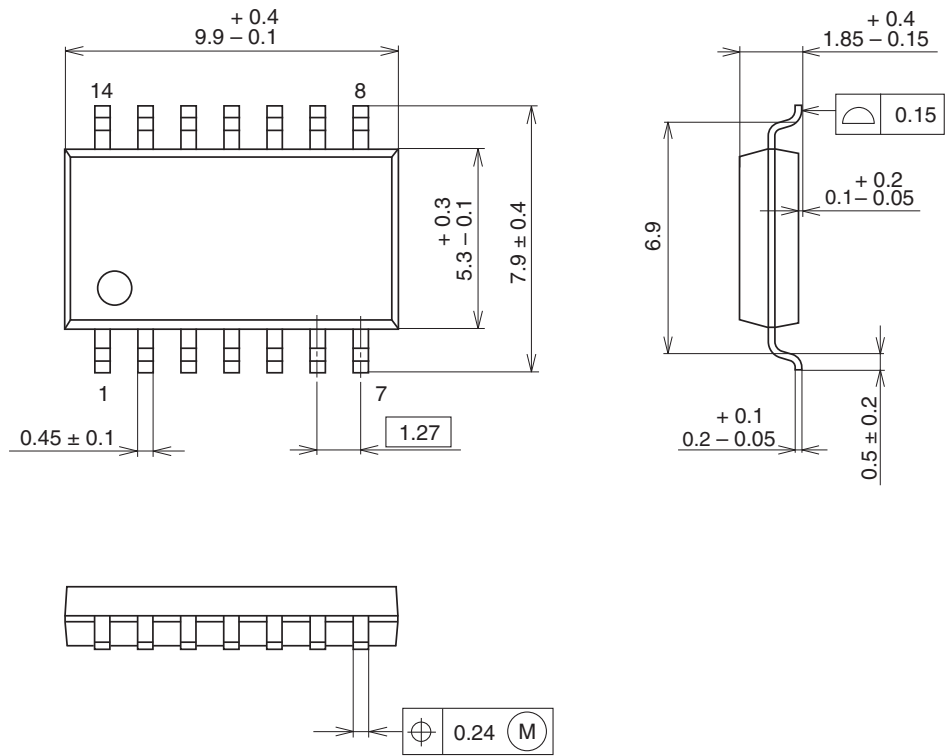


Package Outline

(Unit: mm)

SDT: 875337235

14PIN SOP (PLASTIC)



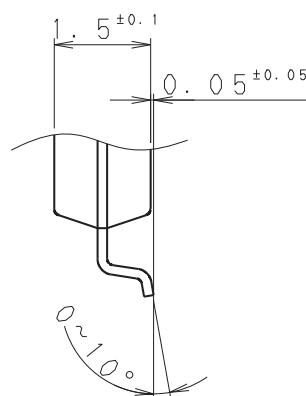
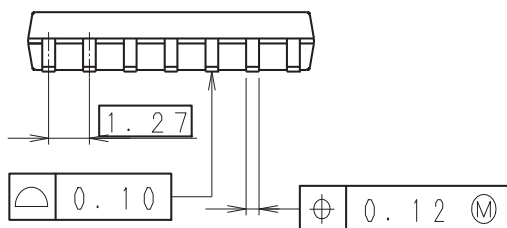
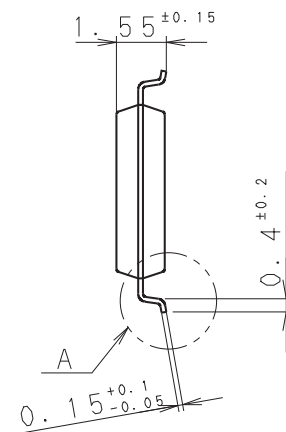
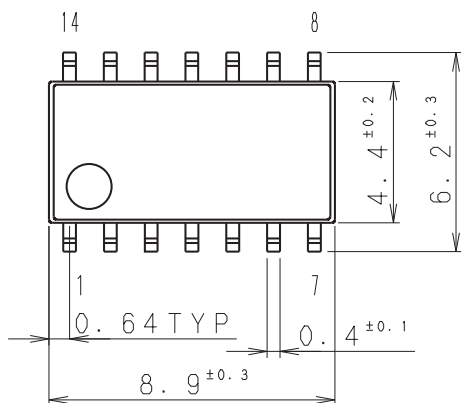
PACKAGE STRUCTURE

SONY CODE	SOP-14P-L01
EIAJ CODE	SOP014-P-0300
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

AOI: 875337236

14 PIN SOP (PLASTIC)



DETAIL A

PACKAGE STRUCTURE

SONY CODE	SOP-14P-L391
JEITA CODE	P-SOP14-8.9X4.4-1.27
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42ALLOY
PACKAGE MASS	0.13g

PART No.	AP-2000-14MAN1	Rev. 0
ISSUED	10.10.05	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR KYUSHU.	
REMARKS	PKG CODE M-14-BAN	