SONY

Audio Driver

CXA3815N

Description

Audio IC for LCD-TVs

Features

- ◆ Operating voltage V_{CC} = 3.0 to 3.6V
- ◆ Differential input
- ◆ Output decoupling capacitor less
- ◆ Gain switching function (6dB／12dB)
- ◆ Mute function

Structure

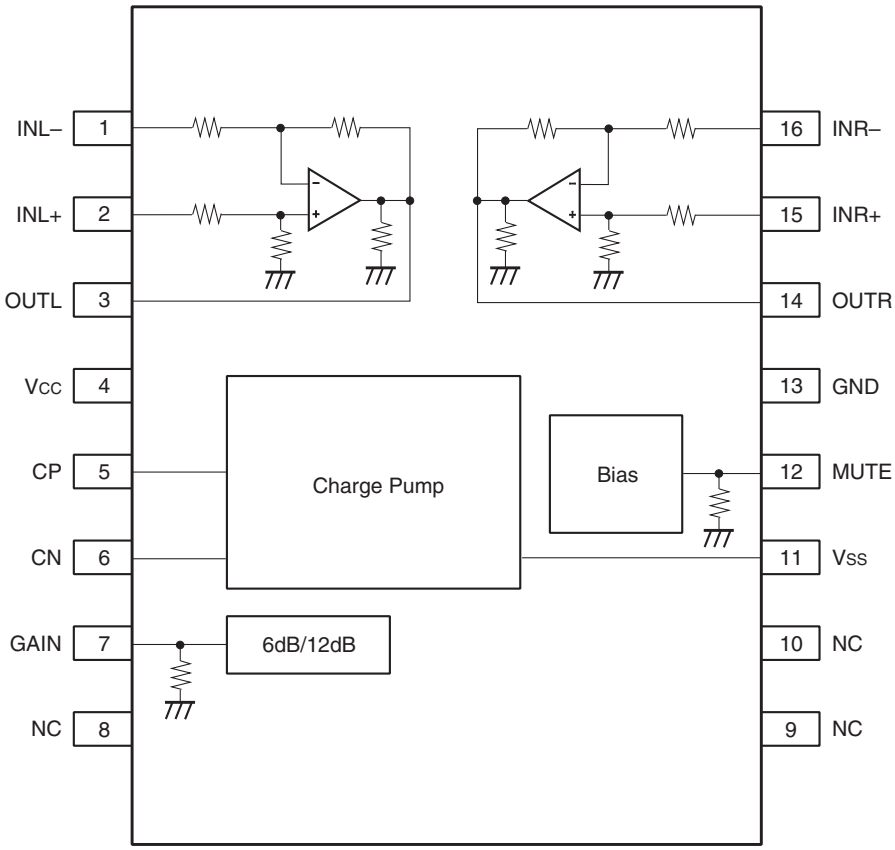
BiCMOS monolithic IC

Package

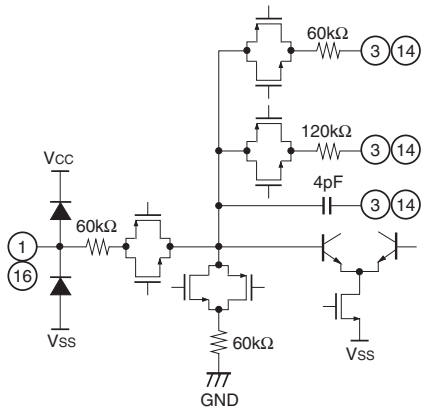
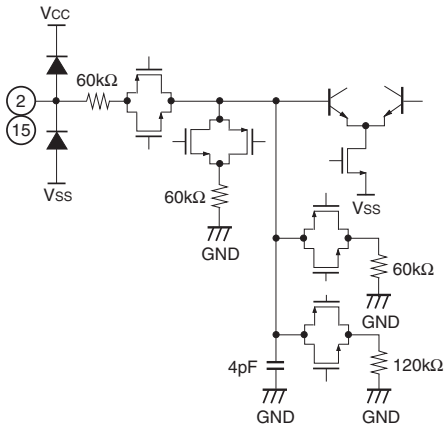
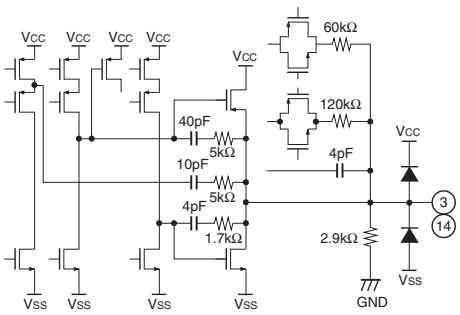
SSOP-16P

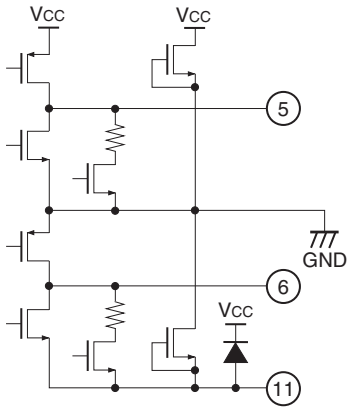
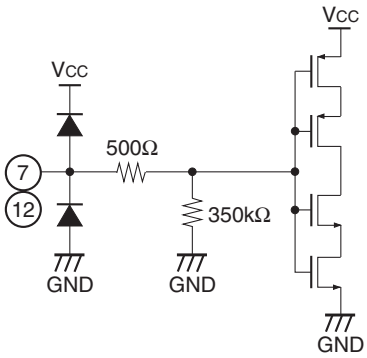
E10718B23

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Pin voltage [V]		Equivalent circuit	Description
			DC	AC		
1	INL–	I	0	—		HP AMP_L input (–)
16	INR–	I	0	—		HP AMP_R input (–)
2	INL+	I	0	—		HP AMP_L input (+)
15	INR+	I	0	—		HP AMP_R input (+)
3	OUTL	O	0	—		HP AMP_L output
14	OUTR	O	0	—		HP AMP_R output

Pin No.	Symbol	I/O	Pin voltage [V]		Equivalent circuit	Description
			DC	AC		
5	CP	I/O	—	3.3		CP capacitance connection
6	CN	I/O	—	–3.3		CP capacitance connection
11	Vss	I/O	–3.26	—		Vss
7	GAIN	I	0	—		Gain switching
12	MUTE	I	0	—		Mute switching
4	Vcc	I/O	—	—		Vcc
13	GND	I/O	—	—		GND

Electrical Characteristics

Unless otherwise specified
(Vcc = 3.3V, Ta = 25℃, fsignal = 1kHz, differential input, Measurement band width = 20Hz to 20kHz)

Power

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Vcc		3.0	3.3	3.6	V
Maximum rating	Vmax		—	—	4.5	V
Operating temperature	Ta		–25	—	+85	℃

Amplifier Block

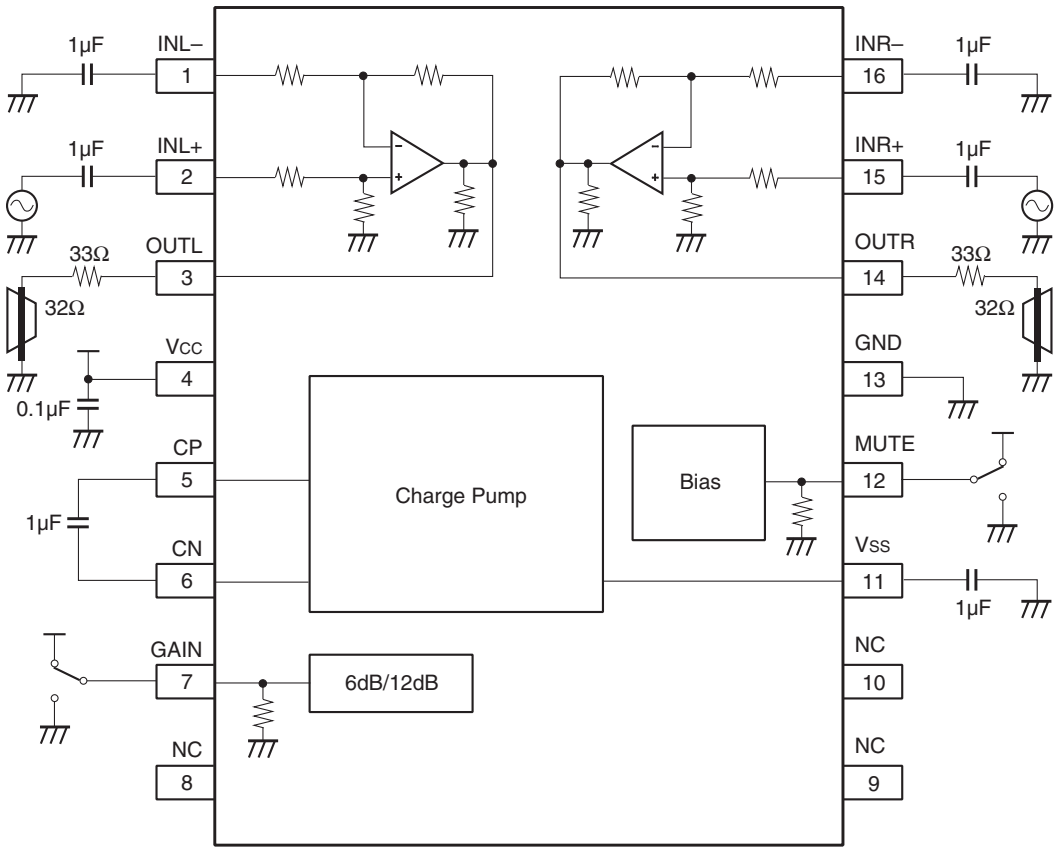
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input impedance	Rin		96	120	144	kΩ
Gain1	Gv1	GAIN Low, 0.1Vrms input	5.5	6	6.5	dB
Gain2	Gv2	GAIN High, 0.1Vrms input	11.5	12	12.5	dB
Total harmonic distortion 1	THD1	RL = 33 + 32Ω GAIN Low, 0.1Vrms input	—	0.01	0.1	%
Total harmonic distortion 2	THD2	RL = 33 + 32Ω, Po = 15mW GAIN Low	—	—	0.5	%
Total harmonic distortion 3	THD3	RL = 470 + 10kΩ, Vo = 2.0Vrms GAIN Low	—	—	1	%
Output noise level	Vno	No signal input, measured at 32Ω ends	—	–100	–95	dBv
Channel separation	CS	RL = 33 + 32Ω, Po = 15mW 1kHz BPF, GAIN Low	70	80	—	dB
DC offset	Vos	No signal input, GAIN Low	–5	—	5	mV
Mute level	Vmute	RL = 33 + 32Ω, Po = 15mW GAIN Low, MUTE ON	—	–70	–60	dB

Control Block

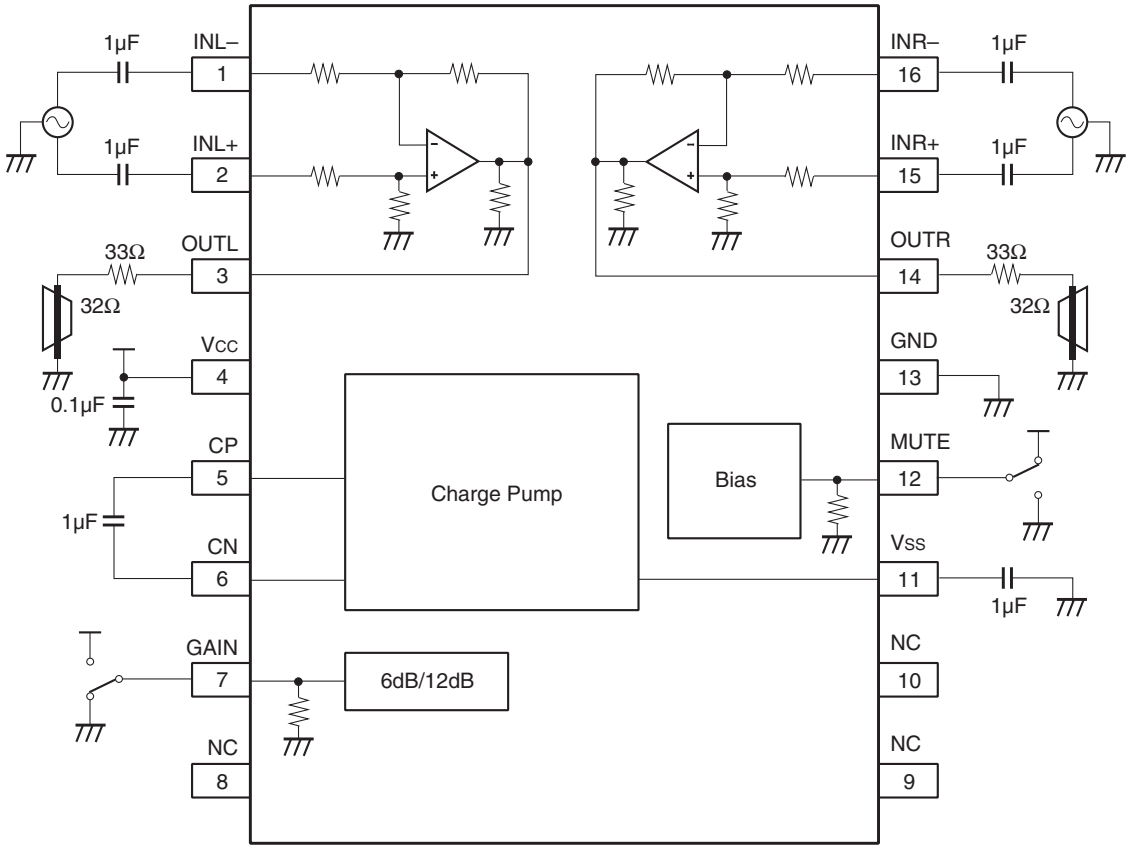
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Mute H	MuteH	Mute = OFF	0.7Vcc	—	Vcc	V
Mute L	MuteL	Mute = ON	0	—	0.8	V
Gain H	GainH	Gain = 12dB	0.7Vcc	—	Vcc	V
Gain L	GainL	Gain = 6dB	0	—	0.8	V

Application Circuit

Single Input



Differential Input



Notes On Handling

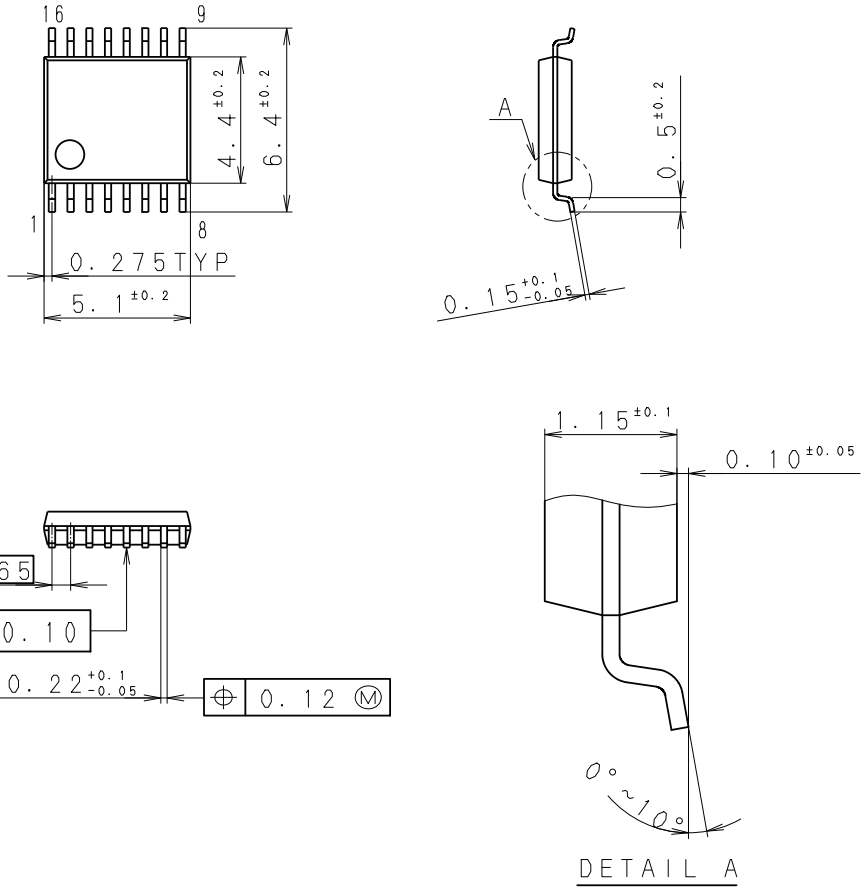
- The capacitor between CP and CN pin and connected to Vss pin are for generating negative voltage.Place these capacitors with the shortest wiring to the pins.
- The capacitor connected to Vcc pin is for smoothing noise.Place this capacitor with the shortest wiring to the pin.

Package Outline

(Unit : mm)

Product Code: 75340635/75341217

16PIN SSOP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SSOP-16P-L391
JEITA CODE	P-SSOP16-5.1X4.4-0.65
JEDEC CODE	————

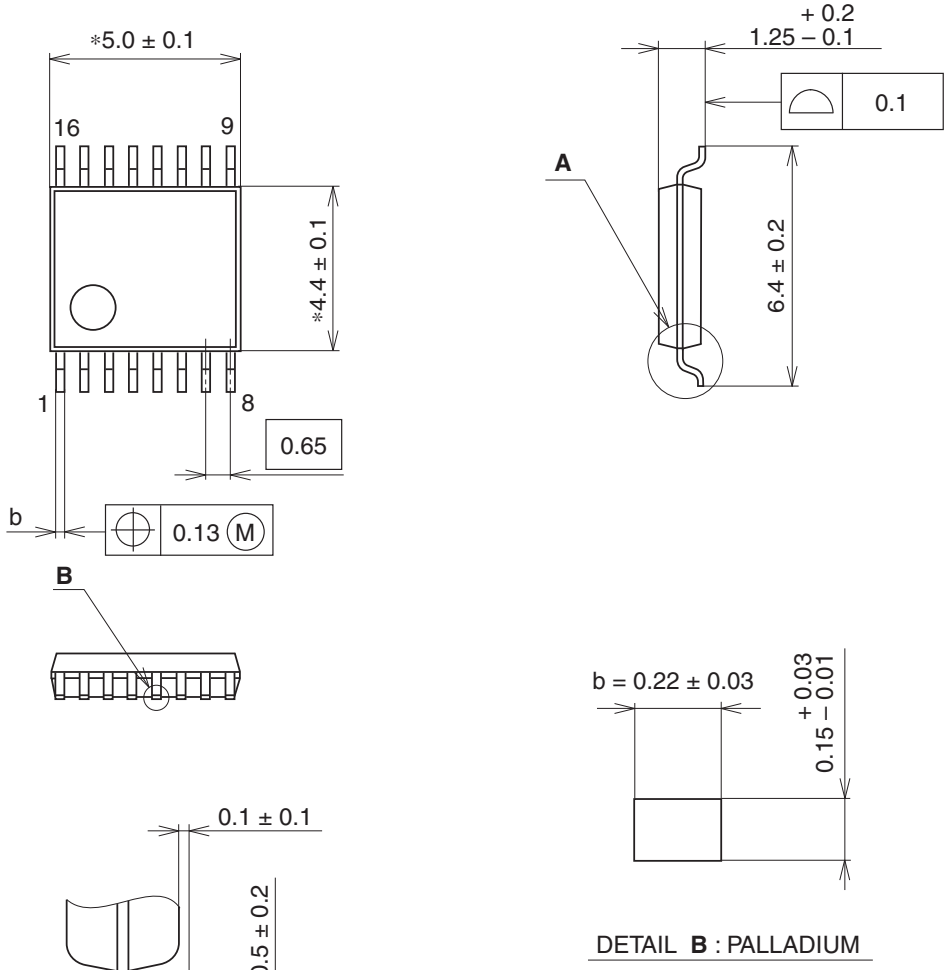
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g

PART No. AP-2000-16MAN1	Rev. 1
ISSUED 11.11.22	REVISED 11.12.28
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CODE N-16-AAN	

(Unit : mm)

Product Code: 75336351

16PIN SSOP (PLASTIC)



DETAIL **B** : PALLADIUM

DETAIL **A**

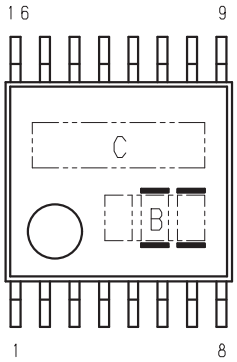
NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-16P-L01
EIAJ CODE	P-SSOP16-4.4x5.0-0.65
JEDEC CODE	————

PACKAGE STRUCTURE

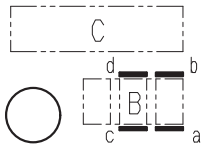
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g

Marking



MARKING C: A3815

注1） B部はロット番号（Ｍａｘ３文字で通し記号）を配置する。
（規定文字数未満につき省略は省略規定に従う。
製造年は下記２進法ビット方式により表示する。）
ａ部年コード（２進法ビット方式の１ビット目を表示）を配置する。
ｂ部年コード（２進法ビット方式の２ビット目を表示）を配置する。
ｃ部年コード（２進法ビット方式の３ビット目を表示）を配置する。
ｄ部年コード（２進法ビット方式の４ビット目を表示）を配置する。
注2） C部は製品名（Ｍａｘ５文字）を配置する。
（５文字を超える場合は製品名省略標示規定に従う。）



DETAIL B

< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
(FOLLOW RULES FOR ABBREVIATIONS.
MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)
A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEN IS DISPLAYED IN 1 DOT)IN SECTION a.
A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEN IS DISPLAYED IN 1 DOT)IN SECTION b.
A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEN IS DISPLAYED IN 1 DOT)IN SECTION c.
A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEN IS DISPLAYED IN 1 DOT)IN SECTION d.
2) TYPE NO.(MAX 5 CHARACTERS) IN SECTION C.
(FOR MORE THAN 5 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)