

## Sync Signal Generator for Camera

### Description

The CXD1159AQ is a sync signal generator for consumer video cameras.

### Features

- Adapts to NTSC or PAL through mode switching
- Low power consumption
- Phase comparator and built-in inverter for active filter (Power supply according to inverter for filter)
- Supports external synchronization

### Structure

Silicon gate CMOS

### Application

Video cameras

### Functions

Generation of various sync signals

### Absolute Maximum Ratings (Ta = 25°C)

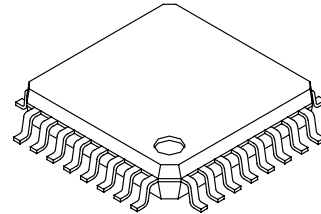
|                       |                  |   |    |
|-----------------------|------------------|---|----|
| • Supply voltage      | V <sub>DD</sub>  | V <sub>SS</sub> *1 – 0.5 to +7.0                  | V  |
| • Input voltage       | V <sub>I</sub>   | V <sub>SS</sub> *1 – 0.5 to V <sub>DD</sub> + 0.5 | V  |
| • Output voltage      | V <sub>O</sub>   | V <sub>SS</sub> *1 – 0.5 to V <sub>DD</sub> + 0.5 | V  |
| • Storage temperature | T <sub>stg</sub> | –55 to +150                                       | °C |

\*1 V<sub>SS</sub> = 0V

### Recommended Operating Conditions

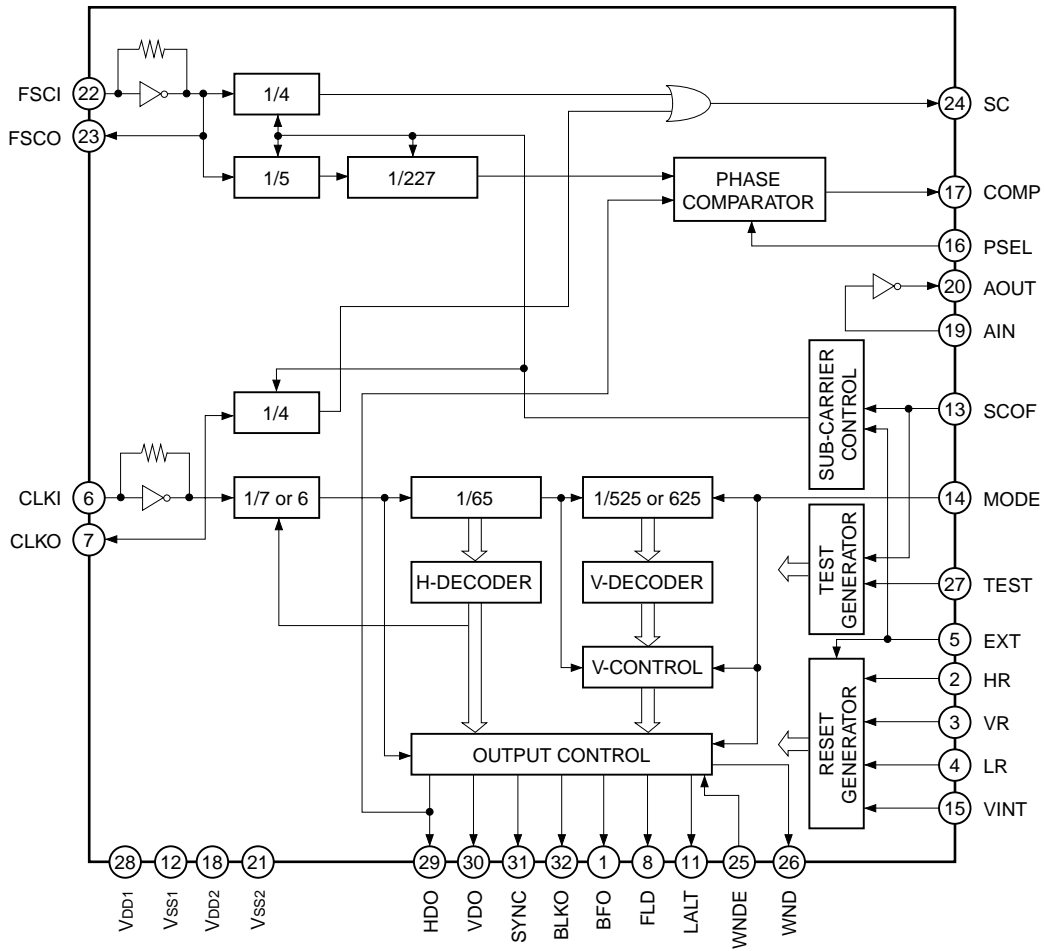
|                         |                  |              |    |
|-------------------------|------------------|--------------|----|
| • Supply voltage        | V <sub>DD</sub>  | 4.50 to 5.50 | V  |
| • Operating temperature | T <sub>opr</sub> | –20 to +75   | °C |

32 pin QFP (Plastic)

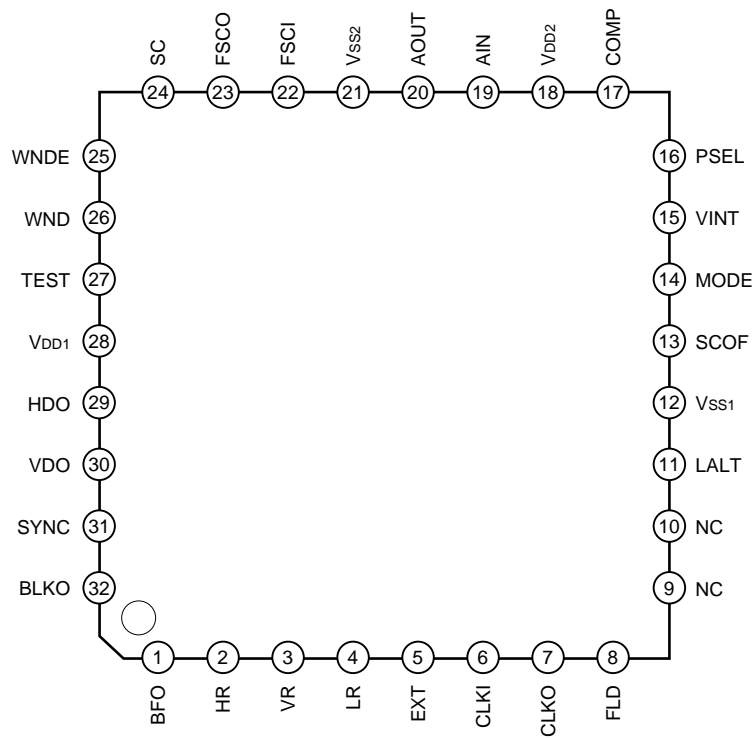


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Block Diagram



Pin Configuration



## Pin Description

| Pin No. | Symbol           | I/O | Description   |
|---------|------------------|-----|---|
| 1       | BFO              | O   | Burst flag pulse  |
| 2       | HR               | I   | H reset input   |
| 3       | VR               | I   | V reset input   |
| 4       | LR               | I   | LALT reset input  |
| 5       | EXT              | I   | Internal/External mode switching $\overline{\text{INT}}/\text{EXT}$ |
| 6       | CLKI             | I   | Clock input (NTSC: 14.31818MHz, PAL: 14.1875MHz)                    |
| 7       | CLKO             | O   | Clock output  |
| 8       | FLD              | O   | Field pulse   |
| 9       | NC               | —   |   |
| 10      | NC               | —   |   |
| 11      | LALT             | O   | Line alternate pulse  |
| 12      | V <sub>SS1</sub> | —   | GND   |
| 13      | SCOF             | I   | Sub carrier suppress input L: OFF                                   |
| 14      | MODE             | I   | NTSC/PAL mode switching $\overline{\text{NTSC}}/\text{PAL}$         |
| 15      | VINT             | I   | Initialize input  |
| 16      | PSEL             | I   | Phase comparator polarity switch                                    |
| 17      | COMP             | O   | Phase comparator output   |
| 18      | V <sub>DD2</sub> | —   | Filter inverter +5V   |
| 19      | AIN              | I   | Filter inverter input   |
| 20      | AOUT             | O   | Filter inverter output  |
| 21      | V <sub>SS2</sub> | —   | Filter inverter GND   |
| 22      | FSCI             | I   | 4fsc clock input  |
| 23      | FSCO             | O   | 4fsc clock output   |
| 24      | SC               | O   | Sub carrier output  |
| 25      | WNDE             | I   | WND output enable input (at L: Enable)                              |
| 26      | WND              | O   | Window output   |
| 27      | TEST             | I   | Test input (Normally "L")   |
| 28      | V <sub>DD1</sub> | —   | +5V   |
| 29      | HDO              | O   | Horizontal drive pulse  |
| 30      | VDO              | O   | Vertical drive pulse  |
| 31      | SYNC             | O   | Composite sync pulse  |
| 32      | BLKO             | O   | Composite blanking pulse  |

## Electrical Characteristics

### DC Characteristics

( $V_{DD} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_{opr} = -20$  to  $+75^{\circ}C$ )

| Item                 | Symbol     | Conditions             | Min.              | Typ.           | Max.        | Unit    |
|----------------------|------------|------------------------|-------------------|----------------|-------------|---------|
| Supply current       | $I_{DD}$   |                        |                   | 4.5            |             | mA      |
|                      | $I_{DDs}$  | Static state*1         | 0                 |                | 0.1         | mA      |
| Output voltage I*2   | High level | $V_{OH}$               | $I_{OH} = -2mA$   | $V_{DD} - 0.8$ |             | V       |
|                      | Low level  | $V_{OL}$               | $I_{OL} = 4mA$    | $V_{SS}$       | 0.4         | V       |
| Output voltage II*3  | High level | $V_{OH}$               | $I_{OH} = -1.5mA$ | $V_{DD}/2$     |             | V       |
|                      | Low level  | $V_{OL}$               | $I_{OL} = 1.5mA$  | $V_{SS}$       | $V_{DD}/2$  | V       |
| Input voltage        | High level | $V_{IH}$               |                   | $0.7V_{DD}$    |             | V       |
|                      | Low level  | $V_{IL}$               |                   |                | $0.3V_{DD}$ | V       |
| Input leak current   | $I_{LI}$   | $V_I = 0V$ to $V_{DD}$ | -10               |                | 10          | $\mu A$ |
| Input leak current*4 | $I_{LZ}$   |                        | -10               |                | 10          | $\mu A$ |

\*1  $V_{IH} = V_{DD}$ ,  $V_{IL} = V_{SS}$

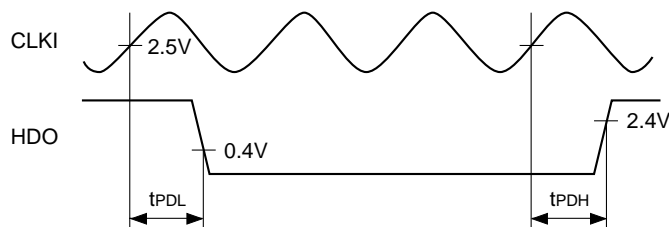
\*2 Output pins except "AOUT"

\*3 "AOUT" pin

\*4 Tri-state pin

### AC Characteristics

| Item            | Symbol    | Conditions      | Min. | Typ. | Max. | Unit |
|-----------------|-----------|-----------------|------|------|------|------|
| Fall delay time | $t_{PDL}$ | $V_{OL} = 0.4V$ |      |      | 45   | ns   |
| Rise delay time | $t_{PDH}$ | $V_{OH} = 2.4V$ |      |      | 45   | ns   |



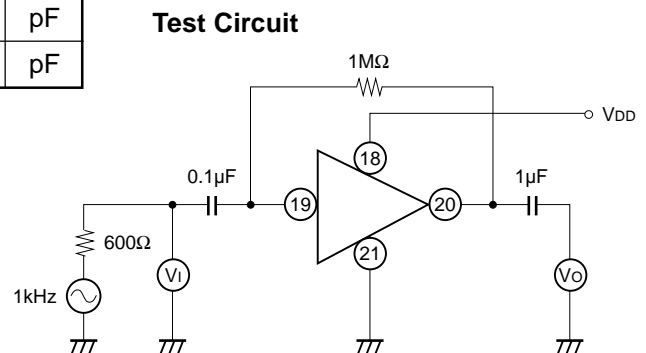
### I/O Capacitance

| Item       | Symbol    | Min. | Typ. | Max. | Unit |
|------------|-----------|------|------|------|------|
| Input pin  | $C_{IN}$  |      |      | 9    | pF   |
| Output pin | $C_{OUT}$ |      |      | 11   | pF   |

Test conditions:  $V_{DD} = V_I = 0V$ ,  $f_M = 1MHz$

### Filter Amplifier Characteristics

Voltage gain  $G_v$  25dB (Typ.)



$$G_v = 20 \log \frac{V_O}{V_I}$$

## Functions

### 1. Generation of various sync signals (See the Timing Chart.)

Various sync signals are generated from clocks.

- Clock frequencies

NTSC:  $910f_H$  (14.31818MHz)

PAL:  $908f_H$  (14.1875MHz)

$4f_{sc}$  (17.734475MHz)

For the system clock

NTSC:  $910f_H/7$

PAL:  $908f_H/7$  or 6

### 2. PAL PLL for $4f_{sc}$

To the master clock of  $908f_H$  is matched a phase of  $4f_{sc}$ . The polarity of the phase comparator can be switched according to the type of external filter (passive or active).

| Filter  | PSEL | Master<br>( $908f_H$ ) | $4f_{sc}$ | COMP |
|---------|------|------------------------|-----------|------|
| Passive | L    | Fast                   | Delay     | H    |
|         |      | Slow                   | Fast      | L    |
| Active  | H    | Fast                   | Delay     | L    |
|         |      | Slow                   | Fast      | H    |

### 3. SC (Sub-Carrier) generation

| Mode | INT or EXT | SC          |
|------|------------|-------------|
| NTSC | INT        | $910f_H/4$  |
| NTSC | EXT        | $4f_{sc}/4$ |
| PAL  | x          | $4f_{sc}/4$ |

INT: Internal mode

(EXT = L)

EXT: External mode

(EXT = H)

In either mode unused counters are stopped. When SC is not required, by setting SCOF to L all SC counters are stopped and SC is not output.

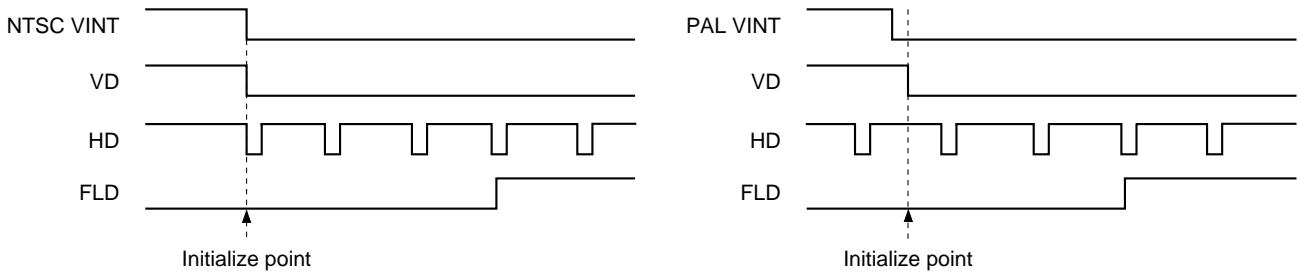
### 4. Initialization and Reset

In INT mode the circuit is initialized with the fall of VINT. At that time, H, V and LALT resets are not accepted.

In EXT mode, VINT is not accepted, whereas H, V and LALT resets are accepted.

• **Initialize (VINT)**

When EXT = L, VINT fall is detected and operation is started as the circuit is initialized at the VD fall position just before field I. (Initialization is completed within 100ns after the fall is detected).

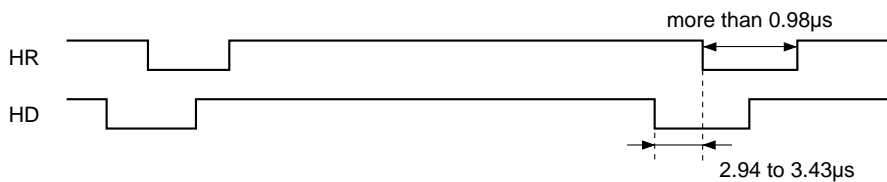


• **H reset (HR)**

Reset is performed with the first fall. However reset is not done anymore unless there is a deviation of more than 2 clocks (0.98μs) to the subsequent edges.

The minimum reset pulse width is 0.98μs.

HD is reset 2.94 to 3.43μs in advance of HR input.



• **V reset (VR)**

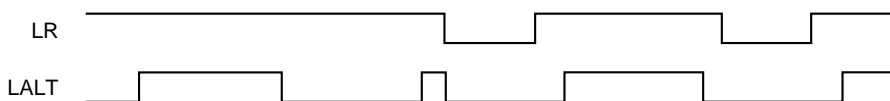
VD is reset 3.5H in advance of VR input.

The minimum reset pulse width is 32μs.

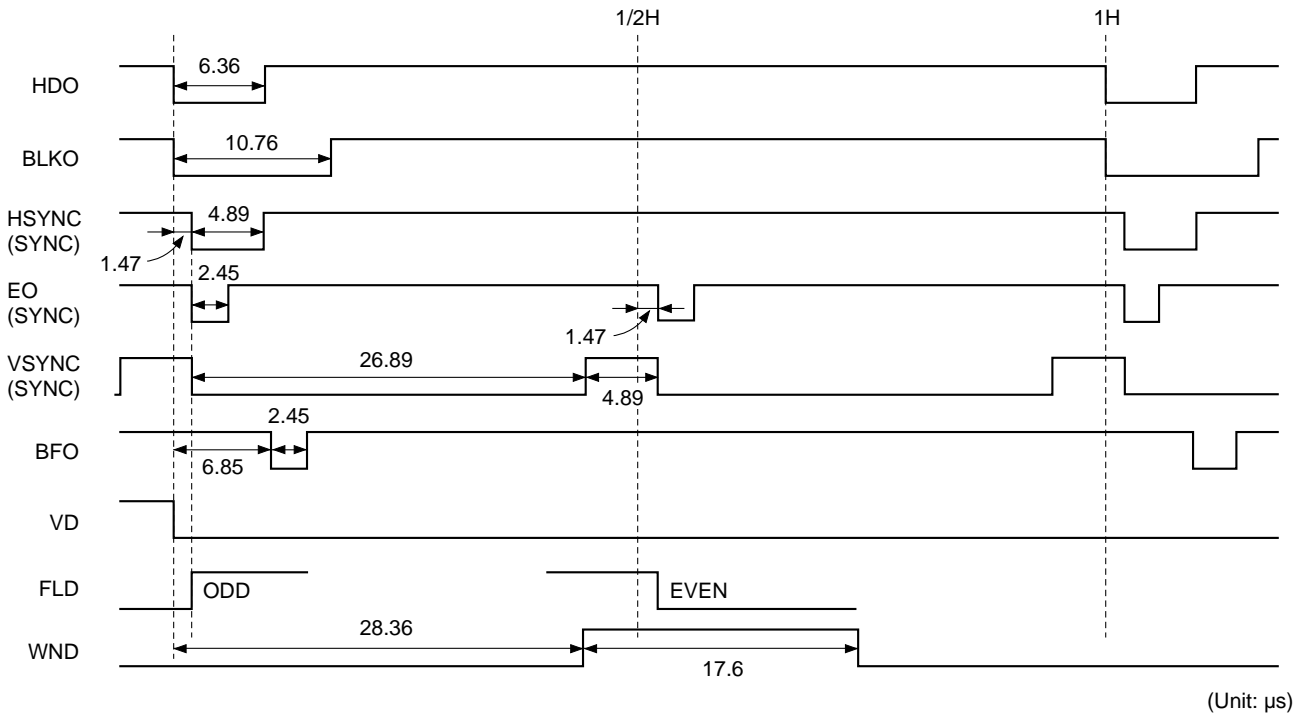
• **LALT reset (LR)**

LALT is reset in the same phase as LR reset.

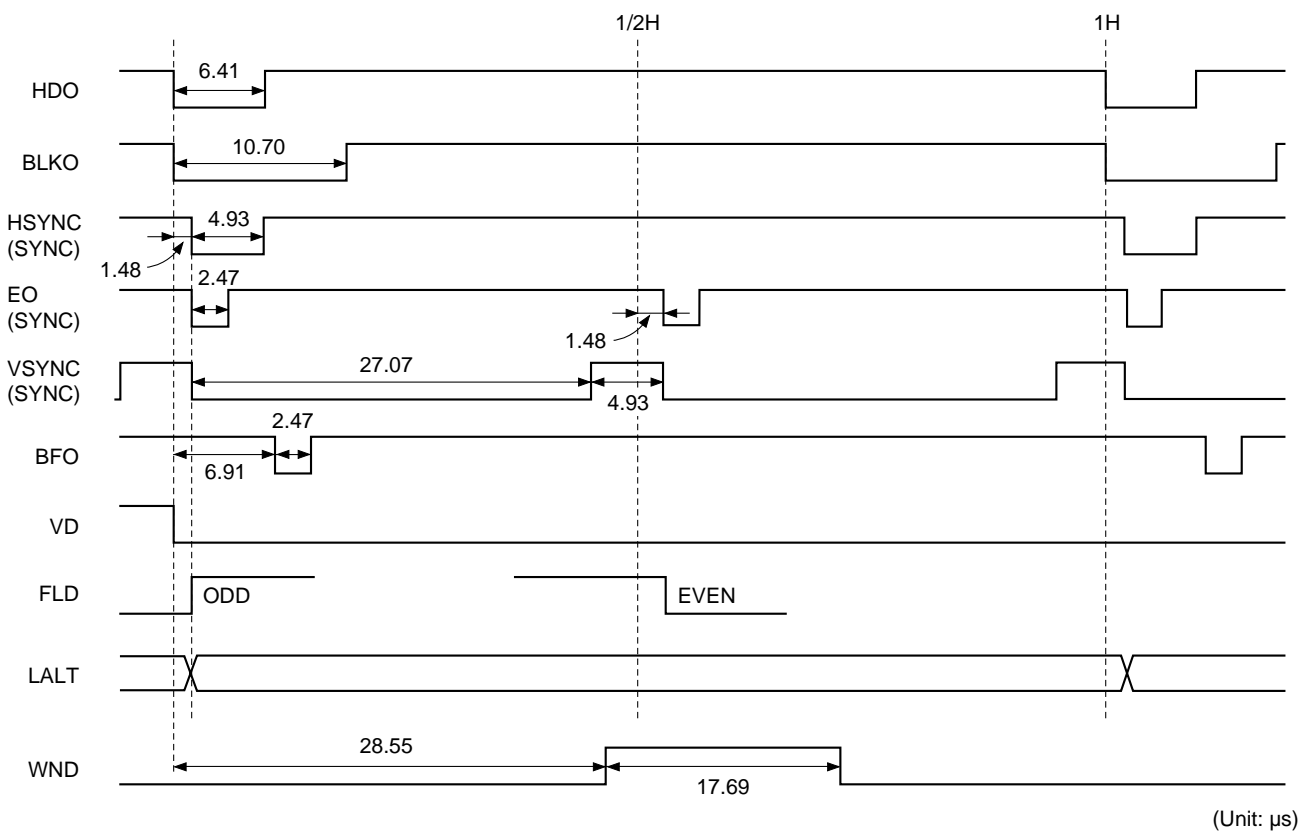
The minimum reset pulse width is 32μs.



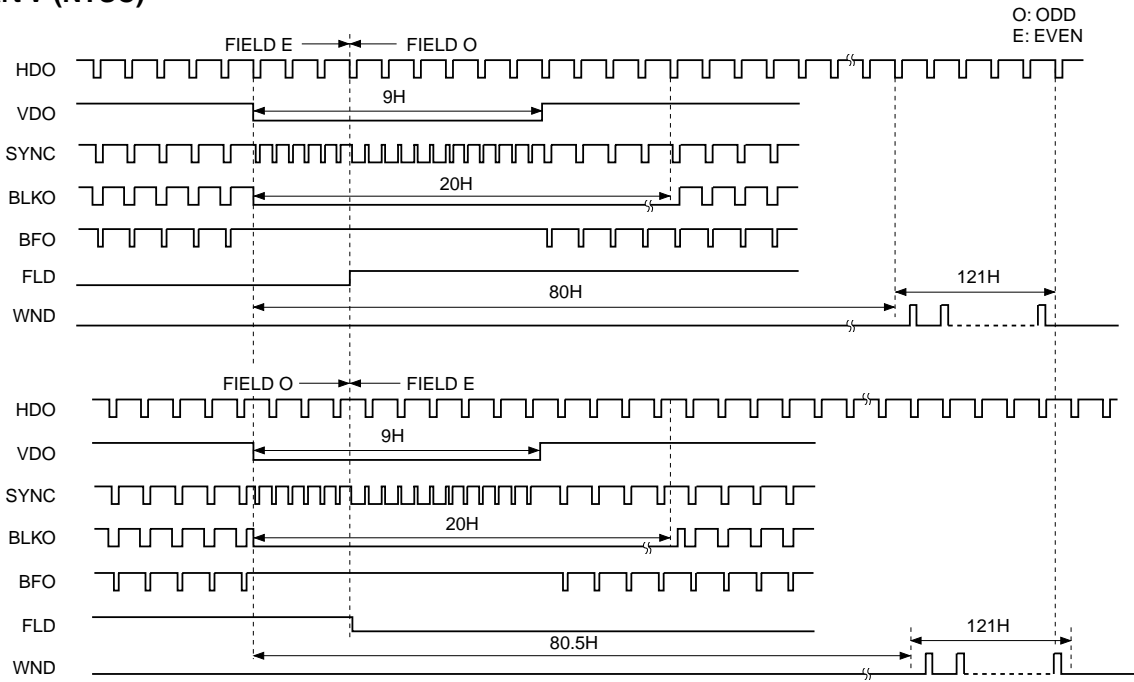
**Timing Chart H (NTSC)**



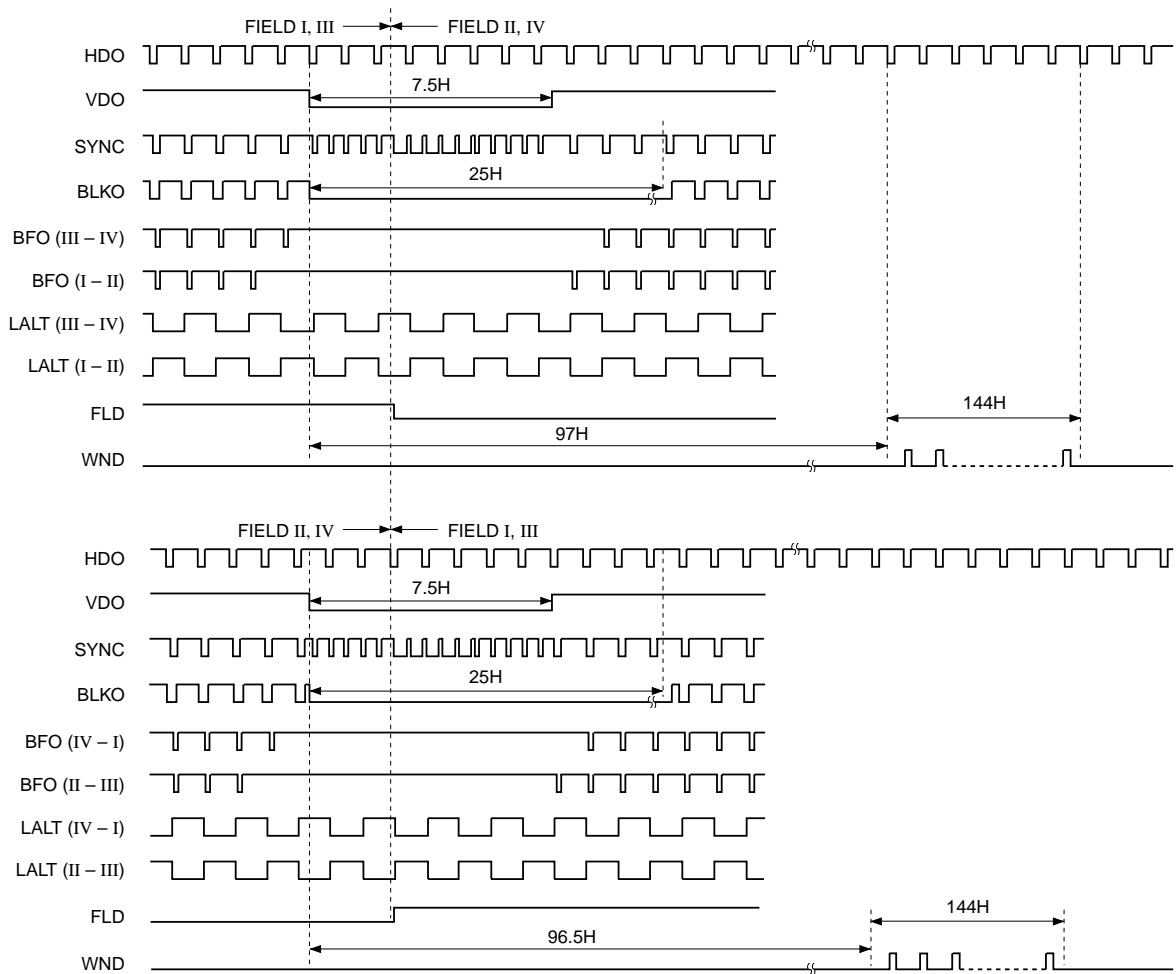
**Timing Chart H (PAL)**



**Timing Chart V (NTSC)**



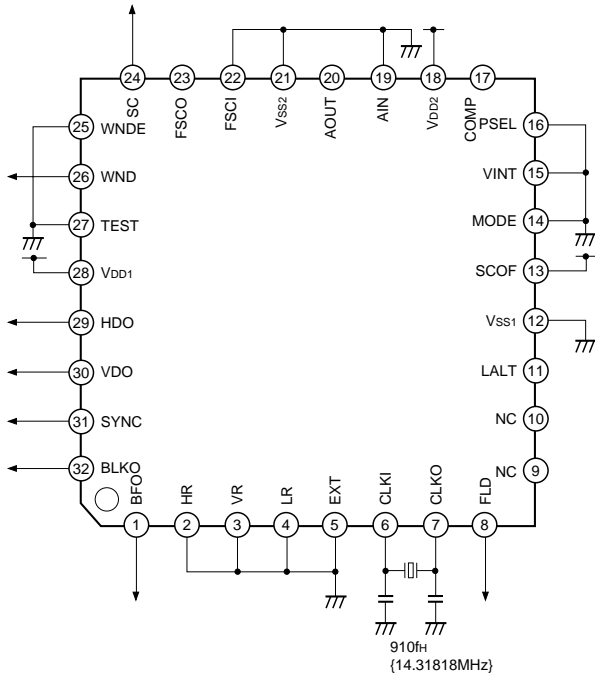
**Timing Chart V (PAL)**



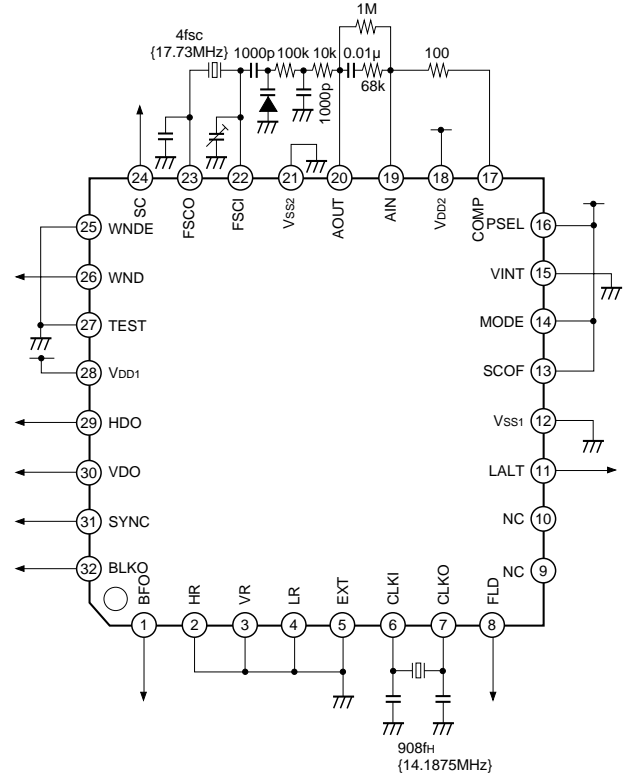


**Application Circuit**

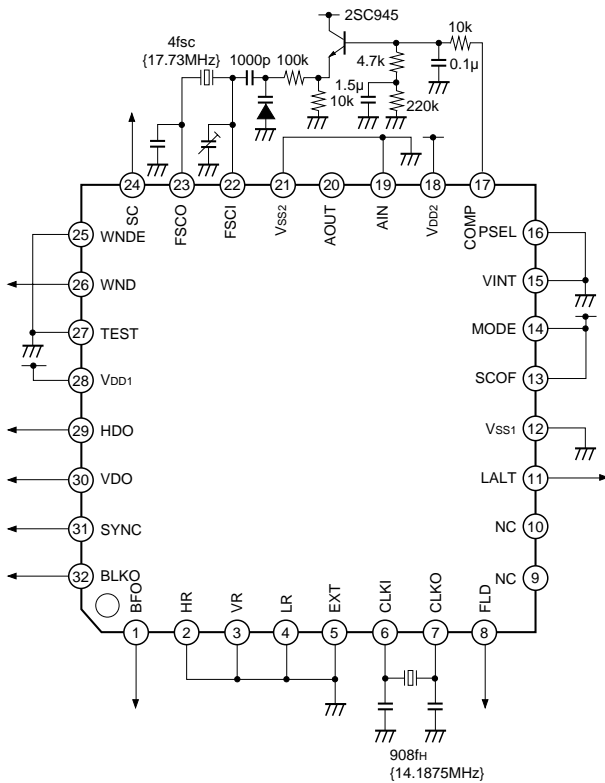
**NTSC (Internal mode)**



**PAL (Filter configuration 1, Internal mode)**



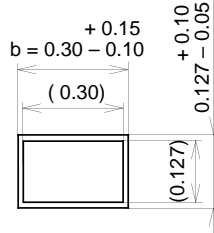
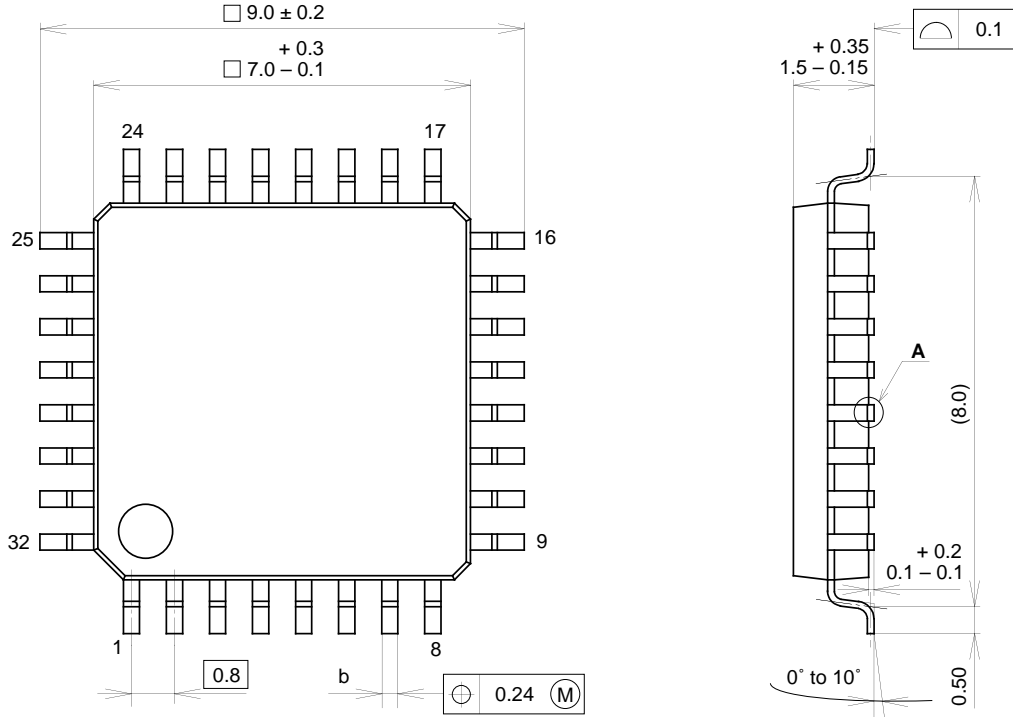
**PAL (Filter configuration 2, Internal mode)**



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Package Outline Unit: mm

32PIN QFP (PLASTIC)



DETAIL A : SOLDER

|            |                 |
|------------|-----------------|
| SONY CODE  | QFP-32P-L01     |
| EIAJ CODE  | P-QFP32-7x7-0.8 |
| JEDEC CODE | _____           |

|                  |                   |
|------------------|-------------------|
| PACKAGE MATERIAL | EPOXY RESIN       |
| LEAD TREATMENT   | SOLDER PLATING    |
| LEAD MATERIAL    | 42 / COPPER ALLOY |
| PACKAGE MASS     | 0.2g              |

LEAD SPECIFICATIONS

| ITEM                     | SPEC.     |
|--------------------------|-----------|
| LEAD MATERIAL            | ALLOY 42  |
| LEAD TREATMENT           | Sn-Pb 10% |
| LEAD TREATMENT THICKNESS | 5-18µm    |