

8-bit 20MSPS Video A/D Converter with Clamp Function

**Description**

The CXD1176Q is an 8-bit CMOS A/D converter for video use that features a sync clamp function. The adoption of a 2 step-parallel method realizes low power consumption and a maximum conversion speed of 20MSPS.

**Features**

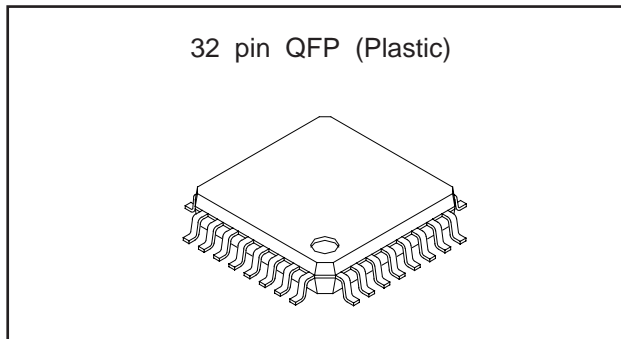
- Resolution power: 8-bit  $\pm 1/2$ LSB (DL)
- Maximum sampling frequency: 20MSPS
- Low power consumption: 60mW (at 20MSPS typ.) (Reference current excluded)
- Built-in sync type clamp function
- Built-in monostable multivibrator for clamp pulse generation
- Built-in sync pulse polarity selection function
- Clamp pulse direct input possible
- Built-in clamp ON/OFF function
- Built-in reference voltage self-bias circuit
- Input CMOS compatible
- 3-state TTL compatible output
- Single 5 V power supply
- Low input capacity: 11 pF
- Reference impedance: 330  $\Omega$  (typ.)

**Applications**

TV and VCR digital systems and a wide range of applications where high-speed A/D conversion is required.

**Structure**

Silicon gate CMOS IC



**Absolute Maximum Ratings (Ta=25 °C)**

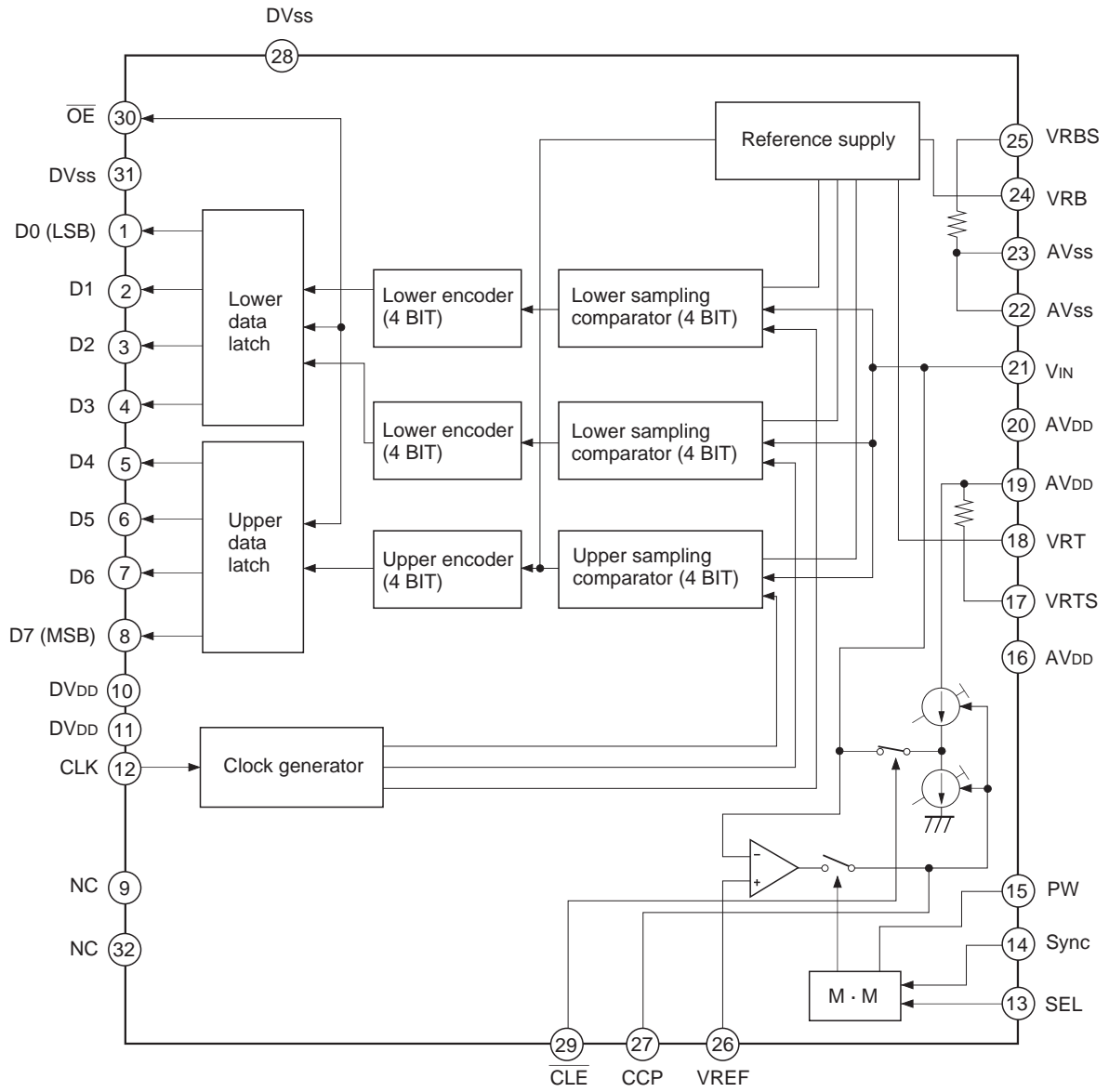
- Supply voltage  $V_{DD}$  7 V
- Reference voltage  
 $V_{RT}, V_{RB}$   $V_{DD} + 0.5$  to  $V_{SS} - 0.5$  V
- Input voltage  $V_{IN}$   $V_{DD} + 0.5$  to  $V_{SS} - 0.5$  V (Analog)
- Input voltage  $V_i$   $V_{DD} + 0.5$  to  $V_{SS} - 0.5$  V (Digital)
- Output voltage  $V_o$   $V_{DD} + 0.5$  to  $V_{SS} - 0.5$  V (Digital)
- Storage temperature  
 $T_{stg}$  -55 to +150 °C

**Recommended Operating Conditions**

- Supply voltage  $AV_{DD}, AV_{SS}$  4.75 to 5.25 V  
 $DV_{DD}, DV_{SS}$   
 $|DV_{SS} - AV_{SS}|$  0 to 100 mV
- Reference input voltage  
 $V_{RB}$  0 to V  
 $V_{RT}$  to 2.7 V
- Analog input  $V_{IN}$  1.8Vp-p above
- Clock pulse width  
 $T_{pw1}, T_{pw0}$  22.5 ns (min) to 1.1  $\mu$ s (max)
- Operating ambient temperature  
 $T_{opr}$  -40 to +85 °C

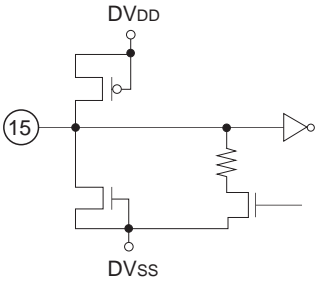
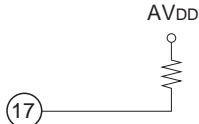
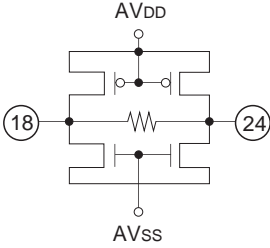
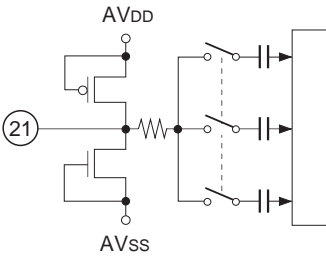

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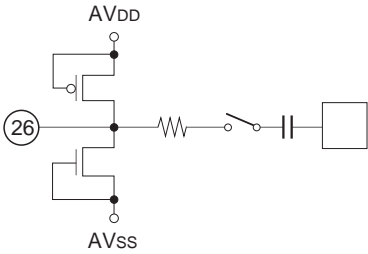
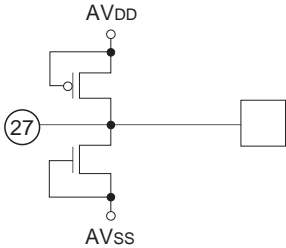
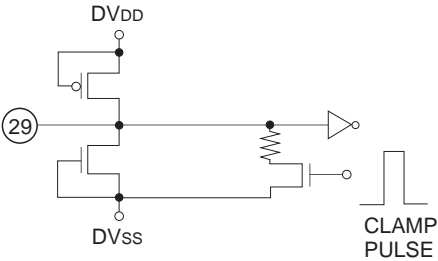
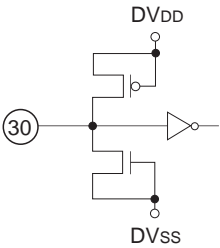
Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Equivalent circuit	Description
1 to 8	D0 to D7		D0 (LSB) to D7 (MSB) output
9, 32	NC		NC pin
10, 11	DV <sub>DD</sub>		Digital +5 V
12	CLK		Clock input
13	SEL		<p>When SEL is at low, with the falling edge of Pin 14 (sync) as trigger, the monostable multivibrator generates clamp pulses.</p> <p>When SEL is at high, with the rising edge of Pin 14 (sync) as trigger, it generates clamp pulses.</p>
14	Sync		<p>Trigger pulse input to the monostable multivibrator.</p> <p>Trigger polarity can be selected through Pin 13 (SEL).</p>

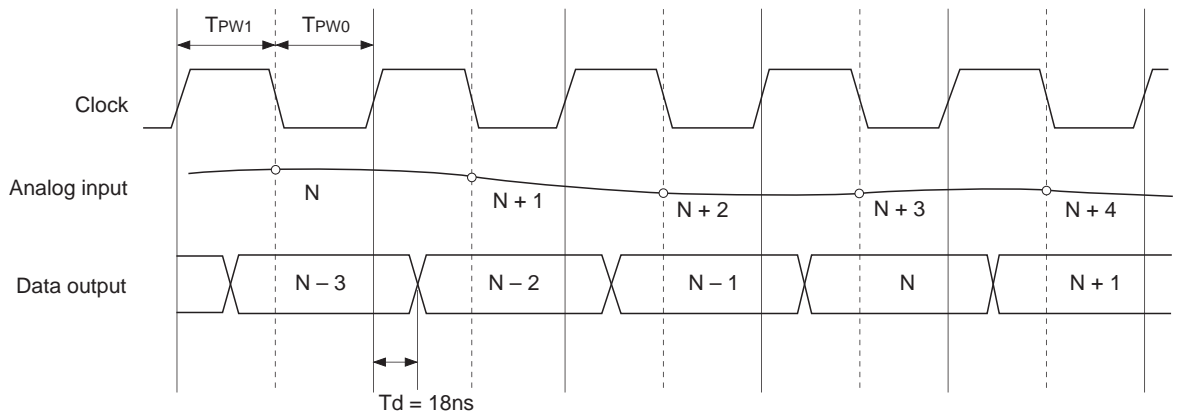
Pin No.	Symbol	Equivalent circuit	Description
15	PW		<p>When a clamp pulse is generated at the monostable multivibrator, the pulse width is determined by the external R and C.</p> <p>When the clamp pulse is directly input, it is input to Pin 15 (PW). The signal voltage of the low period is clamped. (Here, Pin 14 (sync) is fixed to either low or high.)</p>
16, 19, 20	AVDD		Analog +5 V
17	VRTS		When shorted with VRT, generates approx. +2.6 V.
18	VRT		Reference voltage (top)
24	VRB		Reference voltage (bottom)
21	V <sub>IN</sub>		Analog input
22, 23	AVSS		Analog ground
25	VRBS		When shorted with VRB, generates approx. +0.5 V.

Pin No.	Symbol	Equivalent circuit	Description
26	VREF		<p>Clamp reference voltage input. Clamps to provide a clamp period input signal equal to the reference voltage.</p>
27	CCP		<p>Integrates the voltage for clamp control. CCP and V<sub>IN</sub> voltage changes are in positive phase.</p>
28, 31	DVss		<p>Digital ground.</p>
29	$\overline{\text{CLE}}$		<p>When <math>\overline{\text{CLE}}</math> is at low, clamp function is activated.              When <math>\overline{\text{CLE}}</math> is at high, clamp function is OFF and only the usual A/D converter function is active.              By connecting <math>\overline{\text{CLE}}</math> pin to DV<sub>DD</sub> via a several hundred <math>\Omega</math> resistance, the clamp pulse can be tested.</p>
30	$\overline{\text{OE}}$		<p>When <math>\overline{\text{OE}}</math> is at low, Data is output.              When <math>\overline{\text{OE}}</math> is at high, D0 to D7 pins turn to high impedance.</p>

**Digital Output**

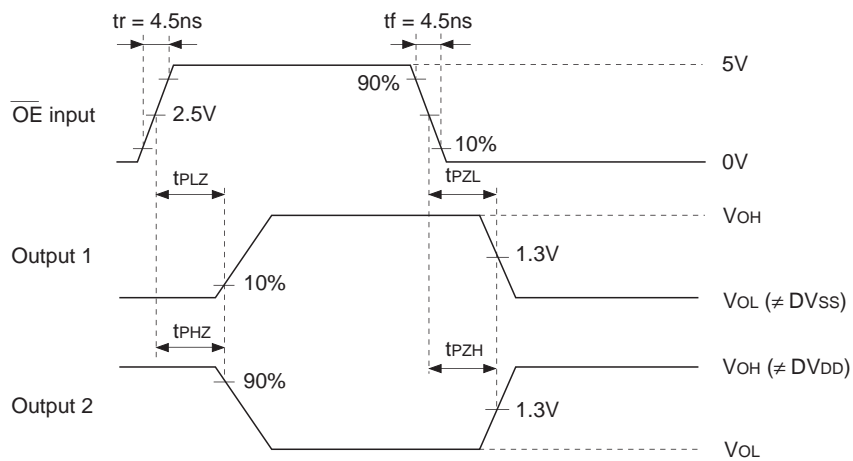
Correspondence between the analog input voltage and the digital output code is indicated in the chart below.

Input signal voltage	Step	Digital output code	
		MSB	LSB
$V_{RT}$	0	1 1 1 1 1 1 1 1	
⋮	⋮	⋮	
127	127	1 0 0 0 0 0 0 0	
128	128	0 1 1 1 1 1 1 1	
⋮	⋮	⋮	
$V_{RB}$	255	0 0 0 0 0 0 0 0	



○ : Points where analog signals are sampled.

**Timing Chart. I**



**Timing Chart. II**

## Electrical Characteristics

## Analog characteristics

(F<sub>C</sub> = 20 MSPS, V<sub>DD</sub> = 5 V, V<sub>RB</sub> = 0.5 V, V<sub>RT</sub> = 2.5 V, T<sub>a</sub> = 25 °C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Conversion speed	F <sub>C</sub>	V <sub>DD</sub> = 4.75 to 5.25 V T <sub>a</sub> = -40 to +85 °C V <sub>IN</sub> = 0.5 to 2.5 V f <sub>IN</sub> = 1 kHz ramp	0.5		20	MSPS	
Analog input band width (-1dB)	BW	Envelope		18		MHz	
Offset voltage*1	E <sub>OT</sub>	Potential difference to V <sub>RT</sub>	-60	-40	-20	mV	
	E <sub>OB</sub>	Potential difference to V <sub>RB</sub>	+20	+40	+60		
Integral non-linearity error	E <sub>L</sub>	End point		+0.5	+1.3	LSB	
Differential non-linearity error	E <sub>D</sub>			±0.3	±0.5		
Differential gain error	DG	NTSC 40 IRE mod ramp F <sub>C</sub> = 14.3 MSPS		1.0		%	
Differential phase error	DP			0.5		deg	
Aperture jitter	t <sub>aj</sub>			30		ps	
Sampling delay	t <sub>sd</sub>			4		ns	
Clamp offset voltage*2	E <sub>oc</sub>	V <sub>IN</sub> = DC, PWS = 3 μs	V <sub>REF</sub> = 0.5 V	0	+20	+40	mV
			V <sub>REF</sub> = 2.5 V	-50	-30	-10	
Clamp pulse width (Sync pin input)	t <sub>cpw</sub>	C = 100 pF, R = 130 kΩ (15 PIN)	1.75	2.75	3.75	μs	
Clamp pulse delay	t <sub>cpd</sub>			25		ns	

\*1 The offset voltage E<sub>OB</sub> is a potential difference between V<sub>RB</sub> and a point of position where the voltage drops equivalent to 1/2 LSB of the voltage when the output data changes from "00000000" to "00000001".  
E<sub>OT</sub> is a potential difference between V<sub>RT</sub> and a potential of point where the voltage rises equivalent to 1/2LSB of the voltage when the output data changes from "11111111" to "11111110".

\*2 Clamp offset voltage varies individually. When using with R, G, B 3 channels, color sliding may be generated.

## DC characteristics

(F<sub>c</sub> = 20 MSPS, V<sub>DD</sub> = 5 V, V<sub>RB</sub> = 0.5 V, V<sub>RT</sub> = 2.5 V, T<sub>a</sub> = 25 °C)

Item		Conditions	Min.	Typ.	Max.	Unit
Supply current	I <sub>DD</sub>	F <sub>c</sub> = 20 MSPS NTSC ramp wave input		12	18	mA
Reference pin current	I <sub>REF</sub>		4.5	6.6	8.7	mA
Analog input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 1.5 V + 0.07 V <sub>rms</sub>		11		pF
Reference resistance (V <sub>RT</sub> to V <sub>RB</sub> )	R <sub>REF</sub>		230	300	450	Ω
Self-bias I	VRB <sub>1</sub>	VRB and VRBS are shorted VRT and VRTS are shorted	0.48	0.52	0.56	V
	VRT <sub>1</sub> to VRB <sub>1</sub>		1.96	2.08	2.22	
Self-bias II	VRT <sub>2</sub>	VRB = AGND VRT and VRTS are shorted		2.32		V
Digital input voltage	V <sub>IH</sub>	V <sub>DD</sub> = 4.75 to 5.25 V T <sub>a</sub> = -40 to +85 °C	4.0			V
	V <sub>IL</sub>				1.0	
Digital input current	I <sub>IH</sub>	V <sub>DD</sub> = max	V <sub>IH</sub> = V <sub>DD</sub>		5	μA
	I <sub>IL</sub>		V <sub>IL</sub> = 0V		5	
Digital output current	I <sub>OH</sub>	OE = V <sub>SS</sub> V <sub>DD</sub> = min	V <sub>OH</sub> = V <sub>DD</sub> - 0.5 V	-1.1		mA
	I <sub>OL</sub>		V <sub>OL</sub> = 0.4V	3.7		
	I <sub>OZH</sub>	OE = V <sub>DD</sub> V <sub>DD</sub> = max	V <sub>OH</sub> = V <sub>DD</sub>		16	μA
	I <sub>OZL</sub>		V <sub>OL</sub> = 0V		16	

## Timing

(F<sub>c</sub> = 20 MSPS, V<sub>DD</sub> = 4.75 to 5.25 V, V<sub>RB</sub> = 0.5 V, V<sub>RT</sub> = 2.5 V, T<sub>a</sub> = -40 to +85 °C)

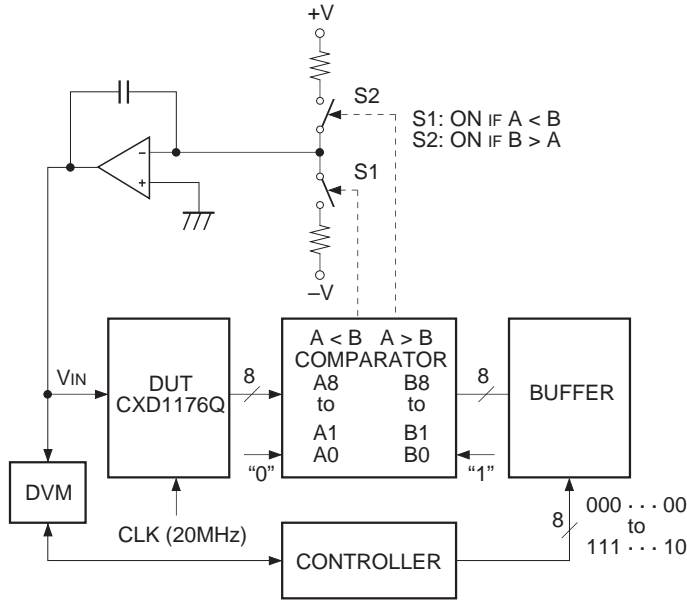
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output data delay	T <sub>DL</sub>	with TTL 1 gate and 10pF load		18	30	ns
Tri-state output enable time	t <sub>PZH</sub>	R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 20 pF OE = 3 V → 0 V	2.5	6	10	ns
	t <sub>PZL</sub>					
Tri-state output disable time	t <sub>PHZ</sub>	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 20 pF OE = 0 V → 3 V	8	18	30	ns
	t <sub>PLZ</sub>					



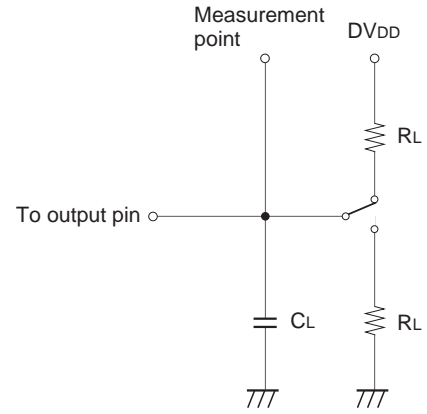
**Electrical Characteristics Measurement Circuit**

Integral non-linearity error  
 Differential non-linearity error  
 Offset voltage

} measurement circuit



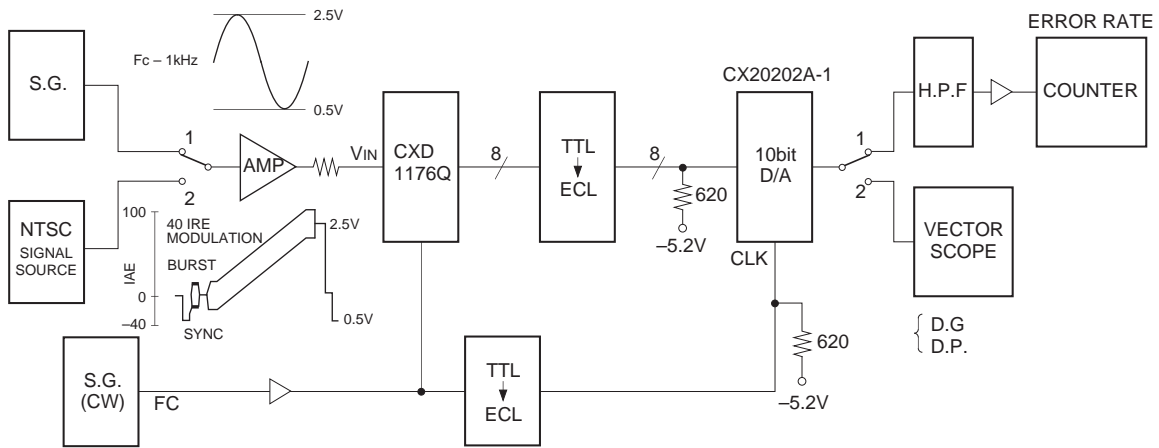
**Tri-state output measurement circuit**



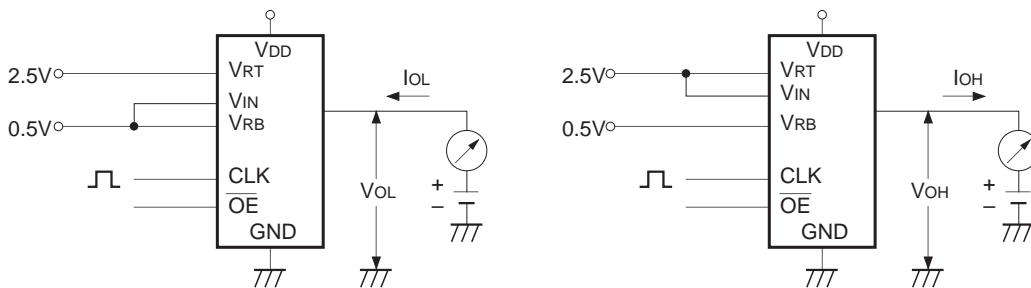
Note) CL includes capacitance of the probe and others.

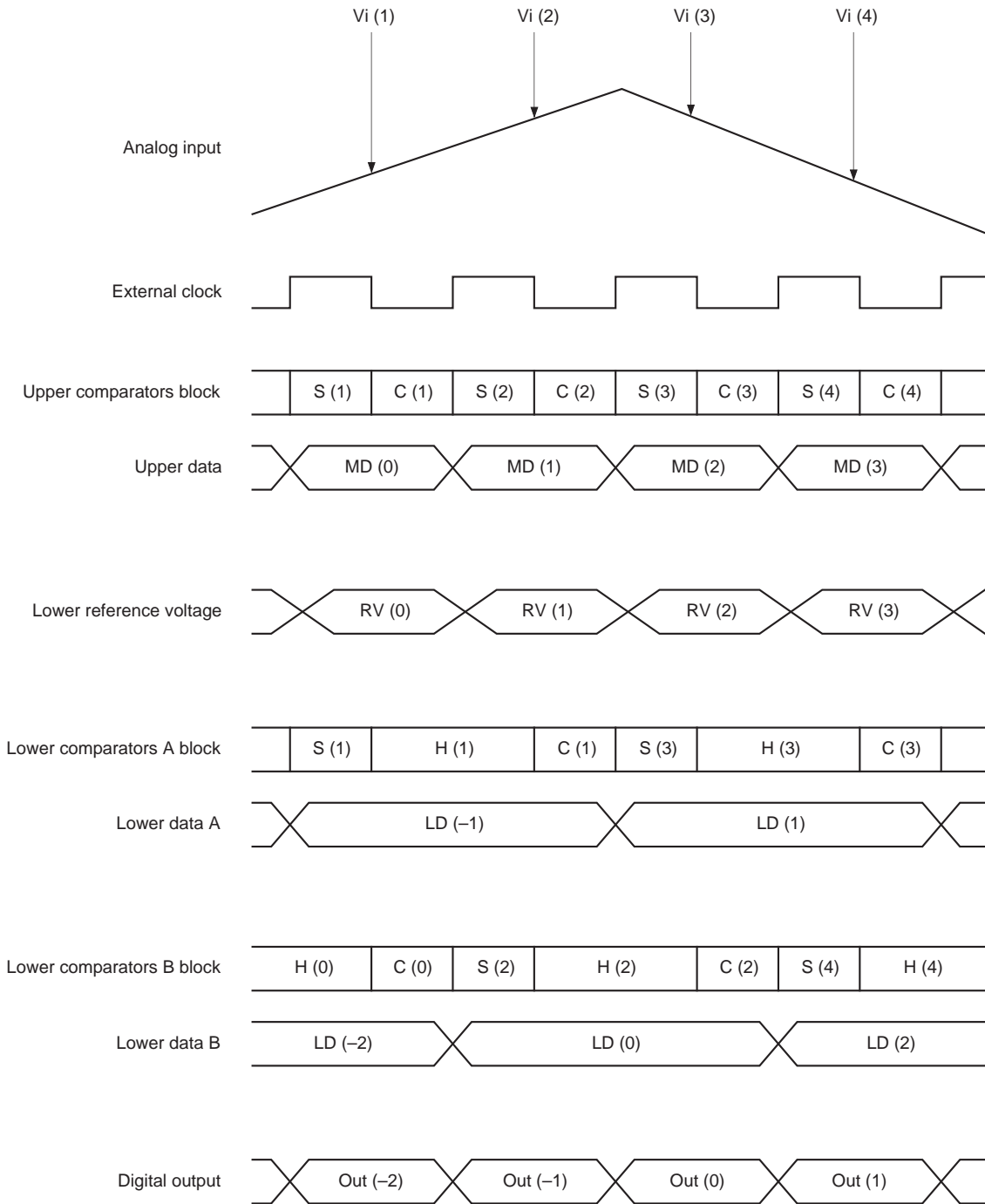
Maximum operational speed  
 Differential gain error  
 Differential phase error

} measurement circuit



**Digital output current measurement circuit**





**Timing Chart 3**

**Operation** (See Block Diagram and Timing Chart 3)

1. The CXD1176Q is a 2-step parallel system A/D converter featuring a 4-bit upper comparators group and 2 lower comparators groups of 4-bit each. The reference voltage that is equal to the voltage between VRT – VRB/16 is constantly applied to the upper 4-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data. VRTS and VRBS pins serve for the self generation of VRT (Reference voltage top) and VRB (Reference voltage bottom).

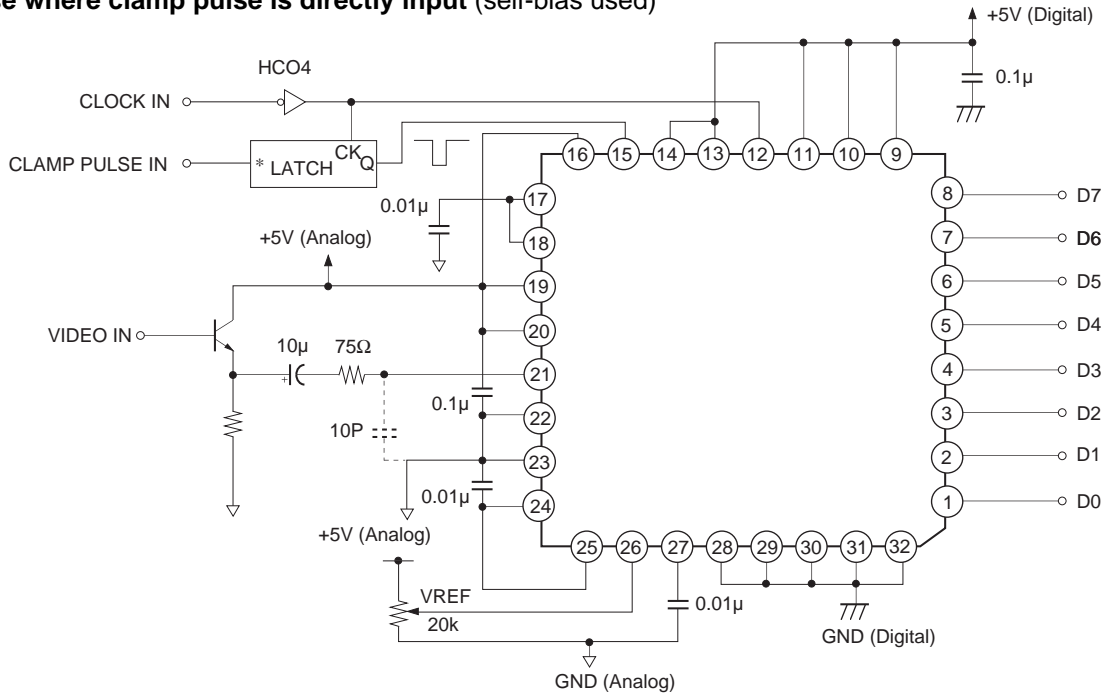
2. This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S, H, C symbols. That is input sampling (auto zero) mode, input hold mode and comparison mode.
3. The operation of respective parts is as indicated in the chart. For instance input voltage  $V_i$  (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.  
The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

## Operation Notes

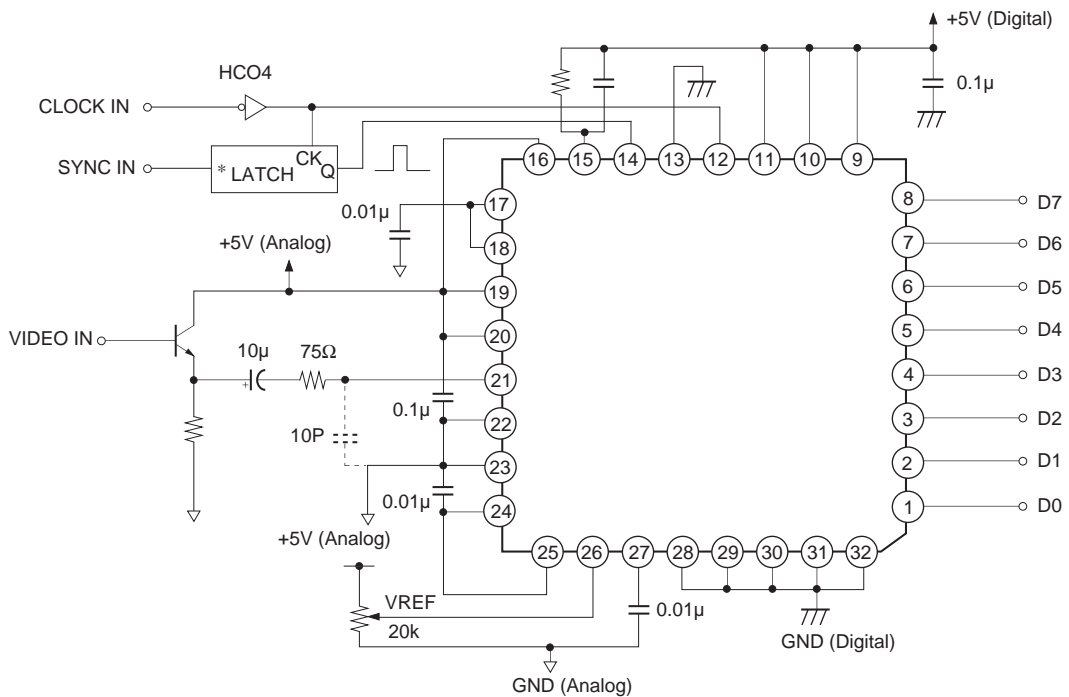
1.  $V_{DD}$ ,  $V_{SS}$   
To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog  $V_{DD}$  pins, use a ceramic capacitor of about 0.1  $\mu\text{F}$  set as close as possible to the pin to bypass to the respective GND's.
2. Analog input  
Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about 100  $\Omega$  in series between the amplifier output and A/D input.
3. Clock input  
The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.
4. Reference input  
Voltage between  $V_{RT}$  to  $V_{RB}$  is compatible with the dynamic range of the analog input. Bypassing  $V_{RT}$  and  $V_{RB}$  pins to GND, by means of a capacitor about 0.1  $\mu\text{F}$ , stable characteristics are obtained. By shorting  $V_{RT}$  and  $V_{RTS}$ ,  $V_{RB}$  and  $V_{RBS}$ , the self-bias function that generates  $V_{RT} = 2.6 \text{ V}$  and  $V_{RB} = 0.6 \text{ V}$ , is activated.
5. Timing  
Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18 ns.
6.  $\overline{\text{OE}}$  pin  
By connecting  $\overline{\text{OE}}$  to GND output mode is obtained. By connecting to  $V_{DD}$  high impedance is obtained.
7. About latch up  
It is necessary that  $\text{AV}_{DD}$  and  $\text{DV}_{DD}$  pins be the common source of power supply.  
This is to avoid latch up due to the voltage difference between  $\text{AV}_{DD}$  and  $\text{DV}_{DD}$  pins when power is ON.

Application Circuit

(1) Case where clamp pulse is directly input (self-bias used)



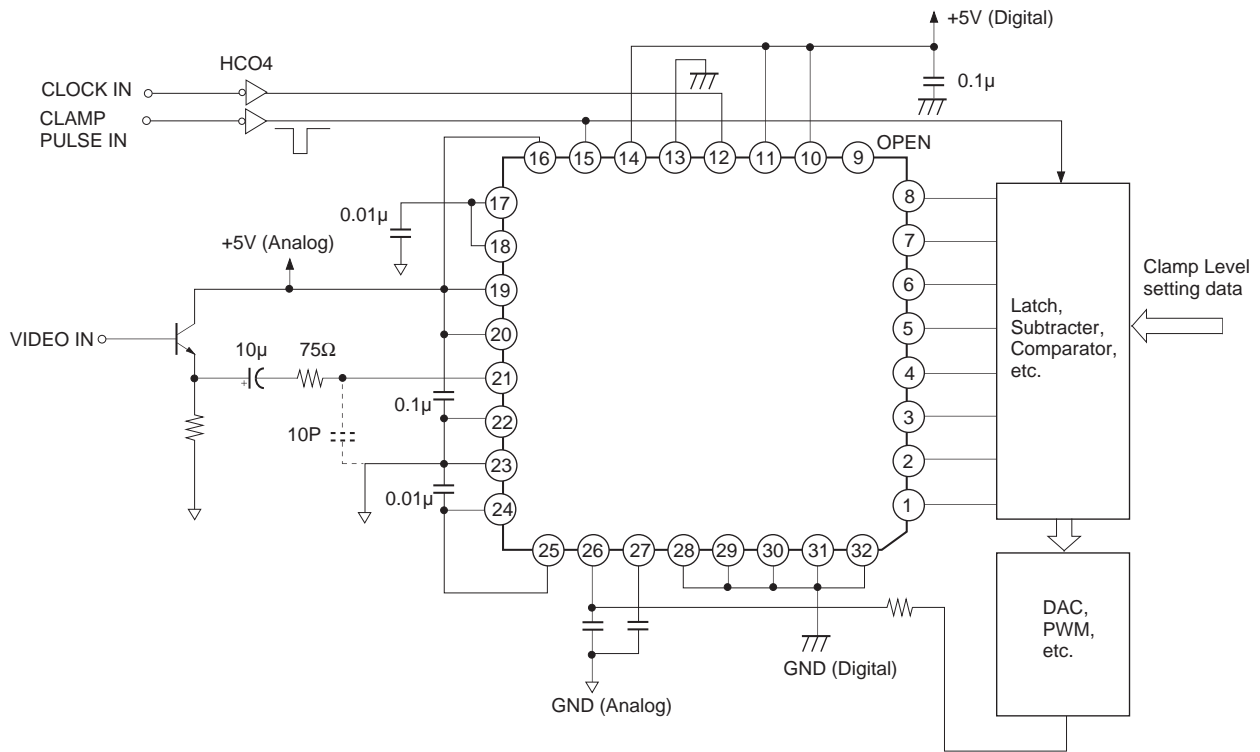
(2) Example where pedestal clamp is executed by sync pulse (self-bias used)



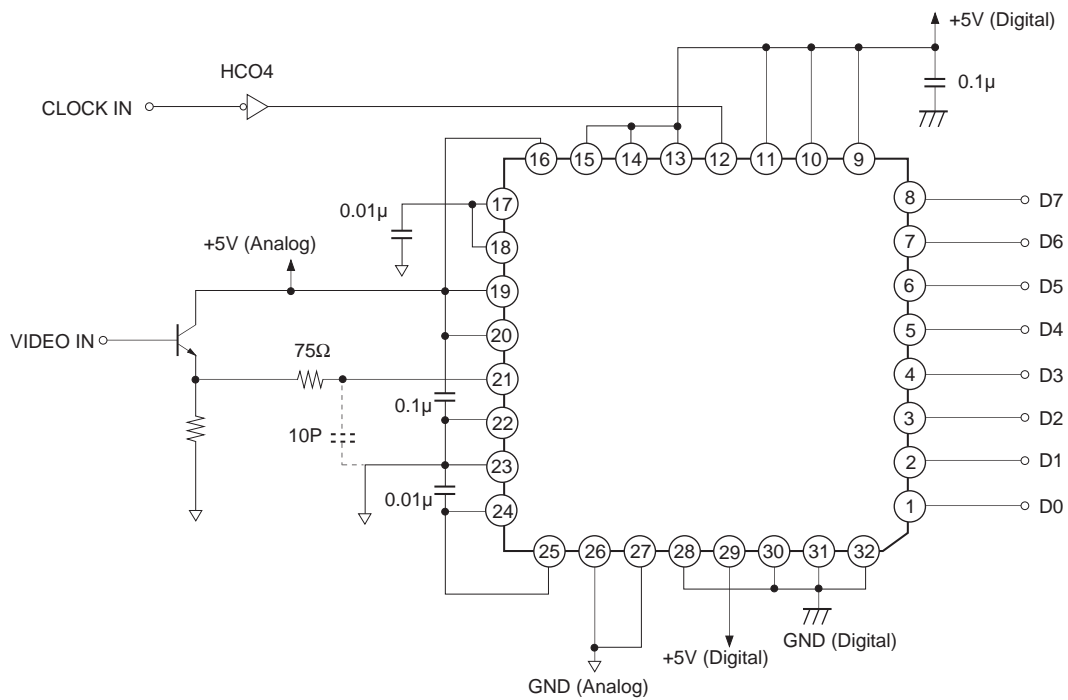
\* The clamp pulse is latched by the ADC sampling clock, but that is not necessary for clamp basic operation. However, slight beat may be generated as vertical sag according to the relation between the sampling frequency and clamp pulse frequency.

At such time, the latch circuit is effective. (See page 20 Notes on Operation 5.)

**(3) Digital clamp (self-bias used)**



**(4) When clamp is not used (self-bias used)**



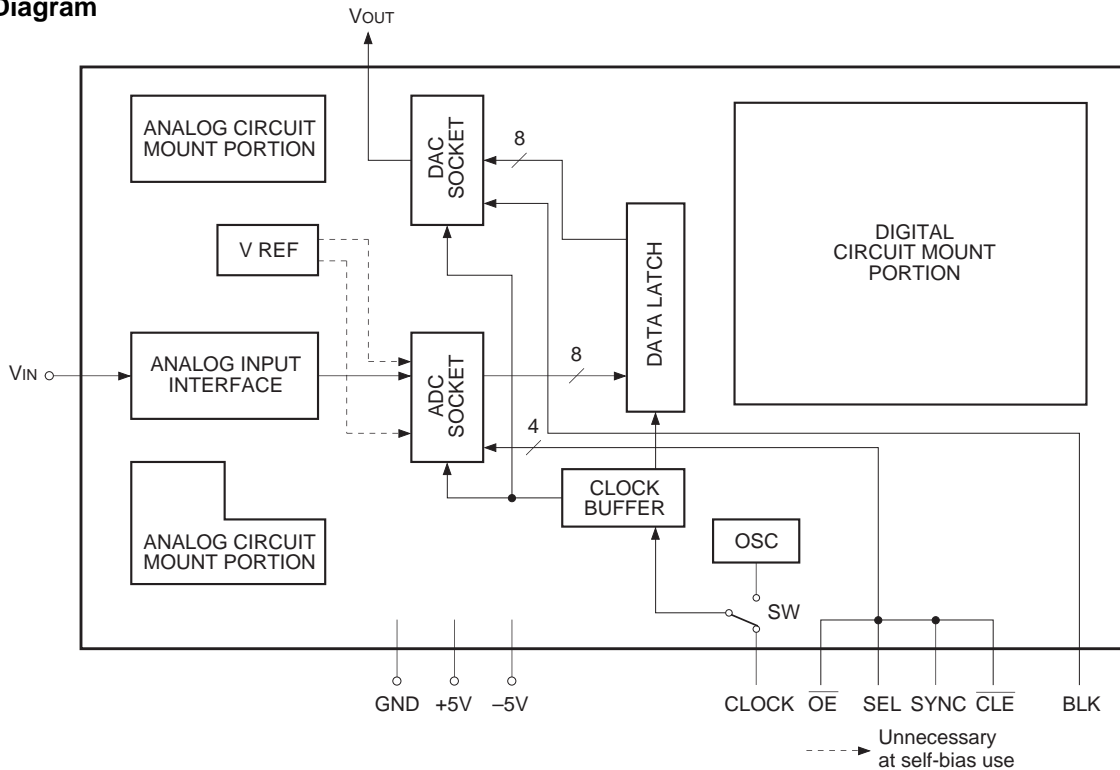
**8-bit 20MSPS ADC and DAC Evaluation Board**

Evaluation boards are available for the high speed, low power consumption CMOS converters, CXD1176Q (8-bit 20MHz A/D) and CXD1171M (8-bit 40MHz D/A).

The evaluation board is composed of a main board common to either type, to which is added sub board CXD1176Q or sub board CXD1171M. The junction is made through a socket.

To the main board are mounted an input interface, clock buffer and latch. To each of the sub boards is mounted CXD1176Q and CXD1171M respectively. Those IC's are mounted according to recommended print patterns designed to provide maximum performance to the A/D and D/A converters.

**Block Diagram**



**Characteristics**

- Resolution 8 bit
- Maximum conversion rate 20 MHz
- Digital input level CMOS level
- Supply voltage  $\pm 5.0$  V (Single +5 V power supply possible at self bias use)

**Supply voltage**

Item	Min.	Typ.	Max.	Unit
+5 V			150	mA
-5 V			20	

**Clock input**

CMOS compatible

- Pulse width  $T_{CW1}$  22.5 ns (min)
- $T_{CW0}$  22.5 ns (min)

**Analog Output (CXD1171M)** (RL > 10 kΩ)

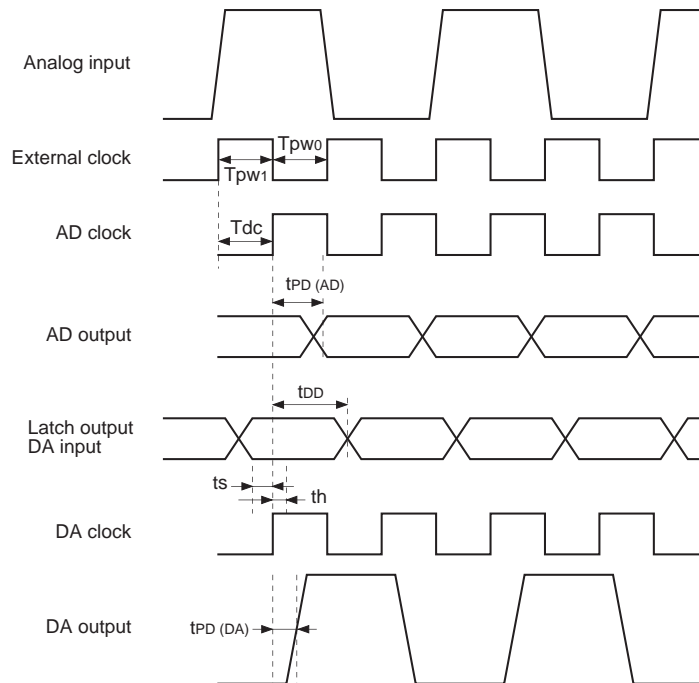
Item	Min.	Typ.	Max.	Unit
Analog output	1.9	2.0	2.1	V

**Output Format (CXD1176Q)**

The table shows the output format of AD Converter.

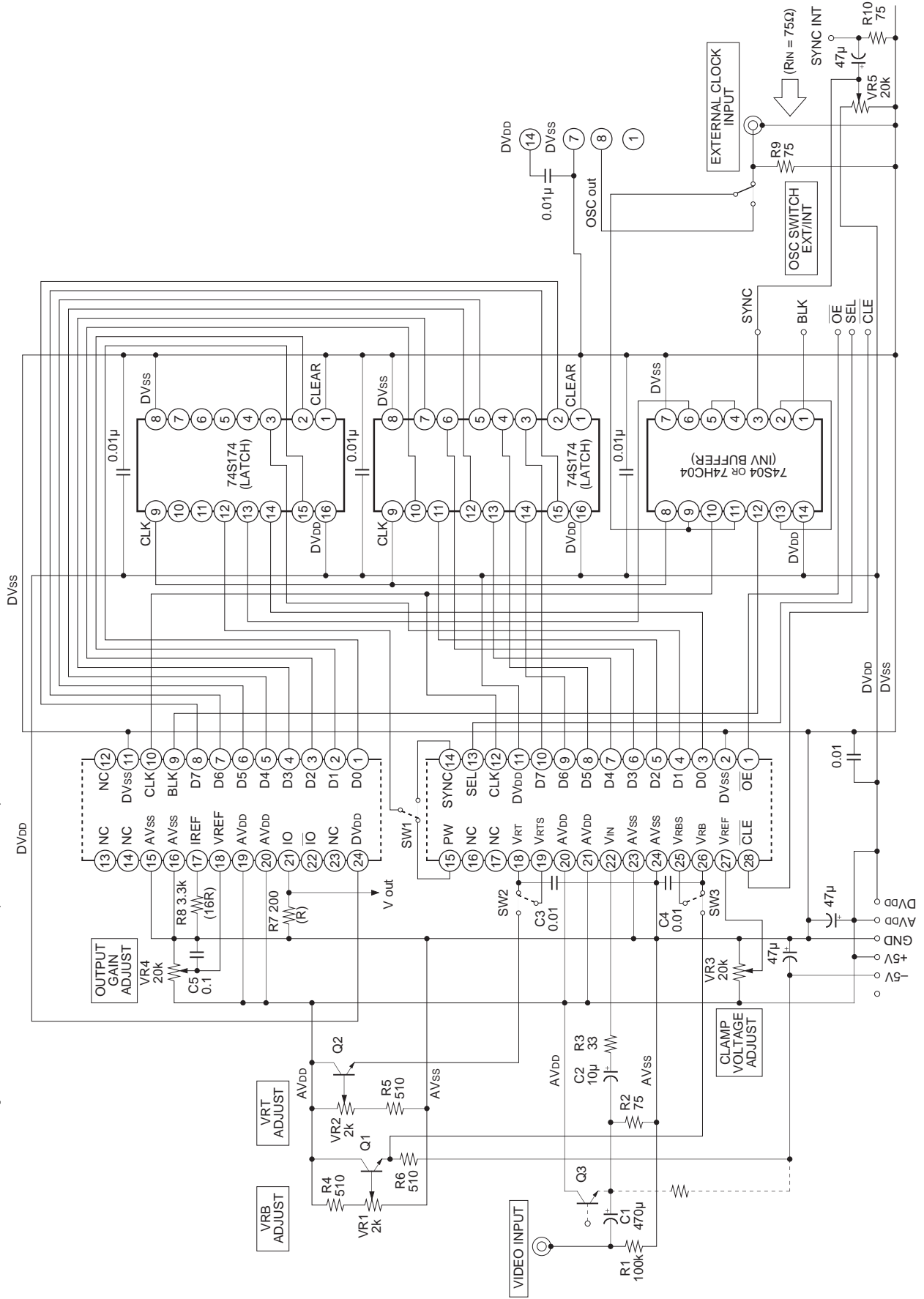
Analog input voltage	Step	Digital output code							
		MSB				LSB			
V <sub>RT</sub>	0	1	1	1	1	1	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	127	1	0	0	0	0	0	0	0
⋮	128	0	1	1	1	1	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
V <sub>RB</sub>	255	0	0	0	0	0	0	0	0

**Timing Chart**



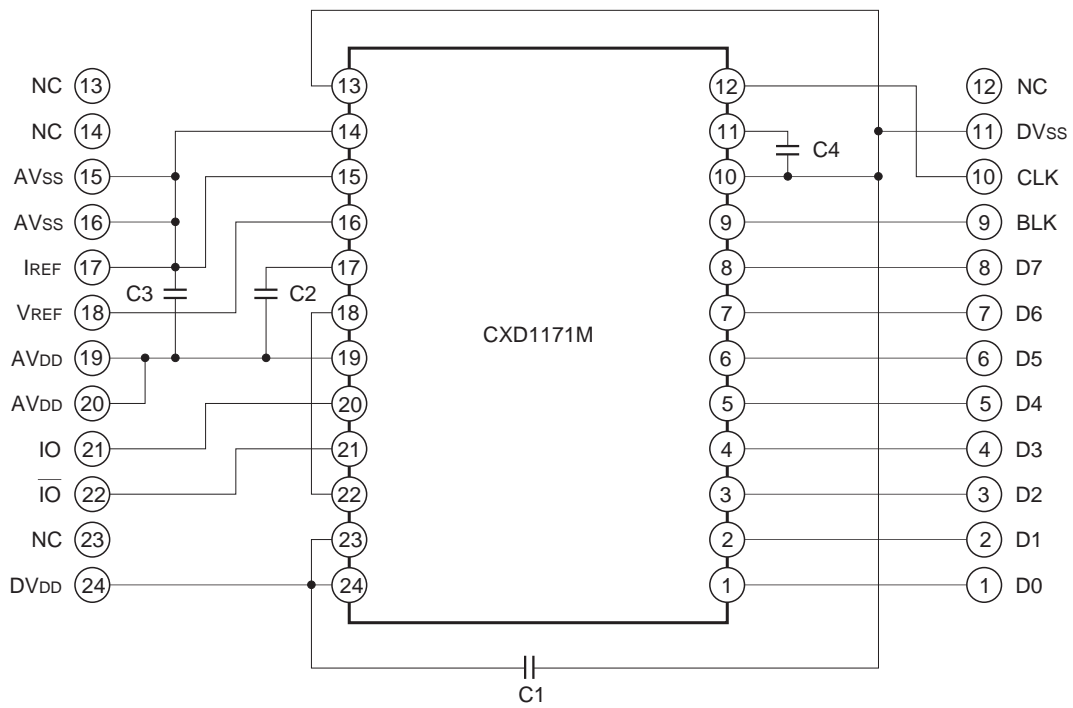
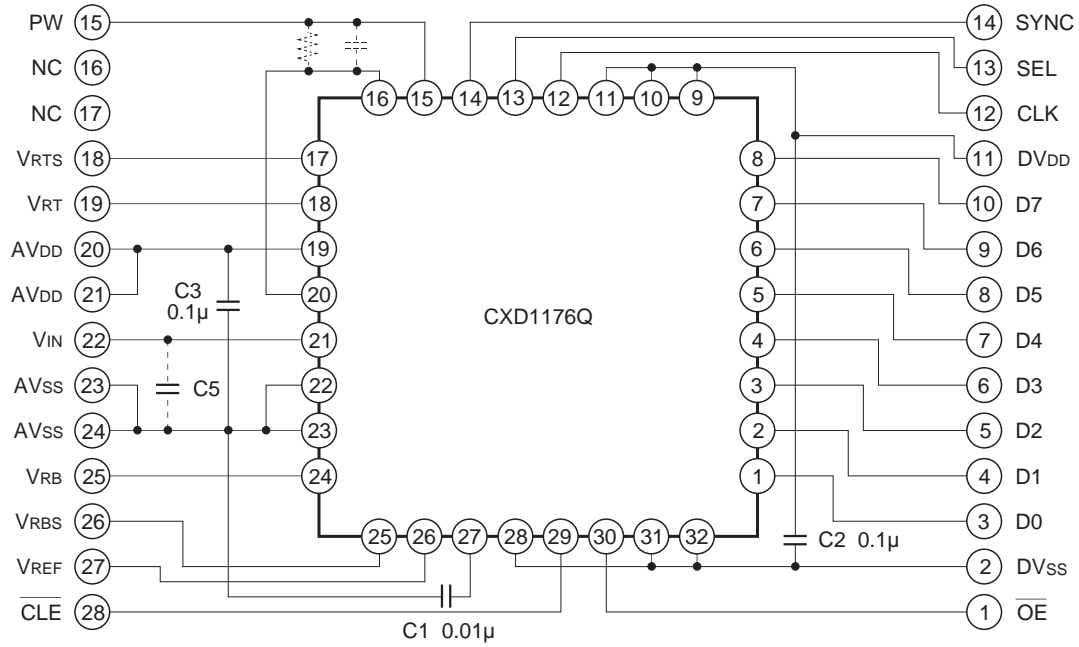
Item	Symbol	Min.	Typ.	Max.	Unit
Clock High time	T <sub>PW1</sub>	25			ns
Clock Low time	T <sub>PW0</sub>	25			ns
Clock Delay	T <sub>dc</sub>			24	ns
Data delay AD	t <sub>PD (AD)</sub>		18	30	ns
Data delay (latch)	t <sub>DD</sub>			5	ns
Set up time	t <sub>s</sub>	5			ns
Hold time	t <sub>h</sub>	10			ns
Data delay DA	t <sub>PD (DA)</sub>		10		ns

CMOS ADC/DAC Peripheral Circuit Board (Main Board)





CMOS ADC/DAC Peripheral Circuit Board (Sub Board)



## List of Parts

### resistance

R1	100 k $\Omega$
R2	75 $\Omega$
R3	75 $\Omega$
R4	510 $\Omega$
R5	510 $\Omega$
R6	510 $\Omega$
R7	R = 200 $\Omega$
R8	18R $\approx$ 3.3 k $\Omega$
R9	75 $\Omega$
R10	75 $\Omega$
VR1	2 k $\Omega$
VR2	2 k $\Omega$
VR3	20 k $\Omega$
VR4	20 k $\Omega$
VR5	20 k $\Omega$

### transistor

Q1	2SC2785
Q2	2SC2785
Q3	2SC2785

### IC

IC1	74S174
IC2	74S174
IC3	74S04

### oscillator

OSC

### others

connector	BNC071
SW	AT1D2M3

### capacitance

C1	470 $\mu$ F/6.3 V (chemical)
C2	10 $\mu$ F/16 V (chemical)
C3	0.01 $\mu$ F
C4	0.01 $\mu$ F
C5	0.1 $\mu$ F
C6	0.1 $\mu$ F
C7	0.1 $\mu$ F
C8	0.1 $\mu$ F
C9	0.1 $\mu$ F
C10	0.1 $\mu$ F
C11	47 $\mu$ F/10 V (chemical)
C12	47 $\mu$ F/10 V (chemical)
C13	47 $\mu$ F/10 V (chemical)
C14	0.1 $\mu$ F

## Adjustment

### 1. Vref adjustment (VR1, VR2)

Adjustment of A/D converter reference voltage. VRB is adjusted through VR1 and VRT through VR2. When self-bias is used, there is no need for adjustment. Reference voltage is set through self-bias delivery.

### 2. Setting of clamp reference voltage (VR3)

Clamp reference voltage is set.

### 3. DAC output full-scale adjustment (VR4)

Full-scale voltage of D/A converter output is adjusted at the PCB shipment, the full-scale voltage is adjusted to approx. 2 V.

### 4. Sync (clamp) pulse interface (VR5)

This adjustment enables interface with the signal generator and others at the PCB shipment, adjustment is performed to obtain a threshold of approx. 2.5 V to an H sync of 0 to 5 V.

#### 5. $\overline{OE}$ , SEL, Sync, BLK, $\overline{CLE}$ , Sync INT

The following pins are set on the main board:  $\overline{OE}$ , SEL, Sync,  $\overline{CLE}$ , Sync INT (CXD1176Q) and BLK (CXD1171M). For the pins function, refer to the specifications. The difference between Sync pin and Sync INT pin is that you input a horizontal synchronizing signal above 3.5 Vp-p Sync INT pin. The pulse threshold is set through VR5. For input through Sync pin, pulse is input at TTL or CMOS level. In this case cut off the junction line between Sync and Sync INT pin.

At the PCB shipment the main board pins are set as follows.

- $\overline{OE}$  ... Low (A/D output ON)
- SEL ... Low (Pulse generated with Sync falling edge as trigger)
- Sync ... Line junction with Sync INT pin
- $\overline{CLE}$  ... Low (Clamp function ON)
- BLK ... Low (Blanking OFF)

#### 6. Clamp pulse input method

One method, as shown in Application Circuit examples (1) and (2), is to directly input the clamp pulse. The other is to use the built-in monostable multivibrator. The method is selected through SW1. At the PCB shipment it is set to direct input. To use the built-in monostable multivibrator, it is necessary to mount on the CXD1176Q sub board, R and C that determine pulse width.

(Ex. R = 130 k, C = 100 p, Tpw = 2.75  $\mu$ s Typ.)

### Points on the PCB Pattern Layout

1. Set the layout not to have Digital current flow into Analog GND (Part 1). (For 1, See p. 23 Component side diagram.)
2. At CXD1176Q sub board, C<sub>2</sub> and C<sub>3</sub> capacitors serve the important role of bringing out CXD1176Q's full performance.  
There are over 0.1  $\mu$ F (ceramic) capacitors with good high frequency characteristics. Layout as close to the IC as possible.
3. Analog GND (AVss) and Digital GND (DVss) are on a common voltage and power source. Keeping ADC's DVss (Part 2) as close as possible to the voltage supply source will provide better results. That is, a layout where ADC is close to the voltage supply source, is recommended. (For 2, see p. 23 Component side diagram.)
4. ADC samples analog signals at the clock falling edge point. Accordingly clocks supplied to ADC should not have any jitter.
5. The PCB layout shows ADC and DAC's Analog GND independently from the voltage generating source. On this PCB, the layout aims at providing an independent evaluation of ADC and DAC, as much as possible. On the actual board, common use will not cause any problems.

## Notes on Operation

### 1. Reference voltage

Shorting  $V_{RT}$  and  $V_{RTS}$ ,  $V_{RB}$  and  $V_{RBS}$  will activate the self-bias function that generates  $V_{RT} = 2.6\text{ V}$  and  $V_{RB} = 0.5\text{ V}$ . On the PCB, either self-bias or the external reference voltage can be selected depending on the junction method of the jumper line. At shipment from the factory, reference voltage is provided in self-bias. Also, to provide external reference voltage, adjust the dynamic range ( $V_{RT} - V_{RB}$ ) to above 1.8 Vp-p.

### 2. Clock input

There are 2 modes for the PCB clock input

- 1) Provided from the external signal generator. (External clock)
- 2) Using the crystal oscillator (built-in clock driver). (Internal clock)

The 2 modes are selected using the switch on the PCB.

### 3. The 2 Latch IC's (74S174) are not absolutely necessary for the evaluation of ADC and DAC. That is, operation will still be normal if ADC output data is directly input to DAC input. However, as ADC output data is hardly ever D/A converted without executing Digital signal processing, it was mounted to indicate an example layout of Digital signal processing IC.

### 4. When $\overline{\text{clamp}}$ is not used

Turning  $\overline{\text{CLE}}$  to H will set OFF the clamp function. In this case, the DC element is cut off by means of  $C_2$  on the main board and DC voltage on the ADC side of  $C_2$  turns to about  $1/2 (V_{RT} + V_{RB})$ . To transfer DC elements of input signals, short  $C_2$ . At that time, it is necessary to bias input signals, but keeping  $R_2$  open,  $Q_3$  can also be used as buffer. Use the open space for the bias circuit.

### 5. Clamp pulse latch

On the evaluation board, the clamp pulse is latched with ADC sampling CLK and then input to either PW pin or Sync pin. This is to minimize  $V_{sag}$  due the synchronizing of noise and clamp pulse beat elements with GND sampling clock around ADC. If there are no problems with  $V_{sag}$ , latch is not necessary.

### 6. Peripheral through hole

There is a group of through holes on the Analog input, output and Logic. There are to be used when mounting additional circuits to the PCB. Use when necessary.

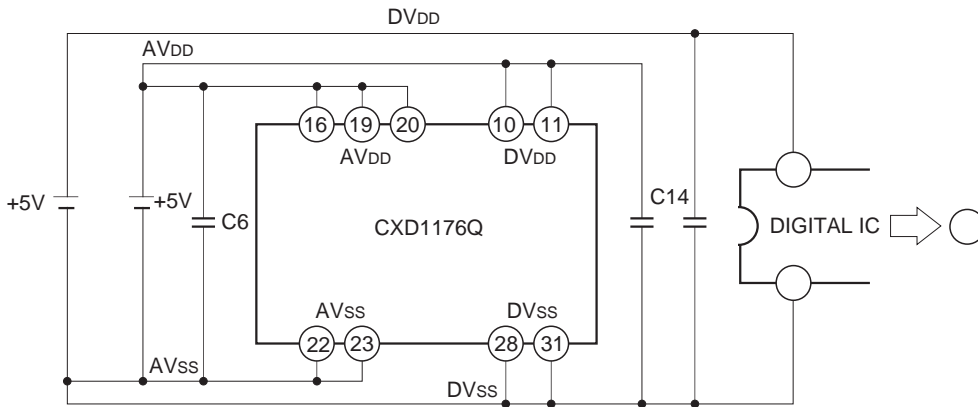
The connector hole on DAC part is used to mount the test chassis and the mount jack.

**Latch Up Prevention**

The CXD1176Q is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV<sub>DD</sub> (Pins 16, 19 and 20) and DV<sub>DD</sub> (Pin 10 and 11), when power supply is ON.

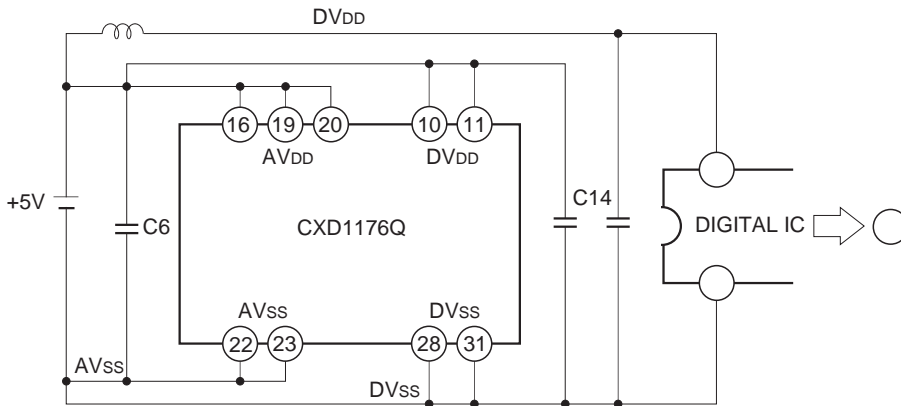
**1. Correct usage**

**a. When analog and digital supplies are from different sources**

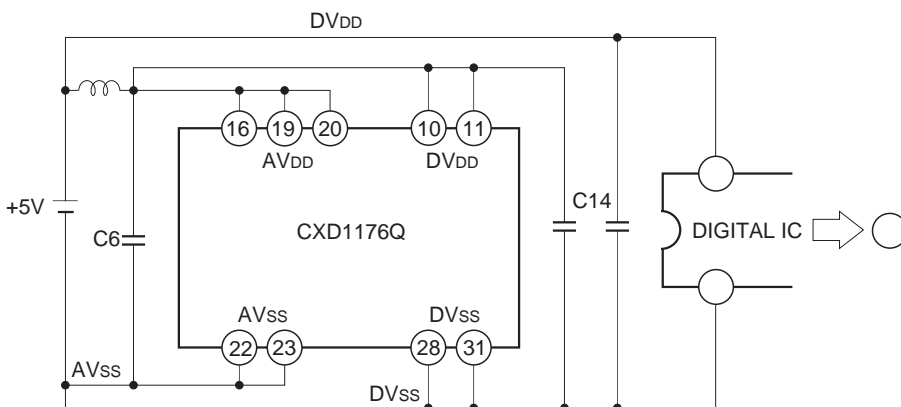


**b. When analog and digital supplies are from a common source**

(i)

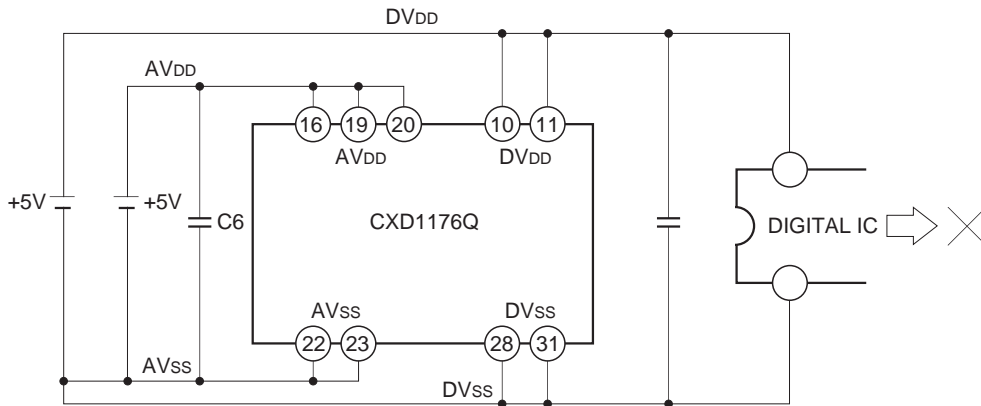


(ii)



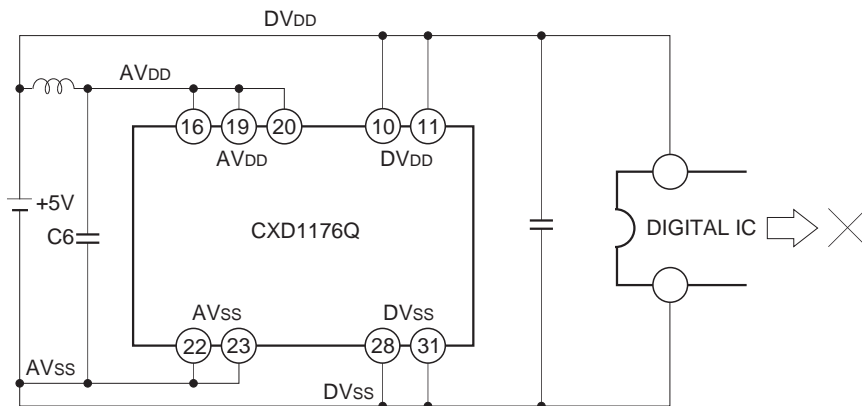
2. Example when latch up easily occurs

a. When analog and digital supplies are from different sources

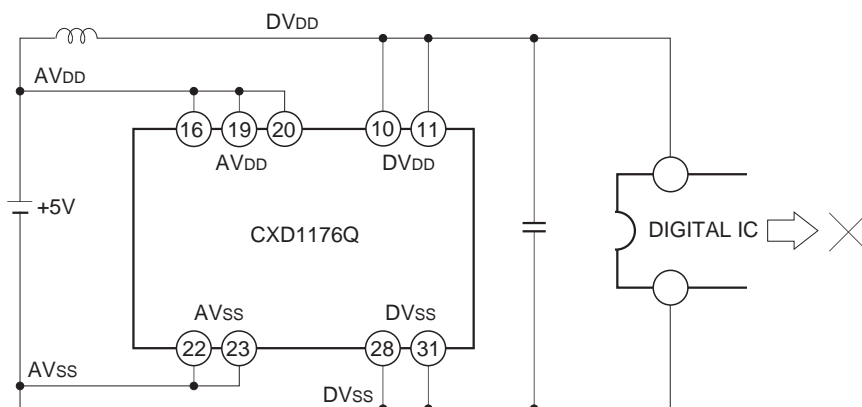


b. When analog and digital supplies are from a common source

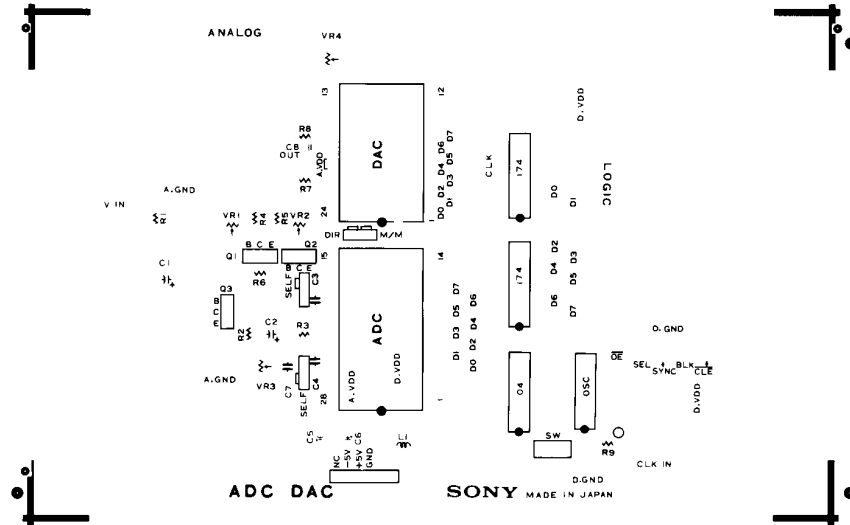
(i)



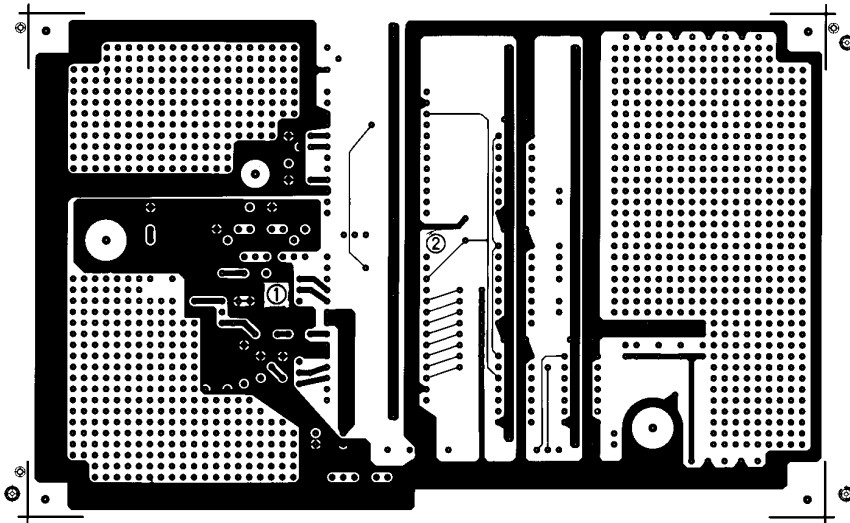
(ii)



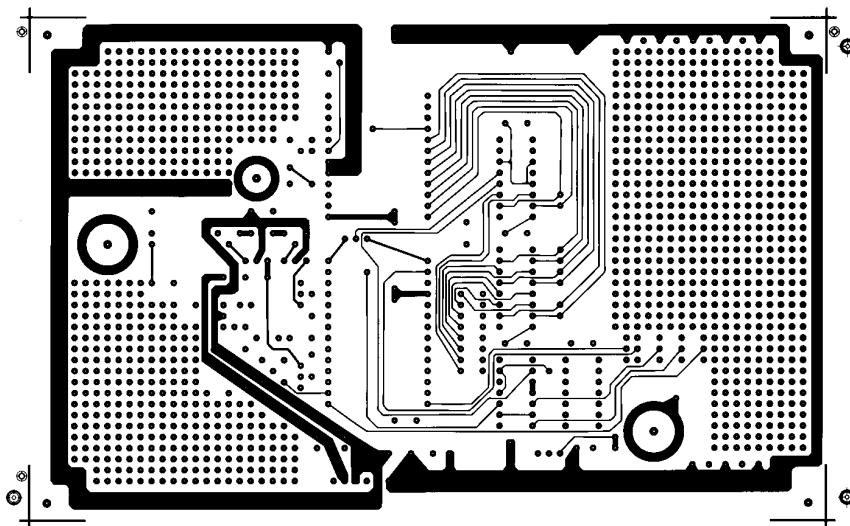
Silk Side



Component Side

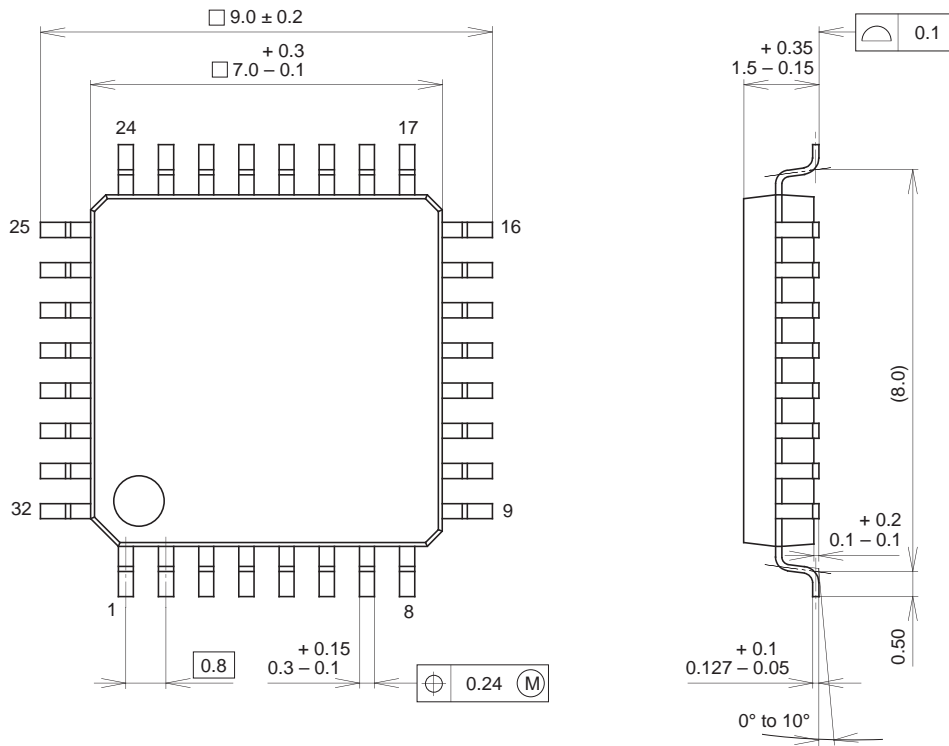


Soldering Side (Diagram seen from the component side)



Package Outline Unit : mm

32PIN QFP (PLASTIC)



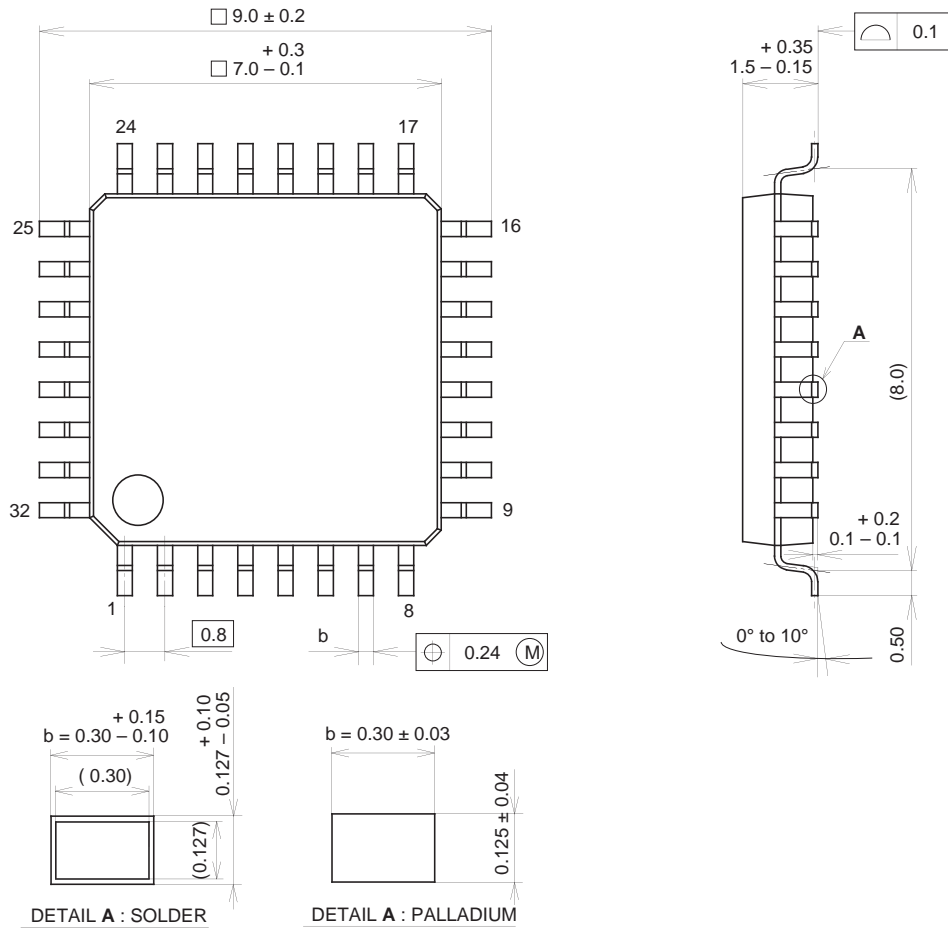
SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g



Package Outline Unit : mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.2g

NOTE : PALLADIUM PLATING

This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).