

CCD Camera Timing Generator

Description

The CXD1257AR generates the timing pulses required by the CCD image sensors as well as signal processing circuits.

Features

- NTSC and PAL compatible
- Electronic shutter function
- H-driver
- Compatible with digital and analog camera systems
- Standby function

Applications

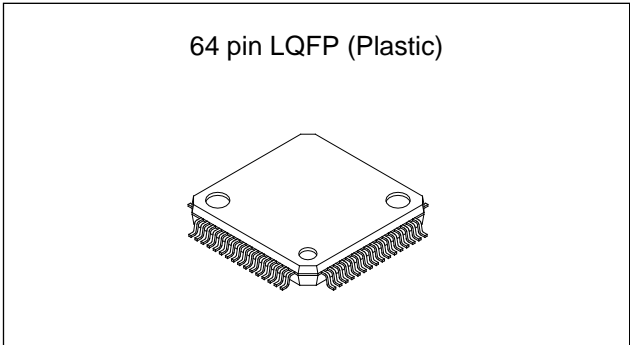
CCD cameras

Structure

Silicon gate CMOS IC

Applicable CCD Image Sensors

- ICX026CKA, ICX027CKA
- ICX054AK, ICX055AK
- ICX056AK



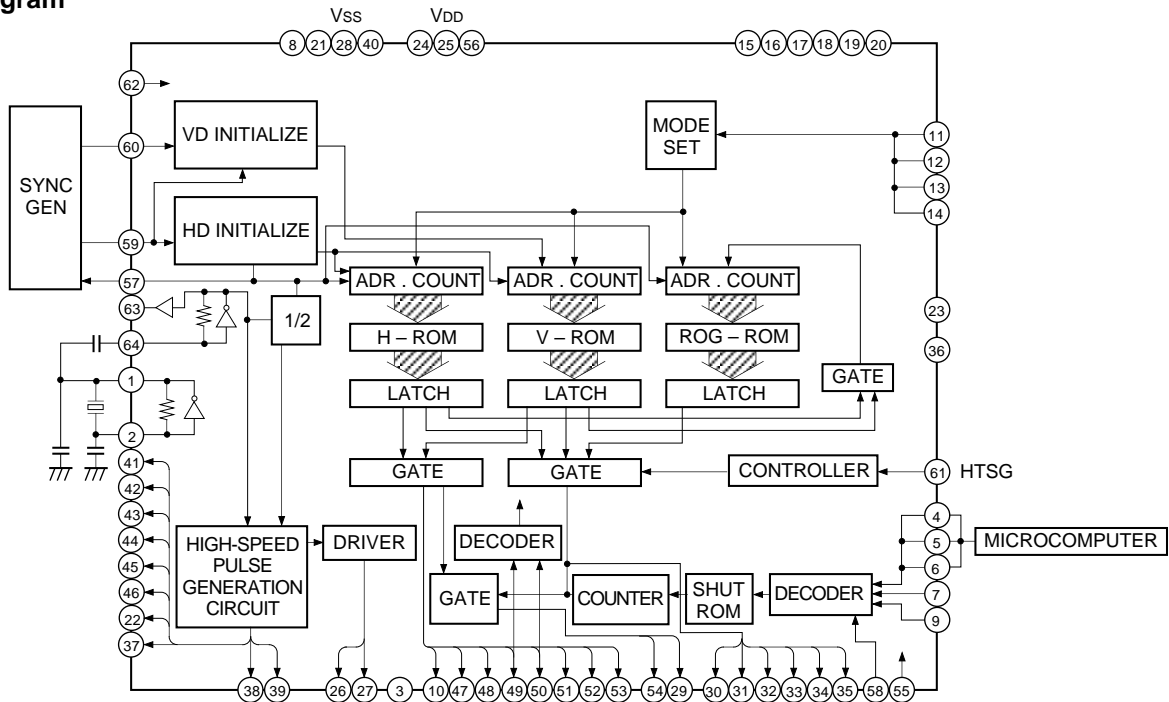
Absolute Maximum Ratings (Ta = 25°C)

- Supply voltage V_{DD} V_{SS} - 0.5 to +7.0 V
- Input voltage V_I V_{SS} - 0.5 to V_{DD} + 0.5 V
- Output voltage V_O V_{SS} - 0.5 to V_{DD} + 0.5 V
- Operating temperature Topr -20 to +75 °C
- Storage temperature Tstg -55 to +150 °C

Recommended Operating Conditions

- Supply voltage V_{DD} 5.0 ± 0.25 V
- Operating temperature Topr -20 to +75 °C

Block Diagram



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Pin Description

Pin No.	Symbol	I/O	Description
1	OSCO	O	Inverter output for oscillation.
2	OSCI	I	Inverter input for oscillation.
3	EF	I	Not used. (With pull-up resistor)
4	ED0	I	Shutter speed setting. Strobe input for serial mode. (With pull-up resistor)
5	ED1	I	Shutter speed setting. Clock input for serial mode. (With pull-up resistor)
6	ED2	I	Shutter speed setting. Data input for serial mode. (With pull-up resistor)
7	SMD1	I	Shutter mode setting. (With pull-up resistor)
8	Vss	—	GND
9	SMD2	I	Shutter mode setting. (With pull-up resistor)
10	XVCT	O	Not used. (Open)
11	D1	I	Fix at Low in normal operation. (With pull-down resistor)
12	D2	I	Fix at Low in normal operation. (With pull-down resistor)
13	D3	I	Fix at Low in normal operation. (With pull-down resistor)
14	D4	I	Low: NTSC, High: PAL. (With pull-down resistor)
15	A5	O	Not used. (Open)
16	A4	O	Not used. (Open)
17	A3	O	Not used. (Open)
18	A0	O	Not used. (Open)
19	A1	O	Not used. (Open)
20	A2	O	Not used. (Open)
21	Vss	—	GND
22	RG	O	Reset gate pulse output.
23	NC	—	
24	V _{DD}	—	Power supply.
25	V _{DD}	—	Power supply for H1 and H2.
26	H1	O	Clock output for CCD horizontal register drive.
27	H2	O	Clock output for CCD horizontal register drive.
28	Vss	—	GND for H1 and H2.
29	XSUB	O	CCD discharge pulse output.
30	XV2	O	Clock output for CCD vertical register drive.
31	XV1	O	Clock output for CCD vertical register drive.
32	XSG1	O	CCD sensor charge readout pulse output.
33	XV3	O	Clock output for CCD vertical register drive.
34	XSG2	O	CCD sensor charge readout pulse output.
35	XV4	O	Clock output for CCD vertical register drive.

Pin No.	Symbol	I/O	Description
36	TEST2	I	Test input. Set at Low in normal operation.
37	MCK	O	NTSC: 1820f _H /3, PAL: 1816f _H /3. Output.
38	XSHP	O	Precharge level sample-and-hold pulse.
39	XSHD	O	Data sample-and-hold pulse.
40	V _{SS}	—	GND
41	XSP1	O	Color separation sample-and-hold pulse.
42	XSP2	O	Color separation sample-and-hold pulse.
43	XSH1	O	Switching sample-and-hold pulse.
44	XSH2	O	Switching sample-and-hold pulse.
45	XDL1	O	Delay line clock output.
46	XDL2	O	Delay line clock output.
47	BFG	O	Pulse output for chroma modulator in encoder.
48	CLP1	O	Clamp pulse output.
49	CLP2	I/O	Clamp pulse output. When GM is set at High, standby mode switching input.
50	CLP3	I/O	Clamp pulse output. When GM is set at High, standby mode switching input.
51	CLP4	O	Clamp pulse output.
52	PBLK	O	Blanking cleaning pulse output.
53	ID	O	Line identification output.
54	WEN	O	Write enable output for low-speed shutter operation.
55	GM	I	Low: Analog signal processing, High: Digital signal processing. (With pull-down resistor)
56	V _{DD}	—	Power supply.
57	CL	O	NTSC: 910f _H , PAL: 908f _H . Clock output.
58	PS	I	Switching for electronic shutter speed input method. (With pull-up resistor) Low: Serial input, High: Parallel input.
59	HD	I	Horizontal synchronizing signal input.
60	VD	I	Vertical synchronizing signal input. (During Low, 9H for NTSC and 7.5H for PAL)
61	HTSG	I	Control input for XSG1 and XSG2. (With pull-up resistor) Low: XSG1, XSG2 halted, High: XSG1, XSG2 generated.
62	TEST	I	Test input. Set at Low in normal operation. (With pull-down resistor)
63	XCK	O	NTSC: 1820f _H , PAL: 1816f _H . Clock output.
64	CK	I	NTSC: 1820f _H , PAL: 1816f _H . Clock input.

Electrical Characteristics

DC Characteristics

(V_{DD} = 5V ± 0.25V, T_{opr} = -20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V _{DD}		4.75	5.0	5.25	V
Input voltage 1 (Input pins other than those below)	V _{IH1}		0.7V _{DD}			V
	V _{IL1}				0.3V _{DD}	V
Input voltage 2 (Pins 59 and 60)	V _{IH2}		2.2			V
	V _{IL2}				0.8	V
Output voltage 1 (Output pins other than those below)	V _{OH1}	I _{OH} = -2mA	V _{DD} - 0.5			V
	V _{OL1}	I _{OL} = 4mA			0.4	V
Output voltage 2 (Pins 22, 37, 38, 39, 57, and 63)	V _{OH2}	I _{OH} = -4mA	V _{DD} - 0.5			V
	V _{OL2}	I _{OL} = 8mA			0.4	V
Output voltage 3 (Pins 26 and 27)	V _{OH3}	I _{OH} = -8mA	V _{DD} - 0.5			V
	V _{OL3}	I _{OL} = 8mA			0.4	V
Output voltage 4 (Pin 1)	V _{OH4}	I _{OH} = -1mA	V _{DD} /2			V
	V _{OL4}	I _{OL} = 1mA			V _{DD} /2	V
Feedback resistor	R _{FB}	V _{IN} = V _{SS} or V _{DD}	500k	2M	5M	Ω
Pull-up resistor	R _{PU}	V _{IL} = 0V	40k	100k	250k	Ω
Pull-down resistor	R _{PD}	V _{IH} = V _{DD}	40k	100k	250k	Ω

I/O Pin Capacitances

(V_{DD} = V_I = 0V, f_m = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C _{IN}			9	pF
Output pin capacitance	C _{OUT}			11	pF
I/O pin capacitance	C _{I/O}			11	pF

Description of Operation**1. Mode Control**

Symbol	Pin No.	L	H
GM	55	Analog signal processing	Digital signal processing
PS	58	Serial shutter speed setting	Parallel shutter speed setting
EF	3	Fix at High in normal operation	
HTSG	61	XSG1, 2 OFF	XSG1, 2 ON
D1	11	Fix at Low in normal operation	
D2	12	Fix at Low in normal operation	
D3	13	Fix at Low in normal operation	
D4	14	NTSC	PAL

2. Changes in I/O Signals in Each Mode

Symbol	Pin No.	Analog color	Digital color 1	Digital color 2
GM	55	L	H	H
D2	12	L	L	L
TEST2	36	L	L	H
XSP1	41	Color separation sample-and-hold pulse output	Halted at High	Color separation sample-and-hold pulse output
XSP2	42	Color separation sample-and-hold pulse output	Halted at High	Color separation sample-and-hold pulse output
XSH1	43	Switching sample-and-hold pulse output	Halted at Low	Switching sample-and-hold pulse output
XSH2	44	Switching sample-and-hold pulse output	Halted at Low	Switching sample-and-hold pulse output
XDL1	45	Delay line clock	Halted at High	Halted at High
XDL2	46	Delay line clock	Halted at Low	Halted at Low
BFG	47	Burst flag gate pulse output	Burst flag gate pulse output (normally not used)	Burst flag gate pulse output (normally not used)
CLP2	49	Clamp pulse output	Standby control input Low: Standby High: Normal operation	Standby control input Low: Standby High: Normal operation
CLP3	50	Clamp pulse output	Standby control* Low: All circuits halted for standby mode High: Only CL output for standby mode	Standby control* Low: All circuits halted for standby mode High: Only CL output for standby mode
ID	53	Line identification output	Line identification output	Line identification output

* When CLP2 = High, normal operation occurs regardless of whether CLP3 is high or low.
(Mode combinations other than those shown above cannot be used.)

Note) In the standby mode described above, XCK, XSG1, XSG2, XV1, XV2, XV3, XV4, XSUB, H1, H2, RG, XSHD, XSHP, XSP1, XSP2, XSH1, XSH2, XDL1, and XDL2 pins are halted at Low. MCK, CLP1, CLP4, PBLK, ID, XVCT, WEN, BFG, A0, A1, A2, A3, A4, and A5 pins are halted at the state just before standby.

3. Electronic Shutter

The operation of the electronic shutter is controlled by the output of XSUB pulse during particular intervals.

<Shutter Modes>

SMD1 SMD2

- L L Flickerless: Eliminates fluorescent frequency-induced flicker.
- L H High-speed shutter: Shutter speed faster than 1/60 (NTSC), 1/50 (PAL)
- H L Low-speed shutter: Shutter speed slower than 1/60 (NTSC), 1/50 (PAL)
- H H No shutter operation.

<Shutter Mode and Speed Setting Method>

PS = High: Parallel input; set by ED0 to ED2, SMD1, and SMD2.

PS = Low: Serial input; set by inputting ED0 (strobe), ED1 (clock), and ED2 (data) to each pin.

3-1. Parallel input (PS = H)

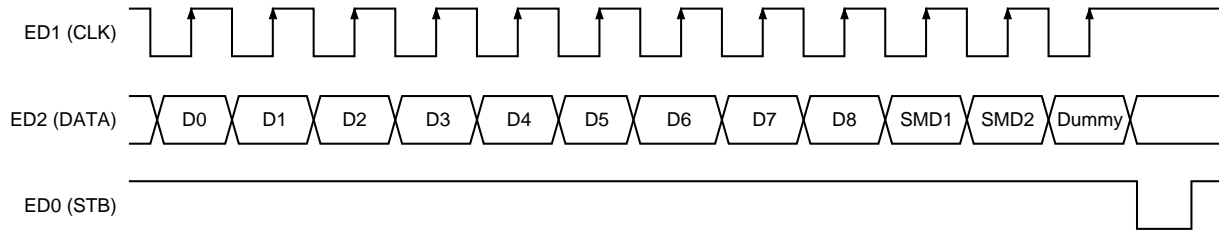
Shutter Speed Compatibility Chart

Mode	NTSC/PAL	SMD1	SMD2	ED0	ED1	ED2	Shutter speed
OFF	X	H	H	X	X	X	Shutter off
Flickerless	NTSC	L	L	X	X	X	1/100 (s)
	PAL	L	L	X	X	X	1/120 (s)
High-speed shutter	NTSC	L	H	H	H	H	1/60 (s)
	PAL	L	H	H	H	H	1/50 (s)
	X	L	H	L	H	H	1/125 (s)
	X	L	H	H	L	H	1/250 (s)
	X	L	H	L	L	H	1/500 (s)
	X	L	H	H	H	L	1/1000 (s)
	X	L	H	L	H	L	1/2000 (s)
	X	L	H	H	L	L	1/4000 (s)
	X	L	H	L	L	L	1/10000 (s)
Low-speed shutter	X	H	L	H	H	H	2FLD
	X	H	L	L	H	H	4FLD
	X	H	L	H	L	H	6FLD
	X	H	L	L	L	H	8FLD
	X	H	L	H	H	L	10FLD
	X	H	L	L	H	L	12FLD
	X	H	L	H	L	L	14FLD
	X	H	L	L	L	L	16FLD

3-2. serial input (PS = L)

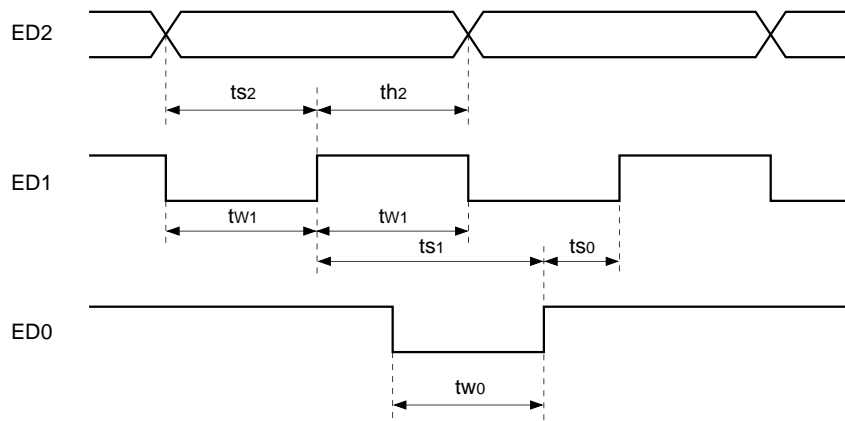
For serial input (PS = L), SMD1 and SMD2 bits within ED2 (DATA) take priority over SMD1 (Pin 7) and SMD2 (Pin 9) pins as SMD1 and SMD2 (shutter mode control).

In this case, control by SMD1 and SMD2 pins is invalid.



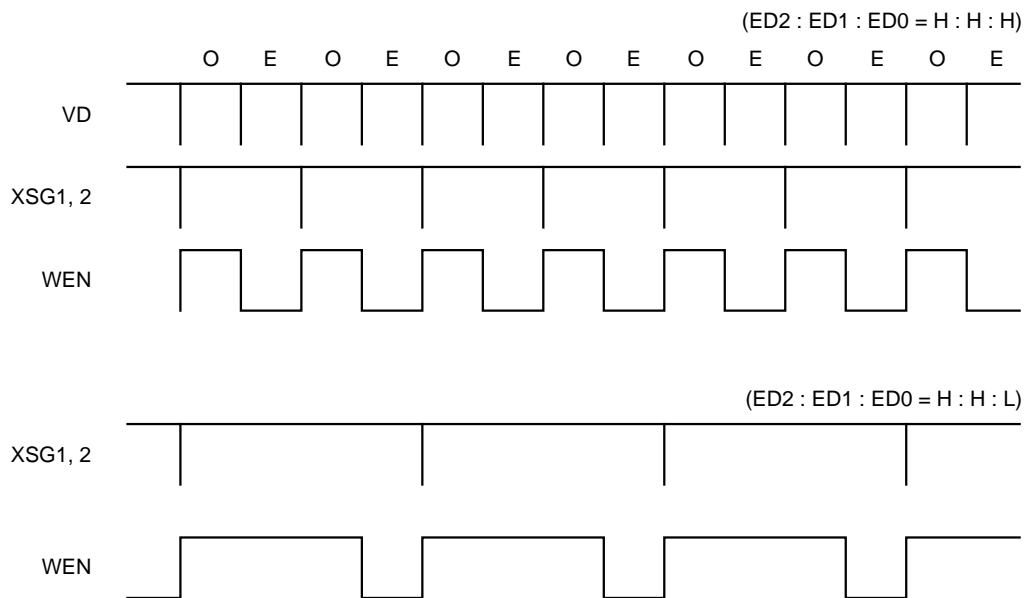
ED2 data is latched to the register at the rise of ED1, and transferred to the within during the Low period of ED0.

AC Characteristics



Symbol		Min.	Max.
ts_2	ED2 set-up time, activated by the rising edge of ED1	20ns	—
th_2	ED2 hold time, activated by the rising edge of ED1	20ns	—
ts_1	ED1 rising set-up time, activated by the rising edge of ED0	20ns	—
tw_0	ED0 pulse width	20ns	50 μ s
ts_0	ED0 rising set-up time, activated by the rising edge of ED1	20ns	—
tw_1	ED1 pulse width (serial input)	20ns	—

3-4. Low-speed shutter timing chart



3-5. Shutter speed calculation formula

High-speed shutter

- NTSC

$$T = [262_{10} - (1FF_{16} - L_{16})] \times 63.56 + 32.37\mu s \quad (L_{16} = \text{Load value})$$

- PAL

$$T = [312_{10} - (1FF_{16} - L_{16})] \times 64 + 32.14\mu s$$

NTSC			PAL		
Load value	Shutter speed	Calculated value	Load value	Shutter speed	Calculated value
0FA ₁₆	1/10000	1/10424	0C8 ₁₆	1/10000	1/10401
0FC ₁₆	1/4000	1/4483	0CA ₁₆	1/4000	1/4461
100 ₁₆	1/2000	1/2095	0CE ₁₆	1/2000	1/2083
108 ₁₆	1/1000	1/1014	0D6 ₁₆	1/1000	1/1008
118 ₁₆	1/500	1/499	0E6 ₁₆	1/500	1/496
137 ₁₆	1/250	1/252	105 ₁₆	1/250	1/250
176 ₁₆	1/125	1/125	143 ₁₆	1/125	1/125
196 ₁₆	1/100	1/100	149 ₁₆	1/120	1/120

Low-speed shutter

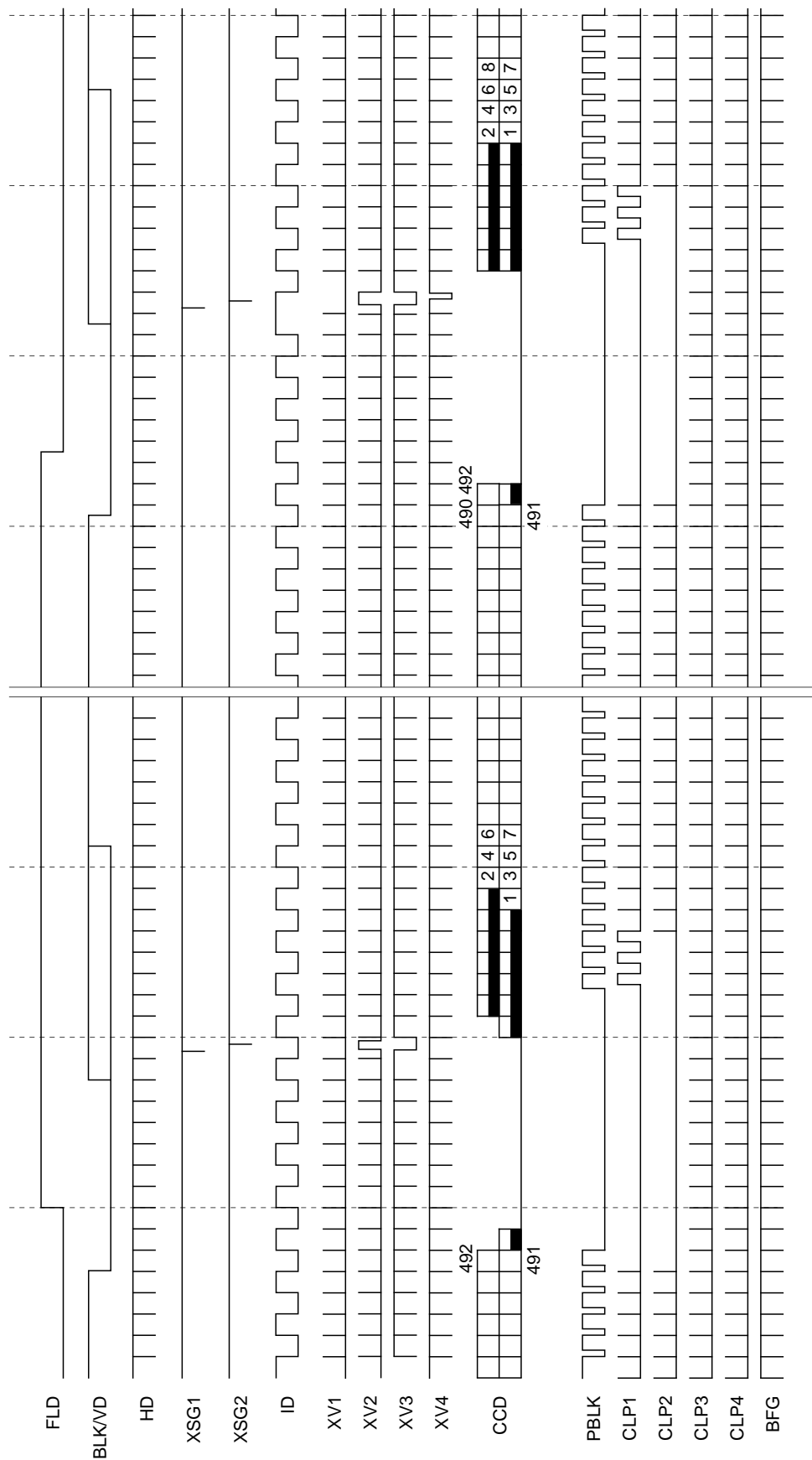
Shutter speed calculation formula

$$N = 2 \times (1FF_{16} - L_{16}) \text{ FLD}$$

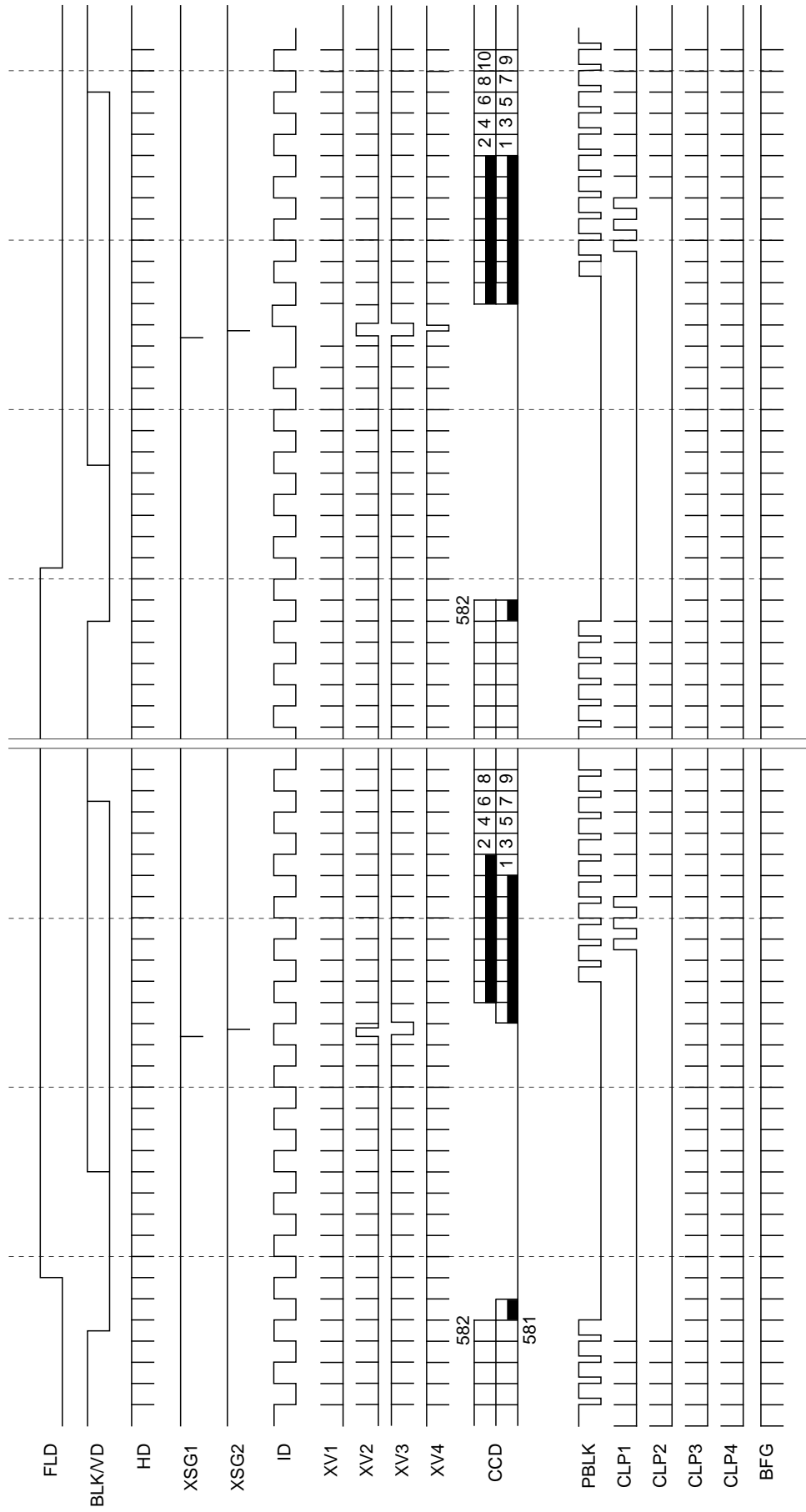
However, "1FF" cannot be used as the load value.

Load value	Shutter speed (FLD)
1FE ₁₆	2
1FD ₁₆	4
⋮	⋮
⋮	⋮
101 ₁₆	508
100 ₁₆	510

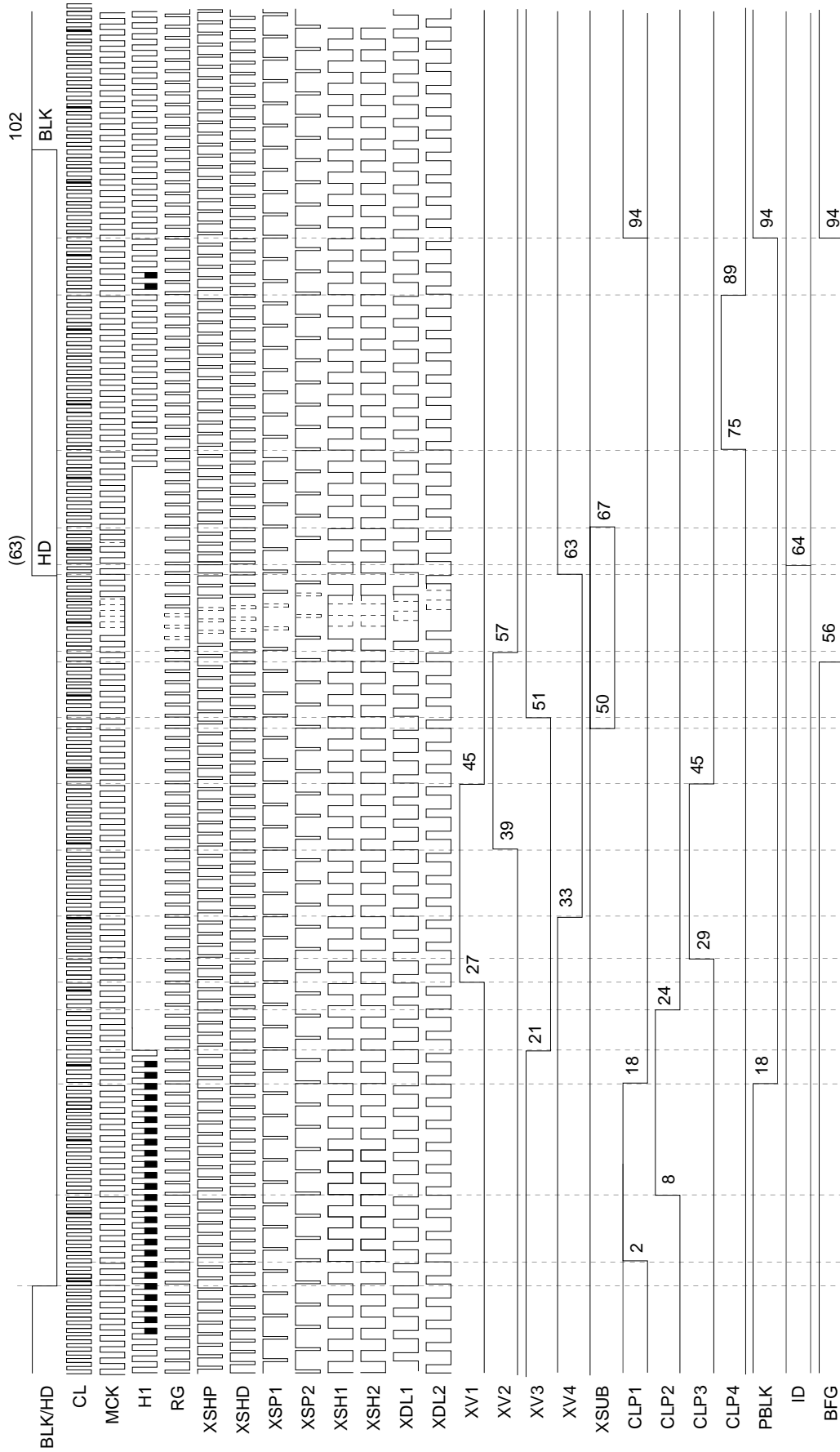
Timing Chart (1)
NTSC vertical direction



Timing Chart (2)
PAL vertical direction

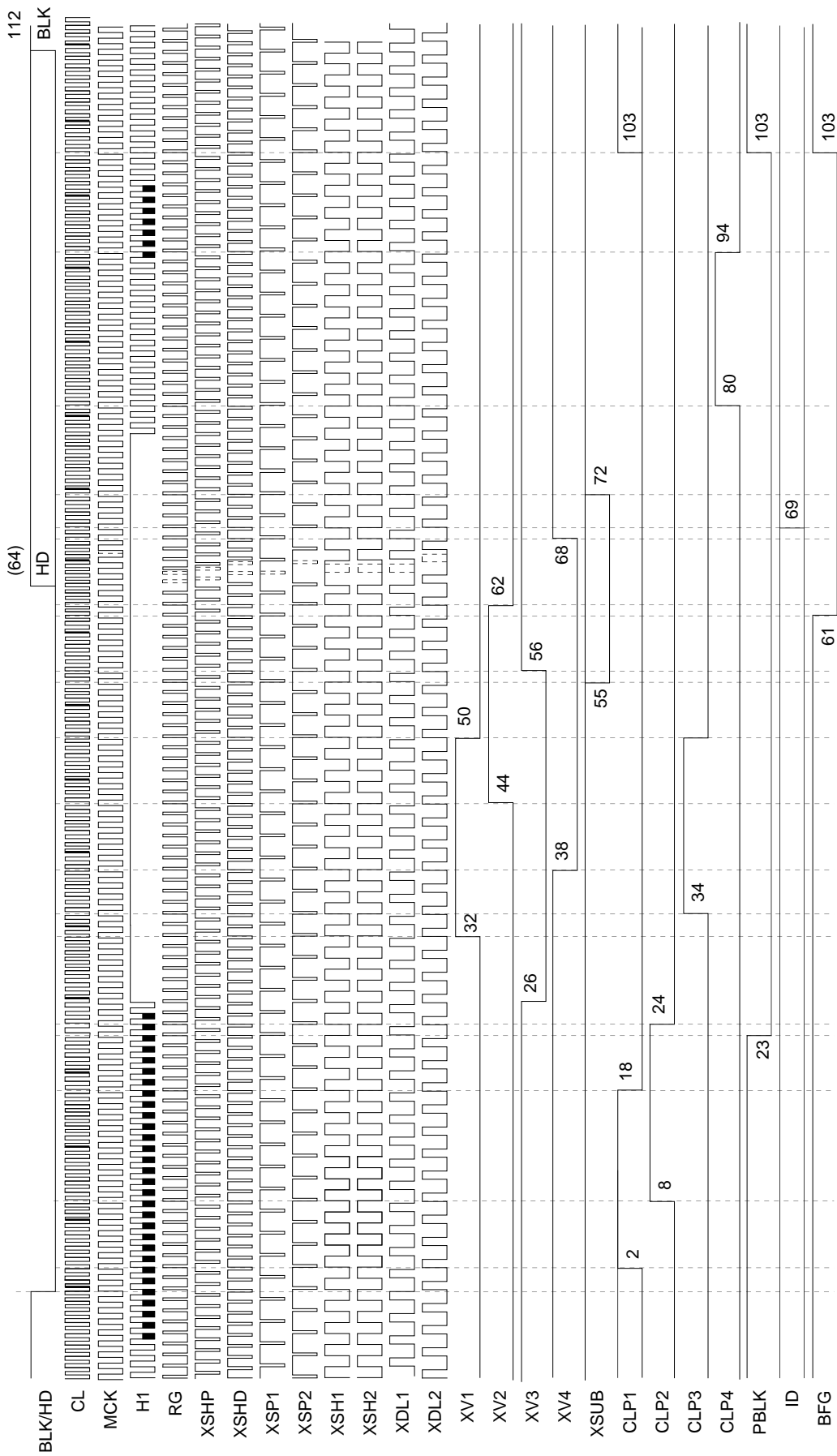


Timing Chart (3)
NTSC horizontal direction



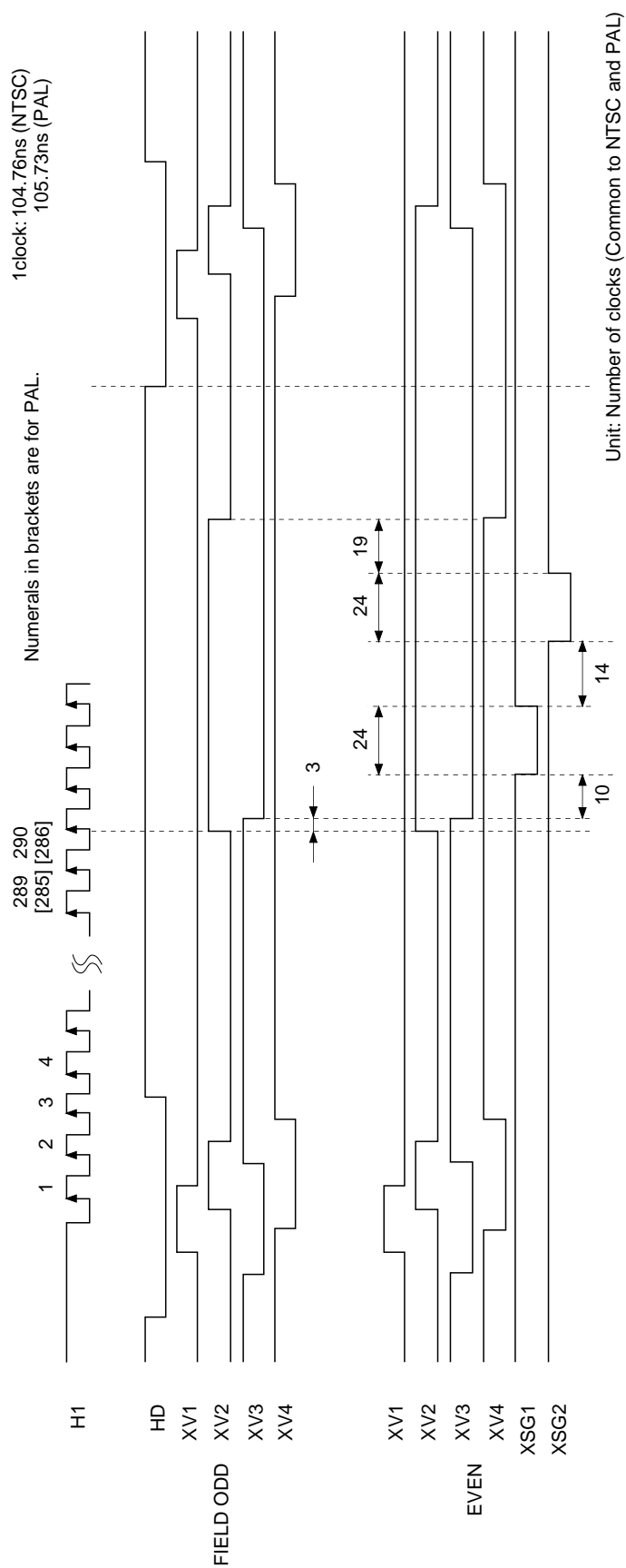
Black painted portions of H1 clock indicate the optical black.

Timing Chart (4)
PAL horizontal direction

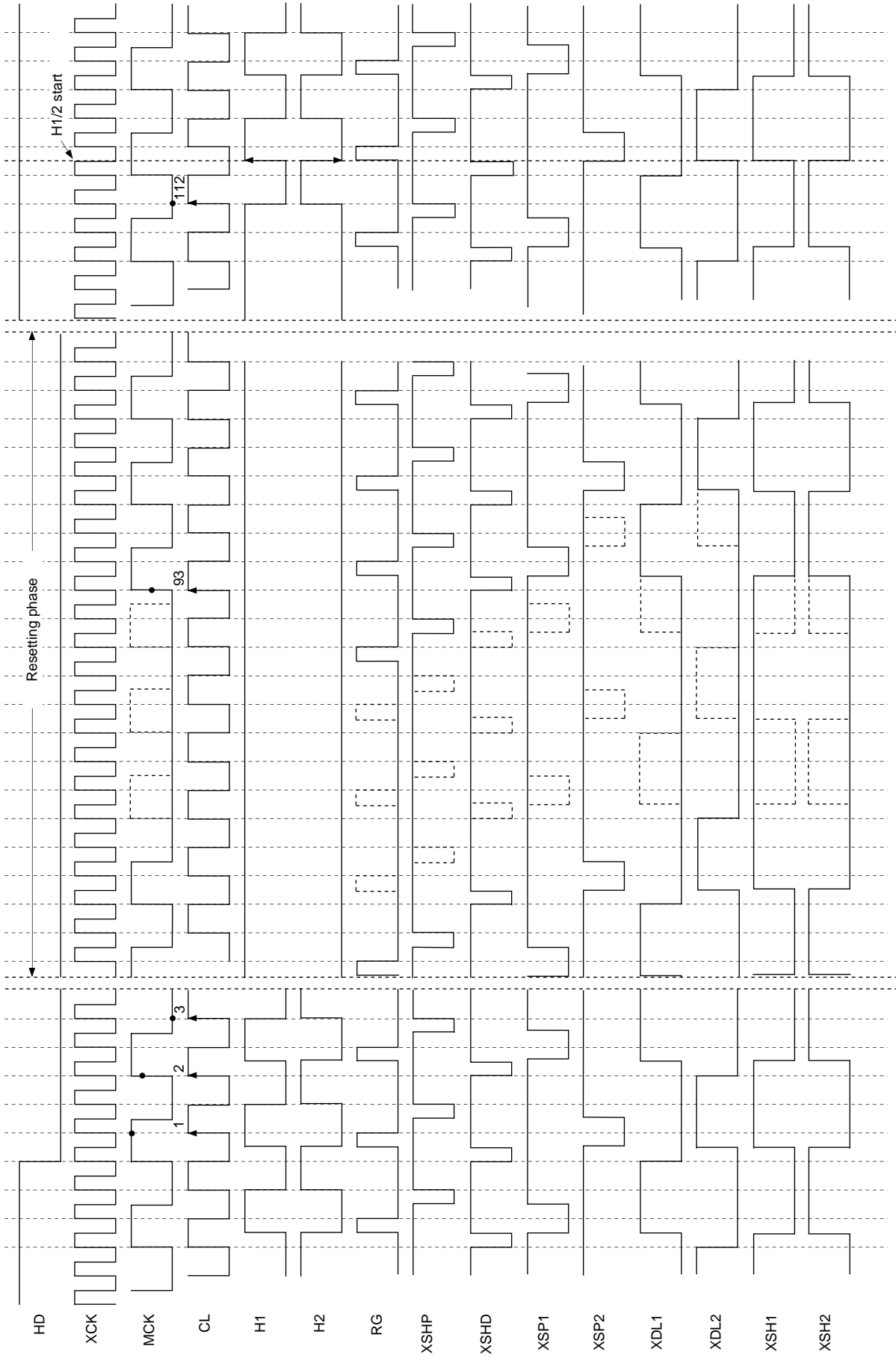


Black painted portions of H1 clock indicate the optical black.

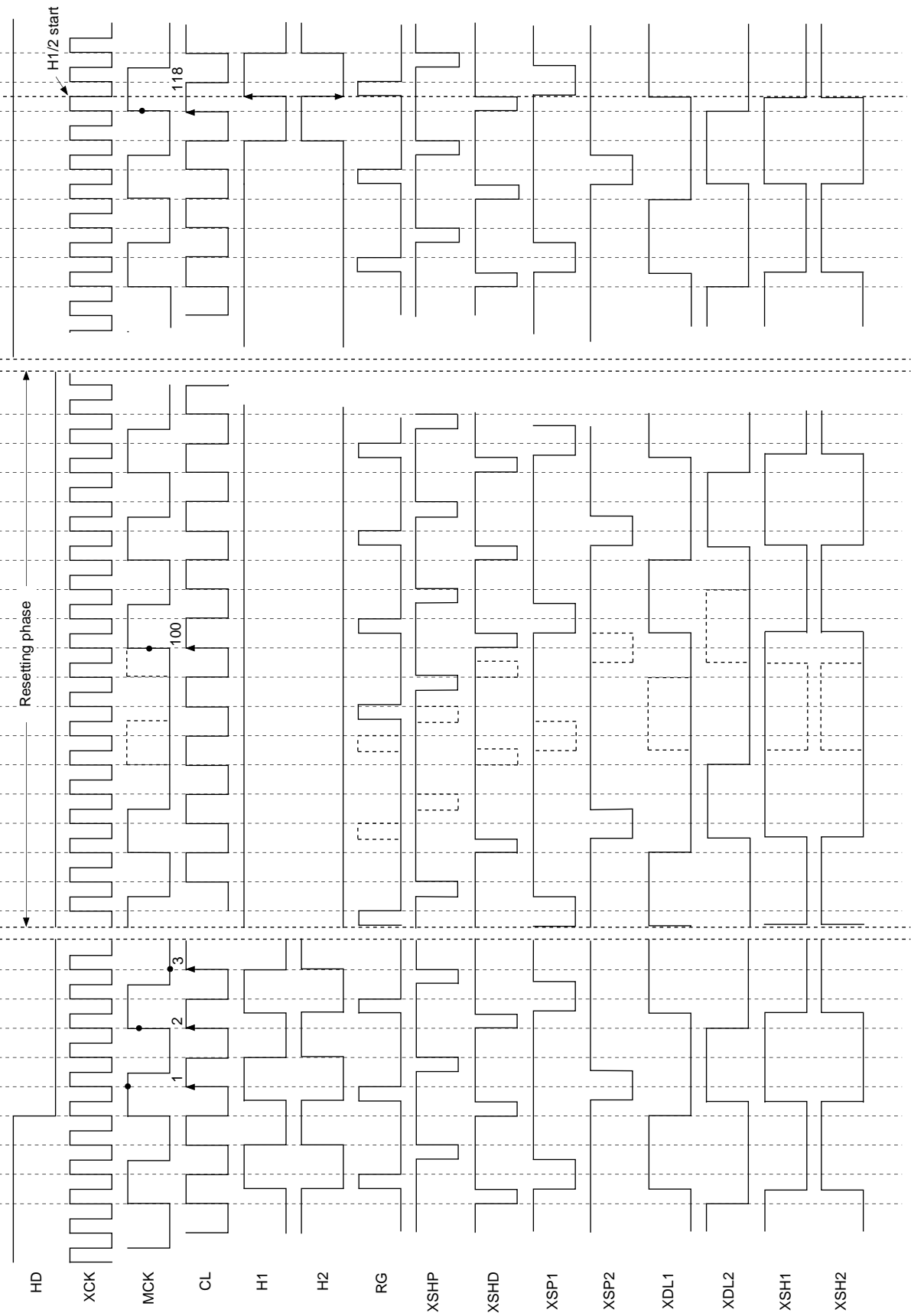
Timing Chart of Readout (NTSC/PAL)



Timing Specifications of Resetting Phase and H1/2 Start — High-speed Waveform (NTSC)



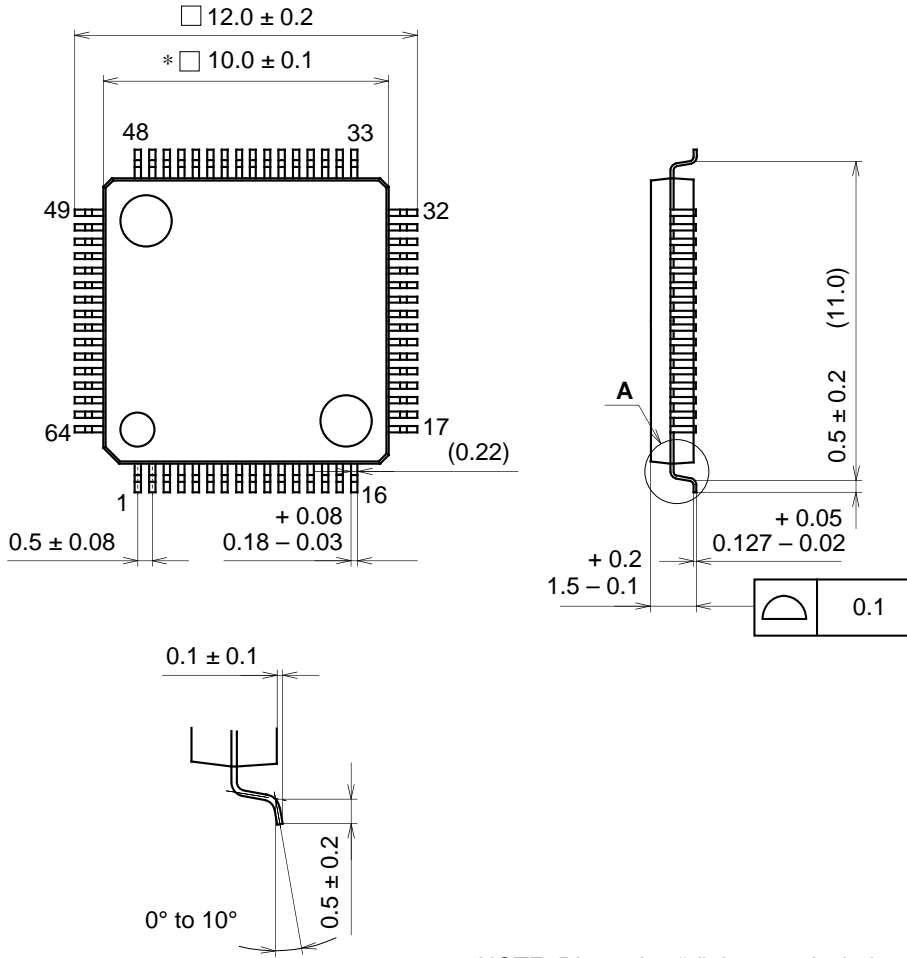
Timing Specifications of Resetting Phase and H1/2 Start — High-speed Waveform (PAL)



Package Outline

Unit: mm

64PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

DETAIL A

PACKAGE STRUCTURE

SONY CODE	LQFP-64P-L01
EIAJ CODE	LQFP064-P-1010
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.3g