

MPEG Video Decoder

Description

The CXD1930Q was developed to provide an integrated, low-cost solution for DVD player and DVB set-top-box (STB) applications. This single chip device combines all of the logic for handling source materials which DVD and DVB systems require.

The CXD1930Q integrates a RISC controller and, with nano-OS™ (Sony's proprietary operating system), and provides advanced trick plays (e.g. no-skipping B reverse), robust audio-video synchronization and error concealment features.

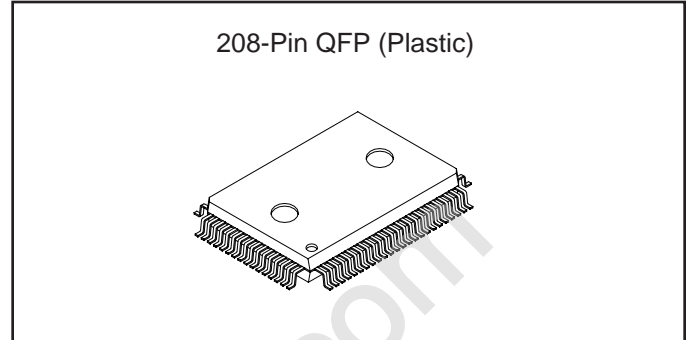
The CXD1930Q offers a cost-effective solution to DVD player, DVB STB and DVD PC applications.

Features

- MPEG1 and MPEG2 (MP@ML) video decoder
- MPEG1, MPEG2 (layer I, II: 5+1 channels) and Dolby Digital™ decoder (5+1 channels), linear PCM output
- Sub-picture decoding
- DVD, VCD, DVB demultiplexing: up to 72Mbps
- Letter box pan-scan output
- On-screen display up to 256 colors
- Teletext output
- DVD standard compliant decoder

The CXD1930Q also integrates:

- NTSC/PAL video encoder with Macrovision™ copy protection, closed-caption, and 10-bit 6-channel DAC
- Off-chip NTSC/PAL video encoder 8-bit interface
- Off-chip host CPU interface (Hitachi SH* and Motorola 68K series CPU bus interface)
- Direct SDRAM interface of 16 bits, with a maximum 81MHz clock rate



Outline of Major Features

The CXD1930Q incorporates the MPEG1/MPEG2 video decoder, MPEG1/MPEG2/Dolby Digital audio decoder, embedded RISC controller, programmable pre-processor for system streams, programmable display controller, sub-picture decoder, configurable host-interface, NTSC/PAL video encoder and high-quality OSD feature. In this section, a brief overview of each distinguishing feature of the CXD1930Q functions is described.

[1] MPEG Video Decoder

1. Decodes MPEG1 (ISO 11172-2) and MPEG2 (MP@ML) (ISO 13818-2) bit streams. The image size of CCIR601 resolution is 720x480 pixels @30fps for NTSC and 720x576 @25fps for PAL.
2. 2.53 frame PAL decoding, with 16Mbits SDRAM configuration is supported (PAL decoding) with high quality AV synchronization.
3. Automatic 3:2 pull down
4. Proprietary patented error concealment by micro code with on-chip RISC software.
5. Advanced trick play (reverse on B frames, etc.) by micro code (on-chip RISC software).

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Dolby Digital is a trademark of Dolby Laboratories.

Macrovision is a trademark of Macrovision Corporation.

[2] On-chip Audio Decoder

1. MPEG1 (ISO 11172-3) and MPEG2 (ISO 13818-3) (up to 5+1 channels) (layer I and II) supporting bit rates of up to 912Kbps (with extension bit stream).
2. Dolby Digital (up to 5+1 channels), supporting bit rates of up to 448Kbps. Down-mixing to two outputs is possible.
3. Supports linear PCM data.
4. IEC958 output interface for audio data and Dolby Digital bit streams (S/PDIF output).

The audio decoder of the CXD1930Q is designed with proprietary Digital Signal Processor (DSP) technology so that it can support various audio standards. MPEG2 and Dolby Digital software will be provided.

[3] Letter Box Filter (LBX)

1. Letter box format display/non-letter box format display
2. 4:2:0 to 4:2:2 chroma interpolation filter
3. Alpha blending
4. Pan-Scan: 1/8 pixel resolution

[DVD mode]

- 720 x 480 (NTSC) / 576(PAL) field display
- 720 x 480(NTSC / 576(PAL) letter box (vertical x 3/4)
- 720 x 480(NTSC) / 576(PAL) Pan-Scan

[VCD mode]

- NTSC → PAL conversion (spatial and temporal)
- PAL → NTSC conversion (decimation) (spatial and temporal)

NTSC → PAL and PAL → NTSC conversion keeps the audio-video synchronization.

[4] High Quality OSD and Sub-Picture Decoder

1. 2bpp and 4bpp OSD: up to full size in frame resolution
2. 8bpp OSD: up to full size in field resolution
 - Size of OSD window is dependent on the size of OSD buffer allotted in SDRAM.
3. The CXD1930Q supports SUBPICTURE decoding. The sub-picture decoder can be used as the second OSD unit (software controlled): 2bpp and 4bpp OSD. This OSD option provides users the ability to add a cursor-like pointer on top of another OSD window or video image.

[5] On-Chip DEMUX

The CXD1930Q's DEMUX will support DVD, VCD bit streams and MPEG2 Transport Stream (e.g. for DVB applications) up to 72Mbps.

[DVD]

- DVD standard-compatible. Also, DEMUX parses VCD bit streams.

[MPEG2 Transport Stream Demultiplexing: DVB]

- MPEG2 transport stream (byte-aligned) parser: 32 PID filters, 16 sector hardware filters, PCR processing and teletext filters.

[6] Host Interface

1. Interface to Hitachi SH* and Motorola 68K series CPU.
2. A maximum of 8Mbytes of linear address space is required for the CXD1930Q address space.. The HOST CPU can access all SDRAM address space and the CXD1930Q internal registers directly (direct-addressing).
3. As the HOST data bus, 8-bit and 16-bit configurations are both supported (on-the-fly configurable).
4. DMA write channel: the HOST CPU can write data to the SDRAM local memory via the DMA channel.
5. Block read (pre-fetch read) is provided when the HOST is accessing SDRAM.

[7] SDRAM Interface

1. Supports NEC, Fujitsu, Hitachi and various other vendors' SDRAM.
2. 16Mbit single (16-bit bus) SDRAM up to 81MHz.

[8] On-Chip Video Encoder (VENC) and Off-Chip VENC Interface

The CXD1930Q has the CXD1914Q which is Sony's equivalent NTSC/PAL video encoder. The CXD1914Q feature supports:

1. NTSC/PAL encoder mode
2. Composite video, separate Y/C video (S-video output)
3. RGB/YUV (BetaCam/SMPTE level) signal out
4. 10-bit, 6-channel DAC
5. Closed caption encode
6. Macrovision pay-per-view protection system (NTSC Rev. 7.0, PAL Rev. 6.1)

7. VBI encode
8. WSS encode

The CXD1930Q also has off-chip NTSC/PAL video encoder interface so that when the Macrovision feature is updated and users wish to use the updated Macrovision, they can easily and quickly reconfigure the systems (products).

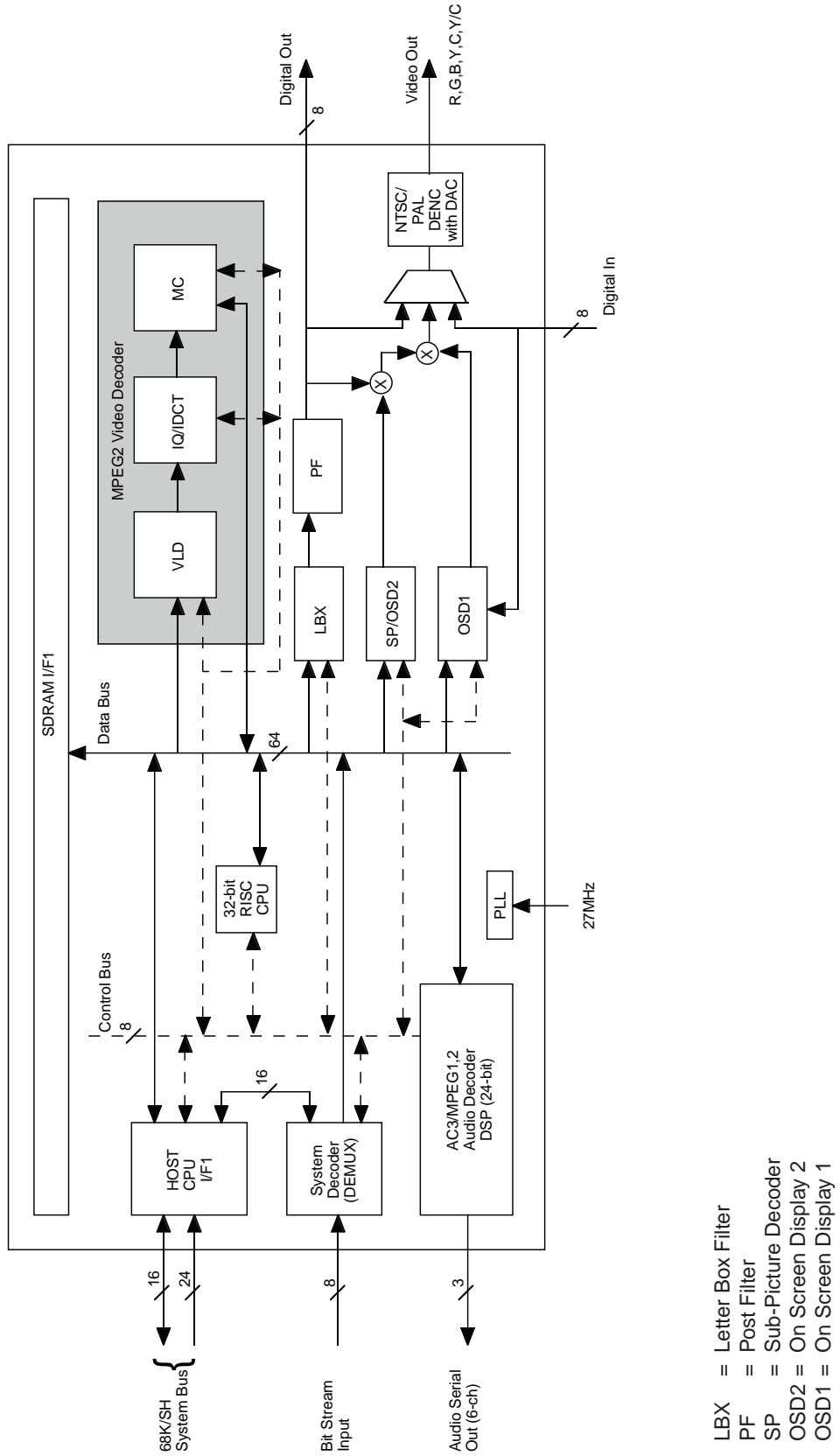
[9] On-Chip PLL

The CXD1930Q integrates on-chip PLL for the SDRAM and internal system (27MHz).

[10] Physical Spec

1. Total number of pins: 208
2. Package: PQFP
 - lead pitch: 0.5mm
 - depth: 28.0mm
 - width: 28.0mm
 - height: 3.45mm
3. Power dissipation: less than 1.2W
3. CMOS process: ASC5 (Sony) [0.4 μ m, 3-layer metal]
4. Supply voltage: 3.3V both digital and analog (separate power source)

Figure 1. Block Diagram



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