SONY

CXD1958Q

MMDS TCM/QAM Demodulator + FEC + ADC *Preliminary*

Description

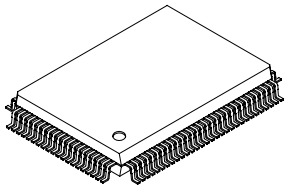
The CXD1958Q is an integrated TCM/QAM demodulator for MMDS systems using the DAVIC MMDS standard. This highly integrated device incorporates an internal 8-bit ADC, image rejection and root-raised cosine filters, all-digital symbol timing recovery PLL, adaptive decision feedback equalizer (DFE) with 10 feedforward and 30 feedback taps, 4-D TCM decoder, and DAVIC/DVB compliant forward error correction comprising (204,188) Reed Solomon decoder, a programmable de-interleaver with I = 12 and I = 204, and a de-randomiser. All internal clocks are generated from a single external 30MHz reference crystal.

Device functionality also includes 3-wire bus interface for configuring up to 2 tuner synthesizers, a sigma delta tuner IF-AGC output, a user programmable RF-AFC sigma delta output, spectrum inversion of the received signal for tuner compatibility, and a highly configurable MPEG2-TS interface. An I^2C bus interface provides on-board configuration and status monitoring of various functions including access to the equalizer tap values and constellation points. JTAG provides boundary scan test compatibility.

Features

- DAVIC MMDS V1.1 and V1.3 compliant
- Supports 16, 64 and 256QAM
- Supports 16, 64 and 256 TCM
- Internal 8-bit ADC
- Interface for 10-bit external ADC
- 36.125MHz nominal IF input
- Symbol rate range 5 – 5.304Mbaud in 6MHz channels
- Integrated matched filtering with 0.15 roll-off factor
- ±400KHz internal carrier offset compensation with negligible losses @ 5Mbaud 6MHz channel
- Symbol timing loop designed to acquire with large offsets. Negligible losses for ±100ppm offsets

100 pin QFP (Plastic)



- All internal clocks derived from single fixed frequency crystal (30MHz)
- Supports fast re-acquisition mode
- 6µs echo cancellation @ 5Mbaud
- Constellation points and equalizer tap values readable via I^2C bus
- C/N estimation readable via I^2C bus
- Low implementation loss for AWGN only:
  0.5dB @ 64QAM (using internal 8-bit A/D);
  0.3dB @ 256QAM (excluding A/D);
  measured at BER of $3x10^{-4}$ Pre R/S
- I = 12 and I = 204 de-interleaving
- Fast I^2C bus compatible control interface
- Tuner IF-AGC output
- User programmable tuner RF-AGC output
- Dedicated 3-wire bus interface to configure up to 2 tuner synthesizers
- 3.3V CMOS technology
- Supports JTAG boundary scan
- 100-pin QFP package

Applications

MMDS set-top boxes

PE99906-PS

Pin Configuration

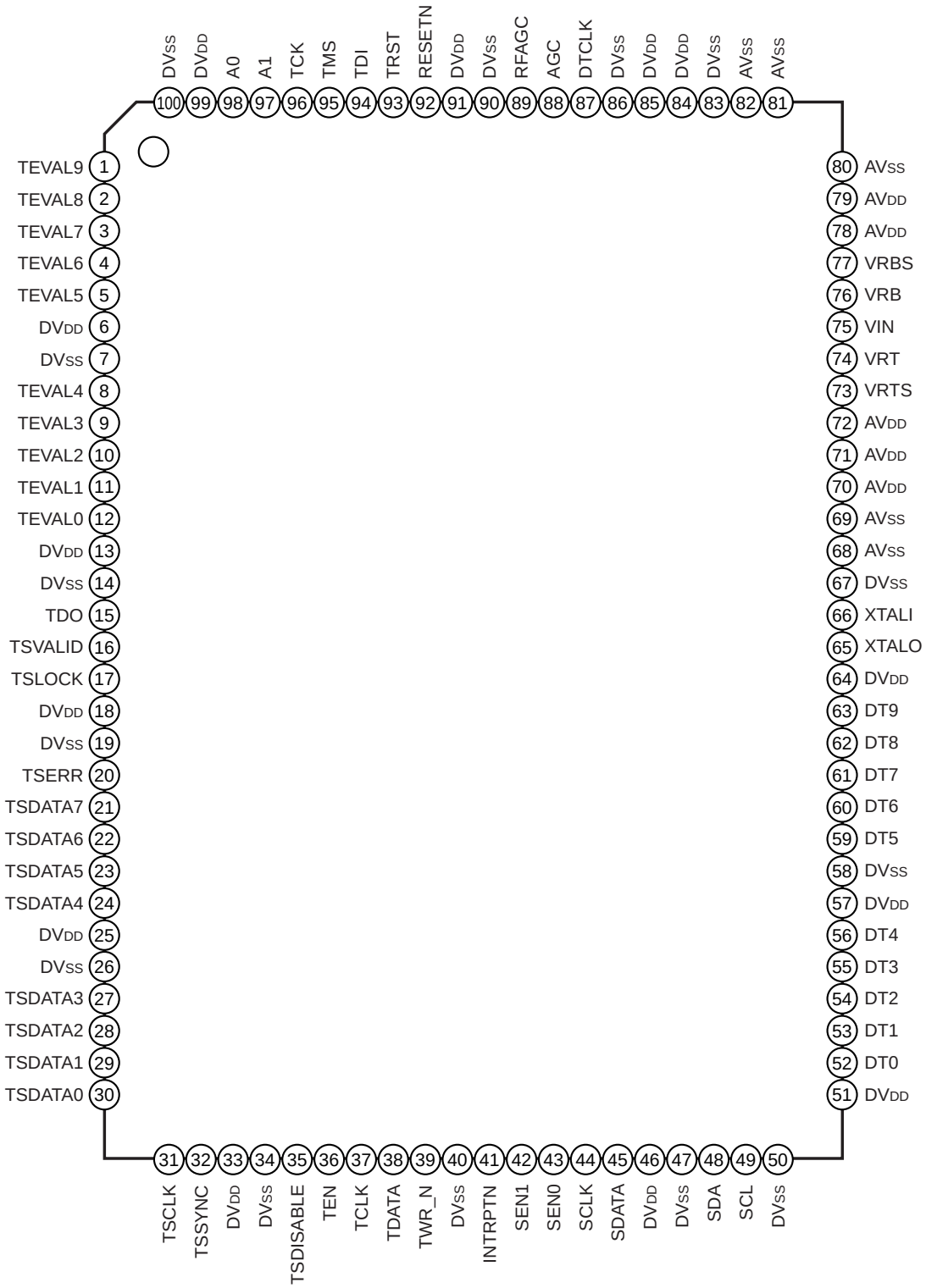


Fig. 1. Pin Configuration

Pin Description

Table 1. Pin Description

Name	Pin No.	Type	Drive	Function
Clock and Reset				
XTALO	65	Crystal oscillator output	N/A	Crystal oscillator cell output.
XTALI	66	Crystal oscillator input	N/A	Crystal oscillator cell input.
RESETN	92	Digital Schmitt-trigger 5V tolerant Input	N/A	Active low hardware reset.
ADC Interface				
VRTS	73	Analog output	N/A	ADC internally generated top reference bias. This pin connects to VRT to self bias the top reference.
VRT	74	Analog input	N/A	ADC top reference voltage. Connects to VRTS for self bias.
VIN	75	Analog input	N/A	Analog IF input.
VRB	76	Analog input	N/A	ADC bottom reference voltage. Connects to VRBS for self bias.
VRBS	77	Analog output	N/A	ADC internally generated bottom reference bias. This pin connects to VRB to self bias the bottom reference.
MPEG2 Transport Stream Interface				
TSVALID	16	Digital tristate output	4mA	Identifies data portion of the MPEG2 transport stream packet (excludes parity bytes). The polarity and timing of this signal is programmable. Tristate following hardware reset. External pull-up or pull-down resistor required.
TSLOCK	17	Digital output	8mA	MPEG2 transport stream lock indicator. The polarity of this signal is programmable.
TSERR	20	Digital tristate output	4mA	MPEG2 transport stream error flag. Indicates uncorrectable errors in current packet. The polarity and timing of this signal is programmable. Tristate following hardware reset. External pull-up or pull-down resistor required.
TSDATA[7:0]	21, 22, 23, 24, 27, 28, 29, 30	Digital tristate output	4mA	MPEG2 transport stream parallel data output. Tristate following hardware reset. External pull-up or pull-down resistor required.

Name	Pin No.	Type	Drive	Function
MPEG2 Transport Stream Interface (Cont.)				
TSCLK	31	Digital tristate output	4mA	MPEG2 transport stream byte clock. The polarity and timing of this signal is programmable. Tristate following hardware reset. External pull-up or pull-down resistor required.
TSSYNC	32	Digital tristate output	4mA	Indicates MPEG2 47H sync byte in transport stream packet. The polarity and timing of this signal is programmable. Tristate following hardware reset. External pull-up or pull-down resistor required.
TSDISABLE	35	Digital Schmitt-trigger 5V tolerant input	N/A	Input to disable MPEG2-TS interface outputs. MPEG2 transport stream output pins TSDATA[7:0], TSCLK, TSSYNC, TSVALID, TSERR to be put into tristate mode if this input is asserted high. The same outputs may also be set tristate via I^2C bus control.
Tuner Interface (Control and AGC)				
AGC	88	Digital output	2mA	External IF AGC control.
RFAGC	89	Digital output	2mA	External RF AGC control.
TEN	36	Digital Schmitt-trigger 5V tolerant input	N/A	Host CPU control input. Can be used to control 3-wire bus outputs SEN0 and SEN1.
TCLK	37	Digital Schmitt-trigger 5V tolerant input	N/A	Host CPU control input. Can be used to control 3-wire bus output SCLK.
TDATA	38	Digital Schmitt-trigger 5V tolerant input	N/A	Host CPU control input. Can be used to control 3-wire bus output SDATA.
TWR_N	39	Digital Schmitt-trigger 5V tolerant input	N/A	Host CPU control input used to register TEN, TCLK, TDATA on rising edge and update SEN, SCLK and SDATA outputs in one mode of the 3-wire bus operation.
SEN1	42	Digital open-drain output	12mA	3-wire bus interface enable output. Polarity programmable and equivalent to polarity of SEN0. Must be pulled up by external resistor to 3.3V or 5V if used.
SEN0	43	Digital open-drain output	12mA	3-wire bus interface enable output or pass-FET contol for tuner I^2C bus. Programmable polarity. Must be pulled up by external resistor to 3.3V or 5V if used.

Name	Pin No.	Type	Drive	Function
Tuner Interface (Control and AGC) (Cont.)				
SCLK	44	Digital open-drain output	12mA	3-wire bus interface clock output. Must be pulled up by external resistor to 3.3V or 5V if used.
SDATA	45	Digital open-drain output	12mA	3-wire bus interface data output. Must be pulled up by external resistor to 3.3V or 5V if used.
Host Control Interface				
SDA	48	Digital bi-directional open-drain output Schmitt trigger 5V tolerant input	3mA	I^2C bus data. Must be pulled up by external resistor.
SCL	49	Digital Schmitt trigger 5V tolerant input	N/A	I^2C bus clock. Must be pulled up by external resistor.
A1	97	Digital CMOS input	N/A	I^2C bus address (variable part)
A0	98	Digital CMOS input	N/A	I^2C bus address (variable part)
INTRPTN	41	Digital open-drain output	12mA	Programmable general interrupt pin. Must be pulled up by external resistor to 3.3V or 5V.
Testability and Evaluation Interface				
DT[9:0]	63, 62, 61, 60, 59, 56, 55, 54, 53, 52	Digital bi-directional tristate output 5V tolerant input	I_{OL} = 4mA I_{OH} = –2mA	ADC digital bypass port for connection of an external ADC.
DTCLK	87	Digital output	8mA	ADC clock for use with DT[9:0].
TRST	93	Digital input with pull-up	N/A	JTAG test reset input.
TDO	15	Digital tristate output	4mA	JTAG test data output.
TDI	94	Digital input with pull-up	N/A	JTAG test data input.
TMS	95	Digital input with pull-up	N/A	JTAG test mode select.
TCK	96	Digital input	N/A	JTAG test clock.
TEVAL[9:0]	1, 2, 3, 4, 5, 8, 9, 10, 11, 12	Digital output	4mA	Test data bus.

Name	Pin No.	Type	Drive	Function
Power Supplies				
DV_{DD}	6, 13, 18, 25, 33, 46, 51, 57, 64, 84, 85, 91, 99	Power		Digital supply. (+3.3V)
DV_{SS}	7, 14, 19, 26, 34, 40, 47, 50, 58, 67, 83, 86, 90, 100	Ground		Digital ground. (0V)
AV_{SS}	68, 69, 80, 81, 82	Ground		Analog ground. (0V)
AV_{DD}	70, 71, 72, 78, 79	Power		Analog supply. (+3.3V)

Description of Functions

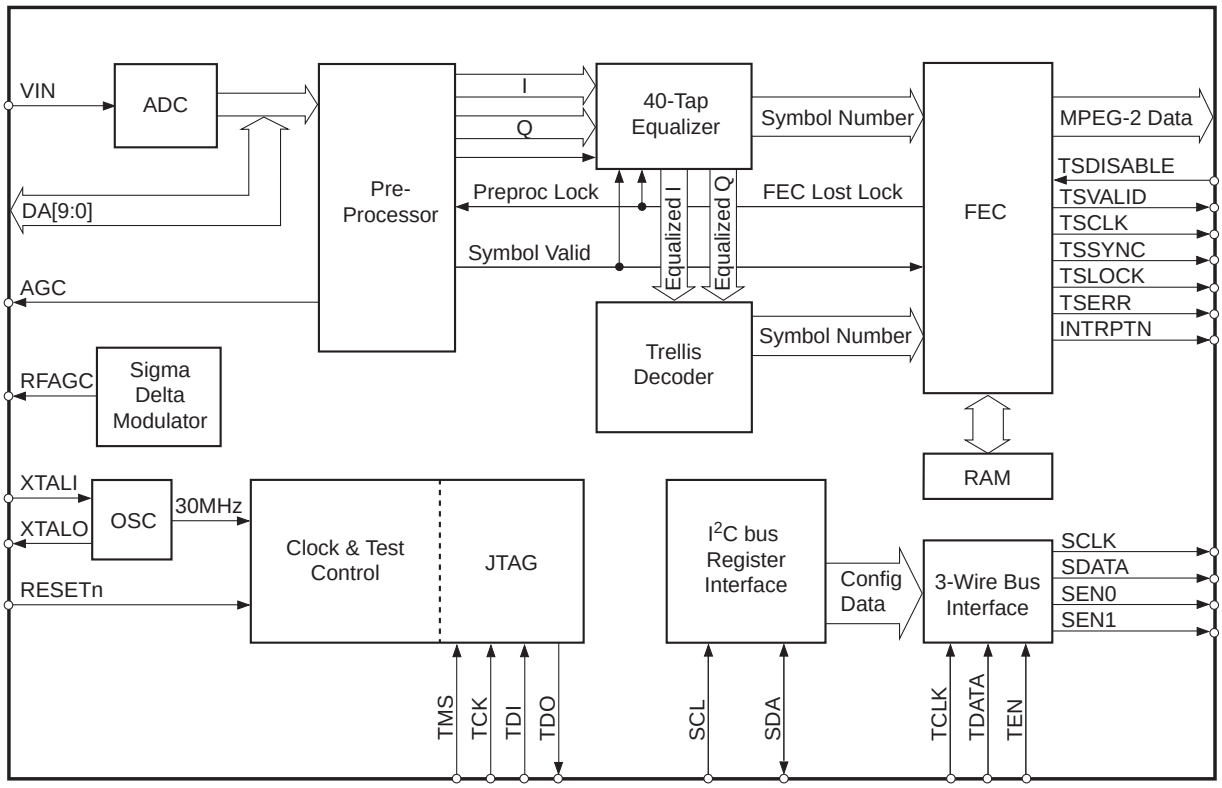


Fig. 2. Block Diagram

1. ADC

Input to the CXD1958Q is a single-ended IF signal centred at 36.125MHz. An integrated 8-bit ADC is clocked at 30MHz and used to directly band-pass sample the IF signal. The 8-bit ADC is self biased by connecting reference pins VRTS to VRT and reference pins VRBS to VRB. An option is provided to allow bypass of the internal ADC if an external converter up to 10 bits is desired.

2. Pre-Processor and Equalizer

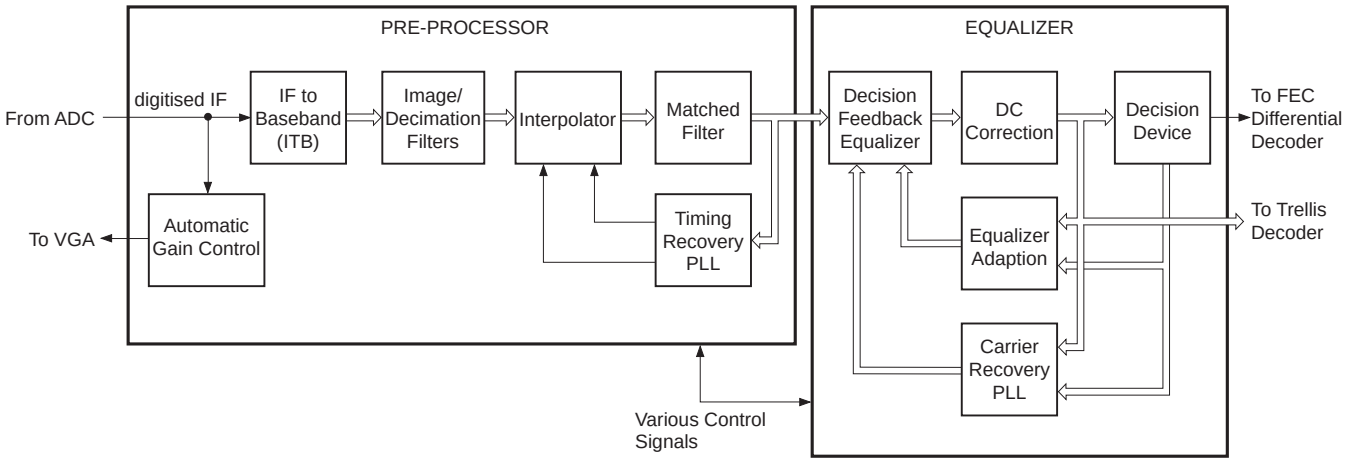


Fig. 3. Pre-Processor and Equalizer Block Diagram

2-1. Automatic Gain Control – External

This block monitors the signal level at the output of the ADC and provides a pulse width-modulated control signal (IF-AGC) to drive an external (analog) variable gain amplifier (VGA). The polarity of this signal is I^2C bus programmable. This circuit operates as an automatic gain control loop and is normally configured to maximize ADC dynamic range. Only a single external RC filter is required. It is possible to read the level being output on the IF-AGC signal via I^2C bus to allow a separate RF-AGC sigma-delta output to be programmed for dual loop AGC systems.

2-2. IF to Baseband Conversion

The IF to Baseband block translates the received digitized IF signal to a complex baseband signal. Subsequent processing is performed in parallel on in-phase (I) and quadrature (Q) data paths.

2-3. Decimation Filter

Sample rate conversion in the Decimation Filter block is used to optimize the operation of the timing loop over the symbol rate range.

2-4. Timing Recovery Loop

Symbol timing recovery is implemented using an all-digital PLL comprised of Interpolator, Matched Filter and Timing Recover PLL blocks in Fig. 3. This allows the sample rate to be unrelated to the symbol rate – sampling is asynchronous. The loop operates over the range (5 – 5.304) Mbaud with minimal performance degradation, surpassing the capability of an equivalent analog loop. The matched filter implements a square-root raised cosine function, matched to the equivalent transmitter filter for rejection of intersymbol interference (ISI).

2-5. Decision Feedback Equalizer

Adaptive equalization is performed using a Decision Feedback Equalizer implementation to remove echoes arising from channel multipath characteristics and any remaining ISI not removed by the matched filter in the pre-processor. The DFE filter structure has a feedforward (10 tap) and feedback (30 tap) section. The 30 tap feedback section removes post-cursive ISI up to 6ms delay which is sufficiently robust to remove long echoes in MMDS.
During acquisition of the QAM constellation, the adaptive equalizer steps through several modes of operation to achieve lock. The equalizer initially operates using a blind error signal to converge tap coefficients as no training sequence is provided in the QAM input data stream. The equalizer then switches to a decision-directed mode of operation where QAM data is used to generate the error signal to optimize convergence of tap coefficients.
An all-digital PLL is implemented for removal of carrier frequency and phase offsets.

2-6. DC Correction

Modulator carrier leakage appears as a DC component in the QAM constellation which must be removed before correct decisions can be made in Decision Device block. The DC Correction block completely removes this offset.

2-7. Decision Device

The Decision Device block performs data slicing and symbol/bit mapping for 16, 64 and 256 QAM constellations. This block can also automatically or manually compensate for an inverted IF spectrum under I^2C bus control. Modulation scheme recognition can be preset via I^2C bus for fast acquisition.

2-8. Configuration and Control

Configuration and control is handled by a register bank accessible to an external processor over an I^2C serial bus.
A pre-processor state machine controls the initial acquisition process until synchronisation is achieved. Once the pre-processor has acquired lock to the input symbol rate the equalizer section is enabled. Once enabled, Equalizer operation is also controlled by a state machine. Once Equalizer acquisition is achieved the condition is then maintained based upon acquisition and mode control information, supplied from the configuration registers, and MPEG Transport Stream status data from the FEC block.

3. Post-Processor

Post-processing on the demodulated QAM/TCM signal implements the DAVIC MMDS standard. This includes differential decoding of the two most significant symbol bits (QAM mode only), mapping of decoded symbols onto bytes, Forney convolutional de-interleaving of the bytes (I = 12, and I = 204) to remove burst errors, Reed-Solomon (255, 239) error correction, MPEG-2 sync byte inversion and data stream de-randomization. Finally a baseband interface is included that provides an MPEG-2 compliant transport stream to the device output.

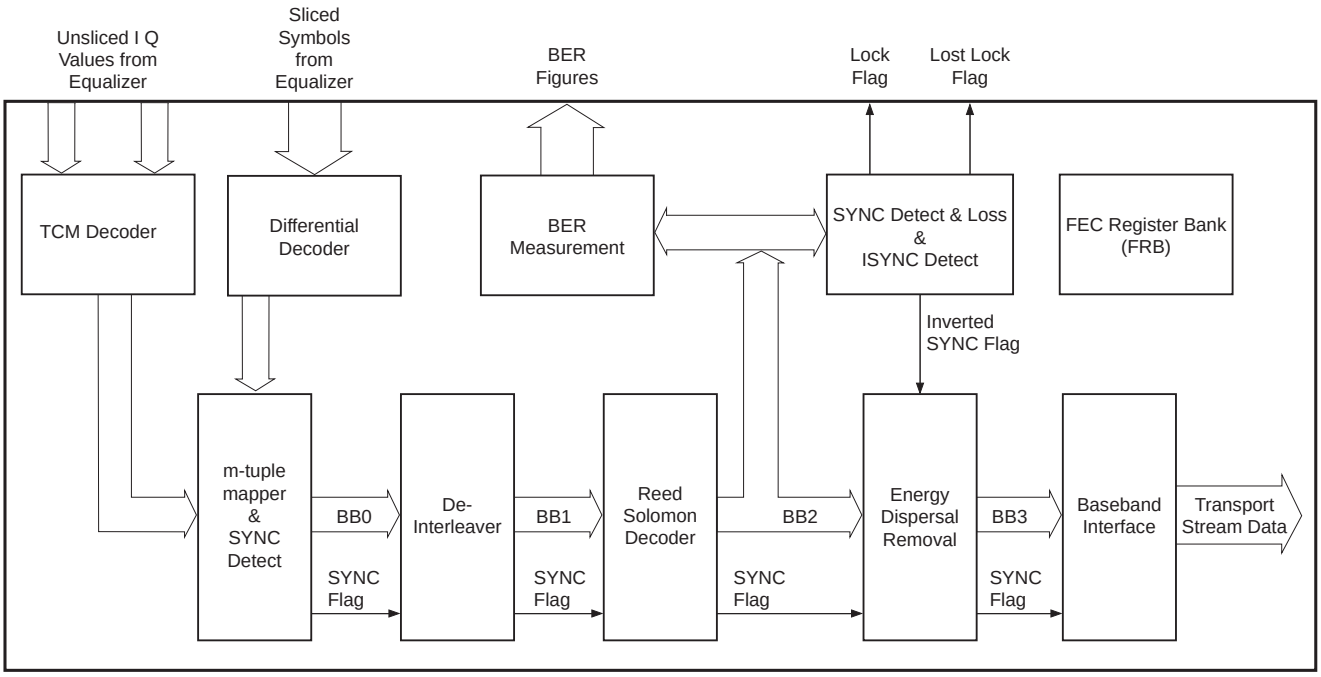


Fig. 4. Post-Processor Block Diagram

3-1. Differential Decoder

In QAM mode, this decodes the MSB of the received QAM signal according to the equations given in the DAVIC MMDS standard. In TCM mode, the differential decoding is performed by the TCM decoder block.

3-2. TCM Decoder

The TCM decoder reduces the signal power required for robust reception in difficult channels whenever trellis coded modulation is used at the transmitter. TCM mode is selected by an I^2C bus register bit. The TCM decoder block takes the equalized I/Q symbols as input data, and provides 7-bit (16-TCM), 11-bit (64-TCM), and 15-bit (256-TCM) outputs for each TCM symbol. Two I/Q pairs are required for each TCM symbol. The TCM block performs an internal synchronization sequence to ensure that the correct pair of QAM symbols is selected. There are several I^2C bus registers to allow user configuration and monitoring of the synchronization sequence.

3-3. Symbol to Byte Mapper

The postprocessor maps differentially decoded symbols to bytes. The byte boundaries are determined by correlating the input symbols with the expected locations of the sync bytes. The number of consecutive successful correlations is compared against a threshold (SYNC_LADDER_LENGTH), and the symbol stream is flagged as locked when that threshold is achieved.

3-4. De-interleaver and Reed Solomon Error Correction

DAVIC compatible forney type convolutional de-interleavering (I = 12, N = 204, M = 17) or (I = 204, N = 204, M = 1), where M = N/I) is applied to the bytes. I = 12 is used for 16/64 QAM/TCM modes. Either I = 12 or I = 204 can be programmed for 256 QAM/TCM modes. The resulting byte stream is corrected by a standard DAVIC/DVB (204, 188) Reed Solomon decoder (GF generation polynomial $p(x) = x^8 + x^4 + x^3 + x^2 + 1$) which can correct up to 8 erroneous bytes per MPEG2 packet.

3-5. Sync Detection and Sync Loss

After R/S correction, the byte stream is checked for the occurrence of n MPEG-2 sync bytes, where n is programmable from 2 to 7 via an I^2C bus register. This sync byte detection is used to indicate transport stream lock by activation of the TSLOCK pin. There are two methods used to indicate loss of Transport Stream Lock, selectable by an I^2C bus register. One method indicates loss of lock immediately a sync byte is lost. The other method decrements the sync byte counter down by 1 from n, and only indicates loss of lock when the counter reaches zero, thus providing a filtering capability to allow easier sync locking.

3-6. Energy Dispersal De-randomiser

The error-corrected bytes are de-randomized with a 15-stage PRBS (Pseudo Random Binary Sequence) generator, with polynomial $1 + X^{14} + X^{15}$ and start-up sequence “100101010000000”. Sync bytes are not de-scrambled, and when an inverted sync byte is detected, every 8th packet, the PRBS resets to the start-up sequence and the sync byte is re-inverted. The de-scrambled data is output through the TSDATA pins, along with a data clock and synchronization signal.

3-7. BER Calculation

In addition to the above functionality, the postprocessor includes comprehensive signal quality measurement logic. The Bit Error Rate (BER) of the received signal (before and after R/S correction) and a measure of the long-term signal quality are available via I^2C bus registers. The calculated Bit Error Rate (BER) of the received signal is accurate for pre R/S BER figures better than 1×10^{-3}.

3-8. MPEG2 Baseband Interface

Fig. 5 illustrates the relationship between the CXD1958Q MPEG2 transport stream interface signals. The transport stream clock (TSCLK) can be programmed for the external device to sample on the rising or falling edge (only rising edge sampling is shown here). The interface supports a number of additional signals, which indicate the integrity of the output data. Once the demodulator has achieved lock to the MPEG2 sync byte, the transport stream interface is activated. Fig. 5 shows a complete MPEG2 packet consisting of a sync byte (47h) data bytes (dd) and Reed Solomon bytes (rr). Note that all the interface control signals have individual programmable polarity; active high signals are shown in the diagram.

TSCLK has two operating modes selected via I^2C bus:

- Whole Packet Mode, where the clock is activated for all 204 bytes of the packet, requiring the external interface to use TSVALID to distinguish between data and 16 Reed Solomon bytes.
- Data Only Mode, where the clock is activated only for each of the 188 sync and data bytes, and remains inactive during the 16 Reed Solomon bytes.

TSDATA[7:0] is the byte wide MPEG2-TS data with programmable MSB/LSB ordering. The default is TSDATA7 being the MSB.

TSVALID has two operating modes selected via I^2C bus:

- Data Only Mode: where TSVALID is set active during the 188 byte data portion of the packet, and reset inactive during the 16 Reed Solomon bytes. It is used by the external device as a clock enable to qualify when data is valid on TSDATA[7:0].
- Pulsed Mode: where TSVALID is set active during the MPEG2 sync byte and reset inactive for the remainder of the packet, and thus becomes equivalent to a sync byte indicator.

TSSYNC is set active during the MPEG2 sync byte and reset inactive for the remainder of the packet.

TSERR is only set active if the Transport Stream Error flag is set. This signal indicates that the Reed Solomon decoder was unable to correct all errors in the packet. There are 3 programmable modes for this signal:

- Whole Packet Mode: Active during the entire 204-byte packet
- Data Only Mode: Active during the 188 byte data portion of packet and inactive during the 16 Reed Solomon bytes
- Pulsed Mode: Pulsed active during sync byte period only

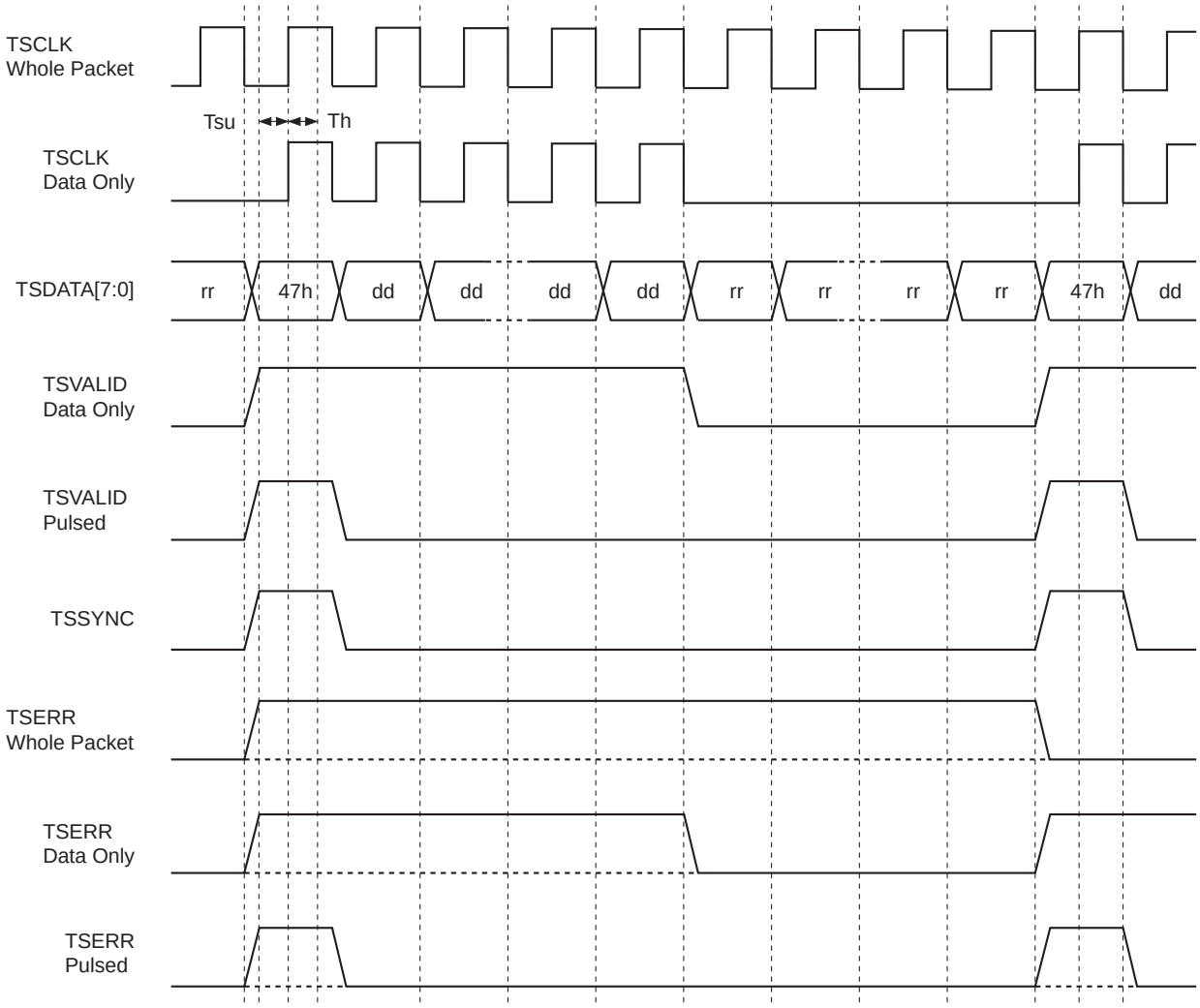


Fig. 5. MPEG2 Transport Stream Output Configurations

4. Tuner 3-Wire Bus Interface

The interface allows two tuner synthesizers to be configured through the use of separate SEN0 and SEN1 enable output signals. The polarity of SEN0 and SEN1 can be programmed both active high or both active low by the SEN_POL I^2C bus register bit. There are two operating modes selected by I^2C bus.

- **Mode 0** : The host CPU drives the 3-wire bus pins via the CPU interface pins TCLK, TDATA and TEN. These pins are connected to the CPU data bus and a decoded active low strobe is connected to the TWR_N input pin. On each rising edge of TWR_N, the data on TCLK, TDATA, and TEN is registered by the CXD1958Q demodulator, and driven out on the SCLK, SDATA and SEN0 or SEN1 pins respectively. The I^2C bus register bit SEL selects whether SEN0 or SEN1 is activated during this transfer. Thus the transfer rate on the 3-wire bus interface in this mode is determined by the rate of CPU accesses. The operation of this mode is shown in Fig. 6.

• **Mode 1** :The CPU loads 4 I^2C bus registers inside the TCM demodulator with 28 bits of data. The CPU selects which SEN0 or SEN1 output should be used by programming the I^2C bus register bit (SEL), and then commands (by setting an I^2C bus register bit SEND) the 3-wire bus state machine to transmit these 28 bits out of the 3-wire interface as shown in Fig. 7. When the transmission is complete, the I^2C bus register bit (SEND) is reset to zero by the 3-wire bus state machine. This allows the CPU to poll the SEND bit to determine when it is able to write further data to the 3 I^2C bus registers if it is necessary to send more data. The rate of transmission is fixed at 10.67µs per bit when using a 30MHz crystal oscillator on the CXD1958Q demodulator IC. The bit ordering of transmission starts with bit 27.

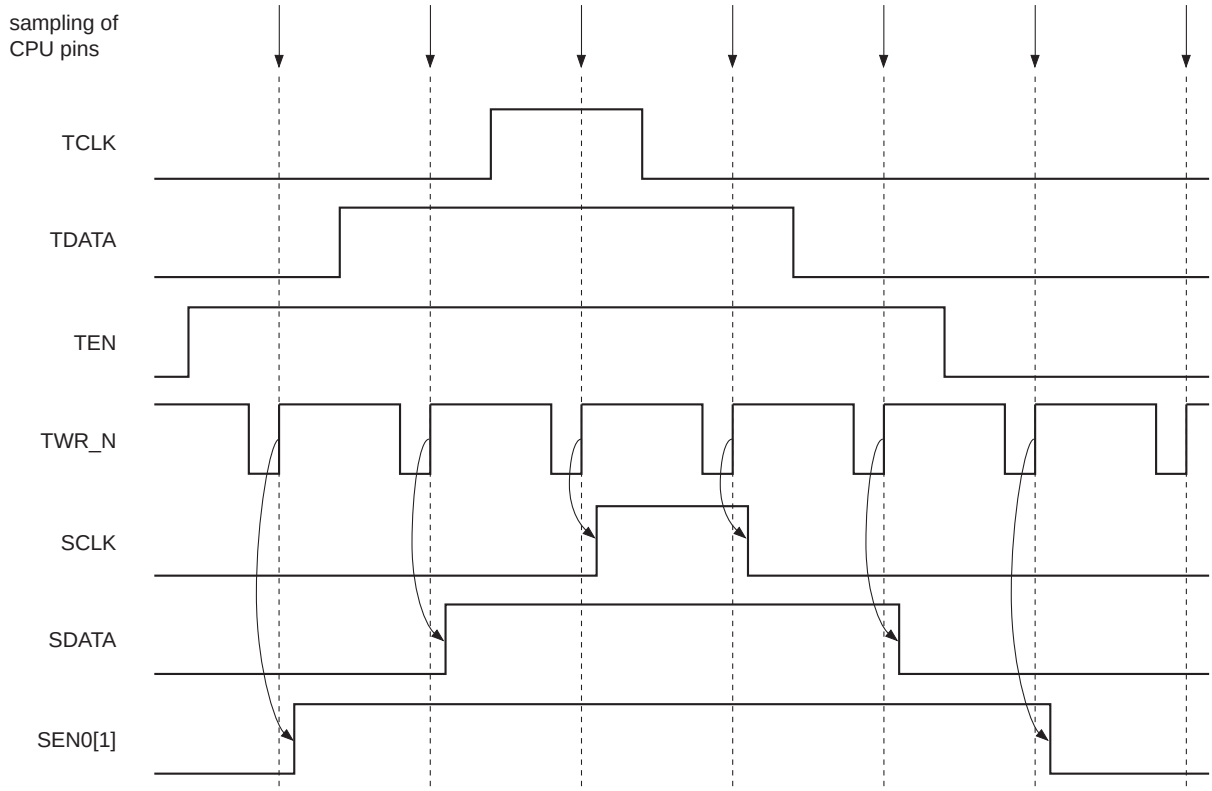


Fig. 6. 3-Wire Bus : Mode 0 Operation

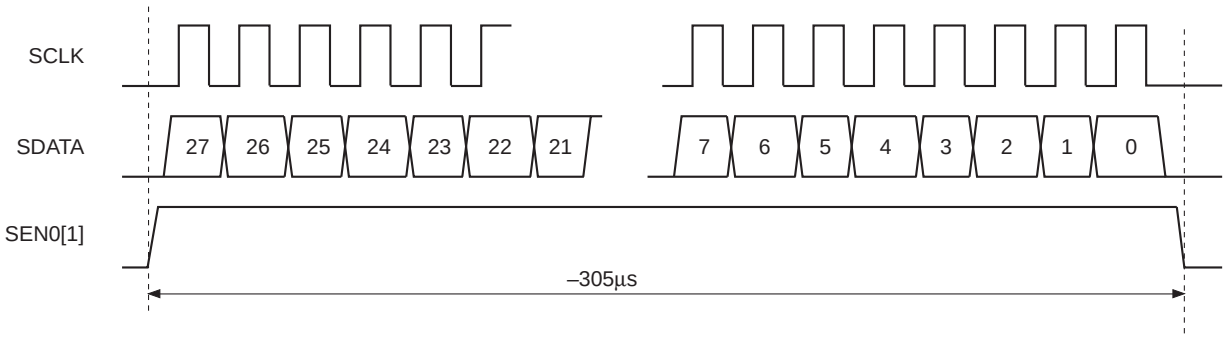


Fig. 7. 3-Wire Bus : Mode 1 Operation

5. I²C Bus Interface

The CXD1958Q includes an I²C bus compatible host interface, to enable access to the internal control registers. This supports accesses via an offset register at bit rates of up to 400Kbit/s. The 7-bit slave address for this device is [0, 0, 1, 1, 1, A1, A0], where A1 and A0 are set externally via device pins.

A summary of the CXD1958Q internal register set which can be accessed via I²C bus is defined in Table 2. A full description of the registers is presented in "Control Register Definitions".

Table 2. I²C bus Interface Registers

Sub-address	Name	R/W	Width bytes	Description	Value on reset of type		
					H/W	Cold	Warm
0	CHIP_INFO	R	1	Device version/revision information	20h	20h	20h
1	RST_REG	RW	1	Device reset register	F4h	F4h	F1h
2	INTERRUPT_SOURCE	RW	1	Interrupt source register	0	0	—
3	TSMSTATUS	R	1	Pre-processor status	0	0	—
4	ESMSTATUS	R	1	Equalizer status	01h	01h	—
5	FEC_STATUS	R	1	FEC status	10h	10h	—
6	QAMCONFIG	RW	1	QAM level configuration	84h	84h	—
7	CARRIEROFFSET	R	1	Detected frequency offset	0	0	—
8	DETECTEDQAM	R	1	Detected QAM level	0	0	—
9 – 0AH	DETECTEDSYMRATE	R	2	Symbol rate at which locked	0	0	—
0BH – 0DH	BER_EST	R	3	Bit Error Rate estimate	0	0	—
0EH – 0FH	CWRJCT_CNT	R	2	Codeword reject count	0	0	—
10H	INTERRUPT_MASK	RW	1	Interrupt mask register	0	0	—
11H	PRECONFIG	RW	1	Pre-processor configuration	89h	89h	—
12H	AGCCTRL	RW	1	External AGC control	0	—	—
13H	EQUCONFIG	RW	1	Equalizer configuration	03h	03h	—

Sub-address	Name	R/W	Width bytes	Description	Value on reset of type		
					H/W	Cold	Warm
14H	FEC_PARAMS	RW	1	FEC configuration	32h	—	—
15H – 16H	SYMRATETRIAL0	RW	2	Symbol rate table entry	0AABh 5Msym/s	0AABh 5Msym/s	—
17H – 18H	SYMRATETRIAL1	RW	2	Symbol rate table entry	0	0	—
19H – 1AH	SYMRATETRIAL2	RW	2	Symbol rate table entry	0	0	—
1BH – 1CH	SYMRATETRIAL3	RW	2	Symbol rate table entry	0	0	—
1DH – 1EH	SYMRATETRIAL4	RW	2	Symbol rate table entry	0	0	—
1FH – 20H	SYMRATETRIAL5	RW	2	Symbol rate table entry	0	0	—
21H – 22H	SYMRATETRIAL6	RW	2	Symbol rate table entry	0	0	—
23H – 24H	SYMRATETRIAL7	RW	2	Symbol rate table entry	0	0	—
25H	SET_SYNC_DETECT	RW	1	FEC sync detect thresholds	1Dh	1Dh	—
26H	LT_QLTY_THRESHOLD	RW	1	Long term quality threshold	04h	04h	—
27H	BER_EST_PERIOD	RW	1	Bit error rate measurement period	0Eh	0Eh	—
28H	ADC_CAL_PERIOD	RW	1	Not used in this application	FFh	FFh	—
29H – 2AH	ITBFREQ	RW	2	Nominal frequency of receive local oscillator	32EFh 36.125MHz	32EFh 36.125MHz	—
2BH	EQUTAPSELECT	RW	1	Equalizer tap address number	0	0	—
2CH	EQUTAPI	R	1	In-phase component of equalizer tap	0	0	—
2DH	EQUTAPQ	R	1	Quadrature component equalizer tap	0	0	—
2EH	CONSTELLATIONI	R	1	In-phase equalizer output	0	0	—
2FH	CONSTELLATIONQ	R	1	Quadrature-phase equalizer output	0	0	—

Sub-address	Name	R/W	Width bytes	Description	Value on reset of type		
					H/W	Cold	Warm
30H – 31H	AGCIFINTG	R	2	IF external gain control integrator output level	0	0	—
32H – 33H	RFAGC	RW	2	RF gain control	0	0	—
34H – 37H	TUNER_CTRL	RW	4	Tuner interface control I/F	0h	0h	—
38H	TCM_CONFIG	RW	1	TCM configuration and synchronization control	ABh	ABh	—
39H	TS_MODE	RW	1	Transport stream output control	B4h	B4h	—
3AH	SNRESTIMATE	R	1	Estimate of SNR in channel	0	0	—
3BH	LMSMUTRACK	RW	1	Equalizer adaption constant	03h	03h	—
3CH	SWEEPRNG	RW	1	Maximum frequency offset carrier loop acquires	80h	80h	—
83H	AGCTGT	RW	1	External gain control target signal level	69h	69h	—

6. JTAG Test Interface

A JTAG test interface is provided using the pins TDI, TDO, TMS, TRST and TCK. The Interface conforms to the IEEE1149.1 standard and provides access to the device boundary scan chain.

Electrical Characteristics

1. Absolute Maximum Ratings

(Ta = 25°C, AVss = 0V, DVss = 0V)

Item	Symbol	Condition	Min.	Max.	Unit
Digital power supply	DV_{DD}		DVss – 0.5	+4.6	V
Analog power supply	AV_{DD}		AVss – 0.5	+4.6	V
Input voltage: –3.3V only input pins	V_I	Pins TRST, TDI, TMS, TCK, A1, A0, VRT, VIN, VRB, XTALI	DVss – 0.5	DV_{DD} + 0.5	V
Input voltage: –5V tolerant input pins		Pins SCL, SDA, RESETN, TEN, TCLK, TDATA, TWR_N, TSDISABLE, DT[9:0]	DVss – 0.5	DV_{SS} + 5.5	
Output voltage: –3.3V only pins	V_O	Pins TEVAL[9:0], TDO, TVALID, TSLOCK, TSERR, TSDATA[7:0], TSCLK, TSSYNC, XTALO, DTCLK, AGC, RFAGC, VRTS, VRBS	DVss – 0.5	DV_{DD} + 0.5	V
Output voltage: –5V tolerant input pins		Pins INTRPTN, SEN0, SEN1, SCLK, SDATA, SDA, DT[9:0]	DVss – 0.5	DV_{SS} + 5.5	
Storage temperature	T_{STG}		–55	+150	°C

Notes:

1. The device must be operated within the limits of the absolute maximum ratings. If the device is operated outside these conditions, the device may be permanently damaged.
2. Functional operation at or outside any of the conditions indicated in the absolute maximum ratings is not implied.
3. Exposure of the device to the absolute maximum rating condition for extended periods can affect system reliability.
4. 5V tolerant inputs and outputs are only 5V tolerant while the device power is applied. If no device power is applied there in no protection to 5V levels and the device may be permanently damaged. It is important to observe the conditions for 5V protection when sequencing power supplies in the application.

2. Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital power supply	DV_{DD}	DVss = 0V	3.0	3.3	3.6	V
Analog power supply	AV_{DD}	AVss = 0V	3.0	3.3	3.6	V
Crystal oscillator frequency	f_{XTAL}		30		30	MHz
Ambient temperature range	Ta		0		+70	°C

3. DC Electrical Characteristics

0°C < Ta < 70°C, DVss = AVss = 0V, 3.0V < DV_{DD}, AV_{DD} < 3.6V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input low voltage	V_{IL}	Except pins SCL, SDA			$0.2DV_{DD}$	V
Input low voltage	V_{IL}	Pins SCL, SDA			$0.3DV_{DD}$	V
Input high voltage	V_{IH}		$0.7DV_{DD}$			V
Input voltage hysteresis	V_{HYST}	Pins RESETN, TSDISABLE, TEN, TCLK, TDATA, TWR_N, SDA, SCL		0.5		V
Input low current	I_{IL}	Vin = DV_{SS}, pins TCK, A1, A0	–10			µA
Input low current	I_{IL}	Vin = DV_{SS}, pins TMS, TDI, TRST	–240	–100	–40	µA
Input low current	I_{IL}	Vin = DVss, pins SCL, SDA, RESETN, TEN, TCLK, TDATA, TWR_N, TSDISABLE, DT[9:0]	–40			µA
Input high current	I_{IH}	Vin = DV_{DD}, pins TRST, TDI, TMS, TCK, A1, A0			+10	µA
Input high current	I_{IH}	Vin = 5.5V, pins SCL, SDA, RESETN, TEN, TCLK, TDATA, TWR_N, TSDISABLE, DT[9:0]			+40	µA
Output voltage LOW	V_{OL}	I_{OL} = 2mA, pins AGC, RFAGC I_{OL} = 3mA, pin SDA I_{OL} = 4mA, pins TSVALID, TSERR, TDATA[7:0], TSCLK, TSSYNC, DT[9:0], TDO, TEVAL[9:0] I_{OL} = 8mA, pins TSLOCK, DTCLK I_{OL} = 12mA, pins SEN0, SEN1, SCLK, SDATA, INTRPTN			0.4	V
Output voltage HIGH	V_{OH}	I_{OH} = –2mA, pins AGC, RFAGC, DT[9:0] I_{OH} = –4mA, pins TSVALID, TSERR, TDATA[7:0], TSCLK, TSSYNC, TDO, TEVAL[9:0] I_{OH} = –8mA, pins TSLOCK, DTCLK	DV_{DD} – 0.4			V
Output voltage HIGH	V_{OH}	I_{OH} = –2mA, pins DT[9:0]	2.4			V
ADC bottom reference voltage	V_{RB}	VRT connected to VRTS and VRB connected to VRBS		$0.33DV_{DD}$		V
ADC top reference voltage	V_{RT}	VRT connected to VRTS and VRB connected to VRBS		$0.66DV_{DD}$		V
ADC input dynamic range	V_{IADC}			$0.33DV_{DD}$		V
Supply current	I_{DD}	Total current AV_{DD} + DV_{DD}		330		mA

4. AC Electrical Characteristics

4-1. Transport Stream Interface

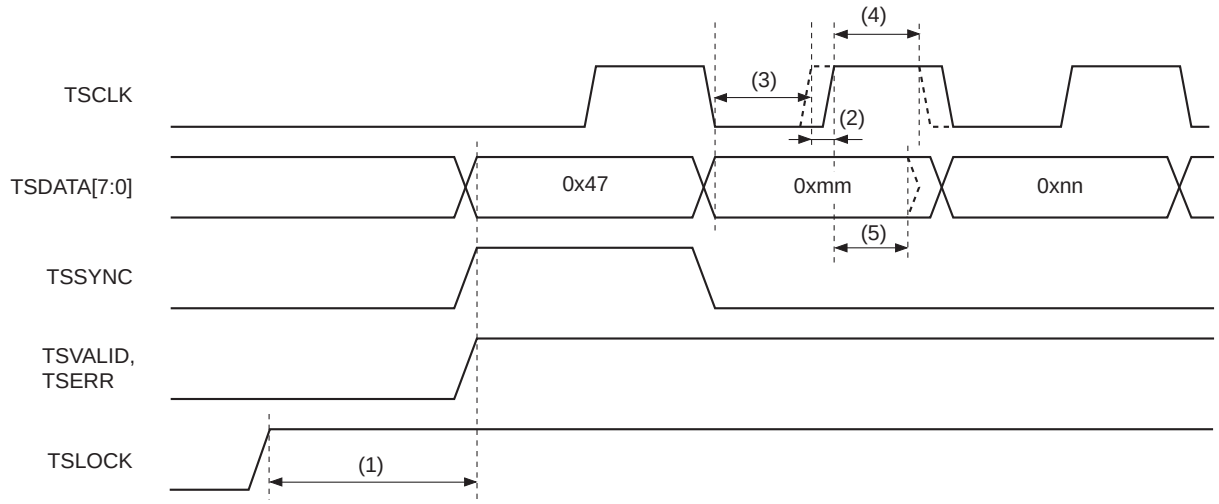


Fig. 8. Transport Stream AC Timing

Table 3. Transport Stream AC Timing Parameters

0°C < Ta < 70°C, DVss = AVss = 0V, 3.0V < DV_{DD}, AV_{DD} < 3.6V

Timing parameter	Description	Min.	Typ.	Max.	Unit
	t_{XTAL}, Clock period defined by crystal oscillator		33.33		ns
1	$t_{TSLOCKSU}$, TSLOCK valid setup time to TSSYNC, TSVALID and TSERR	$3 \times t_{XTAL}$			ns
2	t_{TSJIT}, transport stream clock jitter			t_{XTAL}	ns
3	t_{TSSU}, transport stream TSDATA, TSSYNC, TSVALID and TSERR setup time to TSCLK active edge	$2 \times t_{XTAL}$			ns
4	t_{TSHD}, transport stream TSDATA, TSSYNC, TSVALID and TSERR hold time from TSCLK active edge			$2 \times t_{XTAL}$	ns
5	t_{TSPW}, transport stream TSCLK pulse width	$2 \times t_{XTAL}$			ns

4-2. Tuner 3-Wire Bus Interface

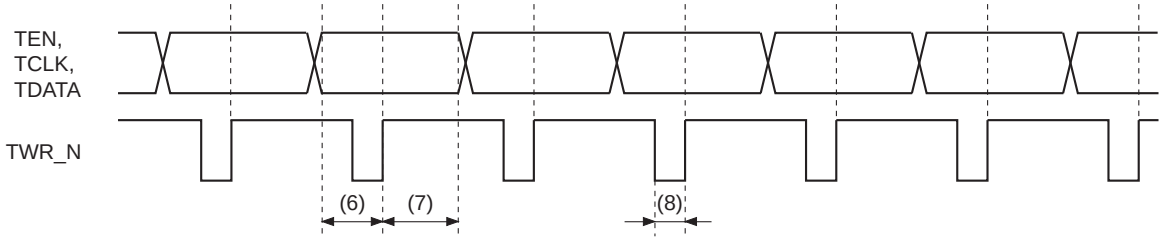


Fig. 9. Tuner 3-Wire Bus Mode 0 AC Timing

Table 4. Tuner 3-Wire Bus Mode 0 AC Timing Parameters

0°C < Ta < 70°C, DVss = AVss = 0V, 3.0V < DV_{DD}, AV_{DD} < 3.6V

Timing parameter	Description	Min.	Typ.	Max.	Unit
6	t_{HCPUSU}, host CPU TEN, TCLK, and TDATA setup time to TWR_N rising edge			40	ns
7	t_{HCPUHD}, host CPU TEN, TCLK, and TDATA hold time from TWR_N rising edge	10			ns
8	t_{HCPUPW}, host CPU TWR_N pulse width	40			ns

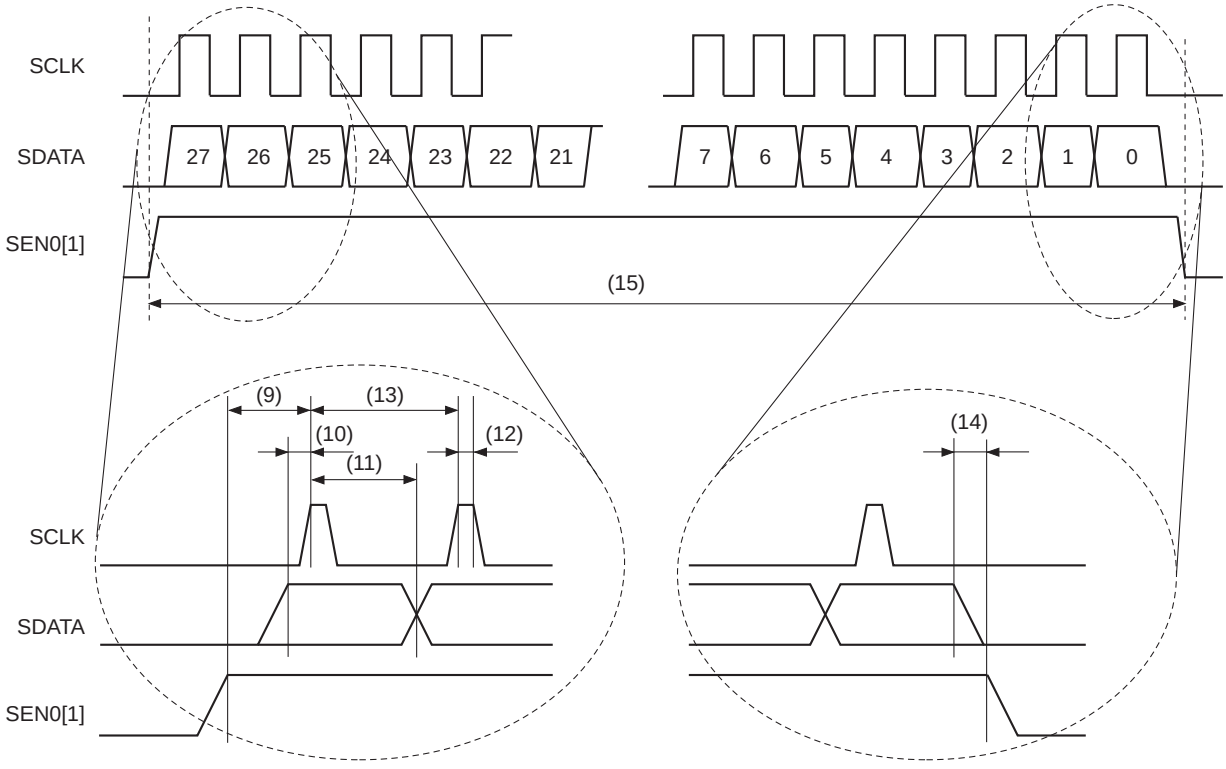


Fig. 10. Tuner 3-Wire Bus Mode 1 AC Timing

Table 5. Tuner 3-Wire Bus Mode 1 AC Timing Parameters

0°C < Ta < 70°C, DVss = AVss = 0V, 3.0V < DV_{DD}, AV_{DD} < 3.6V

Timing parameter	Description	Min.	Typ.	Max.	Unit
	t_{XTAL}, clock period defined by crystal oscillator		33.33		ns
9	t_{SENSU}, 3-wire bus SEN0 or SEN1 active setup time to SCLK rising edge		192 × t_{XTAL}		ns
10	$t_{SDATASU}$, 3-wire bus SDATA setup time to SCLK rising edge		64 × t_{XTAL}		ns
11	$t_{SDATAHD}$, 3-wire bus SDATA hold time from SCLK rising edge		256 × t_{XTAL}		ns
12	t_{SCLKPW}, 3-wire bus SCLK high pulse width		64 × t_{XTAL}		ns
13	$t_{SCLKPER}$, 3-wire bus SCLK period		320 × t_{XTAL}		ns
14	t_{SENHD}, 3-wire bus SEN0 or SEN1 hold time active after final SDATA bit		64 × t_{XTAL}		ns
15	t_{SENPW}, 3-wire bus SEN0 or SEN1 active pulse width		9152 × t_{XTAL}		ns

4-3. I²C Interface

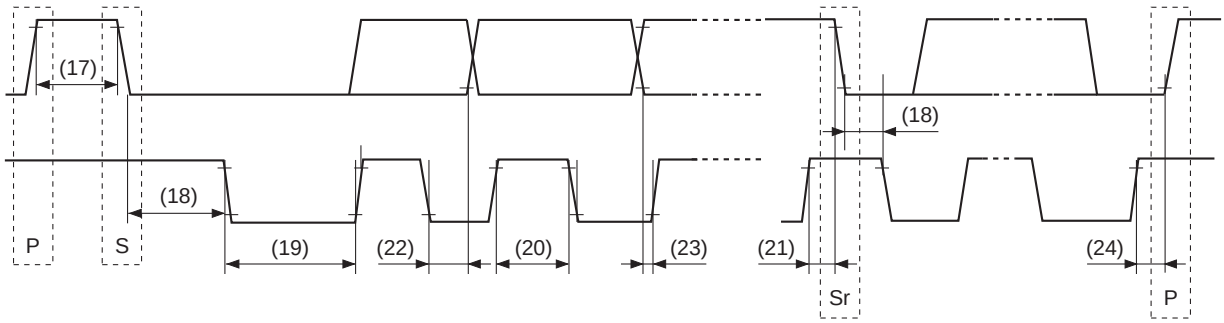


Fig. 11. I²C Interface AC timing

Table 6. I²C Interface AC timing parameters

0°C < Ta < 70°C, DVss = AVss = 0V, 3.0V < DV_{DD}, AV_{DD} < 3.6V

Timing parameter	Description	Min.	Typ.	Max.	Unit
16	f_{SCL}, SCL clock frequency	0		400	kHz
17	t_{SDABUF}, Bus free time between a STOP (P) and START (S) condition	1.3			µs
18	t_{STAHD}, Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6			µs
19	t_{SCLLOW}, LOW period of SCL clock	1.3			µs
20	$t_{SCLHIGH}$, HIGH period of SCL clock	0.6			µs
21	t_{STASU}, Setup time for a repeated START condition	0.6			µs
22	t_{SDAHD}, SDA data hold time	0		0.9	µs
23	t_{SDASU}, SDA data setup time	100			ns
24	t_{STOSU}, Setup time for STOP condition	0.6			µs

Control Register Definitions

1. Notation

Addresses and constant values are defined using decimal or hexadecimal numbers. Where they are used, hexadecimal numbers are prepended with “0x”.
Register definitions are given in the following format:

REGISTERNAME **ACCESS MODE** **CORE**
ADDRESS **DEFAULT VALUE**

7	6	5	4	3	2	1	0

Where,

REGISTERNAME: Name of the register (e.g. EQUCONFIG)
ACCESS MODE: Read (R), Write (W) or Read/Write (RW)
CORE: Which register group it belongs to.
ADDRESS: I^2C bus address used to access register
DEFAULT VALUE: Value after chip reset or software equivalent

The most significant bit of each field is positioned to the left.
Where logical registers occupy more than a single 8-bit physical register (for example where a parameter field requires more than 8 bits of precision) they are defined together and allocated successive (byte) addresses.

2. Number Format

Numerical values which can be positive or negative, use 2's complement number format. Numerical values which can be only positive, use plain unsigned binary representation.

3. Register Definitions

3-1. TSMSTATUS

TSMSTATUS **READ** **CORE**
ADDRESS: 0x03 **DEFAULT: 0x00**

7	6	5	4	3	2	1	0
AGC locked	Reserved				TSM status		

Bits 3 to 0: Current state of pre-processor state machine coded as follows:

TSM status	Synchronization state	State identifier
0	Cold reset	RST
1	Initialize	INI
2	Coarse timing acquisition	CTA
3	Fine timing acquisition A	FTA
4	Fine timing acquisition B	FTB
5	Tracking	TRK
6	Pre-processor lost lock	PLL

Bits 3 to 6: Reserved

Bit 7: Set by the pre-processor when the AGC is in lock. Refer to the description of registers AGCTGT and AGCLKTHR.

3-2. ESMSTATUS

ESMSTATUS **READ** **CORE**
ADDRESS: 0x04 **DEFAULT: 0x00**

7	6	5	4	3	2	1	0
Reserved				ESM status			

Bits 3 to 0: Current state of equalizer state machine coded as follows:

ESM status	Synchronisation state	State identifier
0	Reset	RESET
1	Wait for Pre-processor to Lock	WPL
2	Fine Gain Adjustment	FGA
3	Blind Linear Equalisation (1)	BLE1
4	Blind Linear Equalisation (2)	BLE2
5	Carrier Frequency Recovery	CFR
6	DC Correction	DCC
7	Blind DFE Equalisation	BDE
8	S&G DFE Equalisation	SDE
9	DD DFE Equalisation	DDE
10	Check Spectral Inversion	CSI
11	Tracking	TRK
12	Equalizer Lost Lock	ELL

Bits 4 to 7: Reserved

3-3. QAMCONFIG

QAMCONFIG **READ/WRITE** **CORE**
ADDRESS: 0x06 **DEFAULT : 0x84**

7	6	5	4	3	2	1	0
256 QAM Mapping	Reserved		256 QAM Enable	128 QAM Enable	64 QAM Enable	32 QAM Enable	16 QAM Enable

Bits 0 to 4: Clear appropriate bit to prevent the demodulator from attempting to synchronize with the specified QAM. The default value is such that lock is only attempted with 64 QAM. If more than one QAM level is specified the equalizer attempts lock at each of the specified QAM levels until lock is achieved. This increases the lock time compared to setting the QAM level if known.

Bits 5 to 6: Reserved

Bit 7: Clear this bit to use the DVB 256 QAM mapping. The default value of 1 means that, in 256 QAM mode, the MMDS mapping is used.

3-4. CARRIEROFFSET

FREQOFFSET **READ** **CORE**
ADDRESS: 0x07 **DEFAULT: 0x00**

7	6	5	4	3	2	1	0
Detected Carrier Offset							

Bits 0 to 7: Holds the detected coarse carrier frequency offset. This is a combination of any frequency offset correction applied in the pre-processor to allow symbol timing lock and the carrier frequency offset detected by the carrier recovery loop in the equalizer. It is encoded as follows:

$$Foff = CarrierOffset \cdot \frac{Fs}{256}$$

Where Foff is the frequency offset from the nominal IF (or alias) and Fs is the ADC sample rate (nominally 30MHz). The maximum carrier frequency offset that can be accommodated is currently fixed at 512kHz although there may be SNR degradation for large offsets depending on the SAW filter used.

3-5. DETECTEDQAM

DETECTEDQAM **READ** **CORE**
ADDRESS: 0x08 **DEFAULT: 0x00**

7	6	5	4	3	2	1	0
Reserved					Detected QAM Level		

Bits 0 to 3: Once the equalizer has lock this register contains the QAM level for which the equalizer locked and is decoded as follows:

Register value	QAM level
0	16
1	32
2	64
3	128
4	256

Bits 3 to 7: Reserved

3-6. DETECTEDSYMRATE

DETECTEDSYMRATE **READ** **CORE**
ADDRESS: 0x09 to 0A **DEFAULT: 0x0**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved				TrialSRate				TrialSRate							

Bits 0 to 3 & 0 to 7: Holds the last symbol rate at which the timing recovery PLL locked and which subsequently lead to valid MPEG packets being decoded by the FEC block. This symbol rate is restored as the trial symbol rate when the demodulator performs a hot reset and is encoded as follows:

$$\text{SymbolRate} = \frac{\text{TrialSRate}}{16384} \cdot \text{Fs}$$

Where Fs is the ADC sample rate (nominally 30MHz).

3-7. PRECONFIG

PRECONFIG **READ/WRITE** **CORE**
ADDRESS: 0x11 **DEFAULT: 0x89**

7	6	5	4	3	2	1	0
Discrete Search	Reserved			ADC Offset Binary	ADC External	AGC Hold	Hot Reset

Bit 0: When set this enables a hot reset when the FEC block indicates that it has lost sync. This causes the pre-processor state machine to resume operation at a point where it can exploit prior knowledge of the received signal format gained whilst the chip was in lock. Specifically, a hot reset causes the PSM to restore values for IF carrier frequency offset and symbol rate used when the FEC last indicated that valid MPEG code words were being received. This facility is provided to minimize the time required for re-acquisition of sync in applications using a single symbol rate and can only be invoked from the state where the demodulator once had lock and subsequently lost it.

Bit 1: Set to hold the AGC output at its current value following a warm reset rather than being reset to mid-range. This may reduce AGC acquisition times following a channel switch if signal levels are similar.

Bit 2: Set to select the output of an external A/D converter for connection to the pre-processor instead of the (default) internal A/D.

Bit 3: The signal processing elements of the pre-processor assume 2’s complement data is being supplied. Setting this bit inverts the top bit of the ADC output, converting the data format from offset binary to 2’s complement.

Bits 4 to 6: Reserved

Bit 7: Set to enable a symbol rate search at the discrete frequencies specified in the table SYMBRATETRIAL0 – SYMBRATETRIAL7. In this mode, the pre-processor attempts to recover symbol synchronization at the specified symbol rates only. If lock is not achieved within the time limit specified by CTATIMEOUT acquisition is attempted at the next frequency.

3-8. AGCCTRL

AGCCTL **READ/WRITE** **CORE**
ADDRESS: 0x12 **DEFAULT : 0x00**

7	6	5	4	3	2	1	0
Reserved					Invert AGC	AGC Time Constant	

Bits 0 to 1: This controls the time constant of the AGC loop. The hardware reset value of 0 disables the AGC. A nominal setting of 2 should be programmed following power-up. This will allow the PWM average output to slew from its mid-range value to full scale in approximately 11ms. A setting of 1 doubles the time constant to 22ms and 3 halves it. A subsequent setting of 0 locks the AGC output at its current level. The AGC control loop will be disabled at power-up with the AGC output pin giving a 50% duty cycle output. The host microprocessor should set the correct sense for the control loop and enable the AGC by setting AGC_TC to 2. A subsequent warm or cold reset will not reset either of these parameters.

Bit 2: This controls the sense of the AGC loop. The default value of "0" will give a decreasing control output when the input is overloaded. A value of "1" will give an increasing value.

3-9. EQUCONFIG

EQUCONFIG **READ/WRITE** **CORE**
ADDRESS: 0x13 **DEFAULT : 0x03**

7	6	5	4	3	2	1	0
Reserved					Invert Spectrum	Disable CSI	Hot Reset

Bit 0: When set this enables a hot reset when the FEC block indicates that it has lost lock. This causes the equalizer state machine to resume operation at a point where it can exploit prior knowledge of the received signal format gained whilst the chip was in lock. Specifically, a hot reset causes the ESM to restore the last values for QAM order and spectral inversion used before the FEC indicated loss of lock.

Bit 1: The device will automatically toggle the input spectrum once the equalizer has locked if the FEC has not locked. This toggling feature can be disabled by setting this bit.

Bit 2: Set this to invert the spectrum of the input signal. It is not inverted by default. The setting of this bit is dependent upon the frequency plan used in the tuner.

Bits 3 to 7: Reserved

3-10. SYMRATETRIAL0

SYMRATETRIAL0 **READ/WRITE** **CORE**
ADDRESS: 0x15 & 0x16 **DEFAULT: 0xAAB**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved				Trial Symbol Rate 0				Trial Symbol Rate 0							

Bits 0 to 7 & 0 to 3: The SYMRATETRIAL0 – SYMRATETRIAL7 registers control the frequencies at which the timing loop attempts to lock. Their function depends upon the setting of the discrete search bit (bit 7) in the PRECONFIG register.
When disabled (i.e. set to zero) the pre-processor performs a continuous symbol rate search which extends from the frequency specified in SYMRATETRIAL0 down to that specified in SYMRATETRIAL1. The search must be performed downwards in frequency and so SYMRATETRIAL0 defines the high frequency limit of the search range.
When discrete search is enabled (i.e. set to one) the pre-processor attempts to synchronize at each of up to 8 discrete frequencies specified in SYMRATETRIAL0 – SYMRATETRIAL7. In this case SYMRATETRIAL0 defines the first symbol rate to test. If a discrete rate is set to zero then this causes the search to reset to TRIAL0 and start again. Therefore if a known single symbol rate is used then SYMRATETRIAL0 should be set appropriately and SYMRATETRIAL1 should be set to zero.
For both modes the register setting is given by:

$$\text{SYMRATETRIAL0} = \frac{\text{Fsym}}{\text{Fs}} \cdot 16384$$

Where Fsym is the symbol rate and Fs is the ADC sample rate (nominally 30MHz). The default value of 2731 corresponds to 5Msym/s with a 30MHz sample clock.

3-11. SYMRATETRIAL1

SYMRATETRIAL1 **READ/WRITE** **CORE**
ADDRESS: 0x17 & 0x18 **DEFAULT: 0x0**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved				Trial Symbol Rate 1				Trial Symbol Rate 1							

• See SYMRATETRIAL0 register description.

3-12. SYMRATETRIAL2

SYMRATETRIAL2 **READ/WRITE** **CORE**
ADDRESS: 0x19 & 0x1A **DEFAULT: 0x0**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved				Trial Symbol Rate 2				Trial Symbol Rate 2							

• See SYMRATETRIAL0 register description.

3-13. SYMRATETRIAL3

SYMRATETRIAL3 **READ/WRITE** **CORE**
ADDRESS: 0x1B & 0x1C **DEFAULT: 0x0**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved				Trial Symbol Rate 3				Trial Symbol Rate 3							

• See SYMRATETRIAL0 register description.

3-14. SYMRATETRIAL4

SYMRATETRIAL4 **READ/WRITE** **CORE**
ADDRESS: 0x1D & 0x1E **DEFAULT: 0x0**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved				Trial Symbol Rate 4				Trial Symbol Rate 4							

• See SYMRATETRIAL0 register description.

3-15. SYMRATETRIAL5

SYMRATETRIAL5 **READ/WRITE** **CORE**
ADDRESS: 0x1F & 0x20 **DEFAULT: 0x0**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved				Trial Symbol Rate 5				Trial Symbol Rate 5							

• See SYMRATETRIAL0 register description.

3-16. SYMRATETRIAL6

SYMRATETRIAL6 **READ/WRITE** **CORE**
ADDRESS: 0x21 & 0x22 **DEFAULT: 0x0**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved				Trial Symbol Rate 6				Trial Symbol Rate 6							

• See SYMRATETRIAL0 register description.

3-17. SYMRATETRIAL7

SYMRATETRIAL7 **READ/WRITE** **CORE**
ADDRESS: 0x23 & 0x24 **DEFAULT: 0x0**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved				Trial Symbol Rate 7				Trial Symbol Rate 7							

• See SYMRATETRIAL0 register description.

3-18. ITBFREQ

ITBFREQ **READ/WRITE** **CORE**
ADDRESS: 0x29 & 0x2A **DEFAULT: 0x32EF**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved		ITB Downconversion Frequency						ITB Downconversion Frequency							

Bits 0 to 5 & 0 to 7: Nominal frequency of the receive local oscillator, encoded as follows:

$$\text{ITBFREQ} = -16384 \cdot \frac{Fc}{Fs}$$

Where Fc is the centre frequency of the IF (or alias) and Fs is the ADC sample rate (nominally 30MHz). The setting of a negative value for ITBFREQ implies no spectrum inversion, whereas a positive value inverts the spectrum. This register sets the nominal received local oscillator frequency. Any frequency offsets are recovered separately within the device and fed back to the local oscillator.
The default value of –3345 corresponds to a nominal frequency of 36.125MHz which aliases to 6.125MHz.

3-19. EQUTAPSELECT

TAPSELECT **READ/WRITE** **CORE**
ADDRESS: 0x2B **DEFAULT: 0x00**

7	6	5	4	3	2	1	0
Reserved		Tap Select					

Bits 0 to 5: Set this register to select tap number whose values are loaded into the TAPI and TAPQ registers. The feedforward taps are numbered 0 to 9 with the main tap being tap 9. The feedback taps are numbered 10 to 39 with 10 being the first feedback tap.

Bits 6, 7: Reserved

3-20. EQUTAPI

TAPREAL **READ** **CORE**
ADDRESS: 0x2C **DEFAULT: 0x00**

7	6	5	4	3	2	1	0
Tap value (in-phase)							

Bits 0 to 7: Contains the real (in-phase) component of the equalizer tap specified by the TAPSELECT register. This must be read before the EQUTAPQ register.

3-21. EQUTAPQ

TAPQUAD **READ** **CORE**
ADDRESS: 0x2D **DEFAULT: 0x00**

7	6	5	4	3	2	1	0
Tap value (in-phase)							

Bits 0 to 7: Contains the imaginary (quadrature-phase) component of the equalizer tap specified by the TAPSELECT register. The process of reading this register automatically loads the next tap values into the EQUTAPI and EQUTAPQ registers (i.e. the TAPSELECT register need only be set once to obtain all the tap values).

3-22. CONSTELLATIONI

CONSTELLATIONI **READ** **CORE**
ADDRESS: 0x2E **DEFAULT: 0x00**

7	6	5	4	3	2	1	0
Equalizer Constellation Output (In-phase)							

Bbus its 0 to 7: Contains the real (in-phase) component of the equalizer output before the decision device. Due to the speed limitations of the I^2C bus this data is not continuous but is a sub-sampled version of the equalizer output. Even so, because of the random nature of the data, a constellation plot can still be formed from this data.

3-23. CONSTELLATIONQ

CONSTELLATIONQ **READ** **CORE**
ADDRESS: 0x2F **DEFAULT: 0x00**

7	6	5	4	3	2	1	0
Equalizer Constellation Output (Quadrature-phase)							

Bits 0 to 7: Contains the imaginary (quadrature-phase) component of the equalizer output before the decision device. Due to the speed limitations of the I^2C bus this data is not continuous but is a sub-sampled version of the equalizer output. Even so, because of the random nature of the data, a constellation plot can still be formed from this data.

3-24. AGCIFINTG

AGCIFINTG **READ** **CORE**
ADDRESS: 0x30 & 0x31 **DEFAULT: 0x0**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
AGC integrator								AGC integrator		Reserved					

Bits 0 to 7 & 6 to 7: Contains the setting of the IF external AGC integrator. Note that the data format allows a single byte read if 8-bit resolution is sufficient. It is expected that the AGC range will be approximately 80dB, hence 8 bits should give better than 0.5dB resolution.

3-25. RFAGC

RFAGC **READ/WRITE** **CORE**
ADDRESS: 0x32 & 0x33 **DEFAULT: 0x0**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RFAGC integrator								RFAGC integrator		Reserved					

Bits 0 to 7 & 6 to 7: Allows setting of an RF external AGC level to the RF AGC PWM output. Note that the RF AGC is simply a register controlled PWM output and not a feedback loop. It is intended that the host software should monitor the AGCIFINTG register and manually set the RFAGC to optimize system performance. Note that the data format allows a single byte write if 8 bit resolution is sufficient.

3-26. SNRESTIMATE

SNRESTIMATE **READ** **CORE**
ADDRESS: 0x3A **DEFAULT: 0x00**

7	6	5	4	3	2	1	0
SNR Estimate							

Bits 0 to 7: Once the equalizer has locked this register contains a value from which the channel SNR can be estimated. The register value is based upon a moving average of the MSE of the constellation. The equation below shows the relation between the register value and the SNRo at the output of the equalizer. The estimate can be improved by averaging the contents of this register.

$$SNRo = -9.5 \ln \left[\frac{SN\ Re\ stimate}{760} \right]$$

3-27. LMSMUTRACK

LMSMUTRACK **READ/WRITE** **CORE**
ADDRESS: 0x3B **DEFAULT: 0x03**

7	6	5	4	3	2	1	0
Reserved						DDE MU	

Bits 0, 1: Sets the adaption constant of the equalizer during DDE and TRK states. A value of zero gives the largest adaption constant and tracks fast changes in the channel at the expense of steady-state behaviour whilst a value of three gives the lowest steady-state loss at the expense of dynamic tracking capability. Even the default value of 3 gives significant tracking capability.

Bits 2 to 7: Reserved

3-28. SWEEPRNG

SWEEPRNG **READ/WRITE** **CORE**
ADDRESS: 0x3C **DEFAULT: 0x80**

7	6	5	4	3	2	1	0
Carrier Recovery Loop Sweep Range							

Bits 0 to 7: Sets the maximum frequency offset (positive and negative) over which the device acquires. The offset is twice the register value so, for example, the default value of 128 allows frequency offsets of ±256kHz to be acquired.

3-29. CHIP_INFO

CHIP_INFO **READ** **CORE**
ADDRESS: 0x00 **DEFAULT: 0x20**

7	6	5	4	3	2	1	0
MMDS Version			Major Revision Number			Minor Revision Number	

Holds the revision information for the MMDS. Will always return 0x20.

3-30. RST_REG

RST_REG **READ/WRITE** **CORE**
ADDRESS: 0x01 **DEFAULT: 0xF4**

7	6	5	4	3	2	1	0
ADC RST	PRE RST	EQU RST	FEC RST	Reserved	HARD	COLD	WARM

A hardware reset will occur when the RESETN pin to the IC is driven active. The RST_REG register shall record this action by setting the HARD flag to denote that a hardware reset has occurred.
In a typical application RST_REG may be polled by a microprocessor via the I^2C bus in order to detect whether a hardware reset has occurred. Once detected, the HARD flag may be reset via the I^2C bus by writing 0x00 to the RST_REG.
The microprocessor may also invoke two additional types of software reset (designated COLD and WARM) by writing directly to the RST_REG register as defined below.

ADC RST (Bit 7)	PRE RST (Bit 6)	EQU RST (Bit 5)	FEC RST (Bit 4)	(Bit 3)	HARD (Bit 2)	COLD (Bit 1)	WARM (Bit 0)	Meaning
X	X	X	X	X	X	0	0	Clear register
ADC RST	PRE RST	EQU RST	FEC RST	X	X	0	1	WARM Reset
ADC RST	PRE RST	EQU RST	FEC RST	X	X	1	X	COLD Reset

RST_REG in WRITE mode

The target blocks for the reset are specified via bits 4 to 7. To reset a block the appropriate bit must be set to 1. For example, writing 1001XX10b to RST_REG would initiate a cold reset to the ADC and FEC blocks.
Note that, as before, a write of 0x00 will clear the register.
When the register has been written to, the appropriate reset signals shall be generated. Cold or warm resets are terminated by writing to the RST_REG to clear the associated bit.
Note that bit 2 is unaffected by a software reset, and will remain 0, unless a separate reset occurred in the interim.

3-31. INTERRUPT_SOURCE

INTERRUPT_SOURCE **READ** **CORE**
ADDRESS: 0x02 **DEFAULT: 0x01**

7	6	5	4	3	2	1	0
Reserved	ES_SRC	TS_ERR_SRC	LLCK_FLAG_SRC	TS_LOCK_FLAG_SRC	EQM_LCK_SRC	PRE_LCK_SRC	AGC_LCK_SRC

When the MMDS signals an interrupt by driving the INTRPTN pin low, a bit in the interrupt source register will be set to indicate the source of the interrupt. The expected system operation will be for the STB CPU to read this register to determine the interrupt source, clear the equivalent bit in the mask register so that another interrupt is not immediately re-flagged, and then clear the source register by writing 0x00 to it. When not in auto-clear mode (see "Description of Functions 3-6") this will result in the MMDS releasing the open-drain INTRPTN pin, allowing it to be pulled high by an external resistor.

The possible interrupt sources are:

ES_SRC:
Errored second detected. When 1 or more 204-byte packet is uncorrectable in a second (due to more than 8 errored bytes) an errored second is flagged.

TS_ERR_SRC:
Transport stream error detected. When a 204-byte packet is output with errors (due to more than 8 errored bytes) the transport error indicator in the 4-byte MPEG2 header is set and the TSERR output is driven.

LLCK_FLAG_SRC:
Lost lock. When transport stream lock has been achieved, but is then subsequently lost due to n dropped sync bytes (where n is programmable in SET_SYNC_DETECT).

TS_LOCK_SRC:
Transport stream LOCK. Valid MPEG2 data has started being output from the MMDS.

EQM_LCK_SRC:
Equalizer LOCK. The equalizer is in tracking mode.

PRE_LCK_SRC:
Pre-processor LOCK. The pre-processor is in tracking mode.

AGC_LCK_SRC:
AGC LOCK. The external gain control loop has converged with the input signal in the correct range.
Note that this register must be cleared for INTRPTN to be released when not in auto-clear mode.

3-32. FEC_STATUS

FEC_STATUS **READ** **CORE**
ADDRESS: 0x05 **DEFAULT: 0x10**

7	6	5	4	3	2	1	0
SEVERELY ERRORED SECOND	ERRORED SECOND	LCK_FLAG	LLCK_FLAG	TS_LOCK	NEW_ ERRORED_ SECOND	TCM_LOCK	TCM_ SYNC_ ERROR

This register reflects the current status of the FEC. During normal operation this should return 0x28 to indicate both lock and transport stream lock. Note that the initial value is 0x10 to indicate that lock is lost – or in fact not yet gained.

SEVERELY ERRORED SECOND:
Severely errored second detected. When n or more 204-byte packets are uncorrectable in a second (due to more than 8 errored bytes, with n programmable in LT_QLTY_THRESHOLD) an errored second is flagged.

ERRORED SECOND:
Errored second detected. When 1 or more 204-byte packet is uncorrectable in a second (due to more than 8 errored bytes) an errored second is flagged.

LCK_FLAG:
Lock gained. When n sync bytes have been detected (where n is programmable in SET_SYNC_DETECT).

LLCK_FLAG:
Lost lock. When transport stream lock has been achieved, but is then subsequently lost due to n dropped sync bytes (where n is programmable in SET_SYNC_DETECT).

TS_LOCK:
Transport stream LOCK. Valid MPEG2 data has started being output from the MMDS.

NEW_ERRORED_SECOND:
This bit is high when the errored second and severely errored second values have been updated and not yet read. After FEC_STATUS has been read, this bit will return to zero until the values are next updated. The CWRJCT_COUNT register is updated over the same period as the errored seconds, so NEW_ERRORED_ SECOND could also be polled to determine when CWRJCT_COUNT holds a new value.

TCM_LOCK:
TCM symbol synchronization LOCK. This bit is high when TCM symbol synchronization is achieved.

TCM_SYNC_ERROR:
This bit is set when the TCM symbol synchronization cannot lock in the current channel conditions.

3-33. BER_EST

BER_EST **READ** **CORE**
ADDRESS: 0x0B & 0x0C & 0x0D **DEFAULT: 0x00**

7	6	5	4	3	2	1	0
New_ Estimate	Reserved		Overflow	Bit Error Estimate			

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Bit Error Estimate								Bit Error Estimate							

This register is big endian, with the MSByte at address 0x0B and the LSByte at address 0x0D.
The MSByte actually contains the top nibble of the BER value, together with a new_estimate flag. This flag is set at the end of the BER measurement period, to indicate that an unread BER value is in the register. It is reset after a read to the register has been performed to indicate that the BER value has been read.
The BER value is either an estimate, or measurement depending upon the setting in the FEC_PARAMS register.
If more than 2097151 errors have been seen in the measurement period then the OVERFLOW flag will be set to indicate that the BER_EST reading is invalid. To prevent an overflow, the user should decrease the value in the BER_EST_PERIOD register.

3-34. CWRJCT_CNT

CWRJCT_CNT **READ** **CORE**
ADDRESS: 0x0E & 0x0F **DEFAULT: 0x00**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Codeword reject count								Codeword reject count							

CWRJCT_CNT stands for codeword reject count. A codeword is one 204-byte packet. If such a packet contains more than 8 byte errors, the Reed Solomon will be unable to correct it successfully, and this is termed a rejected codeword. Therefore this register returns the count of rejected codewords in one second. It is intended that this register may be accessed when a severely errored second is flagged, if additional information is required regarding the degree of the severity.
This register is big endian, with the MSByte at address 0x0E and the LSByte at address 0x0F.

3-35. INTERRUPT_MASK

INTERRUPT_MASK **READ/WRITE** **CORE**
ADDRESS: 0x10 **DEFAULT: 0x00**

7	6	5	4	3	2	1	0
AUTO_CLR	ES_MSK	TS_ERR_ MSK	LLCK_ FLAG_MSK	TS_LOCK_ FLAG_MSK	EQM_LCK_ MSK	PRE_LCK_ MSK	AGC_LCK_ MSK

This register should be programmed by setting the bit corresponding to each required interrupt source. It defaults to 0x00, so no conditions will signal an interrupt. If one or more of the bits are set, then when that condition occurs, an interrupt will be by driving the INTRPTN pin low.
With AUTO_CLR turned off once an interrupt has been signalled, the bit corresponding to the interrupt source in INTERRUPT_MASK must be reset to prevent an interrupt being continually signalled. Once this has been done, the INTERRUPT_SOURCE register can also be reset to release the open-drain INTRPTN pin, allowing it to be pulled high by an external resistor.
With AUTO_CLR turned on, when an interrupt occurs the INTRPTN pin goes low for 4 clocks (133ns) and then returns high. The source of the interrupt is latched in the INTERRUPT_SOURCE register, and the INTRPTN pin will go low again each time the interrupt occurs. By this method, for example, an exact count of lock losses, errored seconds or transport stream errors could be gained. Also acquisition times can be easily measured by interrupting on AGC_LCK_MSK and TS_LOCK_MSK with AUTO_CLR on.

The possible interrupt sources are:

ES_MSK:
Errored second detected. When 1 or more 204-byte packet is uncorrectable in a second (due to more than 8 errored bytes) an errored second is flagged.

TS_ERR_MSK:
Transport stream error detected. When a 204-byte packet is output with errors (due to more than 8 errored bytes) the transport error indicator in the 4-byte MPEG2 header is set and the TSERR output is driven.

LLCK_FLAG_MSK:
Lost lock. When transport stream lock has been achieved, but is then subsequently lost due to n dropped sync bytes (where n is programmable in SET_SYNC_DETECT).

TS_LOCK_MSK:
Transport stream LOCK. Valid MPEG2 data has started being output from the MMDS.

EQM_LCK_MSK:
Equalizer LOCK. The equalizer is in tracking mode.

PRE_LCK_MSK:
Pre-processor LOCK. The pre-processor is in tracking mode.

AGC_LCK_MSK:
AGC LOCK. The external gain control loop has converged with the input signal in the correct range.

Note that if the bit corresponding to the interrupt condition is not reset in this register and just the INTERRUPT_SOURCE register is written to (to clear the interrupt), the INTRPTN pin will not trigger an addition interrupt if the interrupt condition is no longer true.
For example, if an interrupt were configured by setting the LLCK_FLAG_ MSK bit, a lost lock condition would be signalled via an interrupt. The interrupt could be cleared by writing to the LLCK_FLAG_ SRC bit in the INTERRUPT_SOURCE register, and in the meantime if the MMDS had regained lock , the interrupt condition would no longer be true and the INTRPTN pin would remain open-drain.

3-36. FEC_PARAMS

FEC_PARAMS **READ/WRITE** **CORE**
ADDRESS: 0x14 **DEFAULT: 0x32**

7	6	5	4	3	2	1	0
Reserved		TS_CLK_POSEDGE_LATCHING	TS_LOCK_ACTIVE_HI	NO_DEEP_DEINT	MEASUREMENT_SELECT	TRI_STATE_OUTPUTS	RS_DISABLE

TS_CLK_POSEDGE_LATCHING:
Defaults to one, which strobes TSCLK such that TSDATA should be latched on its positive edge by any logic interfacing to the MMDS. When zero, TSDATA should be latched on the negative edge of TSCLK.

NO_DEEP_DEINT:
When this bit is set, it prevents a de-interleave depth of I=204 on 256QAM or TCM. A de-interleave depth of I = 12 is used instead.

MEASUREMENT_SELECT:
When this bit is set, the MMDS will be configured to measure the BER, assuming that ETSI standard NULL packets are being transmitted. When set, the RS_DISABLE bit must be set to enable pre Reed Solomon BER measurements to be made or the RS_DISABLE bit must be cleared to enable post Reed Solomon BER measurements to be made. When reset, the MMDS will estimate the BER by measuring the number of bit corrections which the Reed Solomon makes. Note that although termed an estimate, this value should be very accurate until the BER rises to 10^{-4} , where the limits of the Reed Solomon are neared.

TRI_STATE_OUTPUTS:
When this bit is set, all the transport stream pins, TSVALID, TSSYNC, TSERR, TSCORR and TSDATA will go tristate. This is the default reset condition for the MMDS so that in a combined DVB-C / DVB-S or DVB-T system, the transport stream outputs may be simply wired together thereby eliminating the need for any off-chip tri-state buffers.

RS_DISABLE:
When this bit is set the Reed Solomon decoder is disabled, so that the transport stream data retains any errors. This bit MUST be set if the MEASUREMENT_SELECT bit is set to enable BER measurement. When reset the Reed Solomon decoder corrects errors.

3-37. SET_SYNC_DETECT

SET_SYNC_DETECT **READ/WRITE** **CORE**
ADDRESS: 0x25 **DEFAULT: 0x1D**

7	6	5	4	3	2	1	0
SYNC_ CNTR_ MODE	TSSYNC_ CNTR_ MODE	Sync_loss_ladder_length			Sync_ladder_length		

All the bits in this register are used to control the lock and lost lock mechanisms in the MMDS FEC. There are two stages of FEC lock: LOCK and TSLOCK.
LOCK indicates sync byte lock. The FEC hunts for either the MPEG2 sync byte (0x47) or inverted sync byte (0xB8) in the received byte stream. Once either is detected, a search is started 204 bytes later for the next one. Every time a sync byte or inverted sync byte is successfully detected 204 bytes from the previous one a count is incremented. If neither a sync byte nor an inverted sync byte are detected when expected the count is either decremented or reset to zero. The former mode of operation is termed up/down and the latter reset.
TSLOCK indicates transport stream lock. This occurs using a similar mechanism to that described above, except the TSLOCK logic operates upon the post error-corrected data. This ensures that the lock mechanism, and more importantly the lost-lock mechanism gains the benefit of operating on data with a lower BER. This enables the MMDS to remain in lock under conditions where otherwise despite the Reed Solomon being able to successfully correct errors, lock is lost due to errored sync bytes.

The LOCK and TSLOCK logic searches for n consecutive sync or inverted sync bytes where n is given by :

n = SYNC_LADDER_LENGTH – SYNC_LOSS_LADDER_LENGTH.

SYNC_CNTR_MODE:
When this bit is set, the LOCK logic operates in up/down mode. When reset it operates in reset mode.

TS_SYNC_CNTR_MODE:
When this bit is set, the TSLOCK logic operates in up/down mode. When reset it operates in reset mode.

SYNC_LOSS_LADDER_LENGTH[2:0]:
By varying SYNC_LOSS_LADDER_LENGTH, losing sync lock can be made easier (SYNC_LADDER_ LENGTH-1) or harder (small value). SYNC_LOSS_LADDER_ LENGTH must have a value less than SYNC_LADDER_LENGTH.

SYNC_LADDER_LENGTH[2:0]:
By varying SYNC_LADDER_LENGTH, sync lock can be made easier (small value) or harder (large value) to achieve. SYNC_LADDER_LENGTH must have a minimum value of 2.

3-38. LT_QLTY_THRESHOLD

LT_QLTY_THRESHOLD **READ/WRITE** **CORE**
ADDRESS: 0x26 **DEFAULT: 0x04**

7	6	5	4	3	2	1	0
Long term Quality Threshold							

The MMDS retains a count of the number of codewords rejected by the Reed Solomon in one second (where a codeword is one 204-byte packet). This count is compared to the value in LT_QLTY_THRESHOLD and if it exceeds it, a severely errored second is flagged. The default value is one.

3-39. BER_EST_PERIOD

BER_EST_PERIOD **READ/WRITE** **CORE**
ADDRESS: 0x27 **DEFAULT: 0x0E**

7	6	5	4	3	2	1	0
Reserved			BER Estimation Measurement Period				

BER_EST_PERIOD sets the BER estimation/measurement period, governed by the equation:

$$\text{Estimation/measurement period} = 2^{\text{BER\_EST\_PERIOD}} \text{ 204-byte packets}$$

Note that the internal counter supports values of between 0x01 and 0x1f to yield a measurement period between 1 and 2×10^9 204-byte packets. Over the range of QAM levels and data rates this results in a maximum measurement period of 22 hours (256QAM, 7Mbaud). The default is 0x0e, which is 16000 packets.

3-40. TUNER_CTL

TUNER_CTL **READ/WRITE** **CORE**
ADDRESS: 0x34 to 0x37 **DEFAULT: 0x00000000**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Mode	Send	Sel	Sen_pol	SDATA[27:24]				SDATA[23:16]							
SDATA[15:8]								SDATA[7:0]							

MODE:
This selects the source of control data for the tuner interface. If MODE=0 the data driven over the tuner interface is sourced from the CPU interface pins TCLK, TDATA, TEN, TWR_N. This is the default mode after reset. If MODE = 1 SDATA in the TUNER_CTRL register is transmitted over the tuner interface.

SEND:
When this bit is set the SDATA transmission over the tuner interface is initiated. This bit is cleared when the transmission terminates.

SEL:
This bit selects the active tuner PLL pin. If SEL = 0 transmission is active using the SEL0 pin. If SEL = 1 transmission is active using the SEL1 pin.

SEN_POL:
This bit selects the polarity of the SEN outputs. If SEN_POL = 0 the SEN outputs are active low. If SEN_POL = 0 the SEN outputs are active high.

SDATA[27:0]:
Holds data for transmission over the tuner interface.

When the tuner interface is controlled via the CPU pins, during reset the active channel SEN output is low and thereafter it follows the TEN CPU input pin. The inactive channel SEN is set to its inactive state during reset according to the polarity selection of SEN_POL.
When the tuner interface is controlled via the I^2C bus SEND control both the active and inactive SEN pins are driven according to the SEN_POL control.

3-41. TCM_CONFIG

TCM_CONFIG **READ/WRITE** **CORE**
ADDRESS: 0x38 **DEFAULT: 0xAB**

7	6	5	4	3	2	1	0
TCM_ ENABLE	Reserved	FEC_ AUTO_LOCK	Reserved	Equalizer State Threshold			

TCM_ENABLE:
This control is used to select between QAM decoding and TCM decoding. When set TCM decoding is enabled.

FEC_AUTO_LOCK:
This control, if set, enables the FEC lock status to automatically control re-acquisition in the equalizer. If this bit is not set re-acquisition in the equalizer is controlled by software reset.

EQU_STATE_THRES:
This controls when the TCM decoder starts its synchronization to TCM symbols. This control can be programmed to one of the equivalent states in the ESM_STATUS register. When programmed to an equivalent state of the equalizer the TCM decode starts synchronizing when the equalizer reaches that state. If a state is programmed in this control which does not exist in the equalizer the TCM decoder will not synchronize to the input data and no FEC lock can be achieved.

3-42. TS_MODE

TS_MODE **READ/WRITE** **CORE**
ADDRESS: 0x39 **DEFAULT: 0xB4**

7	6	5	4	3	2	1	0
TSVALID_ ACTIVE_HI	TSSYNC_ ACTIVE_HI	TSERR_ ACTIVE_HI	OUTPUT_ SEL_MSB	TSVALID_ PULSE	TSERR_ PULSE	TSERR_ FULL	TSCLK_ FULL

TSVALID_ACTIVE_HI:
When this bit is set, the TSVALID pin will function in active high mode. When reset, it will be active low.

TSSYNC_ACTIVE_HI:
When this bit is set, the TSSYNC pin will function in active high mode. When reset, it will be active low.

TSERR_ACTIVE_HI:
When this bit is set, the TSERR pin will function in active high mode. When reset, it will be active low.

OUTPUT_SEL_MSB:
When this bit is set, the MSB for the TSDATA output will be TSDATA[7]. When reset, the TSDATA output MSB will be TSDATA[0].

TSVALID_PULSE:
Determines whether the TSVALID signal is pulsed or constant. Pulsed when set.

TSERR_PULSE:
Determines whether the TSERR signal is pulsed or constant. Pulsed when set.

TSERR_FULL:
Determines whether the TSERR signal is valid for 204 bytes or for 188 bytes. Valid only when TSERR_PULSE is not set. Valid for 204 bytes when set.

TSCLK_FULL:
Determines whether the TSCLK signal is valid for 204 bytes or 188 bytes. Valid for 204 bytes when set.

3-43. AGCTGT

AGCTGT **READ/WRITE** **EXPERT**
ADDRESS: 0x83 **DEFAULT: 0x69**

7	6	5	4	3	2	1	0
AGC Target Level							

Bits 0 to 7: Sets the target signal level used by the external gain control (AGC) loop. It sets the required mean level of the input IF signal which corresponds to approximately the Peak to Peak range in bits divided by 8. An AGC_TGT setting of 128 corresponds with the onset of clipping when a 256 QAM signal is applied to the 10-bit input.
The gain control loop is deemed to have settled when the integrated magnitude error falls below a threshold value for a period greater than 136ms. The status of the loop is indicated by the AGCLOCK flag in the TSM_STATUS register.
The default value of 105 corresponds to the pk-pk value approximately 3dB below full scale on the ADC in a clear channel. This margin is required to cope with the increased peak to mean signal levels in a multipath channel.

Application Circuit Diagrams

The following circuit diagrams show examples of how to interface to the CXD1958Q. Fig. 12 shows a typical circuit configuration where the tuner section is controlled via I²C bus.

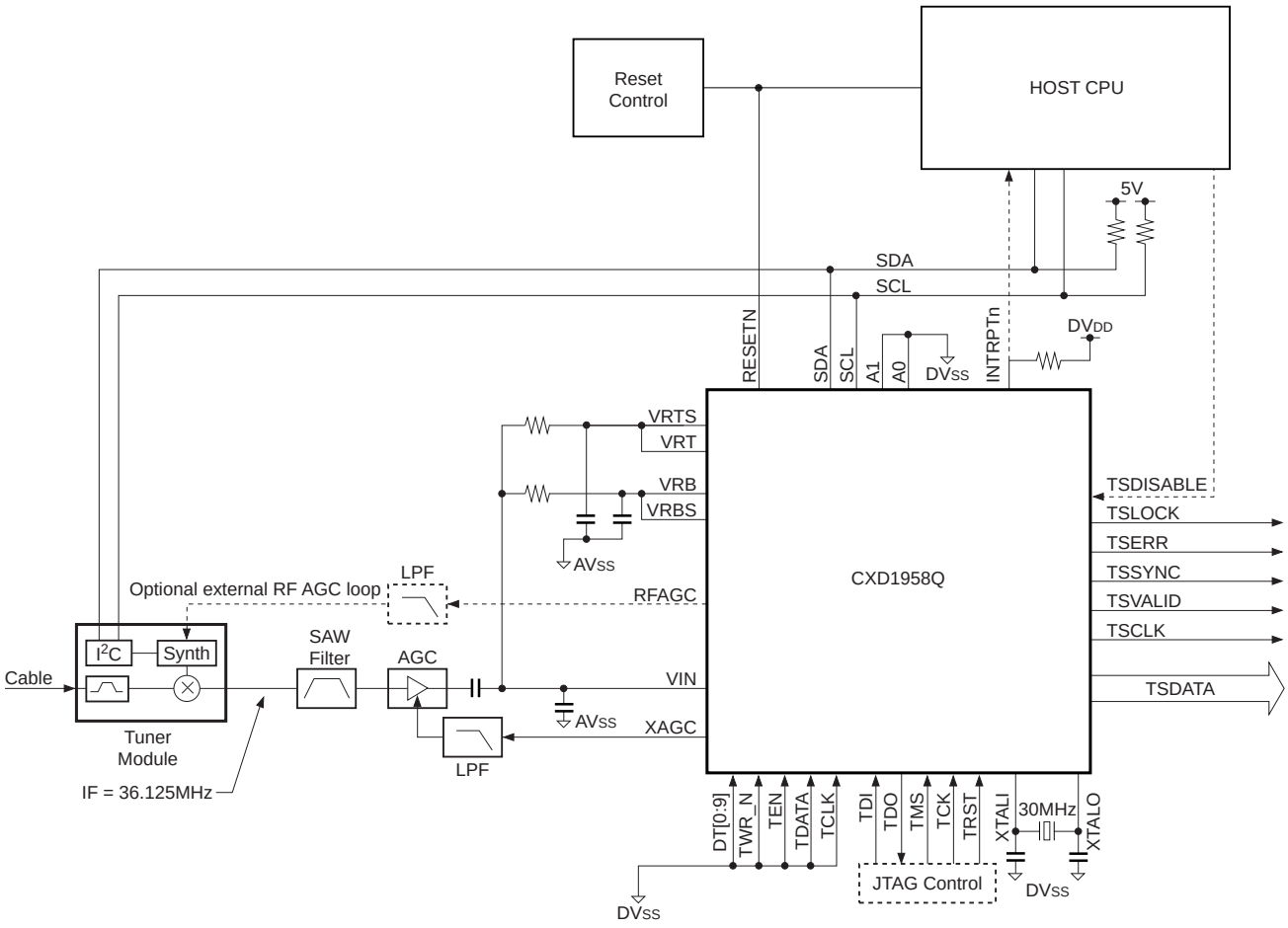


Fig. 12. Typical Circuit for CXD1958Q

If the tuner is controlled via I²C bus it is preferable to prevent general I²C bus traffic from reaching the tuner and only allow tuner specific commands to pass to the tuner. This can be done using the SEN0 pin, which is programmable via I²C bus by writing to the SEL bit in the TUNER_CTL register. The SEN0 pin is then used as a pass-FET control signal thereby isolating the I²C bus traffic from the tuner when not required by the tuner. Fig. 13 shows the connectivity of the tuner when using SEN0 as pass-FET control.

The tuner can also be controlled via 3-wire bus. In this case there are two modes in which the 3-wire bus pins can be controlled. The first is to set the 3-wire bus outputs via the host CPU control lines (TWR_N, TEN, TCLK and TDATA). The second is to set the 3-wire bus outputs via I²C bus. Selection of these two modes is done via the TUNER_CTL register (see "Control Register Definitions" 3-40. TUNER_CTL). Fig. 14 shows the connectivity of the tuner using 3-wire bus pins.

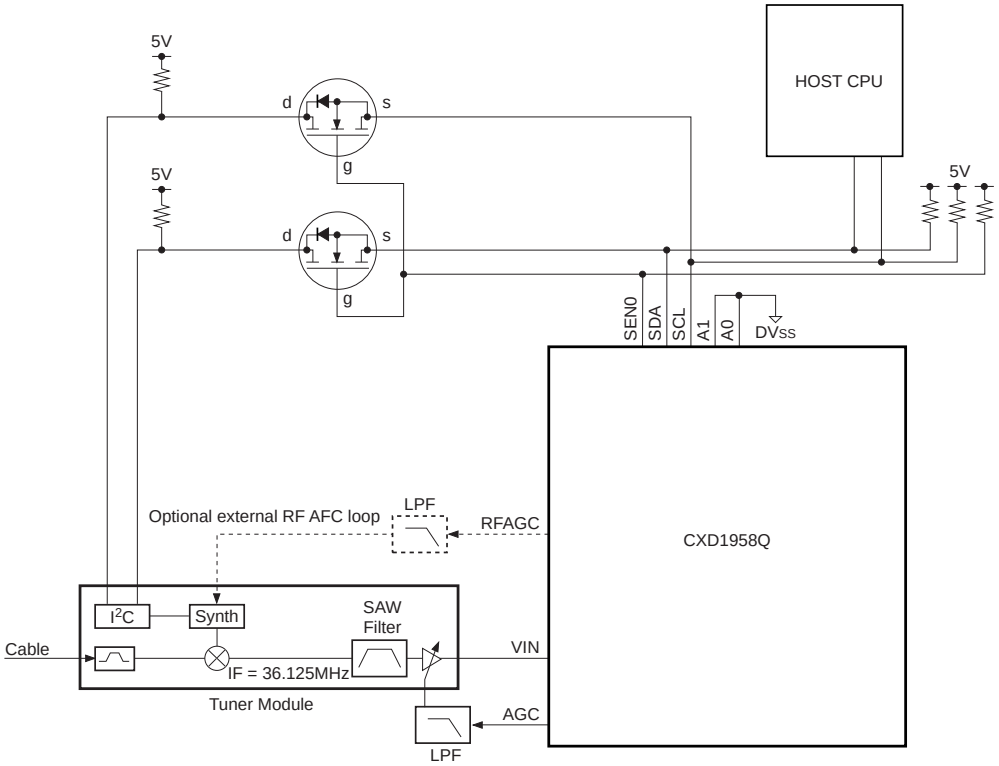


Fig. 13. Interface to Tuner using SEN0 as Pass-FET Control

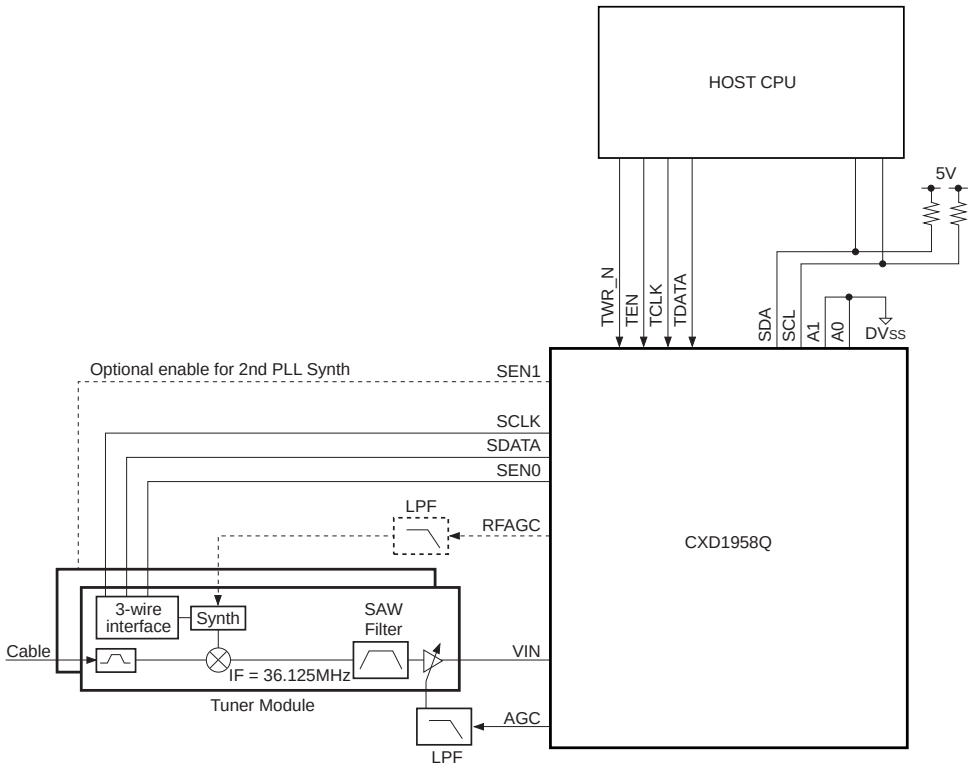
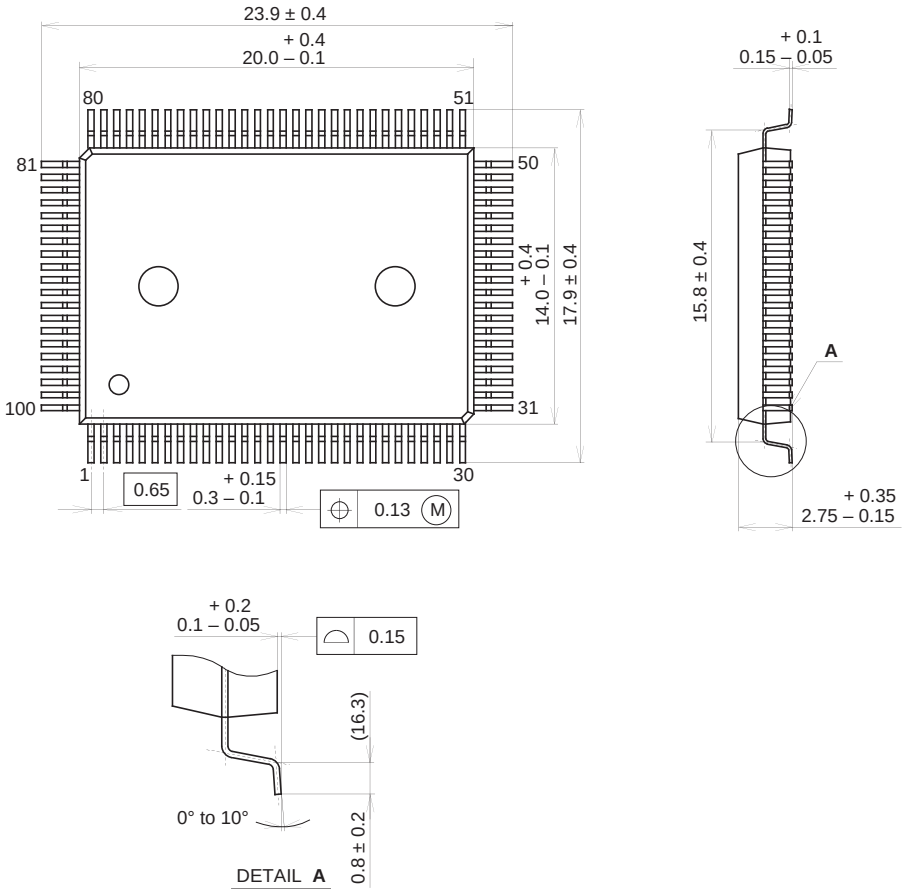


Fig. 14. 3-Wire Bus Interface to Tuner

Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g