SONY

CXD1961AQ

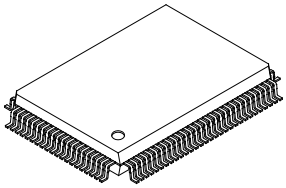
DVB-S Frontend IC (QPSK demodulation + FEC) *Preliminary*

For the availability of this product, please contact the sales office.

Description

The CXD1961AQ is a single chip DVB compliant Satellite Broadcasting Frontend IC, including dual A/D converter for analog baseband I/Q input, QPSK demodulator, Viterbi decoder Reed-Solomon decoder and Energy Dispersal descrambler. It is suitable for use in a DVB Integrated Receiver Decoder.

100 pin QFP (Plastic)



Features

- Dual 6 bit A/D converter
- QPSK demodulator
  - Multi-symbol rate operation
  - Nyquist Roll off filter (α = 0.35)
  - Clock recovery circuit
  - Carrier recovery circuit
  - AGC control (PWM output)
- Viterbi decoder
  - Constraint length 7
  - Truncation length 144
  - BER monitor of QPSK demodulator output
- Frame synchronization circuit
- Convolutional de-interleaver
- Reed-Solomon decoder (204,188)
  - BER monitor of Viterbi decoder output
- Energy dispersal descrambler
- CPU interface circuit
  - I^2C bus interface (5V input capability)
- Package QFP 100pin
- Operating frequency 20 to 30MSPS
- Power consumption 750mW (@3.3V 30MSPS typical)
- Process 0.4µm CMOS Technology

Application

DVB-S Set Top Box (Satellite)

Absolute Maximum Rating (Ta = 25°C, GND = 0V)

• Power Supply	V_{DD}	–0.5 to +4.6	V
• Input Voltage	V_{IN}	–0.5 to V_{DD} + 0.5	V
• Output Voltage	V_{OUT}	–0.5 to V_{DD} + 0.5	V
• I/O Voltage	$V_{I/O}$	–0.5 to V_{DD} + 0.5	V
• CPU I/F pin	Vcpuif	–0.5 to +5.5	V
• Storage Temperature	Tstg	–55 to +150	°C

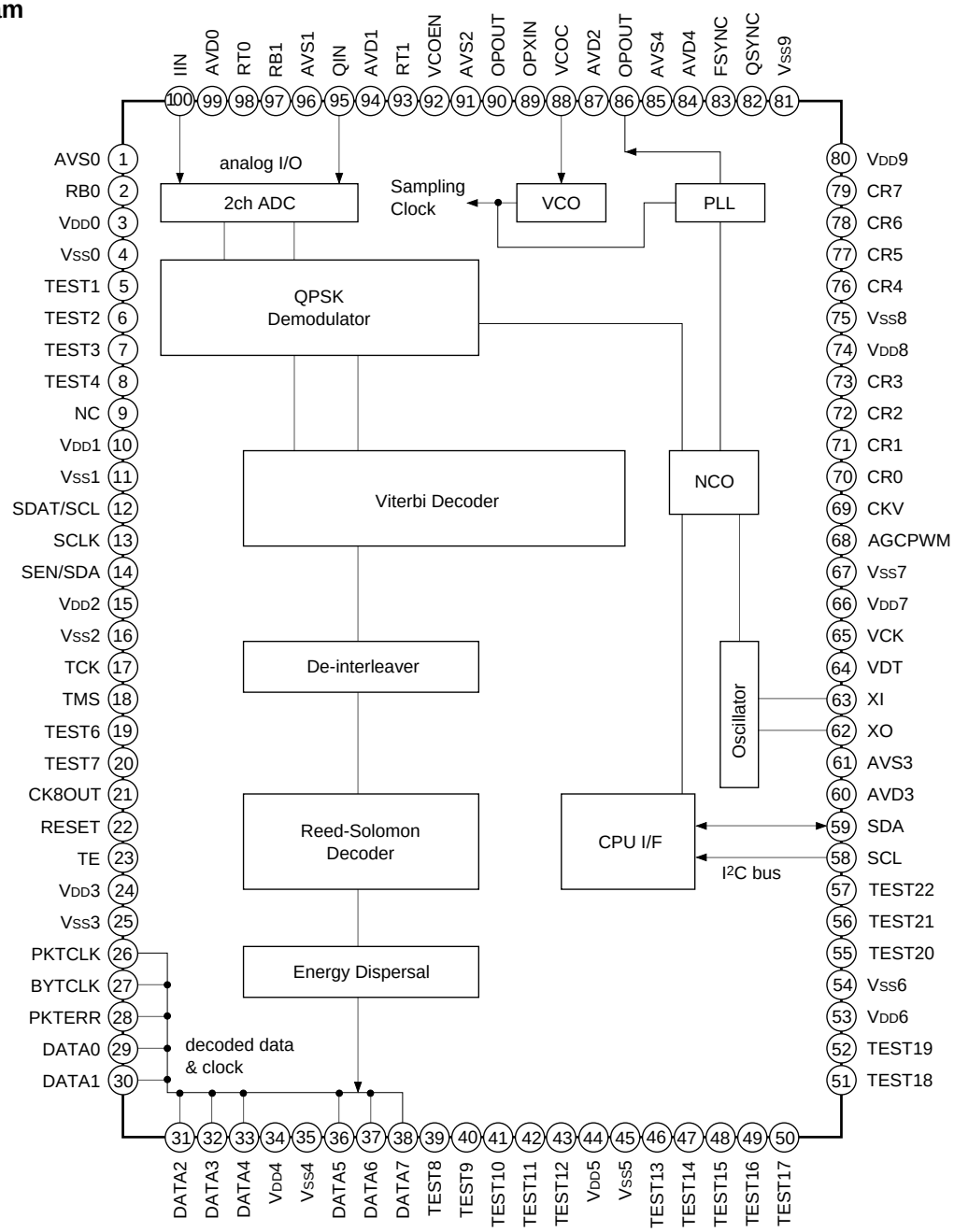
Recommended Operating Condition

(Ta = 0 to 75°C, GND = 0V)

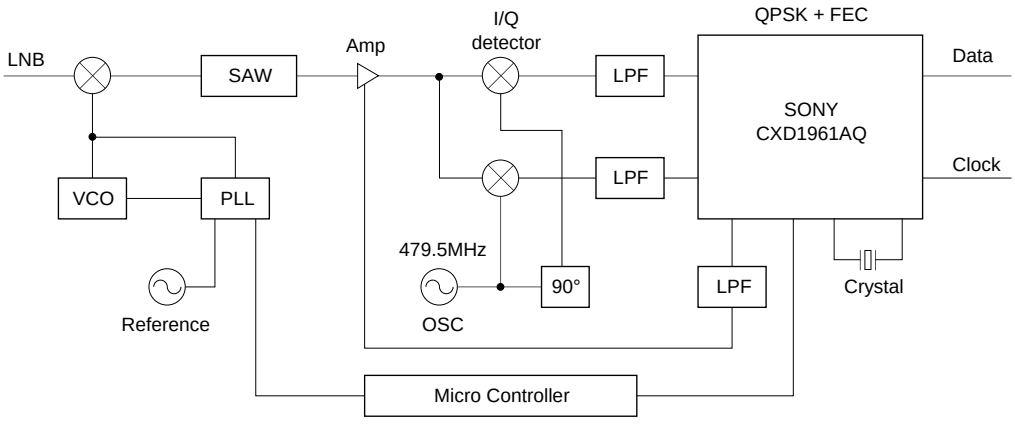
• Power Supply	V_{DD}	3.15 to 3.45	V
• Input High level	V_{IH}	0.7 × V_{DD} to V_{DD} + 0.5	V
• Input Low level	V_{IL}	0.3 to 0.2 × V_{DD}	V

PE97854-PS

Block Diagram



Typical Block Diagram



Functional Description

(1) A/D Converters

The CXD1961AQ has dual 6 bit A/D converters to quantize the analog baseband I/Q signal. The sampling rate is two times the symbol rate. The input range is determined by the external resisters. See reference circuit (1). The DC offset cancellation function is set by setting CPU I/F register 1E,1F(hex).

(2) Clock Recovery Circuit

The CXD1961AQ can operate at multiple symbol rates between 20 to 30MSPS. Initial sampling clock frequency is set by a 24 bit control word via CPU I/F register 18, 19, 1A (hex). This control word is written to the numerically controlled oscillator (NCO). The internal clock recovery loop feeds clock error data to the above NCO to provide sampling timing correction. The relation between the symbol rate and the control word is;

$$(\text{symbol rate}) = 4 \times \text{NCO}[23:0] \times \text{Fcrystal} \div 2^{24} \text{ (Hz)}$$

where NCO [23:0] is the 24 bit control word and Fcrystal is crystal frequency (Hz).
The clock recovery loop coefficient and the loop gain are set by setting CPU I/Fregister 0C (hex) accordingly. See reference circuit (2). The recovered symbol clock can be monitored at Pin 69.

There are three internal sub-registers to save the NCO control word. By setting the number of the preset sub-register, the control word corresponded to the certain symbol rate is set to the internal NCO. Contents of the sub-register are deleted by power off or reset by pin 22. Refer to the explanation of CPU I/F register 0D (hex).

(3) Carrier Recovery Circuit

Any carrier frequency offset which remains on the analog baseband I/Q input is compensated by the internal digital costas loop. The capture range is ±Rs/8 (Rs: symbol rate). When the carrier capture is performed, QPSK lock flag QSYNC goes high. QSYNC is output at Pin 82 and CPU I/F register 09 (hex). In QPSK synchronization, the carrier offset estimation value is output at CPU I/F register 02 (hex) as AFC [7:0]. The frequency offset is;

$$(\text{carrier offset}) = \text{Rs} \times \text{AFC}[7:0] \div 512 \text{ (Hz)}$$

where AFC7 is the sign bit that represents the direction of the offset.

(4) Nyquist Roll off Filter

The Nyquist roll off filter for each channel are embedded. The roll off factor is 0.35.

(5) Auto Gain Control

By comparing the demodulated I/Q amplitude ($I^2 + Q^2$) and the reference level which is set via CPU I/F register 21 (hex), the AGC control signal is generated as PWM output at Pin 68. The polarity of the AGC can be reversed by setting CPU I/F register 10 (hex). For the Tuner interface, see the reference circuit (4).

(6) Viterbi Decoder

The punctured decoding and Viterbi decoding are performed on the demodulated I and Q data. The punctured rate is programmable from 1/2 to 7/8. When punctured mapping is performed, Viterbi lock flag at CPU I/F register 09 (hex) goes one. Bit error count at QPSK demodulator output is estimated and output to CPU I/F register 03, 04 (hex) as 16 bit data.

(7) Frame synchronization and Deinterleaver

By detecting the MPEG2 sync word 47 (hex), the synchronization of the data packet is achieved, and the convolutional deinterleaver then recovers the original data order.

(8) Reed-Solomon Decoder

In DVB systems, 16 parity bytes are added to the 188 data bytes, so that up to 8 error bytes are correctable by the Reed-Solomon decoder. If there are more than 8 error bytes in a packet, error correction is not performed and the packet error flag PKTERR (Pin 28) goes high during the packet to indicate that the packet is not correctable. The MSB of the second byte of the uncorrectable packet also becomes one. Bit error count at Viterbi decoder output is estimated and output every 1280 packet (=$204 \times 8 \times 1280$ bit) to CPU I/F register 06, 07 (hex) at a resolution of 16 bits.

(9) Energy Dispersal Descrambler

Energy dispersal descrambling is represented by the polynomial $X^{15} + X^{14} + 1$. The initial sequence is loaded when an inverted MPEG sync word B8 (hex) is detected. When MPEG sync word including inverted one is detected every 204 bytes, the lock flag of the whole IC "FSYNC" goes high. FSYNC is output at Pin 83 and CPU I/F register 09 (hex).

(10) CPU Interface

The CXD1961AQ has an I^2C bus interface. Serial clock SCL is Pin 58 and serial data in out SDA is Pin 59. Slave address is "1101 111" (DChex).

<Write data>

During the write operation, the second byte is input as the sub-address of the start position. The third byte then forms the data to be written to the start register. Successive data bytes are written to the successive sub-address registers up to 21 (hex). Note that registers of sub-addresses 00 (hex) to 0B (hex) are read only.

STA	Slave address 1101 111	0	ACK	Sub address N (hex)	ACK	Input data for sub-address N (hex)	ACK	Input data for sub-address N + 1 (hex)	ACK	. . .	STP

STA: start condition ACK: acknowledge

STP: stop condition XACK: no acknowledge

<Read operation>

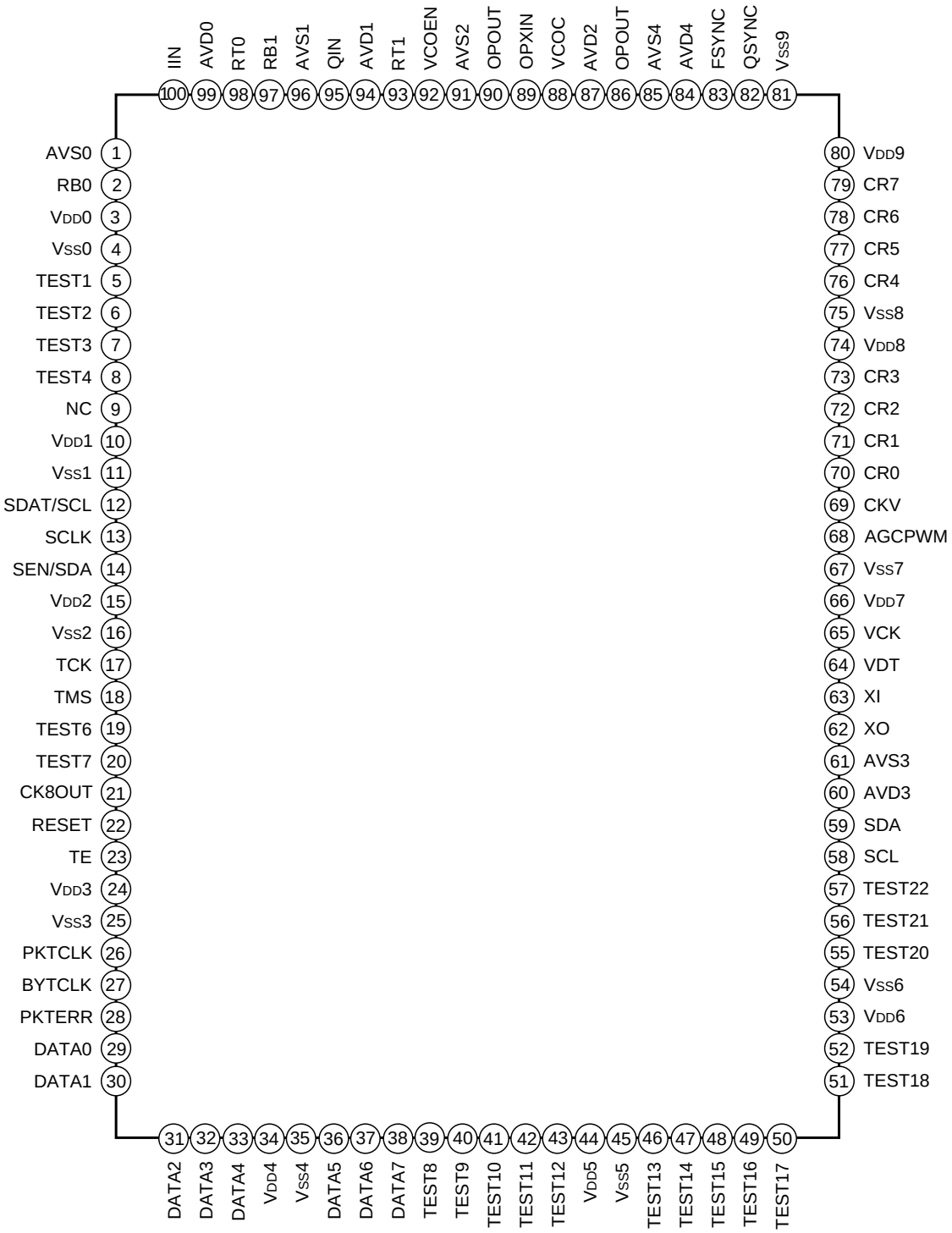
Before the read operation, the sub-address of the start register to be read is input by using write operation, and terminated with a stop condition. Read operation then begins with the second byte which is the data of the start register. Data of the successive sub-address registers are read successively following the second byte. All registers can be read.

STA	Slave address 1101 111	0	ACK	Sub address N (hex)	ACK	STP

STA	Slave address 1101 111	1	ACK	Output data for sub-address N (hex)	ACK	Output data for sub-address N + 1 (hex)	ACK	. . .	XACK	STP

Both SCL and SDA have 5V input capability.

Pin Configuration



Pin List

No.	Symbol	I/O type
1	AVS0	Analog V_{SS}
2	RB0	Ref. voltage input
3	V_{DD}0	Digital V_{DD}
4	V_{SS}0	Digital V_{SS}
5 to 8	TEST1 to 4	CMOS input
9	NC	No Connection
10	V_{DD}1	Digital V_{DD}
11	V_{SS}1	Digital V_{SS}
12	SDAT/SCL	3-state CMOS output
13	SCLK	3-state CMOS output
14	SEN/SDA	In out with Pull up
15	V_{DD}2	Digital V_{DD}
16	V_{SS}2	Digital V_{SS}
17	TCK	Input with pull up
18	TMS	Input with pull up
19	TEST6	CMOS input
20	TEST7	Input with pull up
21	CK8OUT	CMOS output
22	RESET	Input with pull up
23	TE	Input with pull down
24	V_{DD}3	Digital V_{DD}
25	V_{SS}3	Digital V_{SS}
26	PKTCLK	3-state CMOS output
27	BYTCLK	3-state CMOS output
28	PKTERR	3-state CMOS output
29 to 33	DATA0 to 4	3-state CMOS output
34	V_{DD}4	Digital V_{DD}
35	V_{SS}4	Digital V_{SS}
36 to 38	DATA5 to 7	3-state CMOS output
39 to 43	TEST8 to 12	CMOS in out
44	V_{DD}5	Digital V_{DD}
45	V_{SS}5	Digital V_{SS}
46 to 48	TEST13 to 15	CMOS in out
49 to 52	TEST16 to 19	CMOS input

No.	Symbol	I/O type
53	$V_{DD}6$	Digital V_{DD}
54	$V_{SS}6$	Digital V_{SS}
55 to 57	TEST20 to 22	CMOS input
58	SCL	5V input
59	SDA	5V open drain in out
60	AVD3	Crystal V_{DD}
61	AVS3	Crystal V_{SS}
62	XO	Oscillator output
63	XI	Oscillator input
64	VDT	CMOS in out
65	VCK	CMOS in out
66	$V_{DD}7$	Digital V_{DD}
67	$V_{SS}7$	Digital V_{SS}
68	AGCPWM	CMOS output
69	CKV	CMOS in out
70 to 73	CR0 to 3	CMOS output
74	$V_{DD}8$	Digital V_{DD}
75	$V_{SS}8$	Digital V_{SS}
76 to 79	CR4 to 7	CMOS output
80	$V_{DD}9$	Digital V_{DD}
81	$V_{SS}9$	Digital V_{SS}
82	QSYNC	CMOS output
83	FSYNC	CMOS output
84	AVD4	Analog V_{DD}
85	AVS4	Analog V_{SS}
86	CPOUT	3-state CMOS output
87	AVD2	Analog V_{DD}
88	VCOC	Analog input
89	OPXIN	Analog input
90	OPOUT	Analog output
91	AVS2	Analog V_{SS}
92	VCOEN	CMOS input
93	RT1	Ref. voltage input
94	AVD1	Analog V_{DD}

No.	Symbol	I/O type
95	QIN	Analog input
96	AVS1	Analog V_{SS}
97	RB1	Ref. voltage input
98	RT0	Ref. voltage input
99	AVD0	Analog V_{DD}
100	IIN	Analog input

Note) Apply 0.1µF capacitor to every power supply terminal and reference voltage input (RB0, RB1, RT0, RT1).

Pin Explanation

1. A/D Converter

Function	ADC for I input		ADC for Q input	
	Pin No.	Pin name	Pin No.	Pin name
Analog signal input	100	IIN	95	QIN
Top reference level input	98	RT0	93	RT1
Bottom reference level input	2	RB0	97	RB1
Analog power supply (+3.3V)	99	AVD0	94	AVD1
Analog ground	1	AVS0	96	AVS1

See reference circuit (1)

2. Clock Recovery

2-1. Crystal

Function	Pin No.	Pin name
Crystal oscillator (output)	62	XO
Crystal oscillator (input)	63	XI
Crystal oscillator power supply (+3.3V)	60	AVD3
Crystal oscillator ground	61	AVS3

See reference circuit (3)

2-2. VCO · OP-Amp

Function	Pin No.	Pin name
Charge Pump output	86	CPOUT
Charge pump power supply (+3.3V)	84	AVD4
Charge pump ground	85	AVS4
VCO control voltage input	88	VCOC
VCO enable (H: enable)	92	VCOEN
OP-Amp negative input	89	OPXIN
OP-Amp output	90	OPOUT
VCO · OP-Amp power supply (+3.3V)	87	AVD2
VCO · OP-Amp ground	91	AVS2

See reference circuit (2)

2-3. Clock Recovery

Function	Pin No.	Pin name
Clock error output (for clock recovery by VCXO)	70 to 73 76 to 79	CR0 to 3 CR4 to 7
Recovered symbol clock output (switchable to sampling clock output)	69	CKV

3. Carrier Recovery

Function	Pin No.	Pin name
Carrier lock flag (H: lock)	82	QSYNC

4. AGC

Function	Pin No.	Pin name
AGC control data (PWM output)	68	AGCPWM

See reference circuit (4)

5. Viterbi Decoder

Function	Pin No.	Pin name
Viterbi clock output	65	VCK
Viterbi decoded data output	64	VDT

These pins can be fixed to ground by setting CPU I/F register 0E (hex).

6. Frame Synchronization

Function	Pin No.	Pin name
Frame synchronization flag (H: sync)	83	FSYNC

7. Reed-Solomon Decoder/Data output

Function	Pin No.	Pin name
Data output clock (parallel mode) Byte clock (Serial mode) Viterbi clock	27	BYTCLK
Packet clock (H: data, L: parity)	26	PKTCLK
Uncorrectable packet flag	28	PKTERR
Data output (Parallel mode) LSB data (Serial mode) serial data (MSB first)	29	DATA0
Data output (Parallel mode) DATA7 = MSB (Serial mode) Hi-Z	30 to 33 36 to 38	DATA1 to 4 DATA5 to 7

Output mode (Serial or Parallel) is switched by setting CPU I/F register 0F (hex).

8. CPU Interface

Function	Pin No.	Pin name
I^2C bus serial clock input	58	SCL
I^2C bus serial data in out	59	SDA

9. Reset

Function	Pin No.	Pin name
Reset (L: reset/fix H for normal use)	22	RESET

10. Power Supply

Function	Pin No.	Pin name
Digital power supply (+3.3V)	10, 15, 24, 34, 44, 53, 66, 74, 80	V_{DD}0 to 9
Digital ground	11, 16, 25, 35, 45, 54, 67, 75, 81	V_{SS}0 to 9

Apply 0.1µF capacitor to every power supply terminal.

11. Test / Others

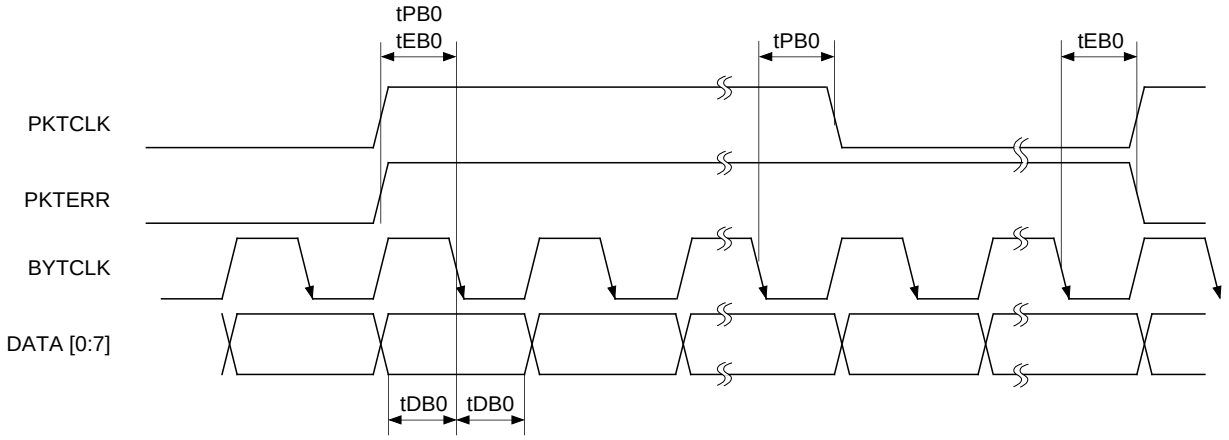
Function	Pin No.	Pin name
Test mode enable (Fix L for normal use)	23	TE
Test clock (Fix H for normal use)	17	TCK
Test mode Control (Fix H for normal use)	18	TMS
Test input (Fix L)	5 to 8, 20 49 to 52 55 to 57	TEST1 to 4, TEST7 TEST16 to 19 TEST20 to 22
Test output (connect nothing)	19	TEST6
Test in out (Fix L)	39 to 43 46 to 48	TEST8 to 12 TEST13 to 15
Tuner interface (3 wire mode) Serial data output (I^2C bus mode) Serial clock output	12	SDAT/SCL
Tuner interface (3 wire) Clock output	13	SCLK
Tuner interface (3 wire mode) Latch enable output (I^2C bus mode) Serial data in out	14	SEN/SDA
Clock output (crystal frequency/8)	21	CK8OUT
No Connection	9	NC

Electrical Characteristics (Ta = 0 to 75°C, V_{DD} = 3.3V)

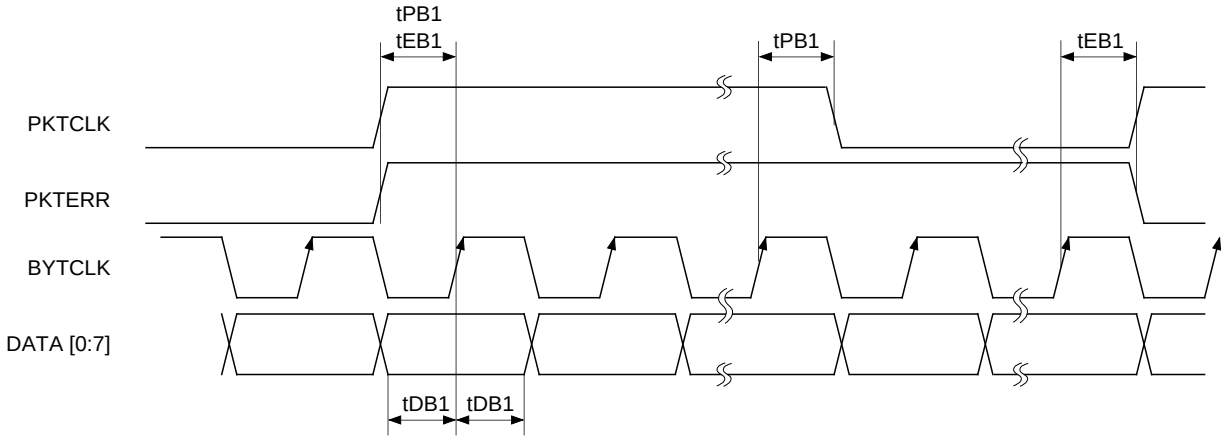
Description	Symbol	Min.	Typ.	Max.	Unit
Symbol rate	Rs	20		30	MSPS
Crystal Frequency	Fxtal		32		MHz
DATA0 to 7 – BYTCLK falling edge (Parallel output mode PBYCK = 0)	tDB0	75			ns
PKTCLK – BYTCLK falling edge (Parallel output mode PBYCK = 0)	tPB0	75			ns
PKTERR – BYTCLK falling edge (Parallel output mode PBYCK = 0)	tEB0	75			ns
DATA0 to 7 – BYTCLK rising edge (Parallel output mode PBYCK = 1)	tDB1	75			ns
PKTCLK – BYTCLK rising edge (Parallel output mode PBYCK = 1)	tPB1	75			ns
PKTERR – BYTCLK rising edge (Parallel output mode PBYCK = 1)	tEB1	75			ns
Serial output mode cycle time (Serial output mode)	tSOC	16			ns
DATA0 to 7 – BYTCLK hold time (Serial output mode)	tDBH	12			ns
PKTCLK, PKTERR – BYTCLK setup time (Serial output mode)	tPBS	6			ns
PKTCLK, PKTERR – BYTCLK hold time (Serial output mode)	tEBH	10			ns
I^2C bus Serial clock cycle time	FscI			400	kHz
I^2C bus Data setup time	tDSI	100			ns
I^2C bus Data hold time	tDHI	0			ns

Timing Waveform

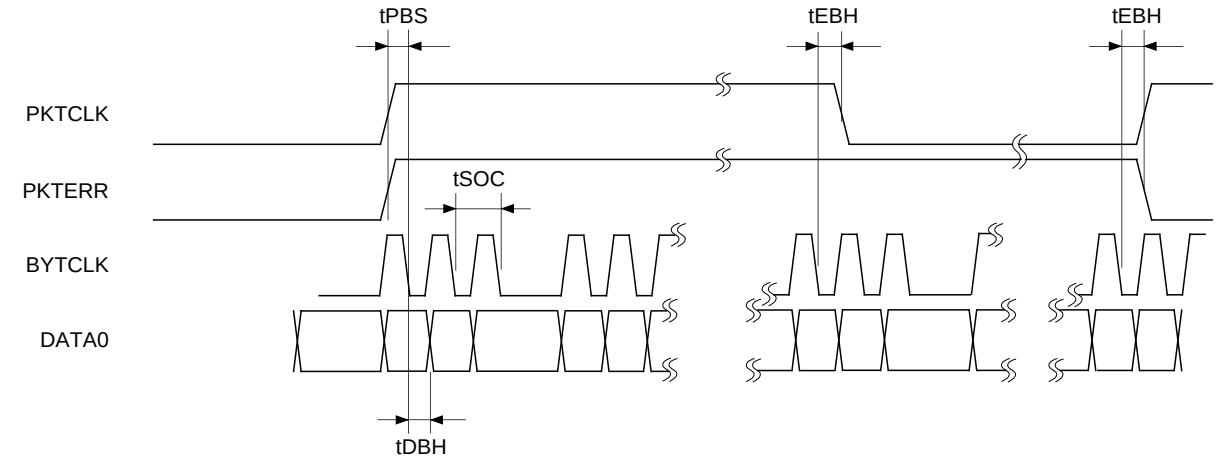
(1) Parallel output mode, PBYTCK = 0



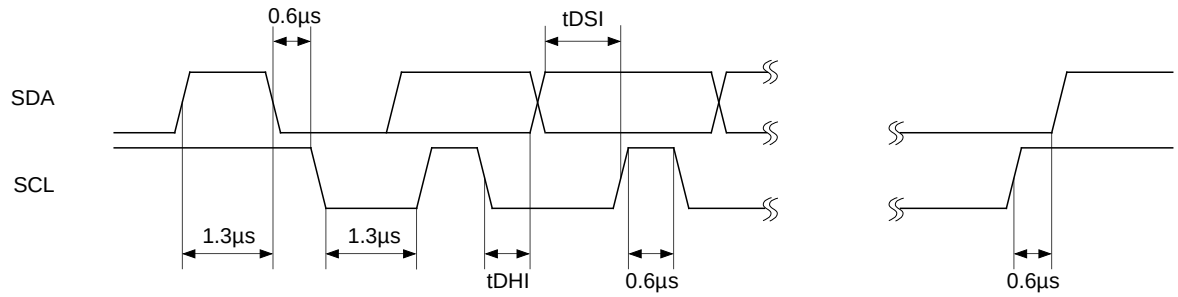
(2) Parallel output mode, PBYTCK = 1



(3) Serial output mode (Example of R = 3/4)



(4) I²C Bus interface



CPU Interface Registers

	Sub address (hex)	Name	MSB bit7	bit6	bit5	bit4	bit3	bit2	bit1	LSB bit0
READ REGISTER	00	INP_LEV	INP7	INP6	INP5	INP4	INP3	INP2	INP1	INP0
	01	PWM_VAL	PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
	02	AFC_VAL	AFC7	AFC6	AFC5	AFC4	AFC3	AFC2	AFC1	AFC0
	03	QBEC_LO	QBEC7	QBEC6	QBEC5	QBEC4	QBEC3	QBEC2	QBEC1	QBEC0
	04	W	QBEC15	QBEC14	QBEC13	QBEC12	QBEC11	QBEC10	QBEC9	QBEC8
	05	QBEC_UP	VBEC7	VBEC6	VBEC5	VBEC4	VBEC3	VBEC2	VBEC1	VBEC0
	06	R	VBEC15	VBEC14	VBEC13	VBEC12	VBEC11	VBEC10	VBEC9	VBEC8
	07	VBEC_LO	—	RO2	RO1	RO0	QBER1	QBER0	VBER1	VBER0
	08	W	OFI3	OFI2	OFI1	OFI0	OFQ3	OFQ2	OFQ1	OFQ0
	09A	VBEC_UPR	VCOLK	NAK	—	FSYNC	VSYNC	QSYNC	—	ID
	09B	CODE/BER	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
	0A	DC_OFST	CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
	0B	FLAG	OFC7	OFC6	OFC5	OFC4	OFC3	OFC2	OFC1	OFC0
WRITE REGISTER	0C	CM_LOW	MQS3	MQS2	MQS1	MQS0	AK1	AK0	CE1	CE0
	0D	CM_UPR	—	RATE2	RATE1	RATE0	SRSAVE	—	SRS1	SRS0
	0E	CAR_OFST	PBYCK	DOH1Z	DOPS	PPKER	PPKCK	MBYCK	VCKVDT	SEL09
	0F	MQS/CLK	SINV	SYSSEL	DFSKIP	RSSKIP	TUNSEL	TUNEN	MFSYNC	AGCLP
	10	CODE/SRS	MAGC	PAGC	MVSYNC	CKVSEL	QPRST	VTRST	RSRST	VCORST
	11	OUT_CNT	QTH5	QTH4	QTH3	QTH2	QTH1	QTH0	TQBEC1	TQBEC0
	12	MOD_CNT	VTH4	VTH3	VTH2	VTH1	VTH0	TVS2	TVS1	TVS0
	13	AGC/RST	TUD17	TUD16	TUD15	TUD14	TUD13	TUD12	TUD11	TUD10
	14	QTH	TUD27	TUD26	TUD25	TUD24	TUD23	TUD22	TUD21	TUD20
	15	VTH	TUD37	TUD36	TUD35	TUD34	TUD33	TUD32	TUD31	TUD30
	16	TUN_DAT1	TUD47	TUD46	TUD45	TUD44	TUD43	TUD42	TUD41	TUD40
	17	TUN_DAT2	TUD57	TUD56	TUD55	TUD54	TUD53	TUD52	TUD51	TUD50
	18	TUN_DAT3	NCO7	NCO6	NCO5	NCO4	NCO3	NCO2	NCO1	NCO0
	19	TUN_DAT4	NCO15	NCO14	NCO13	NCO12	NCO11	NCO10	NCO9	NCO8
	1A	TUN_DAT5	NCO23	NCO22	NCO21	NCO20	NCO19	NCO18	NCO17	NCO16
	1B	SYM_RATE1	CALRST	CADRST	CLKRST	—	RANGE	FSYSEL	FSYTHD	—
	1C	SYM_RATE2	—	—	—	—	—	—	—	—
	1D	SYM_RATE3	BSI3	BSI2	BSI1	BSI0	BSQ3	BSQ2	BSQ1	BSQ0
	1E	CAR_RST	RSTEN	GAIN1	GAIN0	TCAR1	TCAR0	MOFST	OFSTEN	OFSTGN
	1F	N.A.	TQS1	TQS0	FLOOP	TRACK	FLMOD	FLSTEP	QTLEV1	QTLEV0
	20	DC_BIAS	BSC7	BSC6	BSC5	BSC4	BSC3	BSC2	BSC1	BSC0
	21	CAR/DC	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0

Input "0" to write registers which are not assigned ("—").

Description of CPU Interface Registers

Sub address 00 (hex)	Read	INP_LEV	Input level estimation

INP7 to INP0
(MSB) (LSB)

Upper 8 bit of $I^2 + Q^2$ of analog I/Q input.
(Ex.) The value is about 40 (hex) when the analog I/Q amplitude is half the input range.

Sub address 01 (hex)	Read	PWM_VAL	AGC PWM output value

PWM7 to PWM0
(MSB) (LSB)

PWM output value of AGC control.

Sub address 02 (hex)	Read	AFC_VAL	Carrier offset value

AFC7 to AFC0
(MSB) (LSB)
AFC7: Sign

Carrier offset estimation
Carrier offset = (Symbol rate) × AFC [7:0] ÷ 512 (Hz)
Ex.) 20MSPS AFC [7:0] = 11110000 (bin)
offset = 20MHz × (–16) ÷ 512
= –625kHz
In this case, by changing tuner PLL value by -625kHz, the offset may be cancelled.

Sub address 03 (hex)	Read	QBEC_LOW	Bit error count at QPSK output
Sub address 04 (hex)	Read	QBEC_UPR	Bit error count at QPSK output

QBEC15 to QBEC0
(MSB) (LSB)

Bit error count at the QPSK output (16 bit).
Measuring period is set by TQBEC [1:0] of CPU I/F register 11 (hex) .
BER is the ratio of QBEC [15:0] and the measuring period.
QBEC [15:0] is valid when QSYNC, VSYNC and FSYNC are all High.

Sub address 05 (hex)	Read	VBEC_LOW	Bit error count at Viterbi output
Sub address 06 (hex)	Read	VBEC_UPR	Bit error count at Viterbi output

VBEC15 to VBEC0
(MSB) (LSB)

Bit error count at the Viterbi output (16 bit).
Measuring period is 204 × 8 × 1280 = 2,088,960.
BER is the ratio of VBEC [15:0] and 2,088,960.
VBEC [15:0] is valid when QSYNC, VSYNC and FSYNC are all High.

Sub address 07 (hex)	Read	CODE/BER	Code rate and BER

RO2 to RO0

Current punctured rate (code rate)

RO2	RO1	RO0	Code rate
0	0	1	1/2
0	1	0	2/3
0	1	1	3/4
1	0	0	4/5
1	0	1	5/6
1	1	0	6/7
1	1	1	7/8

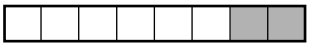
QBER1 to QBER0

4 level BER indicator of QPSK output.

This indicator is valid when QSYNC, VSYNC and FSYNC are all High and TQBEC [1:0] = 10 (bin). TQBEC [1:0] is in register 11 (hex).

QBER1	QBER0	Bit Error Rate
0	0	more than 10^{-2}
0	1	$10^{-3} < * < 10^{-2}$
1	0	$10^{-4} < * < 10^{-3}$
1	1	less than 10^{-4}

VBER1 to VBER0



4 level BER indicator of Viterbi output.

This indicator is valid when QSYNC, VSYNC and FSYNC are all High.

VBER1	VBER0	Bit Error Rate
0	0	more than 10^{-2}
0	1	$10^{-3} < * < 10^{-2}$
1	0	$10^{-4} < * < 10^{-3}$
1	1	less than 10^{-4}

Sub address 08 (hex)	Read	DC_OFST	DC offset level of A to D converter

OFI3 to OFI0 DC offset value of the I channel A/D converter.

OFI3: Sign

OFQ3 to OFQ0 DC offset value of the Q channel A/D converter.

In both cases, the value is depend on the operation mode.

OFQ3: Sign

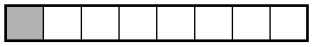
MOFST (reg. IE)	Operating mode	OFI [3:0] / OFQ [3:0]
0	Offset bias mode	Current offset value.
1	Offset cancel mode	Compensation value for each A/D converter.

Refer to the explanation of register 1E (hex).

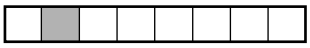
Sub address 09 (hex)-A	Read	FLAG	Status Flag

Register 09 (hex) has an irregular structure. Two register -A and -B are correspond to the sub-address 09 (hex). When SEL09 of the register 0E (hex) is 0, register 09 (hex)-A is selected, else register 09 (hex)-B is selected.

VCOLK This bit become 0 in case of abnormal oscillation of embedded VCO.



NAK (Tuner interface I^2C bus mode)

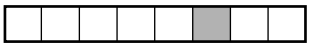


This bit becomes 1 in case of no acknowledge from the tuner PLL.

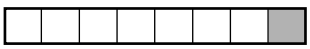
FSYNC This bit becomes 1 iwhen Frame synchronization is achieved.

VSYNC This bit becomes 1 when the punctured mapping synchronization is achieved.

QSYNC This bit becomes 1 when carrier lock is achieved.



ID This bit is always 1.



Sub address 09 (hex)-B	Read	CM_LOW	Constellation Monitor
Sub address 0A (hex)	Read	CM_UPR	Constellation Monitor

These registers can be access when SEL09 of register 0E (hex) is 1.

CM15 to CM0 (MSB) (LSB) Monitor value of the QPSK constellation. This value depends on the AGC reference (reg. 21 (hex)). Refer to Fig.1.

Sub address 0B (hex)	Read	CAR_OFST	Carrier Capture offset value

OFC7 to OFC0
OFC7: Sign

Offset frequency at the point of carrier capture
(Latest offset frequency is output to register 02 (hex))
(offset frequency) = (Symbol rate) × OFC [7:0] ÷ 1024 (Hz)
Ex.) 20MSPS OFC [6:0] = 11110000 (bin)
(offset freq.) = 20MHz × (–16) ÷ 1024
= –312.5kHz

Sub address 0C (hex)	Write	MQS/CLK	Qsync mode/Clock recovery

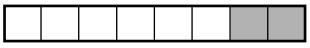
MQS3 to MQS0
(MSB) (LSB)

Threshold for carrier lock detection

AK1 to AK0

Clock recovery loop filter coefficient
00: Max. 11: min.

CE1 to CE0



Clock recovery loop filter gain
00: Min. 11: Max.
Clock recovery range is approximately ±200ppm with CE (1:0) = 11.

Sub address 0D (hex)	Write	CODE/SRS	Code rate select/Symbol rate select

RATE2 to RATE0

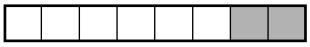
Code rate setting

RATE2	RATE1	RATE0	Code rate R
0	0	1	1/2
0	1	0	2/3
0	1	1	3/4
1	0	0	4/5
1	0	1	5/6
1	1	0	6/7
1	1	1	7/8

SRSAVE

By saving several NCO control word to sub registers initially, symbol rate can be changed by setting the number of the sub register in which the desired control word is saved. There are three sub registers.

SRS1 to SRS0



(To set the symbol rate directly without the above function)
Set SRSAVE = 0, SRS [1:0] = (1,1) and set control word to registers 18, 19, 1A (hex).

(To save control word to sub registers)
Set SRSAVE = 1 and set sub register No. ((0, 0) or (0, 1) or (1, 0)) to SRS [1:0].
Then set control word to registers 18, 19, 1A (hex).
The control word is set to both the clock recovery circuit and the selected sub register.

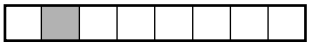
(To set the symbol rate with the above function)
Set SRSAVE = 0, and set sub register No. of control word to be set. The control word saved in the sub register is set to the clock recovery circuit.

Sub address 0E (hex)	Write	OUT_CNT	Output control and polarity

PBYCK

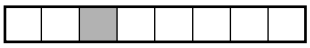
BYTCLK polarity 0: For falling edge 1: For rising edge

DOH1Z



1: Output Hi-Z mode (PKTCLK, BYTCLK, PKTERR, DATA [7:0])

DOPS



0: Parallel output mode 1: Serial output mode
Refer to Electric characteristics

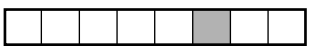
PPKER

PKTERR polarity 0: PKTERR: H at uncorrectable packet
1: PKTERR: L at uncorrectable packet

PPKCK

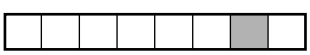
PKTCLK polarity 0: PKTCLK: H at data / L at parity
1: PKTCLK: L at data / H at parity

MBYCK



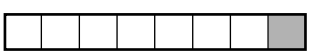
1: BYTCLK mask mode
In this mode BYTCLK is forced Low during parity data output

VCKVDT



1: Viterbi decode data VDT (Pin 64) and clock VCK (Pin 65) output enable
0: VDT and VCK are fixed low.

SEL09



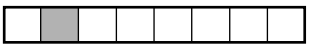
Read register 09 (hex)-A, -B selection
0: 09 (hex)-A is selected
1: 09 (hex)-B is selected

Sub address 0F (hex)	Write	MOD_CONT	Mode Control

SINV

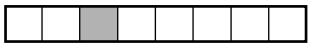
I/Q exchange
1: normal operation

SYSSEL



Not assigned. Input 0.

DFSK1P



1: Nyquist roll off filter bypass mode

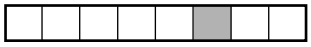
RSSK1P

1: Reed-Solomon decoder bypass mode

TUNSEL

Tuner interface mode 0: I^2C bus mode 1: 3 wire mode

TUNEN

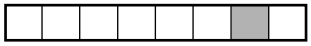


1: Tuner interface enable

TUNSEL	TUNEN	Pin 12	Pin 13	Pin 14	mode
Don't care	0	Hi-Z	Hi-Z	Hi-Z	—
0	1	clock out	Hi-Z	data in out	I^2C bus
1	1	data out	clock out	Latch Enable	3 wire

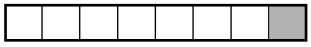
Refer to reference circuit (5).

MFSYNC



Parameter for frame synchronization protection
0: normal operation mode
1: powerful protection mode

AGCLP



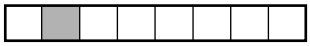
AGC loop filter gain
1: normal operation
0: large gain

Sub address 10 (hex)	Write	AGC/RST	AGC and Reset

MAGC

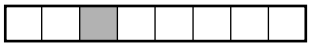
AGC mode 0: normal mode 1: bus control mode
In normal mode, PWM output is controlled so that $I^2 + Q^2$ (register 00hex) should become approximately equal to the reference level set in register 21 (hex). In bus control mode, data of the register 21 (hex) is directly converted to PWM output.

PAGC



AGC polarity 0: For tuner whose gain increases by higher AGC control voltage
1: For tuner whose gain increases by lower AGC control voltage
Select mode according to tuner AGC type.

MVSYNC



Input 0

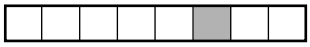
CKVSEL

CKV (Pin 69) output mode
0: symbol clock output
1: sampling clock output

QPRST

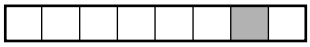
1: QPSK block reset (set 0 for normal operation)
To reset QPSK block, set this bit to 1 and then set this bit to 0 again.

VTRST



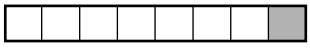
1: Viterbi block reset (set 0 for normal operation)
Reset operation is same as QPRST.

RSRST



1: Deinterleaver and Reed-solomon block reset (set 0 for normal operation)
Reset operation is same as QPRST.

VCORST



1: NCO block reset (set 0 for normal operation)
Reset operation is same as QPRST.

Sub address 11 (hex)	Write	QTH	Qsync Threshold and QBEC period

QTH5 to QTH0
(MSB) (LSB)

Threshold for carrier lock detection
These parameters relate to QTLEV [1:0] in register 1F (hex) and AGC reference 21 (hex).
Ex.) QTLEV [1:0] = 01 AGC ref = 32 (hex)
QTH [5:0] = 101000

TQBEC1 to TQBEC0

Count period of QPSK bit error count

TQBEC1	TQBEC0	Count period
0	0	2^8
0	1	2^{16}
1	0	2^{19}
1	1	2^{23}

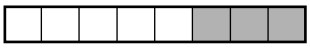
Select TQBEC [1:0] = 10 to use QPSK BER indicator (register 07 (hex))

Sub address 12 (hex)	Write	VTH	Viterbi sync threshold and period

VTH4 to VTH0

Threshold for punctured mapping synchronization
11110: Min. 00000: Max.

TVS2 to TVS0



Detection period for punctured mapping synchronization
110: Min 000: Max.

code rate	VTH4 to VTH0, TVS2 to TVS0
1/2	8B (hex)
2/3	BB (hex)
3/4	CB (hex)
4/5	D3 (hex)
5/6	DB (hex)
6/7	E3 (hex)
7/8	E3 (hex)

Sub address 13 (hex)	Write	TUN_DAT1	Tuner control data
Sub address 14 (hex)	Write	TUN_DAT2	Tuner control data
Sub address 15 (hex)	Write	TUN_DAT3	Tuner control data
Sub address 16 (hex)	Write	TUN_DAT4	Tuner control data
Sub address 17 (hex)	Write	TUN_DAT5	Tuner control data

(I^2C bus mode) Set TUNSEL = 0 and TUNEN = 1 in the register 0F (hex).
13 (hex): Tuner PLL IC slave address + 0 (write mode)
14 to 17 (hex): Write data (tuning parameter)
I^2C bus starts write operation when data setting to register 17 (hex) is finished. In case of no acknowledge from tuner PLL IC, NAK in the register 09 (hex)-A is set to 1.

(3 wire mode) Set TUNSEL = 1 and TUEN = 1 in the register 0F (hex). 28 bits data (register 13 to 15 (hex) and upper 4bit of the register 16 (hex)) are transmitted serially. To start operation, dummy data setting to the register 17 (hex) is needed.
Refer to the reference circuit (5).

Sub address 18 (hex)	Write	SYM_RATE1	Control word for multi-rate oscillation
Sub address 19 (hex)	Write	SYM_RATE2	Control word for multi-rate oscillation
Sub address 1A (hex)	Write	SYM_RATE3	Control word for multi-rate oscillation

NCO23 to NCO0
(MSB) (LSB)

The relation between symbol rate and the control word of the NCO is:
NCO [23:0] = (symbol rate) $\times 2^{22} \div$ (crystal frequency)

Ex.) Symbol rate 20MSPS crystal 32MHz

$$NCO\,[23:0] = 20 \times 10^6 \times 2^{22} \div 32 \times 10^{-6}$$
$$= 2{,}621{,}440$$
$$= 2^{21} + 2^{19}$$

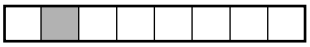
NCO21 = NCO19 = 1, other = 0

Sub address 1B (hex)	Write	CAR_RST	Carrier loop reset

CARRST

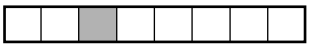
1: Carrier loop filter reset
Reset operation is same as QPRST (register 10hex)

CADRST



1: Carrier recovery frequency loop reset
Reset operation is same as QPRST (register 10hex)

CLKRST

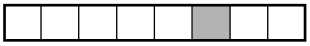


1: Clock recovery loop reset
Reset operation is same as QPRST (register 10hex)

RANGE

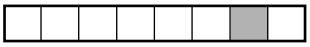
Carrier capture range
0: Carrier capture range = ±Rs/8
1: Carrier capture range = ±Rs/16

FSYSEL



Frame synchronization detector mode
0: Hard decision
1: Soft decision

FSYTHD



Frame synchronization threshold
0: Low
1: High

Sub address 1C (hex)	Write	N.A.	Not Assigned

Input 0 to all bits.

Sub address 1D (hex)	Write	DC_BIAS	A/D Converter DC_BIAS

DC offset is added to the output of the A/D converter when MOFST in the register 1E (hex) is 0.

BSI3 to BSI0

DC offset for I channel A/D converter. BSI3: sign
Offset range is from –8 to +7.

BSQ3 to BSQ0

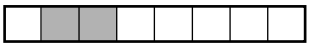
DC offset for Q channel A/D converter. BSI3: sign
Offset range is from –8 to +7.

Sub address 1E (hex)	Write	CAR/DC	Carrier recovery and DC offset

RSTEN

1:Carrier loop filter reset enable (Set to 1 for normal operation)

GAIN1 to GAIN0



Gain setting for carrier recovery loop

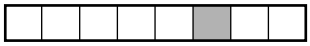
GAIN1	GAIN0	Gain
0	0	×1
0	1	×2
1	0	×4
1	1	×8

(default ×1)

TCAR1 to TCAR0

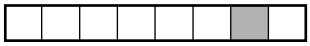
Mode setting for carrier recovery frequency loop: default TCAR [1:0] = 10.

MOFST



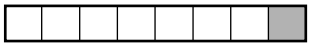
1: A/D converter DC offset cancellation mode
0: A/D converter DC offset addition mode

OFSTEN



1: A/D converter DC offset control (cancel or add) enable
0: A/D converter DC offset control (cancel or add) disable

OFSTGN



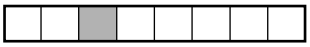
A/D converter DC offset cancellation loop filter gain
1: ×1
0: ×1/2

Sub address 1F (hex)	Write	CAR_MODE	Carrier recovery mode

TQS1 to TQS0

Carrier lock detection period 00: min. 11: max.
Default is TQS [1:0] = 10

FLOOP



0: Carrier recovery by phase loop
1: Carrier recovery by phase and frequency loop (default)

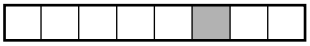
TRACK

default: 0

FLMOD

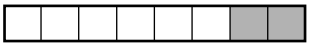
1: Carrier offset frequency is set by BSC [6:0].
0: Carrier offset frequency is set by the internal loop. (default)

FLSTEP



default: 1

QTLEV1 to QTLEV0



Gain for carrier lock detection circuit.
Default is QTLEV [1:0] = 00

Sub address 20 (hex)	Write	CAR_BIAS	Carrier frequency offset bias

BSC7 to BSC0
BSC7: sign

Carrier offset frequency setting
This mode is good when FLMOD = 1.

(Carrier offset) = (Symbol rate) × BSC [7:0] ÷ 1024 (Hz)

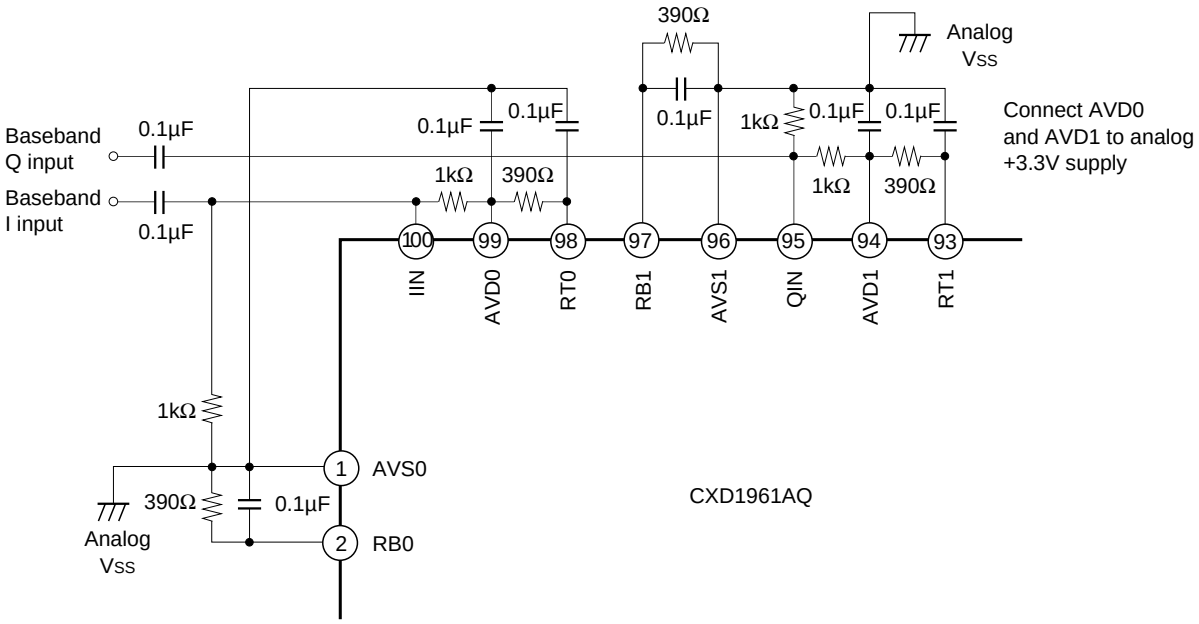
Sub address 21 (hex)	Write	AGC_REF	AGC reference

AGCR7 to AGCR0

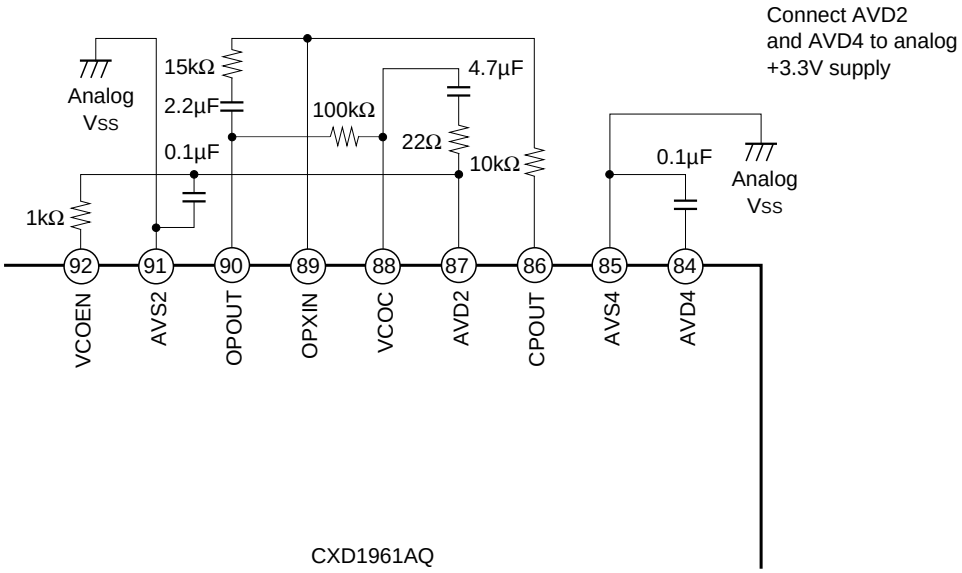
Input level reference for AGC operation
Refer to the explanation of register 10 (hex)

Application Circuit

(1) A/D Converter

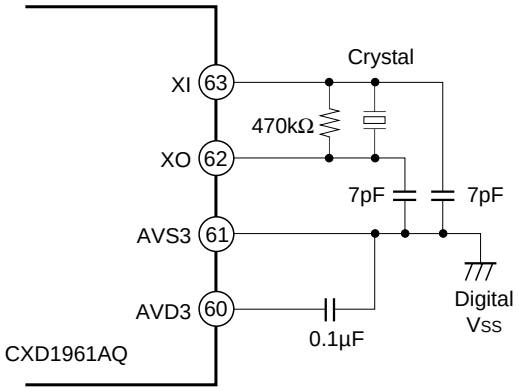


(2) Clock Recovery circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

(3) Crystal

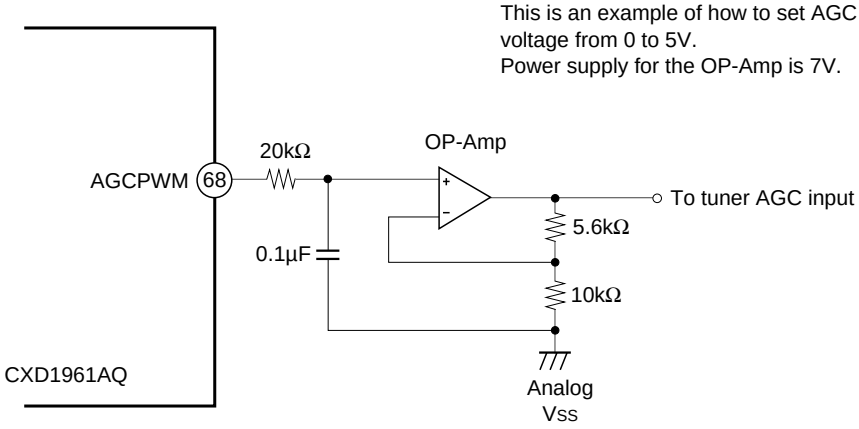


Crystal
Daishinku AT-49
32.0MHz

Connect AVD3 to ditital +3.3V supply

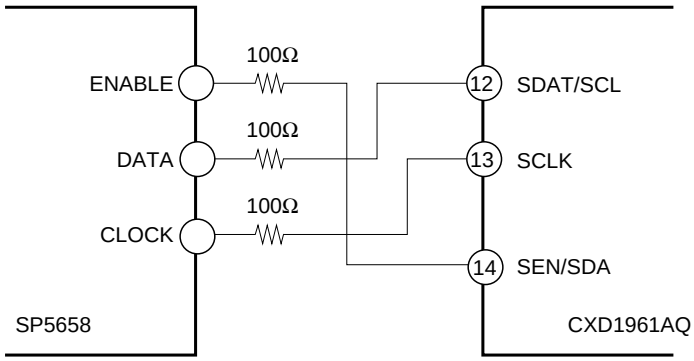
(4) AGC

This is an example of how to set AGC control voltage from 0 to 5V.
Power supply for the OP-Amp is 7V.



(5) Tuner Interface

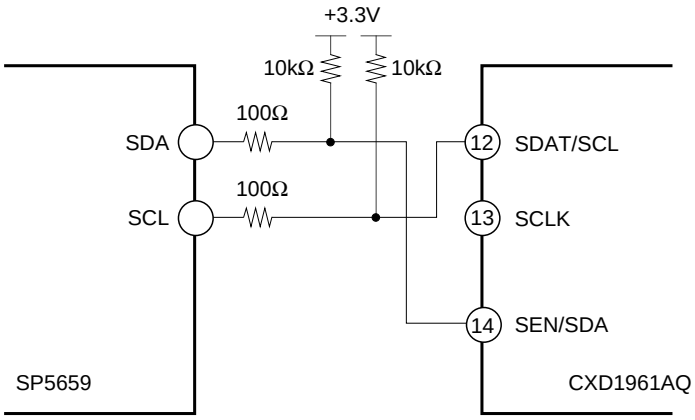
(3 wire type) suitable for GEC Plessey SP5658



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

(5) Tuner Interface

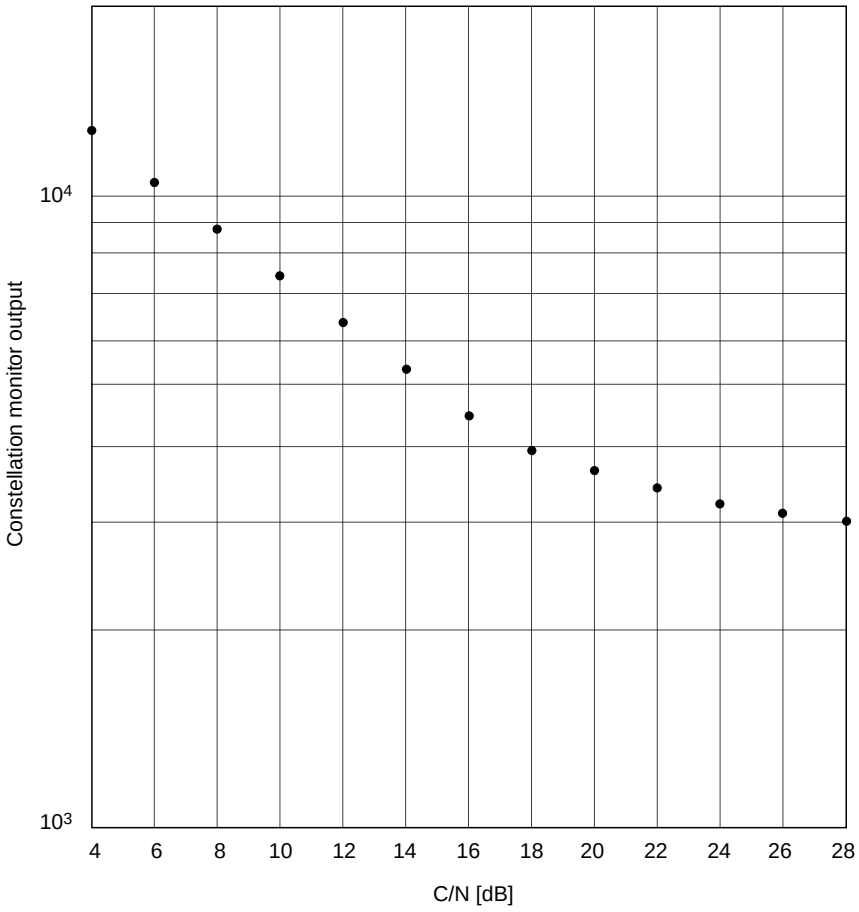
(I^2C bus type) suitable to GEC Plessey SP5659 etc. (4 bytes of data can be written)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Appendix

Fig.1 Constellation monitor output vs. C/N

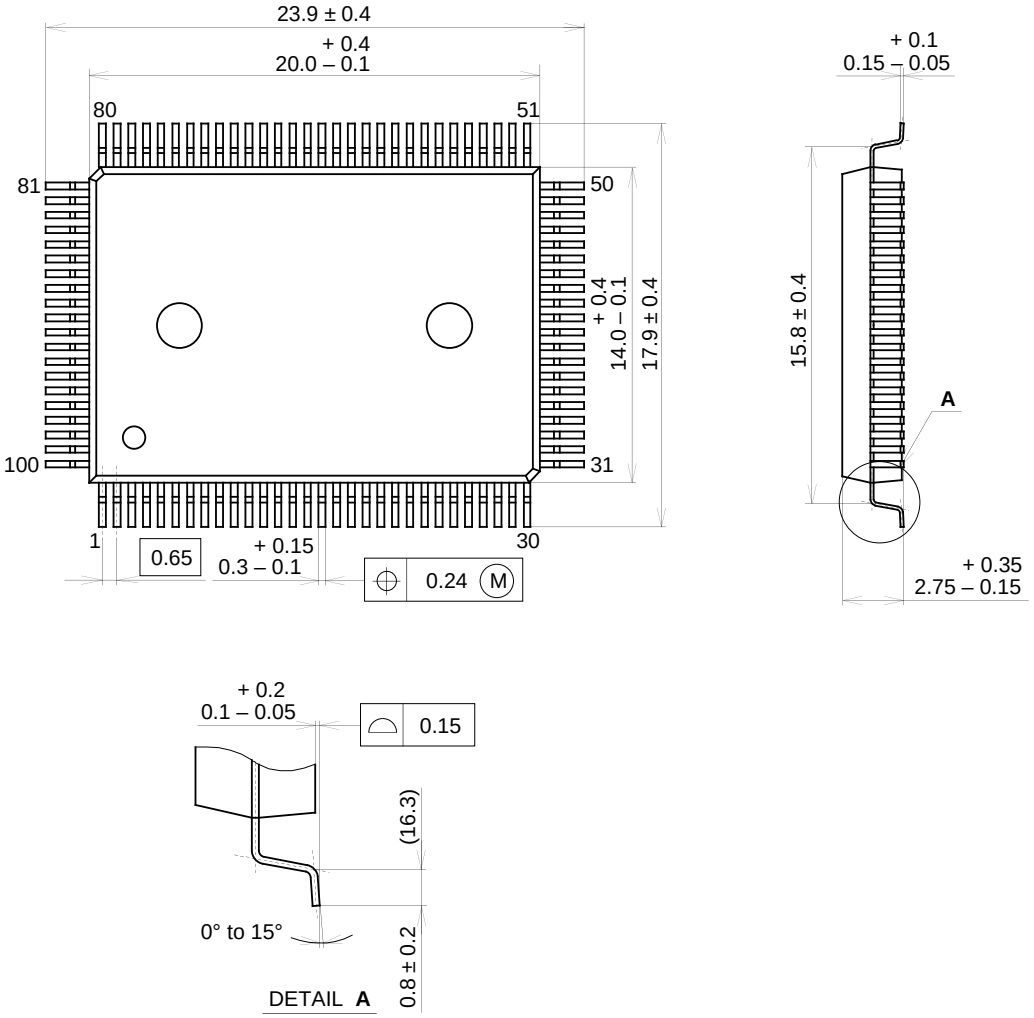


This figure is an example when AGCREF is set to 32 (hex).
The monitor output value is proportional to AGCREF.

Monitor output : CM [15:0] CPU I/F register 09-B (hex) and 0A (hex)

Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g