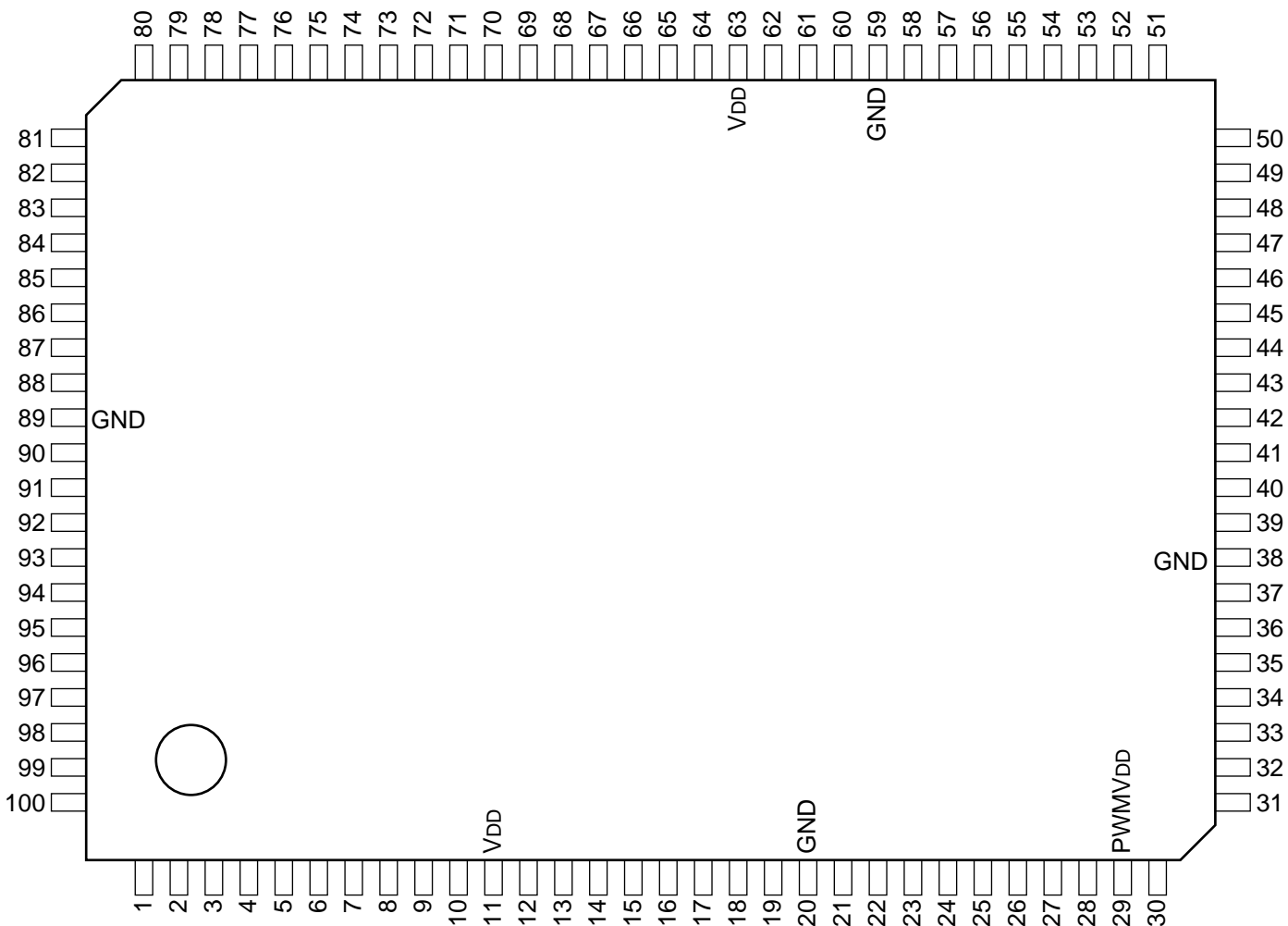


# SERVO IC

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	FG1/IP24	26	I/O	IOP2	51	I/O	D7	76	O	PPG11/OP21
2	I	FG0/IP23	27	I/O	IOP1	52	I/O	D6	77	O	PPG10/OP20
3	I	PBH/IP22	28	I/O	IOP0	53	I/O	D5	78	O	PPG0F/OP17
4	I	SYNC1/IP21	29	—	PWM VDD	54	I/O	D4	79	O	PPG0E/OP16
5	I	SYNC0/IP20	30	O	PWM7/OP37	55	I/O	D3	80	O	PPG0D/OP15
6	I	FG02/IP14	31	O	PWM6/OP36	56	I/O	D2	81	O	PPG0C/OP14
7	I	FG01/IP13	32	O	PWM5/OP35	57	I/O	D1	82	O	PPG0B/OP13
8	I	FG00/IP12	33	O	PWM4/OP34	58	I/O	D0	83	O	PPG0A/OP12
9	I	CTL/IP11	34	O	PWM3/OP33	59	—	GND	84	O	PPG09/OP11
10	I	LAT/IP10	35	O	PWM2/OP32	60	I	RES	85	O	PPG08/OP10
11	—	VDD	36	O	PWM1/OP31	61	I	MD1	86	O	CLKO
12	I	UD/IP07	37	O	PWM0/OP30	62	I	MD0	87	I	EXTAL
13	I	CCLK/IP06	38	—	GND	63	—	VDD	88	O	XTAL
14	I	FGC1/IP05	39	I	AS14	64	I	WR	89	—	GND
15	I	FGC0/IP04	40	I	AS13	65	I	RD	90	O	PPG07/OP07
16	I	FGB1/IP03	41	I	A15	66	I	CE	91	O	PPG06/OP06
17	I	FGB0/IP02	42	I	A14	67	O	IREQ2	92	O	PPG05/OP05
18	I	FGA1/IP01	43	I	A13	68	O	IREQ1	93	O	PPG04/OP04
19	I	FGA0/IP00	44	I	A6	69	O	IREQ0	94	O	PPG03/OP03
20	—	GND	45	I	A5	70	I	FXSEL	95	O	PPG02/OP02
21	I/O	IOP7	46	I	A4	71	O	OP26	96	O	PPG01/OP01
22	I/O	IOP6	47	I	A3	72	O	EXCS1/OP25	97	O	PPG00/OP00
23	I/O	IOP5	48	I	A2	73	O	EXCS0/OP24	98	I	FG12/IP27
24	I/O	IOP4	49	I	A1	74	O	PPG13/OP23	99	I	FG11/IP26
25	I/O	IOP3	50	I	A0	75	O	PPG12/OP22	100	I	FG10/IP25

41	A15	D7	51
42	A14	D6	52
43	A13	D5	53
44	A6	D4	54
45	A5	D3	55
46	A4	D2	56
47	A3	D1	57
48	A2	D0	58
49	A1		
50	A0	IOP7	21
		IOP6	22
39	AS14	IOP5	23
40	AS13	IOP4	24
		IOP3	25
98	FG12/IP27	IOP2	26
99	FG11/IP26	IOP1	27
100	FG10/IP25	IOP0	28
6	FG02/IP14		
7	FG01/IP13	PWM7/OP37	30
8	FG00/IP12	PWM6/OP36	31
1	FG11/IP24	PWM5/OP35	32
2	FG01/IP23	PWM4/OP34	33
		PWM3/OP33	34
4	SYNCT/IP21	PWM2/OP32	35
5	SYNCO/IP20	PWM1/OP31	36
		PWM0/OP30	37
3	PBH/IP22		
		PPG0F/OP17	78
9	CTL/IP11	PPG0E/OP16	79
10	LAT/IP10	PPG0D/OP15	80
12	UD/IP07	PPG0C/OP14	81
13	CCLK/IP06	PPG0B/OP13	82
		PPG0A/OP12	83
14	FGC1/IP05	PPG13/OP23	74
15	FGC0/IP04	PPG12/OP22	75
16	FGB1/IP03	PPG11/OP21	76
17	FGB0/IP02	PPG10/OP20	77
18	FGA1/IP01	PPG09/OP19	84
19	FGA0/IP00	PPG08/OP18	85
61	MD1	PPG07/OP07	90
62	MD0	PPG06/OP06	91
60	RES	PPG05/OP05	92
70	FXSEL	PPG04/OP04	93
87	EXTAL	PPG03/OP03	94
		PPG02/OP02	95
		PPG01/OP01	96
		PPG00/OP00	97
		OP26	71
		PPG00 - PPG0F	
		PPG10 - PPG13	72
		EXCS1/OP25	73
		EXCS0/OP24	
		IREQ2	67
		IREQ1	68
		IREQ0	69
		CLKO	86
		XTAL	88

**INPUT**

A0 - A15 ; ADDRESS BUS  
AS13, AS14 ; SELECTING CONDITION OF ADDRESS DECODER AS13 AND AS14 BITS  
CCLK ; 8-BIT COUNTER CLOCK INPUT  
CE ; CHIP ENABLE  
CTL ; RESOLUTION 2.5MHz WITH EDGE SELECT FUNCTION.  
WITH FREQUENCY DIVISION MASK TIMER  
EXTAL ; CRYSTAL OSCILLATION OR EXTERNAL CLOCK INPUT  
FG0 ; RESOLUTION 2.5MHz  
FG00 - FG02 ; FREQUENCY DIVISION ENABLE RESOLUTION 2.5MHz.  
WITH FREQUENCY DIVISION MASK TIMER  
FG1 ; RESOLUTION 2.5MHz BOTH EDGES  
FG10 ; EDGE SELECTION ENABLE RESOLUTION 10MHz  
FG11, FG12 ; FREQUENCY DIVISION ENABLE RESOLUTION 10MHz  
FGA0 ; PERFORMS FORWARD/REVERSE ROTATION DETECTION  
AND 4FG COUNT (UP/DOWN) BY FGA0 AND FGA1. 10BITS. UP/DOWN IS MADE BY  
CONTROLLING THE UP/DOWN OF 8-BIT COUNTER.  
FGA1 ; 4FG PERFORMS FREQUENCY DIVISION AND FRC CAPTURE  
THROUGH MASK TIMER.  
\*1 : SELECTS ONE OF FGA0 TO FGC1 INPUT AND DETECTS  
BOTH EDGES AND PERFORM THE FRC CAPTURE THROUGH  
THE MASK TIMER.  
FGB0 ; PERFORMS FORWARD/REVERSE ROTATION DETECTION AND 4FG COUNT  
BY FGB0 AND FGB1.  
FGB1 ; \*1 : SELECTS ONE OF FGA0 TO FGC1 INPUT AND DETECTS  
BOTH EDGES AND PERFORM THE FRC CAPTURE THROUGH  
THE MASK TIMER.  
FGC0 ; PERFORMS FORWARD/REVERSE ROTATION DETECTION AND 4FG COUNT  
BY FGC0 AND FGC1.  
FGC1 ; \*1 : SELECTS ONE OF FGA0 TO FGC1 INPUT AND DETECTS  
BOTH EDGES AND PERFORM THE FRC CAPTURE THROUGH  
THE MASK TIMER.  
FXSEL ; FREQUENCY DIVISION SELECTION CLOCK INPUT  
LAT ; EXTERNAL LATCH TIMING OF UP/DOWN COUNTER  
MDO, 1 ; TEST MODE DESIGNATION  
PBH ; INPUT OF COMPOSITE SYNC OR H SYNC.  
RESOLUTION 10MHz. WITH HALF H KILLER.  
RD ; REDE  
RES ; RESET  
SYNCO, 1 ; INPUT OF COMPOSITE SYNC OR V SYNC. RESOLUTION 2.5MHz  
UD ; 8-BIT COUNTER UP/ DOWN INPUT  
WR ; WRITE

**OUTPUT**

CLKO ; CLOCK OUTPUT  
EXCS0, 1 ; DECODE AT ADDRESS A3 LEVEL  
IREQ0 ; INTERRUPTION SIGNAL OF FRC CAPTURE UNIT  
IREQ1 ; COINCIDENCE INTERRUPTION OF PPG0  
IREQ2 ; COINCIDENCE INTERRUPTION OF PPG1  
OP26 ; EXCLUSIVELY OUTPUT PORT  
PPG00 - PPG0F  
PPG10 - PPG13 ; PROGRAMMABLE PULSE GENERATOR RESOLUTION 1.25MHz  
PPG00 : WITH HLOCK  
PWM0 - PWM5 ; PWM OUTPUT NORMALLY PWM, OR PWM0 AND PWM1, PWM2 AND PWM3,  
OR PWM4 AND PWM5 OUTPUT SIGNAL CORRESPONDED TO PUSH-PULL.  
PWM6, 7 ; PWM OUTPUT  
XTAL ; CRYSTAL OSCILLATION

**INPUT/OUTPUT**

D0 - D7 ; DATA BUS  
IOP0 - IOP7 ; SELECTS AND USES INPUT AND OUTPUT BY EVERY 1 BIT.

