

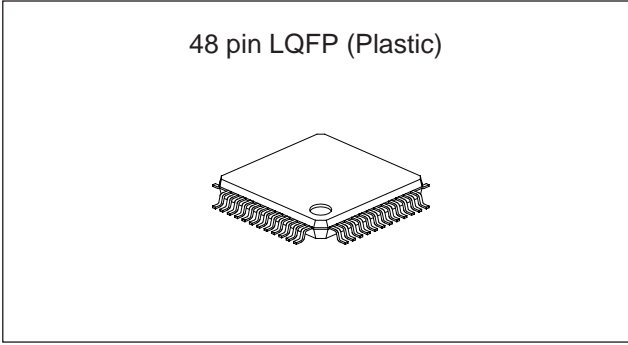
**9-bit 20MSPS Video A/D Converter**

**Description**

The CXD2314R is a 9-bit CMOS A/D converter for video applications. This IC is ideally suited for the A/D conversion of video signals in TVs, VCRs, camcorders, etc.

**Features**

- Resolution: 9-bit  $\pm 0.5$  LSB (D.L.E.)
- Maximum sampling frequency: 20MSPS
- Low power consumption: 130mW (at 20MSPS typ.)  
(Not including reference current)
- TTL compatible input
- Tri-state TTL compatible output ( $DV_{DD} = 3.3V$ )
- Low input capacitance
- Reference impedance: 280 $\Omega$  (typ.)



**Structure**

Silicon gate CMOS IC

**Absolute Maximum Ratings** ( $T_a = 25^\circ C$ )

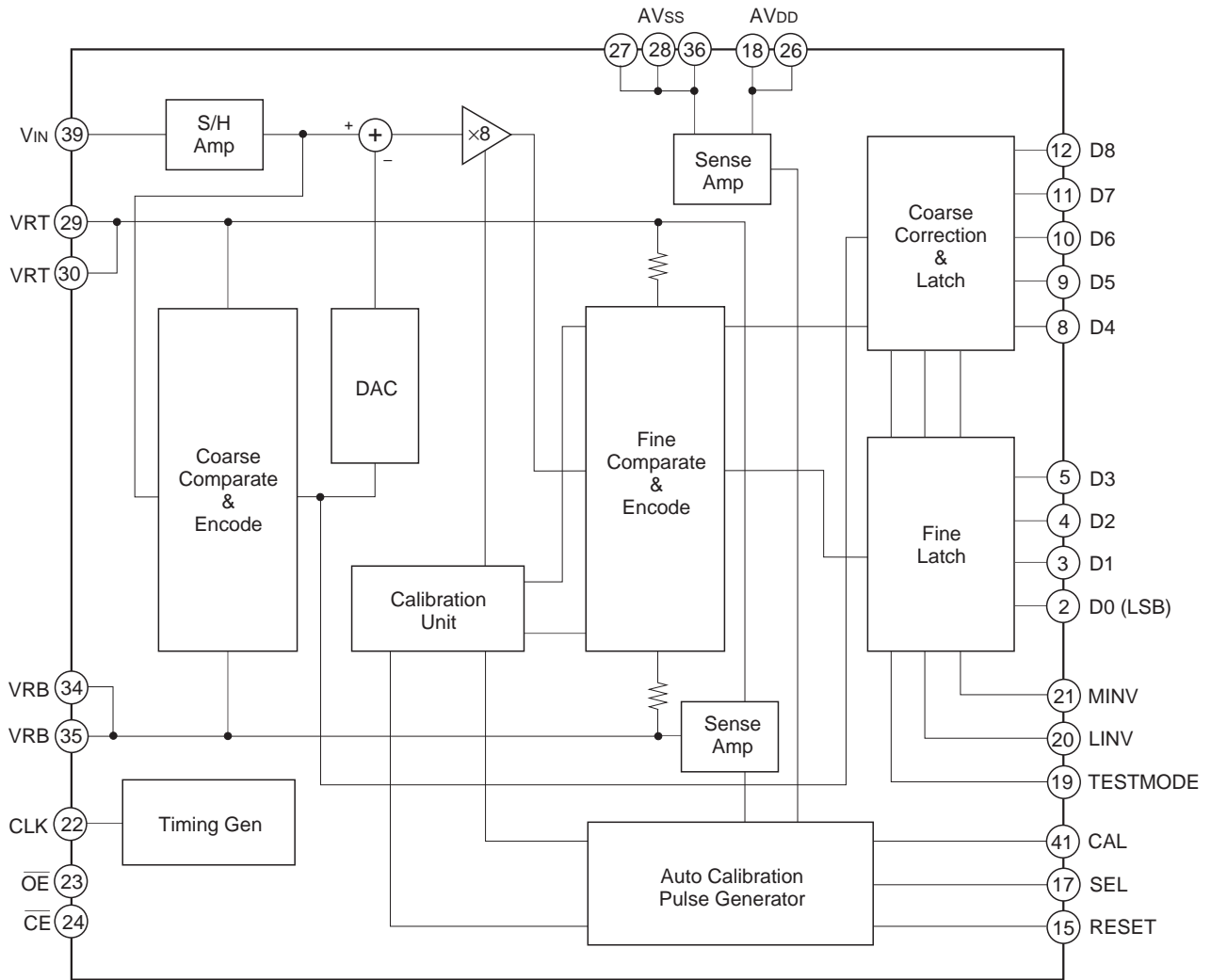
• Supply voltage	$V_{DD}$	7	V
• Reference voltage	$V_{RT}, V_{RB}$	$V_{DD}+0.5$ to $V_{SS}-0.5$	V
• Input voltage (analog)	$V_{IN}$	$V_{DD}+0.5$ to $V_{SS}-0.5$	V
• Input voltage (digital)	$V_{IH}, V_{IL}$	$V_{DD}+0.5$ to $V_{SS}-0.5$	V
• Output voltage (digital)	$V_{OH}, V_{OL}$	$V_{DD}+0.5$ to $V_{SS}-0.5$	V
• Storage temperature	$T_{stg}$	-55 to +150	$^\circ C$

**Recommended Operating Conditions**

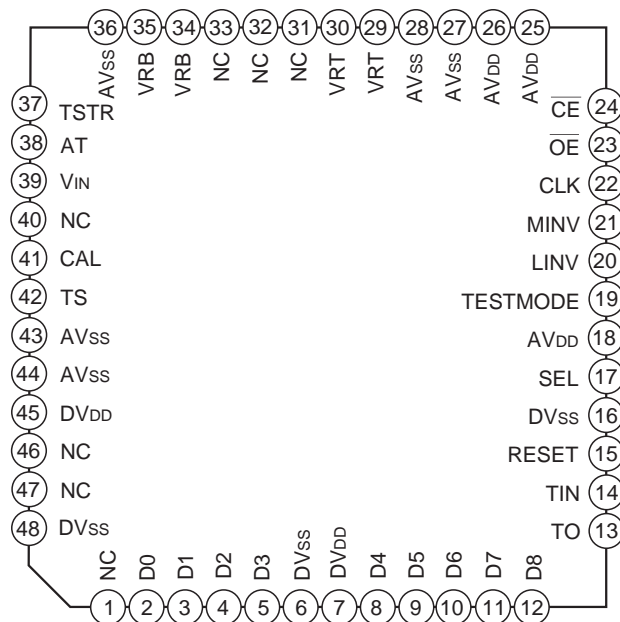
• Supply voltage	$AV_{DD}, AV_{SS}$	$5.0 \pm 0.25$	V
	$DV_{DD}, DV_{SS}$	3.0 to 5.25	V
	$ DV_{SS} - AV_{SS} $	0 to 100	mV
• Reference input voltage	$V_{RB}$	More than 1.8	V
	$V_{RT}$	to $AV_{DD}-0.4$	V
• Analog input	$V_{IN}$	More than 1.8Vp-p	
• Clock pulse width	$T_{PW1}$	25 (min.)	ns
	$T_{PW0}$	25 (min.)	ns
• Operating ambient temperature	$T_{opr}$	-20 to +75	$^\circ C$

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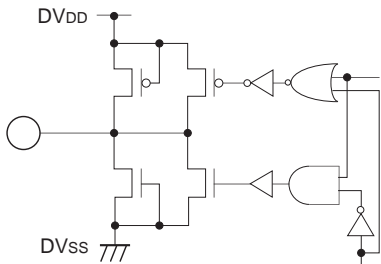
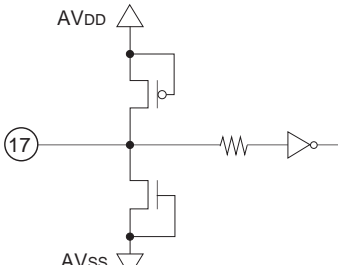
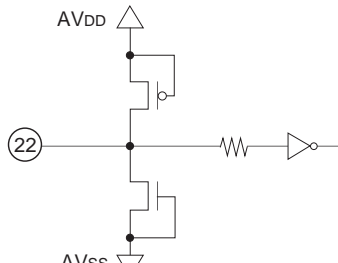
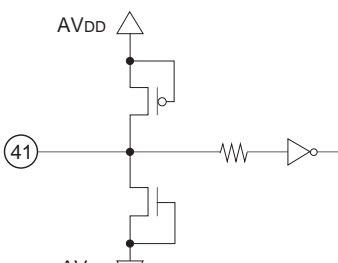
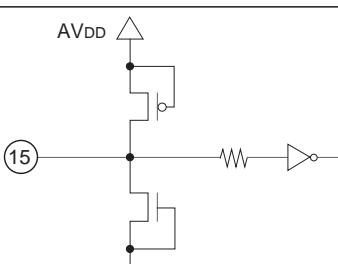
Block Diagram



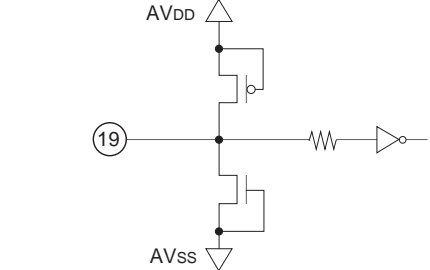
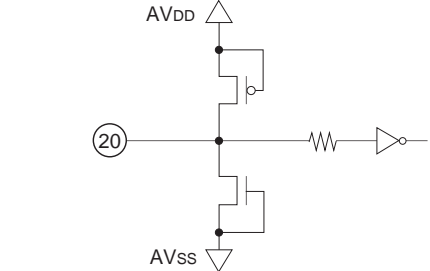
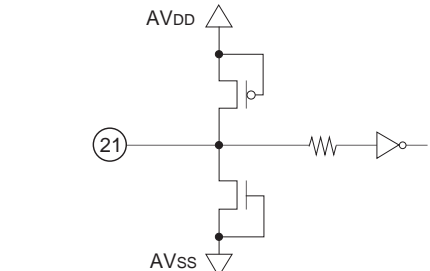
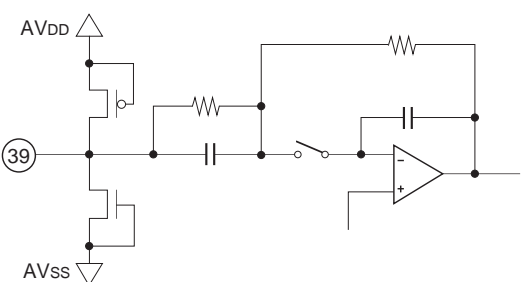
Pin Configuration



Pin Description

Pin No	Symbol	Equivalent circuit	Description
2 to 5 8 to 12	D0 to D8		D0 (LSB) to D8 (MSB) output.
13	TO		Test pin. TS = High: High impedance state
7, 45	DVDD		Digital VDD.
6, 16, 48	DVSS		Digital VSS.
27, 28, 36, 43, 44	AVSS		Analog VSS.
17	SEL		Calibration input pulse select after completion of the startup calibration. High : Internal pulse generation Low : External input
22	CLK		Clock pin.
41	CAL		Calibration pulse input.
15	RESET		Calibration circuit reset and startup calibration restart.

Pin No.	Symbol	Equivalent circuit	Description
14	TIN		Test signal input. Normally fixed to AV <sub>DD</sub> or AV <sub>SS</sub> .
29, 30	VRT		Reference top.
34, 35	VRB		Reference bottom.
38	AT		Test signal output. TS = High: High impedance state
42	TS		Test signal input. Normally fixed to AV <sub>DD</sub> .
37	TSTR		Test signal input. Normally fixed to AV <sub>SS</sub> .
23	$\overline{OE}$		D0 to D8 output enable. Low : Output state High : High impedance state
24	$\overline{CE}$		Chip enable. Low : Active state High : Standby state

Pin No.	Symbol	Equivalent circuit	Description
19	TESTMODE		<p>Test mode.                      High : Output state                      Low : Output fixed</p>
20	LINV		<p>Output inversion.                      High : D0 to D7 are inverted and output.</p>
21	MINV		<p>Output inversion.                      High : D8 is inverted and output.</p>
18, 25, 26	AVDD		Analog VDD.
39	VIN		Analog input.

**Digital Output**

The following table shows the correlation between the analog input voltage and the digital output code (TESTMODE=1, LINV, MINV=0)

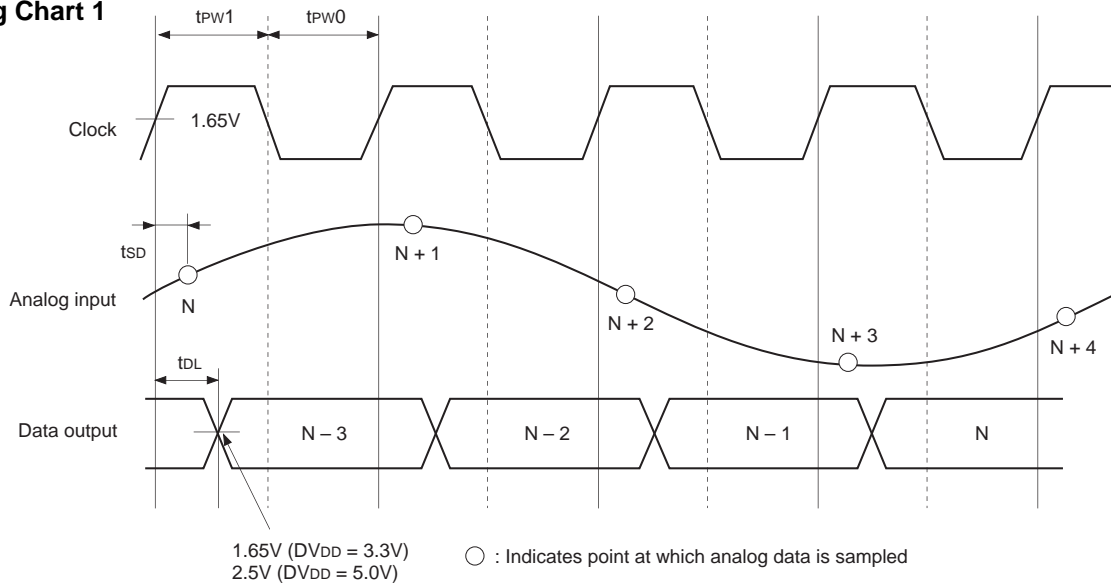
Input signal voltage	Step	Digital output code								
		MSB							LSB	
VRT	0	1	1	1	1	1	1	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	255	1	0	0	0	0	0	0	0	0
	256	0	1	1	1	1	1	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
VRB	511	0	0	0	0	0	0	0	0	0

The following table shows the output state for the combination of TESTMODE, LINV, and MINV states.

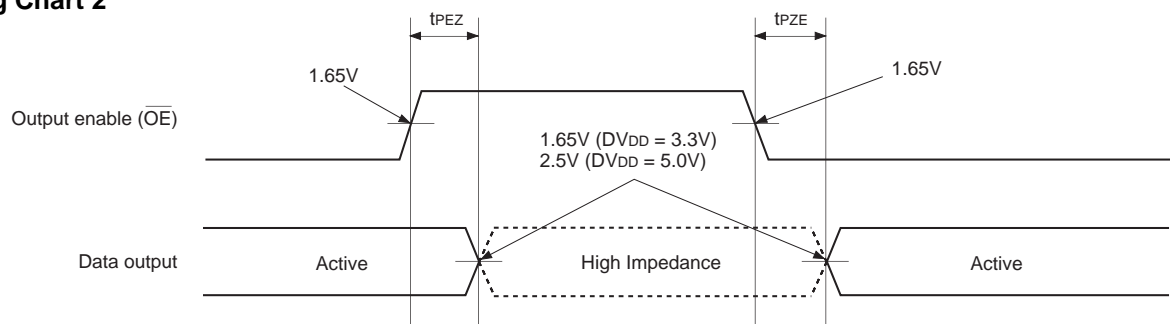
TESTMODE	LINV	MINV	D0	D1	D2	D3	D4	D5	D6	D7	D8
1	0	0	P	P	P	P	P	P	P	P	P
1	1	0	N	N	N	N	N	N	N	N	P
1	0	1	P	P	P	P	P	P	P	P	N
1	1	1	N	N	N	N	N	N	N	N	N
0	0	0	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0	0
0	0	1	0	1	0	1	0	1	0	1	1
0	1	1	1	0	1	0	1	0	1	0	1

P: Forward-phase output N: Inverted output

**Timing Chart 1**



**Timing Chart 2**

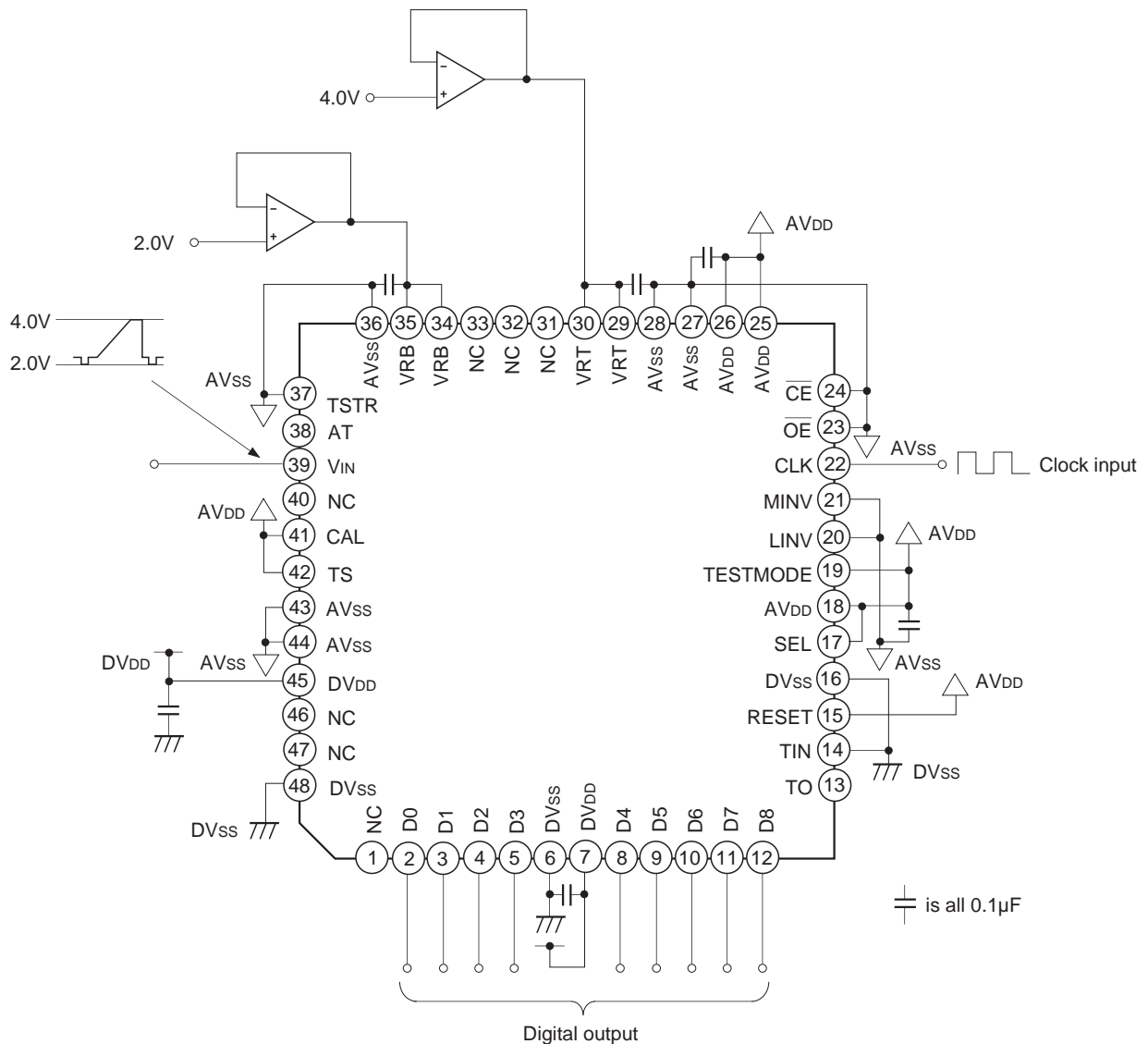


**Electrical Characteristics** (Fc = 20MSPS, AVDD = 5V, DVDD = 3.3V, VRB = 2.0V, VRT = 4.0V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Max. conversion rate	Fc max	FIN = 1.0kHz triangular wave input	20			MSPS
Min. conversion rate	Fc min				0.5	
Supply current	Analog	FIN = 1.0kHz triangular wave input	20	27	34	mA
	Digital				3.0	
Standby current	Analog	$\overline{CE}$ = High			1.0	$\mu$ A
	Digital					
Reference pin current	IRT		5.0	7.0	11.0	mA
	IRB		-11.0	-7.0	-5.0	
Analog input band	BW	-1dB		70		MHz
Analog input capacitance	CIN			9		pF
Reference resistance value (VRT - VRB)	RREF		180	280	380	$\Omega$
Offset voltage	EOT	EOT=theoretical value-actual measured value	40	90	140	mV
	EOB	EOB=actual measured value-theoretical value	-120	-70	-20	
Startup calibration start voltage	VCAL1	AVDD - AVSS		2.5		V
	VCAL2	VRT - VRB		1.0		
Digital input voltage	VIH	AVDD = 4.75V to 5.25V	2.3			V
	VIL				0.8	
Analog input current	AIH	VIN = 4V		40	50	$\mu$ A
	AiL	VIN = 2V	-50	-40		
Digital input current	IiH	DVDD = max	VIH = DVDD VIL = 0V		5	$\mu$ A
	IiL				5	
Digital output current	IOH	$\overline{OE}$ = AVSS	VOH = DVDD-0.5V	3.5		mA
	IOl	DVDD = min	VOL = 0.4V	3.5		
Digital output current	IOZH	$\overline{OE}$ = AVDD	VOH = DVDD		1	$\mu$ A
	IOZL	DVDD = max	VOL = 0V		1	
Tri-state output disable time	tPEZ	Clock not synchronized for active → high impedance	20	25	30	ns
Tri-state output enable time	tPZE	Clock not synchronized for high impedance → active	10	15	20	ns
Integral non-linearity error	EL			$\pm$ 0.5	$\pm$ 1.0	LSB
Differential non-linearity error	ED			$\pm$ 0.3	$\pm$ 0.5	
Differential gain error	DG	NTSC 40 IRE mod ramp, Fc = 14.3MSPS		1.0		%
Differential phase error	DP			0.3		deg
Output data delay	tDL	CL = 20pF	8	13	18	ns
Sampling delay	tSH		4	6	8	ns
	tSL		2	4	6	

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SNR	SNR	$F_{IN} = 100\text{kHz}$		53		dB
		$F_{IN} = 500\text{kHz}$		52		
		$F_{IN} = 1\text{MHz}$		53		
		$F_{IN} = 3\text{MHz}$		52		
		$F_{IN} = 7\text{MHz}$		48		
		$F_{IN} = 10\text{MHz}$		44		
SFDR	SFDR	$F_{IN} = 100\text{kHz}$		69		dB
		$F_{IN} = 500\text{kHz}$		68		
		$F_{IN} = 1\text{MHz}$		68		
		$F_{IN} = 3\text{MHz}$		62		
		$F_{IN} = 7\text{MHz}$		56		
		$F_{IN} = 10\text{MHz}$		45		

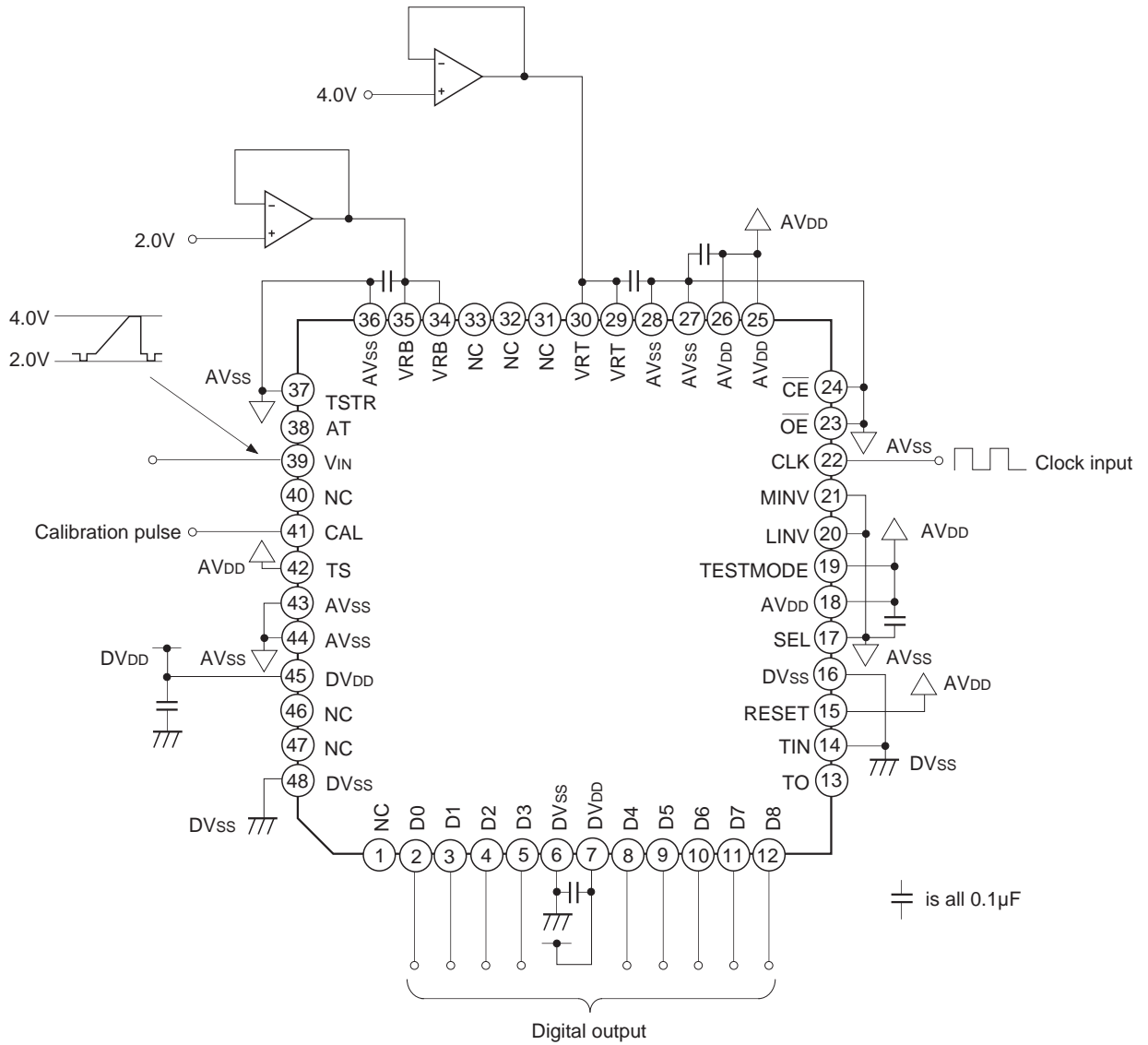
**Application Circuit 1. Startup calibration + internal auto calibration**



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.



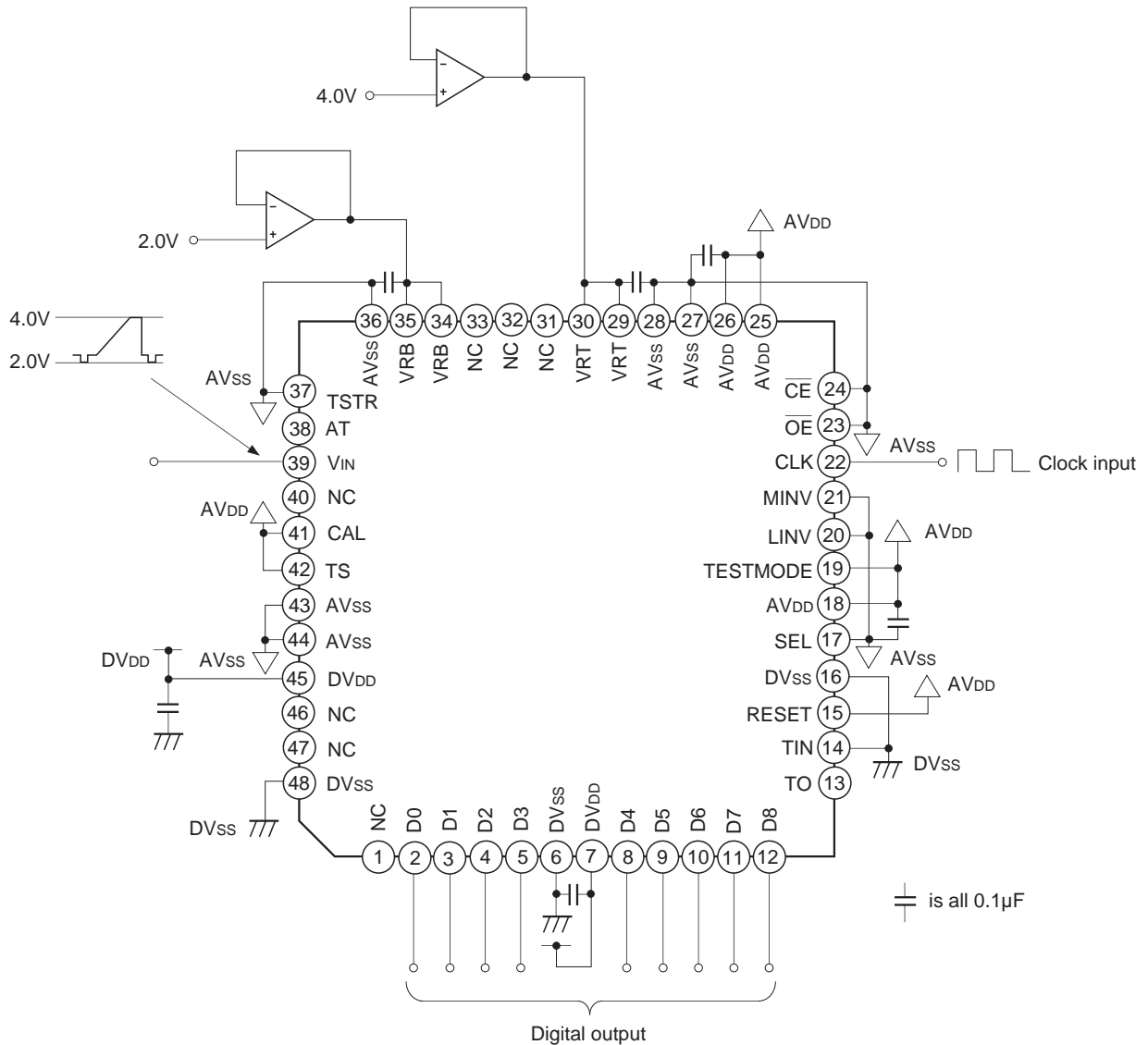
**Application Circuit 2. Startup calibration + external sync calibration**



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**Application Circuit 3. Only startup calibration**

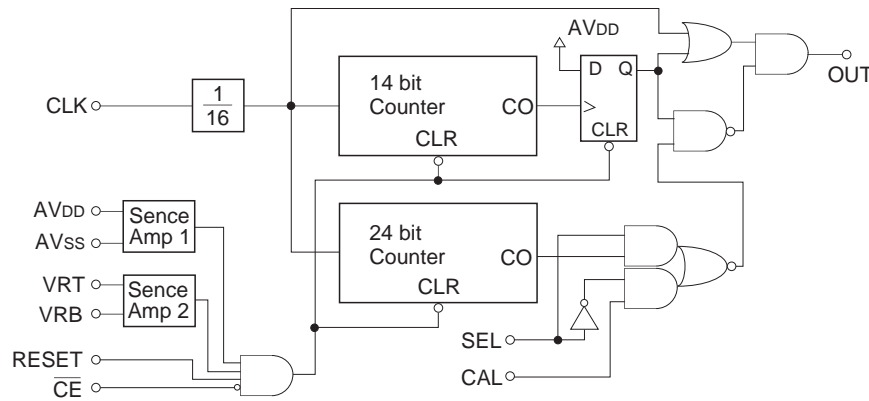
(Less than supply voltage fluctuation range of AVDD = ±100mV and reference voltage fluctuation range of |VRT – VRB| = 200mV)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

**1. Calibration Function**

In order to achieve superior linearity, the CXD2312R has a built-in calibration circuit and a calibration pulse auto generation circuit which is used to execute a calibration circuit. Fig. 1 shows a block diagram of the calibration pulse generation circuit.

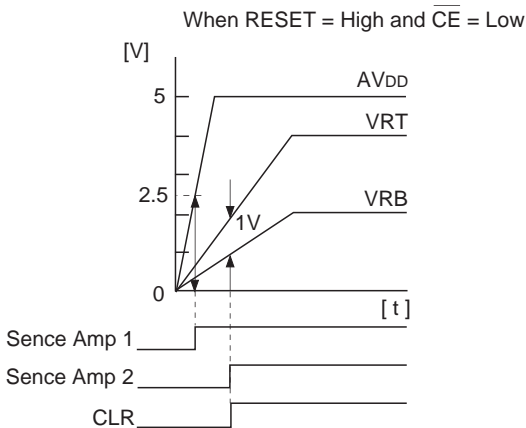


**Fig. 1. Calibration Pulse Generation Circuit**

**(1) Startup Calibration Function**

Over 600 calibration pulses are needed to complete the initial calibration process when the power is first supplied to the IC. The startup calibration function automatically generates these pulses internally and completes the initial calibration process.

The following five conditions must be satisfied to initiate the startup calibration function.



- a) The voltage between AV<sub>DD</sub> and AV<sub>SS</sub> is approximately 2.5V or more.
- b) The voltage between VRT and VRB is approximately 1V or more.
- c) The RESET pin (Pin 15) must be high.
- d) The CE pin (Pin 24) must be low.
- e) Condition b is met after condition a.

Once all five of these conditions have been met, the calibration pulses are generated. The pulses are generated by counting 16 main clock cycles on a 14-bit counter and closing the gate when the carry-out occurs. Therefore, the time required for startup calibration after the above five conditions have been met is determined by the following formula:

$$\text{Startup calibration time} = \text{main clock cycle} \times 16 \times 16,384$$

For example, if the main clock frequency is 14.3MHz, the time required for startup calibration is 18ms.

**(2) Auto Calibration Pulse Generation Function**

After startup calibration is completed, this function periodically generates calibration pulses so that calibration can be performed constantly without any need for input of calibration pulses from an external source. This function counts 16 main clock cycles on a 24-bit counter and uses the carry-out as the calibration pulse. The cycle of the calibration pulse generated in this fashion is as follows:

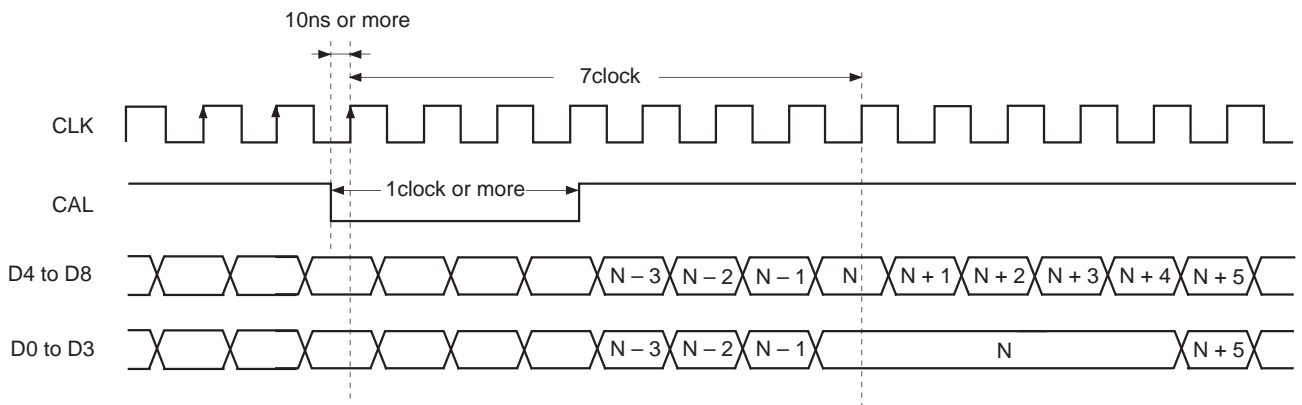
$$\text{Internal calibration pulse generation cycle} = \text{main clock cycle} \times 16 \times 16,777,216$$

Therefore, if the main clock frequency is 14.3MHz, the calibration pulse cycle is approximately 19 seconds; since calibration is performed once every seven pulses, the calibration cycle is approximately 130 seconds. In order to use this function, the SEL pin (Pin 17) must be high.

Note that this function cannot be used if fixing the lower bits in the calibration operation as described below will cause problems because this function is executed asynchronously without regard to the input signals.

**(3) External Calibration Pulse Input Function**

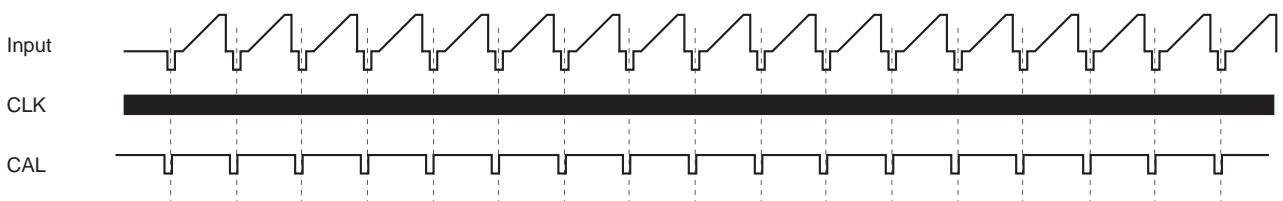
If the auto calibration function cannot be used, calibration can be performed in synchronization with the input signals when a calibration pulse is input from the CAL pin (Pin 41) by setting the SEL pin (Pin 17) low.



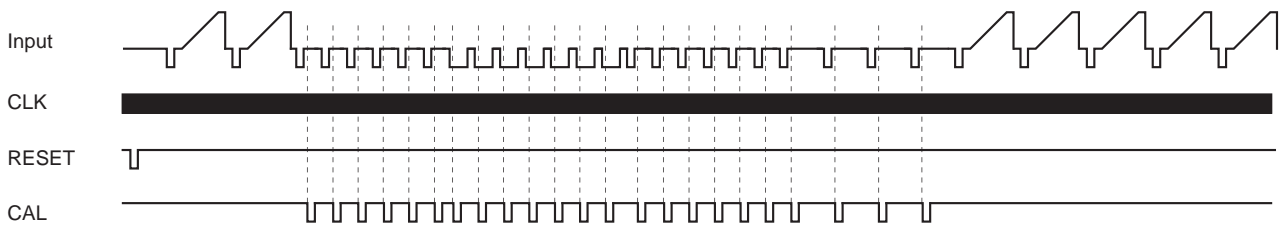
**Fig. 2. Calibration Timing Chart**

Calibration starts when the falling edge of the pulse input to the CAL pin (Pin 41) is detected. Because the lower comparator is occupied for four clock cycles at this point, the previous lower data is held for four clock cycles after seven clock cycles since the rising edge of the clock cycle in which the falling edge of CAL was detected. Calibration can be performed outside of video intervals by using the sync signal, etc., to input the CAL signal. An example of this is shown below.

**[1] Inputting CAL every H-sync**



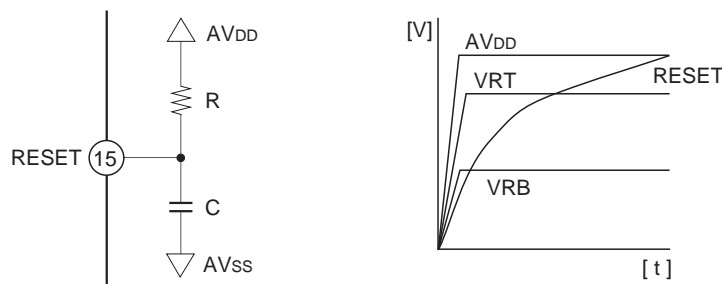
[2] Inputting CAL every V-sync



It is also possible to use only the startup calibration function by leaving the SEL pin (Pin 17) low and fixing the CAL pin (Pin 41) either high or low. Note that this method requires restriction of the fluctuation range of the supply voltage and the reference voltage.

**(4) Re-initiating the Startup Calibration Function**

The startup calibration function can be re-initiated after the power and reference voltage are supplied by using the CE pin (Pin 24) and the RESET pin (Pin 15). Particularly in cases where the riseup characteristics of the power supply and the reference voltage are unstable, it is possible to initiate startup calibration properly by connecting a CR and delaying startup until after power supply riseup.



**Fig. 3. Initiation of the Startup Calibration Function Using the RESET pin**

**2. Power supply**

To prevent the influence of noise, connect the power supply to a 0.1 $\mu$ F by-pass capacitor as near the device as possible.

**3. DV<sub>DD</sub>**

Either a 3.3V or 5.0V digital power supply can be used. Compared to the 5.0V power supply, the 3.3V power supply generates a decreased amount of radiation noise but offers a decreased drive capacity. These two power supplies do not virtually differ in static and dynamic characteristics. Further, the High output level rises up to DV<sub>DD</sub>.

**4. Reference input**

The voltage to be supplied to the reference pins must be driven by a buffer having a 10mA or more drive capacity. For supplied voltage stabilization, connect the buffer to a 0.1 $\mu$ F by-pass capacitor as near the pins as possible.

**5. Latch-up**

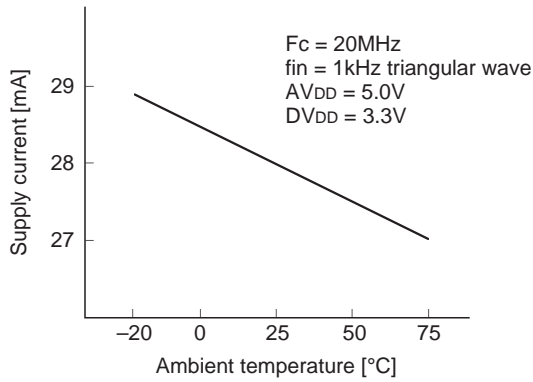
Ensure that the AV<sub>DD</sub> and DV<sub>DD</sub> pins share the same power supply on a board to prevent latch-up which may be caused by power ON time-lag.

**6. Board**

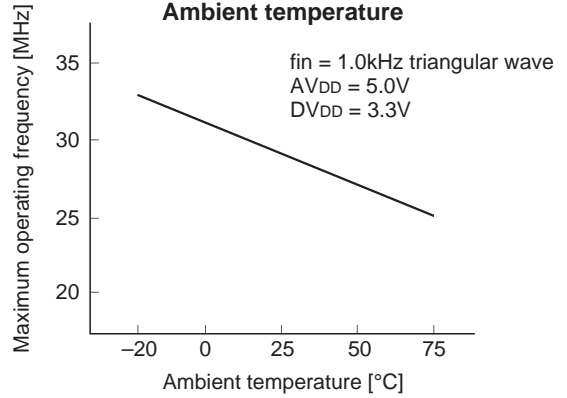
To obtain full-expected performance from this IC, be sure that the mounting board has a large ground pattern for lower impedance. It is recommended that the IC be mounted on a board without using a socket to evaluate its characteristics adequately.

Example of Representative Characteristics

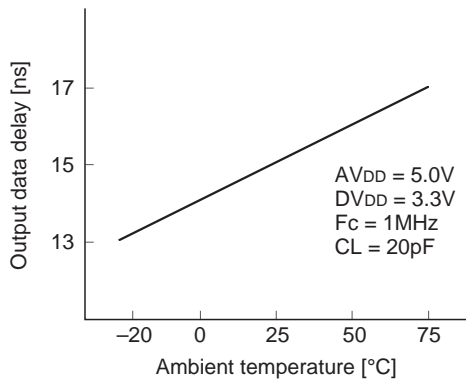
Supply current vs. Ambient temperature



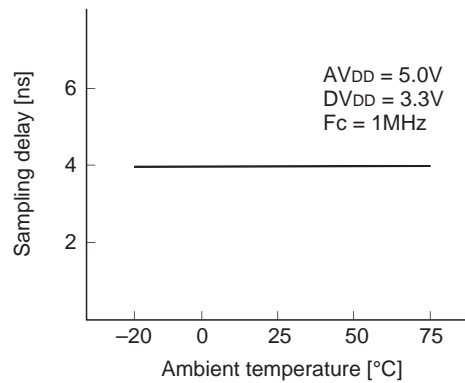
Maximum operating frequency vs. Ambient temperature



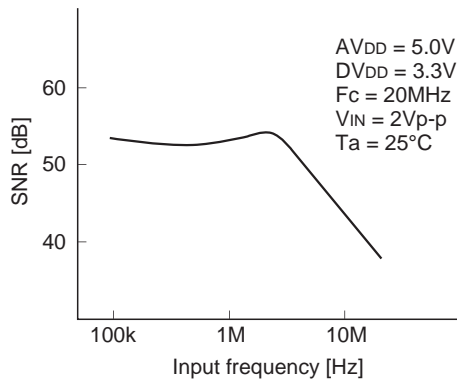
Output data delay vs. Ambient temperature



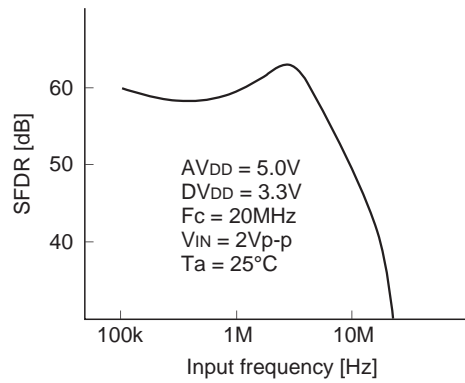
Sampling delay vs. Ambient temperature



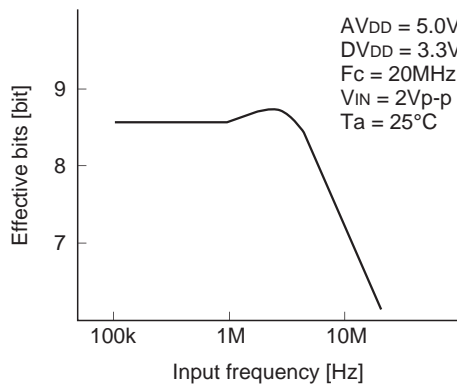
Input frequency vs. SNR



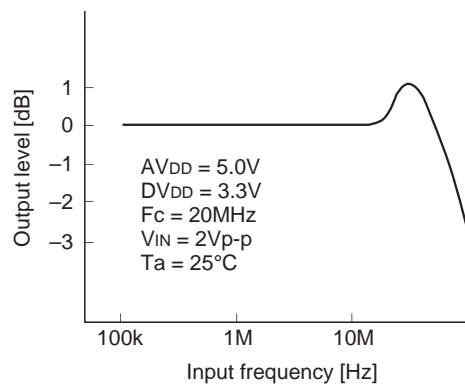
Input frequency vs. SFDR



Input frequency vs. Effective bits



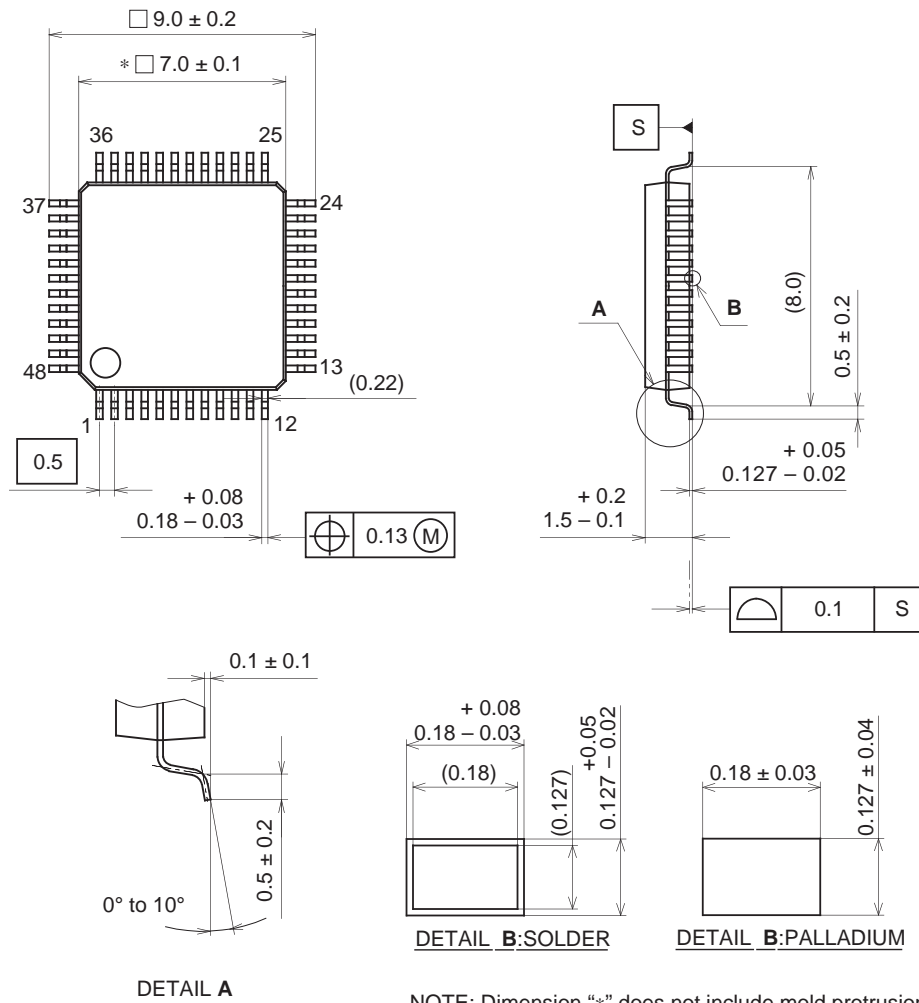
Input band



Package Outline

Unit : mm

48PIN LQFP (PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g