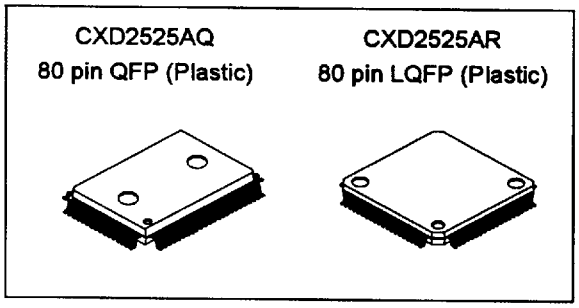
SONY

CXD2525AQ/AR

EFM/ACIRC Encoder/Decoder



Description

The CXD2525AQ/AR is an EFM/ACIRC encoder/decoder that is compatible with the MiniDisc format.

- EFM encoding/decoding
- ACIRC encoding/decoding
- ADIP decoding
- EFM/ADIP CLV control circuit
- EFM digital PLL
- RAM for error correction
- Digital in/out (U bits, C bits, SCMS supportable)
- Peak level meter circuit
- 64-bit slot audio interface
- New CPU interface (serial bus)
- Powerful error correction
  (C1: double correction; C2: quadruple correction)

Structure

Silicon gate CMOS

Absolute Maximum Ratings (Vss = 0V)

• Supply voltage	V_{DD}	–0.3 to +7.0	V
• Input voltage	V_I	–0.3 to +7.0	V
• Output voltage	V_O	–0.3 to +7.0	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–40 to +125	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	+3.0 to +5.25	
• Input voltage	V_{IN}	Vss–0.3 to V_{DD}+0.3	V
• Supply voltage differential	Vss – AVss	–0.1 to +0.1	V
	V_{DD} – AV_{DD}	–0.1 to +0.1	V

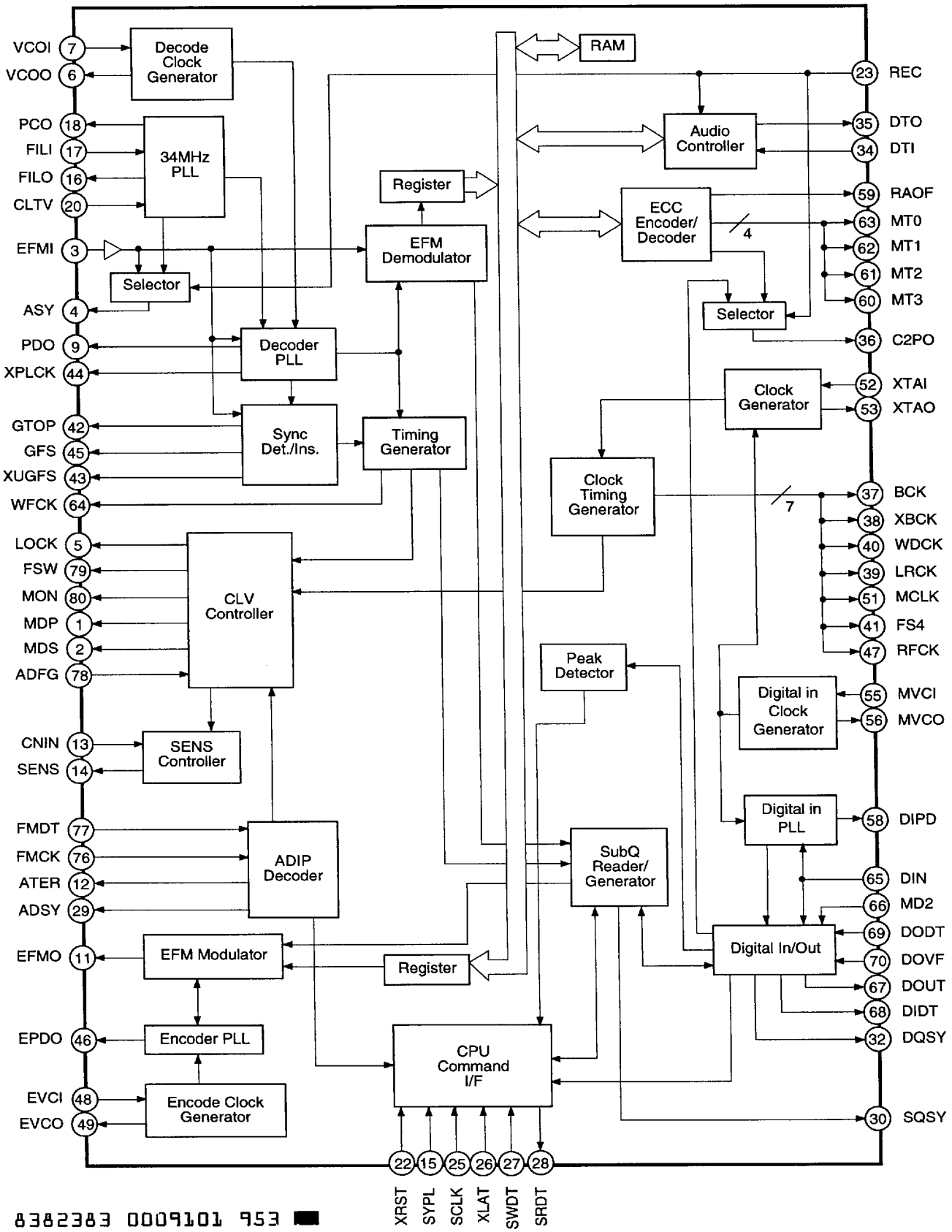
I/O Capacitance

• Input pin	C_I	Max. 12	pF
• Output pin	C_O	Max. 12	pF (when at high impedance)

Note: Measuring conditions $V_{DD} = V_I = 0V$
f_M = 1MHz

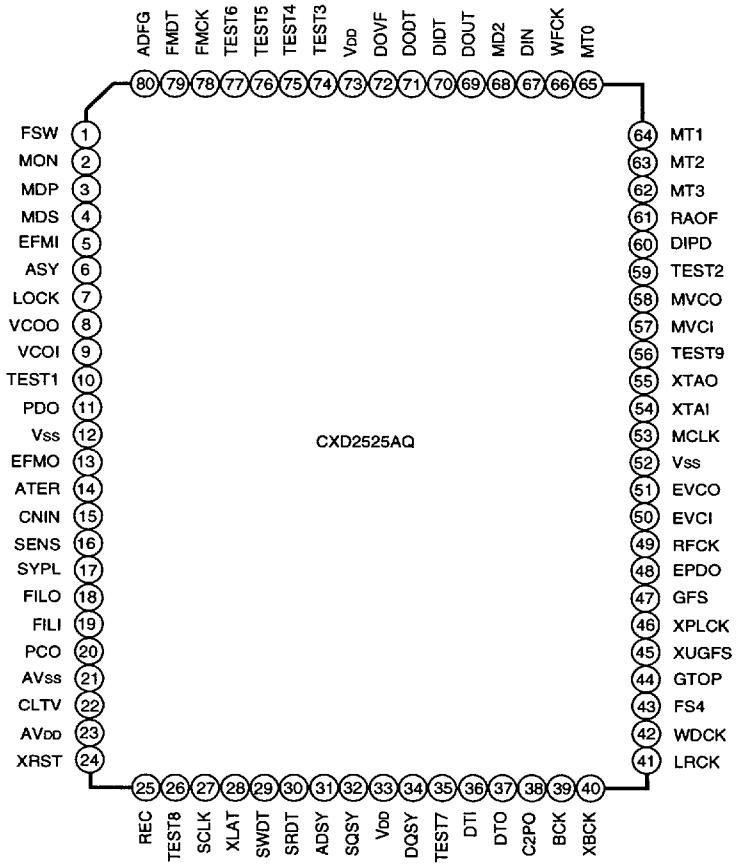
E94343-PP

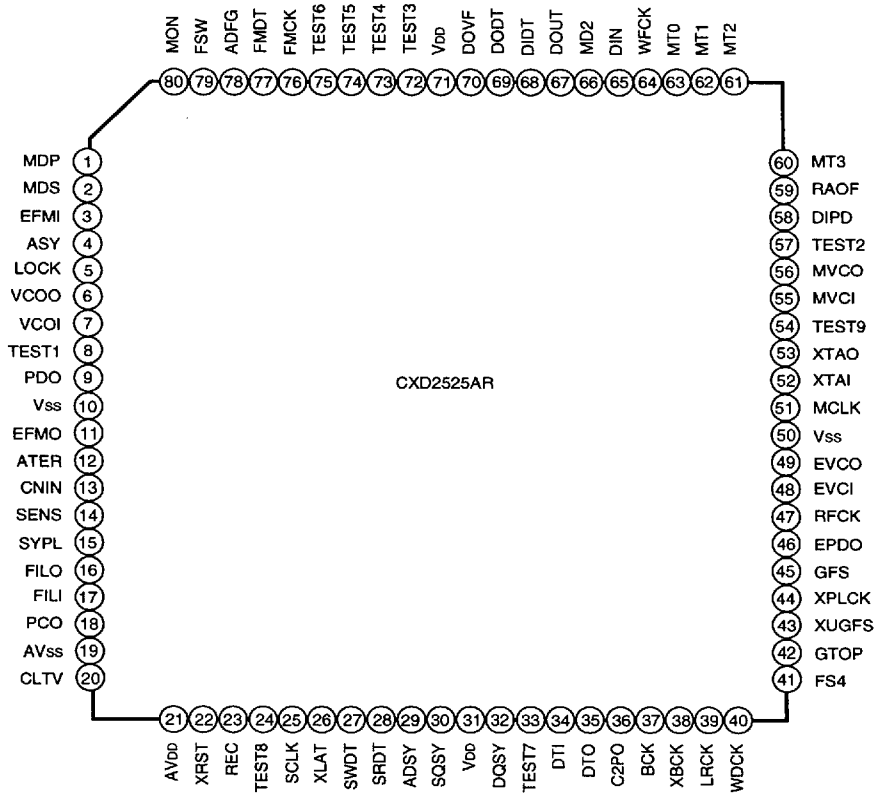
Block Diagram



Note) The pin numbers shown are for LQFP (CXD2525AR). Refer to the "Pin Description" for the pin numbers of QFP (CXD2525AQ).

Pin Configuration





Pin Description

Pin No. Q	Pin No. R	Symbol	I/O		Description
1	79	FSW	O	Z, L	LPF time constant switch used to remove the carrier component from the MDP and MDS pin outputs.
2	80	MON	O	H, L	Spindle motor on/off control output. High: on
3	1	MDP	O	H, Z, L	Spindle motor servo control signal. (Controls synchronization of speed and phase.)
4	2	MDS	O	H, Z, L	Spindle motor servo control signal. (Controls synchronization of speed.)
5	3	EFMI	I		EFM input.
6	4	ASY	O	H, L	EFM full-swing output during playback. 1/2 frequency output of internal VCO during recording.
7	5	LOCK	O	H, L	Lock status monitor of spindle servo (CLV). High: locked; Low: unlocked
8	6	VCOO	O		Analog PLL oscillation circuit output for EFM decoder (inverted output of VCOI pin).
9	7	VCOI	I		Analog PLL oscillation circuit input for EFM decoder (196Fs = 8.6436MHz).
10	8	TEST1	I		Test. Connect to GND.
11	9	PDO	O	H, Z, L	Analog PLL phase comparison output for EFM decoder.
12	10	Vss			Digital GND.
13	11	EFMO	O	H, L	Low during playback. EFM (encoder data) output during recording.
14	12	ATER	O	H, L	ADIP CRC flag. High: error
15	13	CNIN	I		Track jump number count signal input.
16	14	SENS	O	H, Z, L	Internal status output for the microcomputer serial interface data.
17	15	SYPL	I		Polarity switch input for the SQSY, ADSY, and DQSY pins. When the SYPL pin is low, sync is active low; when high, sync is active high.
18	16	FILO	O	Analog	Master PLL filter output for digital PLL.
19	17	FILI	I		Master PLL filter input for digital PLL.
20	18	PCO	O	H, Z, L	Master PLL phase comparison output for digital PLL.
21	19	AVss			Analog GND.
22	20	CLTV	I		Master PLL internal VCO control voltage input for digital PLL.
23	21	AV_{DD}			Analog power supply.
24	22	XRST	I		System reset input. Low: reset
25	23	REC	I		Recording/playback switch. Low: playback; high: recording
26	24	TEST8	I		Test. Connect to GND.
27	25	SCLK	I		Shift clock input for microcomputer serial interface.
28	26	XLAT	I		Latch input for microcomputer serial interface. Latches at the falling edge.
29	27	SWDT	I		Data input for the microcomputer serial interface.
30	28	SRDT	O	H, Z, L	Data output for the microcomputer serial interface.

Pin No. Q	Pin No. R	Symbol	I/O		Description
31	29	ADSY	O	H, L	ADIP sync output.
32	30	SQSY	O	H, L	Subcode Q sync output.
33	31	V_{DD}			Digital power supply.
34	32	DQSY	O	H, L	Subcode Q sync output in U-bit CD or MD format when the digital input source is CD or MD.
35	33	TEST7	O		Test. Leave open.
36	34	DTI	I		Recording data input from the CXD2526.
37	35	DTO	O	H, Z, L	During playback, playback data output to the CXD2526. During recording, high impedance.
38	36	C2PO	O	H, L	During playback, C2 pointer output for playback data. During digital recording, V bits output for digital input. During analog recording, low.
39	37	BCK	O	H, L	64Fs output (2.8224MHz).
40	38	XBCK	O	H, L	BCK inverted output.
41	39	LRCK	O	H, L	Fs output (44.1kHz).
42	40	WDCK	O	H, L	2Fs output (88.2kHz).
43	41	FS4	O	H, L	4Fs output (176.4kHz).
44	42	GTOP	O	H, L	Operation status monitor for frame sync protection window. High: frame sync protection window released
45	43	XUGFS	O	H, L	Frame sync output before frame sync protection. Low: frame sync
46	44	XPLCK	O	H, L	EFM decoder PLL clock. (98Fs = 4.3218MHz)
47	45	GFS	O	H, L	Frame sync OK for high.
48	46	EPDO	O	H, Z, L	PLL phase comparison output when EFM encoder PLL = external VCO.
49	47	RFCK	O	H, L	Read frame clock output. (Fs/6)
50	48	EVCI	I		PLL oscillation circuit input for EFM encoder (196Fs = 8.6436MHz).
51	49	EVCO	O		PLL oscillation circuit output for EFM encoder (inverted output of EVCI pin).
52	50	Vss			Digital GND.
53	51	MCLK	O	H, L	Master clock output (512Fs = 22.5792MHz). Duty is not guaranteed.
54	52	XTAI	I		Crystal oscillation circuit input (512Fs = 22.5792MHz).
55	53	XTAO	O		Crystal oscillation circuit output (inverted output of XTAI pin).
56	54	TEST9	I		Test. Connect to GND.
57	55	MVCI	I		Oscillation circuit input for digital in PLL (512Fs = 22.5792MHz).
58	56	MVCO	O		Oscillation circuit output for digital in PLL (inverted output of MVCI pin).
59	57	TEST2	O		Test. Leave open.
60	58	DIPD	O	H, Z, L	Phase comparison output for digital in PLL.
61	59	RAOF	O	H, L	During playback, RAM overflow output.

Pin No. Q	Pin No. R	Symbol	I/O		Description
62	60	MT3	O	H, L	Error correction status monitor output.
63	61	MT2	O	H, L	Error correction status monitor output.
64	62	MT1	O	H, L	Error correction status monitor output.
65	63	MT0	O	H, L	Error correction status monitor output.
66	64	WFCK	O	H, L	Write frame clock output.
67	65	DIN	I		Digital audio interface signal input.
68	66	MD2	I		DOUT pin output on/off. High: on; low: off, and the DOUT pin goes low.
69	67	DOUT	O	H, L	Digital audio interface signal output.
70	68	DIDT	O	H, L	Audio data output for signal input from the DIN pin.
71	69	DODT	I		Audio data input for signal output from the DOUT pin.
72	70	DOVF	I		V bit input for signal output from the DOUT pin.
73	71	V_{DD}			Digital power supply.
74	72	TEST3	I		Test. Connect to GND.
75	73	TEST4	O		Test. Leave open.
76	74	TEST5	I		Test. Connect to GND.
77	75	TEST6	I		Test. Connect to GND.
78	76	FMCK	I		ADIP data transfer clock input (6.3kHz). (TTL Schmitt input)
79	77	FMDT	I		ADIP data input. (TTL Schmitt input)
80	78	ADFG	I		ADIP carrier signal input (22.05kHz). (TTL Schmitt input)

- Refer to the SSP (CXA1082 or CXA1602) specifications for the FSW pin.
- Refer to address $83 (CLV MODE) in "§1. Microcomputer Interface" for the MON, MDP, MDS, and LOCK pins.
- Refer to "§12. Asymmetry Compensation" for the ASY pin.
- Feedback resistance between the following pins is built in: VCOI and VCOO, EVCI and EVCO, MVCI and MVCO, and XTAI and XTAO.
- Refer to "§3. PLL" for the PDO, EPDO, and DIPD pins.
- Refer to "§2. Description of SENS Pin" for the SENS pin.
- Refer to "§3. PLL" for the connection of the FILO, FILI, PCO, and CLTV pins.
- Error correction is not possible if the C2PO pin is high during playback. Refer to "§7. Audio Interface" for the output timing.
- Refer to "§4. Frame Sync Protection" for the GTOP pin.
- The GFS pin goes high when the frame sync and built-in protection timing match.
- The RAOF signal is generated when the 32K RAM exceeds the ±4-frame jitter margin during playback. During recording, this signal is not monitored.
- The MT3 to MT0 pins are valid when the REC pin is low (playback). When the REC pin is high (recording), the error correction status is not monitored. Refer "§5. Error Correction" for details on the monitoring method.
- Connect the FMCK, FMDT, and ADFG pins to the FMCK, FMDT, and ADIPFG pins of the CXA1380, respectively.

Electrical characteristics

DC characteristics 1 (V_{DD} = AV_{DD} = 4.5 to 5.25V, Vss = AVss = 0V, Topr = –20 to +75°C)

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		0.7V_{DD}			V	*1
	Low level input voltage	V_{IL} (1)				0.3V_{DD}	V	
Input voltage (2)	High level input voltage	V_{IH} (2)	Schmitt input	0.8V_{DD}			V	*2
	Low level input voltage	V_{IL} (2)				0.2V_{DD}	V	
Input voltage (3)	Input voltage	V_{IN} (3)	Analog input	Vss		V_{DD}	V	*3
Output voltage (1)	High level output voltage	V_{OH} (1)	I_{OH} = –4.0mA	V_{DD}–0.8			V	*4
	Low level output voltage	V_{OL} (1)	I_{OH} = 4.0mA			0.4	V	
Output voltage (2)	High level output voltage	V_{OH} (2)	I_{OH} = –2.0mA	V_{DD}–0.8			V	*5
	Low level output voltage	V_{OL} (2)	I_{OH} = 4.0mA			0.4	V	
Output voltage (3)	Low level output voltage	V_{OL} (3)	I_{OH} = 4.0mA			0.4	V	*6
Output voltage (4)	High level output voltage	V_{OH} (4)	I_{OH} = –0.28mA	V_{DD}–0.5			V	*7
	Low level output voltage	V_{OL} (4)	I_{OH} = 0.36mA			0.4	V	
Input leak current		I_{LI}	V_I = 0 to V_{DD}			±5	µA	*1, 2, 3
Tri-state current Output leak current		I_{LO}	V_{IO} = 0 to V_{DD}			±5	µA	*8

Applicable pins

*1 EFMI, SYPL, REC, XLAT, SWDT, DTI, DIN, MD2, DODT, DOVF

*2 CNIN, XRST, SCLK, FMCK, FMDT, ADFG

*3 CLTV, FILI

*4 MDP, PDO, PCO, EPDO, DIPD

*5 MON, ASY, LOCK, EFMO, ATER, ADSY, SQSY, DQSY, C2PO, BCK, XBCK, LRCK, WDCK, FS4, GTOP, XUGFS, XPLCK, GFS, RFCK, MCLK, RAOF, MT3, MT2, MT1, MT0, WFCK, DOUT, DIDT, MDS, SENS, SRDT, DTO

*6 FSW

*7 FILO

*8 FSW, MDP, MDS, PDO, SENS, PCO, SRDT, DTO, EPDO, DIPD

DC characteristics 2 (V_{DD} = AV_{DD} = 3.3V±10%, Vss = AVss = 0V, Topr = –20 to +75°C)

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		0.7V_{DD}			V	*1
	Low level input voltage	V_{IL} (1)				0.3V_{DD}	V	
Input voltage (2)	High level input voltage	V_{IH} (2)	Schmitt input	0.8V_{DD}			V	*2
	Low level input voltage	V_{IL} (2)				0.2V_{DD}	V	
Input voltage (3)	Input voltage	V_{IN} (3)	Analog input	Vss		V_{DD}	V	*3
Output voltage (1)	High level output voltage	V_{OH} (1)	I_{OH} = –2.4mA	V_{DD}–0.8			V	*4
	Low level output voltage	V_{OL} (1)	I_{OH} = 2.4mA			0.4	V	
Output voltage (2)	High level output voltage	V_{OH} (2)	I_{OH} = –1.2mA	V_{DD}–0.8			V	*5
	Low level output voltage	V_{OL} (2)	I_{OH} = 2.4mA			0.4	V	
Output voltage (3)	Low level output voltage	V_{OL} (3)	I_{OH} = 2.4mA			0.4	V	*6
Output voltage (4)	High level output voltage	V_{OH} (4)	I_{OH} = –0.19mA	V_{DD}–0.5			V	*7
	Low level output voltage	V_{OL} (4)	I_{OH} = 0.27mA			0.4	V	
Input leak current		I_{LI}	V_I = 0 to V_{DD}			±5	µA	*1, 2, 3
Tri-state current Output leak current		I_{LO}	V_{IO} = 0 to V_{DD}			±5	µA	*8

Applicable pins

*1 EFMI, SYPL, REC, XLAT, SWDT, DTI, DIN, MD2, DODT, DOVF
*2 CNIN, XRST, SCLK, FMCK, FMDT, ADFG
*3 CLTV, FILI
*4 MDP, PDO, PCO, EPDO, DIPD
*5 MON, ASY, LOCK, EFMO, ATER, ADSY, SQSY, DQSY, C2PO, BCK, XBCK, LRCK, WDCK, FS4, GTOP, XUGFS, XPLCK, GFS, RFCK, MCLK, RAOF, MT3, MT2, MT1, MT0, WFCK, DOUT, DIDT, MDS, SENS, SRDT, DTO
*6 FSW
*7 FILO
*8 FSW, MDP, MDS, PDO, SENS, PCO, SRDT, DTO, EPDO, DIPD

AC Characteristics

(1) XTAI, VCOI, EVCI, and MVCI pins

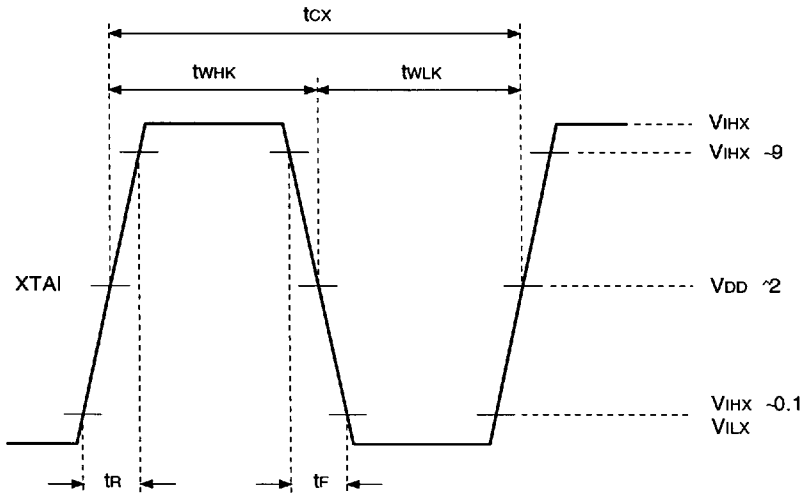
1) When using self-oscillation (Topr = –20 to +75°C, V_{DD} = AV_{DD} = 3.0 to 5.25V)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	7	22.5792	25	MHz

2) When inputting a pulse to the XTAI, VCOI, EVCI, and MVCI pins

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 3.0 to 5.25V)

Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}	20		500	ns
Low level pulse width	t_{WLX}	20		500	ns
Pulse cycle	t_{CX}	40		1,000	ns
Input high level	V_{IHX}	V_{DD}–1.0			V
Input low level	V_{ILX}			0.8	V
Rise time Fall time	t_R, t_F			10	ns



3) When inputting a sine wave to the XTAI, VCOI, EVCI, and MVCI pins via a capacitor

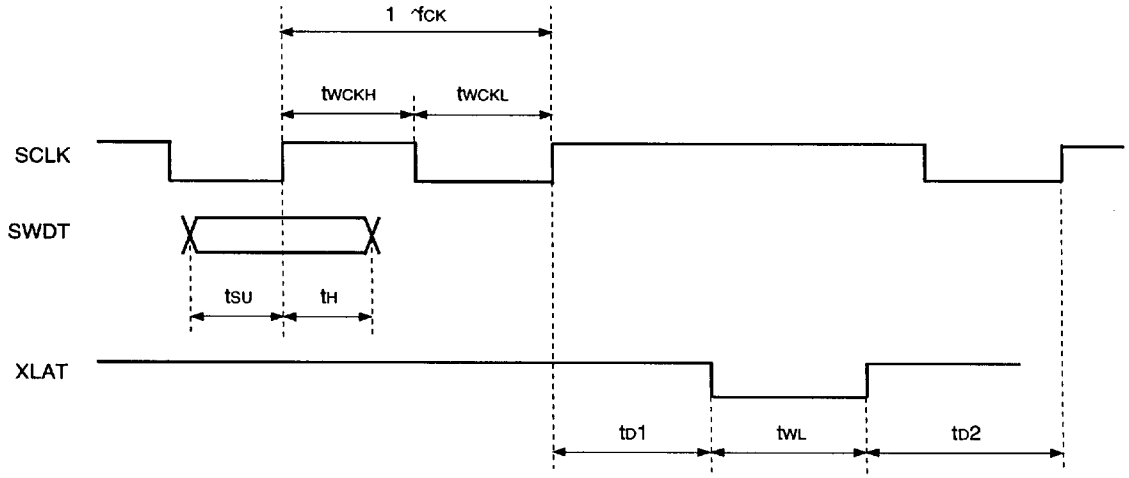
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 3.0 to 5.25V)

Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_I	2.0		V_{DD}+0.3	Vp-p

(2) SCLK, SWDT, and XLAT pins

(V_{DD} = AV_{DD} = 3.0 to 5.25V, Vss = AVss = 0V, Topr = −20 to +75°C)

Item	System	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}	4.2		650	kHz
Clock pulse width	t_{WCKH}, t_{WCKL}	0.75		120	µs
Setup time	t_{SU}	200			ns
Hold time	t_H	200			ns
Delay time 1	t_{D1}	200			ns
Delay time 2	t_{D2}	0			ns
Latch pulse width	t_{WL}	250			ns



Description of Functions

§1. Microcomputer Interface (related pins: SCLK, XLAT, SWDT, SRDT)

In an MD system, the microcomputer sets the various modes and reads and writes data to each IC, all through serial transfers. Chip addresses are assigned to each IC as shown in the following table.

A7	A6	A5	A4	Assignment
1	0	0	×	CXD2525
1	0	1	×	CXD2526
1	1	0	×	
1	1	1	0	CXD2527, CXD2531
0	×	×	×	CXA1082, CXA1602

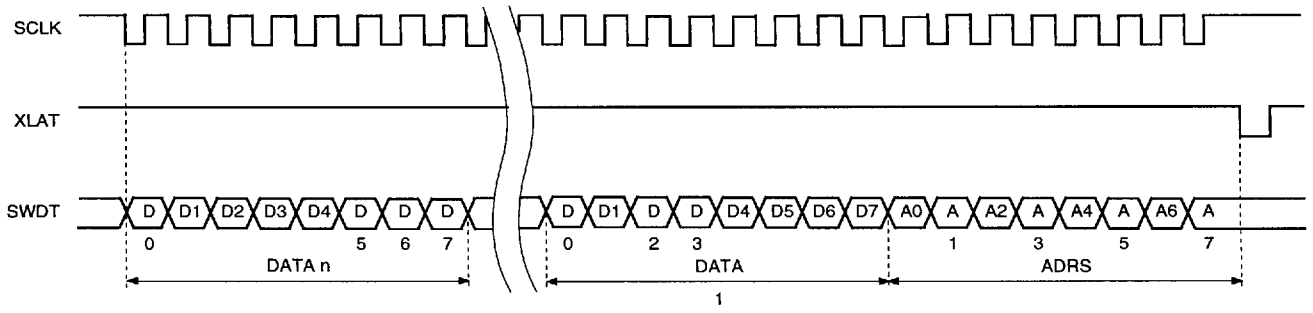
Chip Address Table

§1-1. Microcomputer Interface Transfer Format

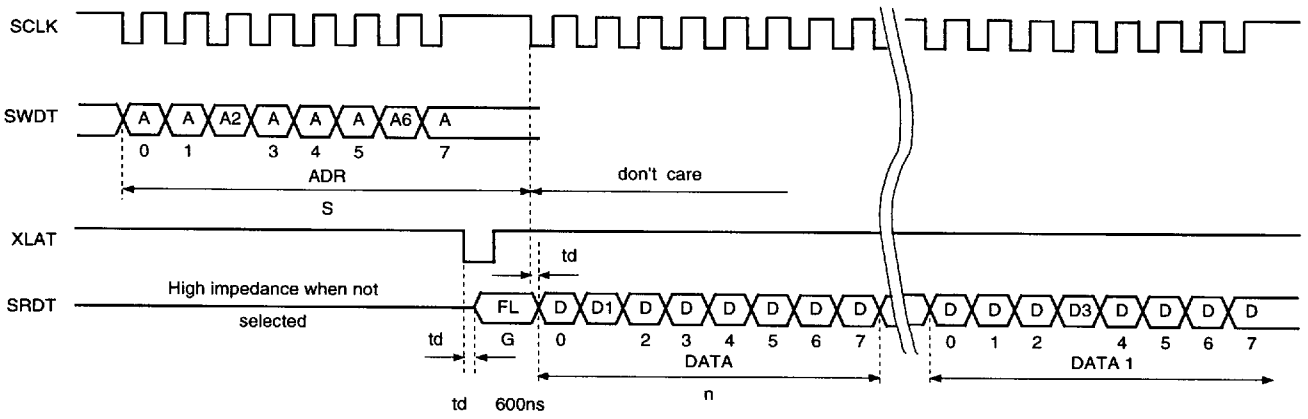
There are two methods used for transfer between this IC and the microcomputer: transferring the SYSTEM command or the DATA WRITE command, or reading data from this IC using the READ CTRL command. The format for SWDT and SRDT pin data transfers is MS byte first, LS bit first.

Note: Refer to "§1-2. Command/Status".

- When transferring the SYSTEM command or DATA WRITE command
  The microcomputer transfers the data, address and latch signal.



• When the microcomputer reads data using the READ CTRL command
When the address and latch signal are transferred from the microcomputer, a flag is output from the SRDT pin. After the flag is read by the microcomputer, if the transfer clock is sent the data is output from the SRDT pin.



Note: When an address that is not for the READ CTRL command is sent, the SRDT pin goes to high impedance.

§1-2. Command/Status

• SWDT pin input

The write data and address are transferred from the microcomputer to the SWDT pin.

—: Don't Care
Z : High impedance

COMMAND		ADDRESS HEX	Chip ADRS A7 A6 A5	R/W A4	A3 A2 A1 A0	DATA DATA1 D7	D6	D5	D4	D3	D2	D1	D0	DATA2 D7 to D0	DATA3 to DATA10	SENS pin output
SYSTEM	SYSTEM SET	$80	1 0 0	0	0 0 0 0	GSEL (4/$\overline{13}$)	WSEL (26/$\overline{6}$)	0	0	0	ENCPLL EXT/$\overline{INT}$	DECPLL A/$\overline{D}$	0	—	—	GFS
	SYSTEM CTRL	$81			0 0 0 1	0	0	0	0	VCO/$\overline{XTAL}$	ECC 2/$\overline{4}$	0	FLFC	—	—	$\overline{OV64}$
	COUNT monitor	$82			0 0 1 0	0	0	0	0	0	0	0	0	—	—	$\overline{COUNT}$
	CLV MODE	$83		0	0 0 1 1	CM3	CM2	CM1	CM0	GAIN1	GAIN0	—	—	—	—	CLV LOCK
DATA WRITE	Traverse counter set	$88			1 0 0 0	MSB	16bit							LSB	—	$\overline{COMPLT}$
	D. Out-Cbit	$89			1 0 0 1	bit15	16bit							bit0	—	Z
	Sub Q	$8B			1 0 1 1	80bit										
READ CTRL	STATUS	$90		1	0 0 0 0	Output from SDRT pin										Z
	ADIP	$91			0 0 0 1											
	D. In-Ubit Sub Q	$93			0 0 1 1											
	D. In-Cbit	$94			0 1 0 0											STID
	PEAK-DATA	$95			0 1 0 1											Z
	Disc Sub Q	$97			0 1 1 1											

Command/Status Table

Note: In reset initialization, the data from address $80 to $8B is set to "0".

• SENS pin output (Refer to "§2. Description of SENS Pin")

If the address is set by the microcomputer interface, the internal status of the IC can be monitored corresponding to that address. If the address is not $80 to $83, $88, or $94, the SENS pin goes to high impedance.

• SYSTEM command ($80 to $83)

$80 : SYSTEM SET

DATA1	D7	GSEL	*1	0	Number of playback EFM SYNC insertion frames: 13 frames
				1	Number of playback EFM SYNC insertion frames: 4 frames
	D6	WSEL	*2	0	Playback EFM SYNC protection WINDOW: ±6 clock
				1	Playback EFM SYNC protection WINDOW: ±26 clock
	D2	ENCPLL EXT/$\overline{INT}$	*3	0	Encoder PLL = use of internal VCO used
				1	Encoder PLL = use of external VCO used
	D1	DECPLL A/$\overline{D}$	*4	0	Decoder PLL = digital PLL
				1	Decoder PLL = analog PLL

Note: Set D5, D4, D3, and D0 of DATA1 to "0".

*1) 13 insertion frames are recommended because more frames means better playability.

*2) When WINDOW is ±6 clocks, the sync window protection is enhanced and the possibility of incorrect detection is reduced. When WINDOW is ±26 clocks, the anti-rolling characteristics are improved. The clock frequency is 98Fs (4.3218MHz). Refer to "§4. Frame Sync Protection."

*3) When the encoder PLL = internal VCO, use the divided master PLL internal VCO (784Fs = 34.5744MHz) for the digital PLL. In this case, the phase comparison frequency of master PLL internal VCO is Fs (44.1kHz). In addition, because an external VCO is not used, connect the EVCI pin to GND and leave the EVCO and EPDO pins open.
When the encoder PLL = external VCO, the phase comparison frequency of the master PLL internal VCO for the digital PLL is 8Fs (352.8kHz).
Refer to "§3. PLL."

*4) When decoder PLL = digital PLL, use the master PLL internal VCO for the digital PLL. Connect the VCOI pin to GND and leave the VCOO and PDO pins open.
When the decoder PLL = analog PLL, use the external VCO.
Refer to "§3. PLL."

$81 : SYSTEM CONTROL

DATA1	D3	VCO/$\overline{XTAL}$ *1	0	X' TAL
			1	External VCO for digital in PLL
	D2	ECC 2/$\overline{4}$ *2	0	C2 error: quadruple correction
			1	C2 error: double correction
	D0	FLFC *3	0	Phase and frequency comparison
			1	Phase comparison only

Note: Set D7 through D4 and D1 of DATA1 to "0".

*1) Selects the source of the master clock (512Fs).
During analog recording or playback, select "X'TAL". The clock input through the XTAI pin becomes the master clock.
During digital recording, select the external VCO for the digital in PLL. The clock input through the MVCI pin becomes the master clock.

*2) Although either quadruple correction or double correction can be selected for C2 error correction during playback, quadruple correction (D2 = 0) is recommended since the higher correction capability is better.

*3) If the decoder PLL = digital PLL, then when FLFC = 0, the capture range is approximately ±150kHz. When FLFC = 1, the capture range is approximately ±50kHz.
Refer to "§3-3. Channel Clock Playback through the Digital PLL Circuit."
When decoder PLL = analog PLL, the FLFC setting is "don't care".

$82 : COUNT monitor

This is used to monitor the number of track jumps through the SENS pin or the SRDT pin ($90).
Refer to "§11. Using the Traverse Counter."

$83 : CLV MODE

The CLV operation mode is set by D7 to D4 of DATA1, and the CLV gain is set by D3 and D2. D1 and D0 do not matter.

Z: High impedance

DATA1				HEX	Mode	MON pin	FSW pin
D7	D6	D5	D4				
CM3	CM2	CM1	CM0				
0	0	0	0	0	STOP	L	L
1	0	0	0	8	KICK	H	L
1	0	1	0	A	BRAKE	H	L
1	1	1	0	E	EFM-CLVS	H	L
1	1	0	0	C	EFM-CLVH	H	L
1	1	1	1	F	EFM-CLVP	H	Z
0	1	1	0	6	EFM-CLVA	H	L or Z
0	0	0	1	1	ADIP-CLVS	H	L
0	0	1	0	2	ADIP-CLVP	H	Z
0	0	1	1	3	ADIP-CLVA1	H	L or Z
0	1	0	0	4	ADIP-CLVA2	H	L or Z
0	1	0	1	5	ADIP-CLVA3	H	L or Z

CLV Operation Mode

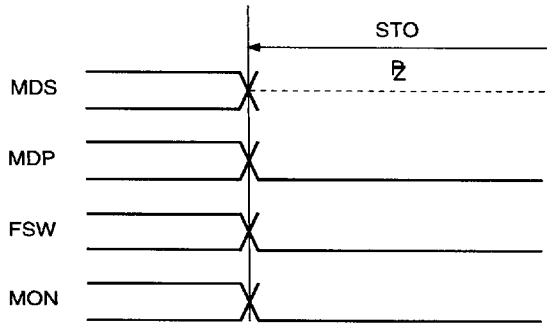
DATA1		CLV GAIN
D3	D2	
GAIN1	GAIN0	
0	0	–6dB
0	1	–12dB
1	0	–18dB
1	1	0dB

CLV Gain

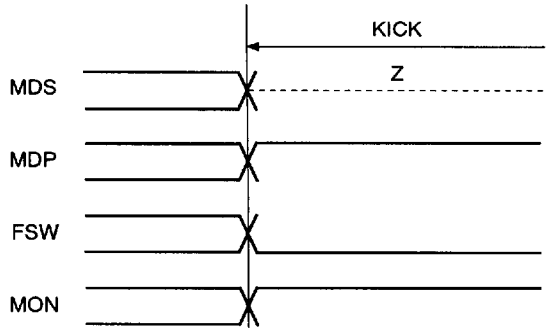
Note: The CLV gain is set in all cases (including STOP, KICK, and BRAKE).

• CLV Operation Mode (the timing chart is for the gain of 0dB.)

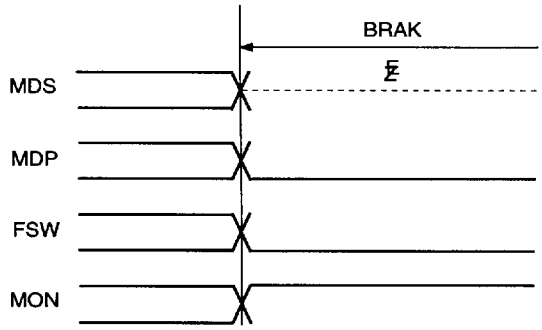
STOP: Stops the spindle motor.



KICK: Rotates the spindle motor in the normal direction.



BRAKE: Rotates the spindle motor in the reverse direction.



EFM — CLVn (n = S, H, P, or A)

The CLV servo is turned on according to the playback EFM signal input from the EFMI pin. This is effective when turning the CLV servo on in the pit sections of the disc.

Rough servo mode (EFM — CLVS and EFM — CLVH)

The longest pulse width in the pulse cycle of the playback EFM signal input from the EFMI pin is assumed to be the frame sync, and the spindle motor servo control signal is output from the MDP pin so that the frame sync pulse width is 22T (T = 1/8.6436MHz).

Frame sync detection method

If T = 1/8.6436MHz, the frame sync pulse width is 22T at the prescribed rate of rotation, which is the maximum pulse width within one RFCK cycle. However, in actuality, missing EFM signal pulses, etc., cause the pulse width to sometimes be greater than 22T. If they are not eliminated, the frame sync signal cannot be detected properly. Therefore, in each cycle (TP) the maximum (peak) pulse width of the EFM signal is detected. Then, the minimum value for the peak in each TP cycle is detected over a period (TB) longer than the TP cycle, and that signal is assumed to be the frame sync signal.

EFM — CLVS: Pull-in rough servo mode

This mode is used at the start of rotation, during track jumps, and other times when the EFM-PLL circuit lock is lost.

The peak hold and bottom hold cycles are TP = RFCK/4 and TB = RFCK/32.

EFM — CLVH: Rough servo mode during high-speed access

This mode is used during track jumps between pits.

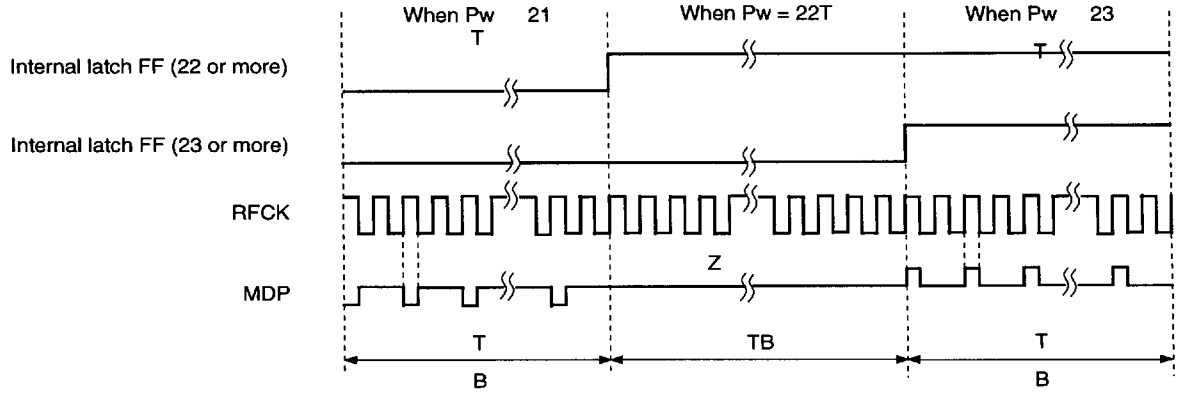
As an example, assume that a 5000-track jump is made in one second from the inner track to the outer track. In that case, the mirrored sections between tracks (the section where there are no pits) becomes a 5-kHz signal, and it is superimposed on the EFM signal. If the signal is input in EFM-CLVS mode, a mirrored section longer than the original frame sync signal may be detected as the peak value, destabilizing the operation of the servo.

Therefore, in EFM-CLVH, by performing peak hold at a cycle of TP = 8.6436MHz/256 (approximately 34kHz), and bottom hold at a cycle of TB = RFCK/32, the mirrored sections are excluded and the operation of the servo during high-speed accesses is stabilized. Only the cycles where the peak value is detected is different for EFM-CLVH and EFM-CLVS.

Note: The MON pin is high, the FSW pin is low, and the MDS pin is high impedance for both EFM — CLVS and EFM — CLVH.

MDP pin output in EFM — CLVS and EFM — CLVH

Assume Pw as the frame sync pulse width after frame sync detection.

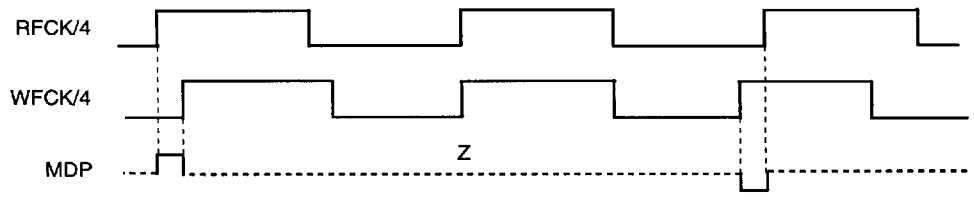


MDP Pin Output in EFM — CLVS and EFM — CLVH (CLV gain = 0dB)

EFM — CLVP: PLL servo mode

MON pin = high and FSW pin = high impedance.

The MDP pin controls phase synchronization.



MDP Pin Output Example in EFM — CLVP (CLV gain = 0dB)

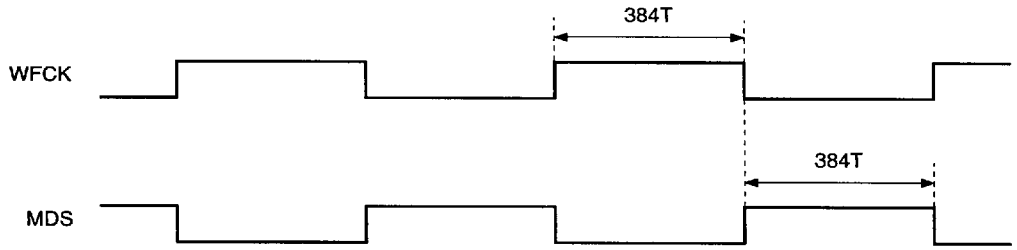
The MDS pin controls high-speed synchronization.

T_{MDS}, the time when the MDS pin is high, is derived according to the following formula when the gain is 0dB:

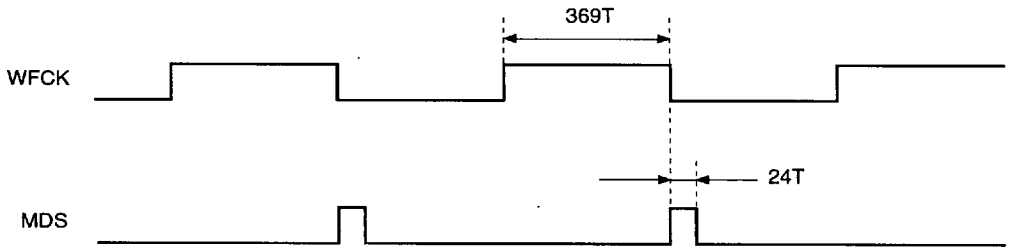
T_{MDS} = (High duration of the WFCK pin–368T) × 24

Here, T = 1/ (5.6448MHz).

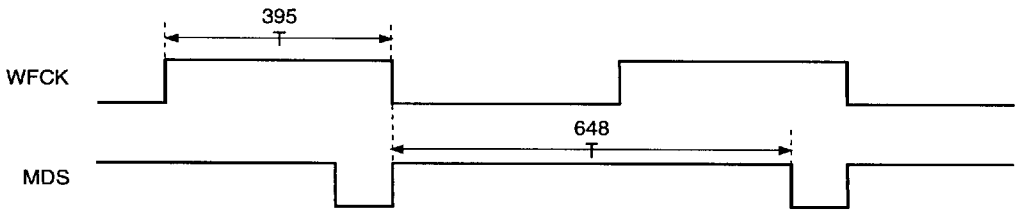
1) MDS pin output when rotating at prescribed speed (CLV gain = 0dB)



2) Example of MDS pin output when rotating at faster than prescribed speed (CLV gain = 0dB)



3) Example of MDS pin output when rotating at slower than prescribed speed (CLV gain = 0dB)



EFM — CLVA: Auto mode

The GFS signal is sampled at WFCK/16; when high: EFM-CLVP. If low in eight consecutive samples: EFM – CLVS. This mode is used when the RF signal is read from the disc.

ADIP — CLVn (n = S, P, or A1 to A3)

The CLV servo is turned on according to the signals input from the FMCK and ADFG pins. This mode is effective when the CLV servo is turned on in the disc groove section.

ADIP — CLVS: Pull-in rough servo mode

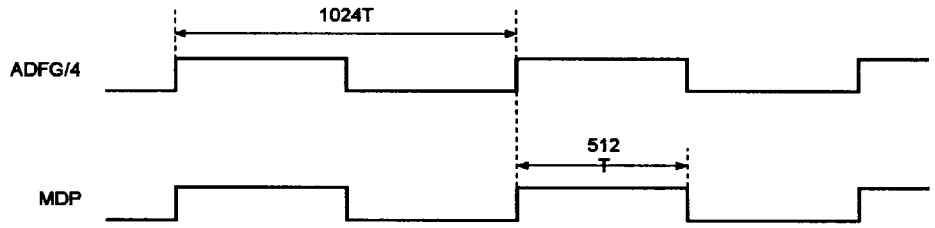
The MON pin = high, the FSW pin = low, and the MDS pin = high impedance.

A high signal is output from the MDP pin for the time T_{MDP} as determined according to the following formula so that the signal input from the ADFG pin is 22.05kHz (when the gain is 0dB):

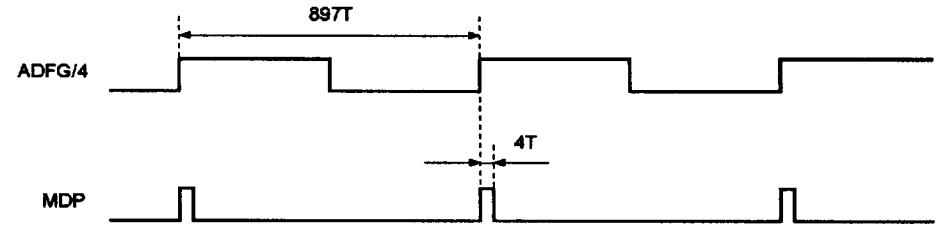
T_{MDP} = (ADFG/4 cycle – 896T) ¥ 4

Here, T = 1/5.6448MHz.

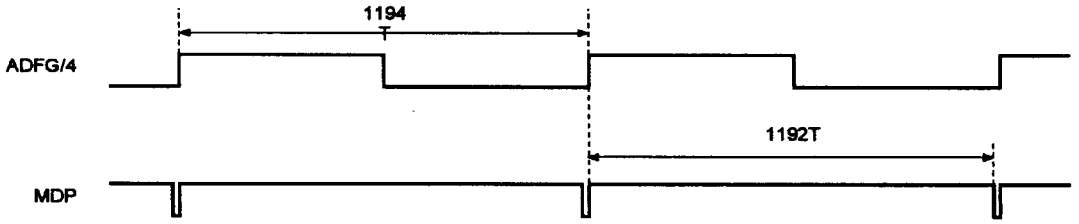
1) MDP pin output when rotating at prescribed speed (CLV gain = 0dB)



2) Example of MDP pin output when rotating at faster than prescribed speed (CLV gain = 0dB)



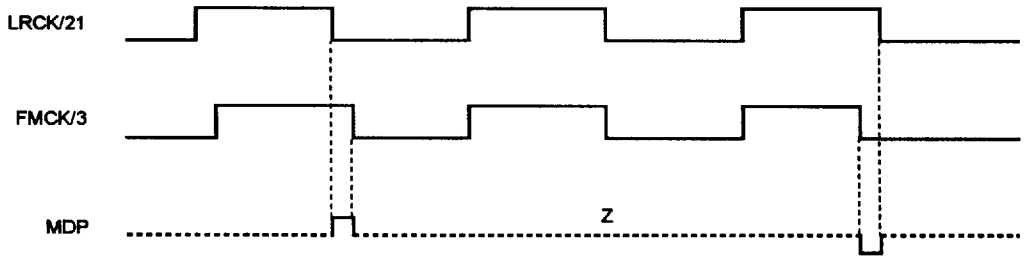
3) Example of MDP pin output when rotating at slower than prescribed speed (CLV gain = 0dB)



ADIP — CLVP: PLL servo mode

The MON pin = high and the FSW pin = high impedance.

The MDP pin controls phase synchronization.



MDP Pin Output Example in ADIP — CLVP (CLV gain = 0dB)

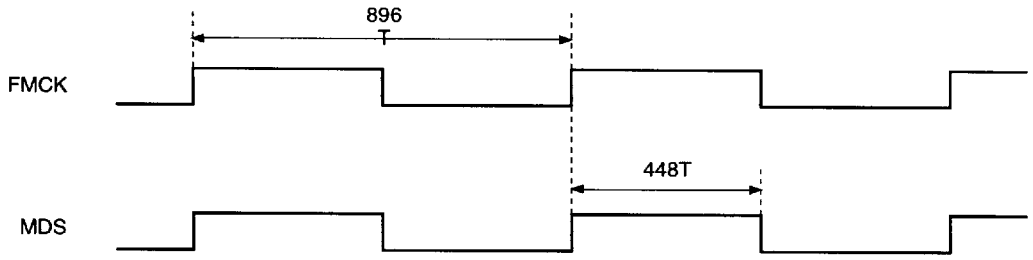
The MDS pin controls speed synchronization.

A high signal is output from the MDS pin for the time T_{MDS} as determined according to the following formula so that the signal input from the FMCK pin is 6.3kHz (when the gain is 0dB):

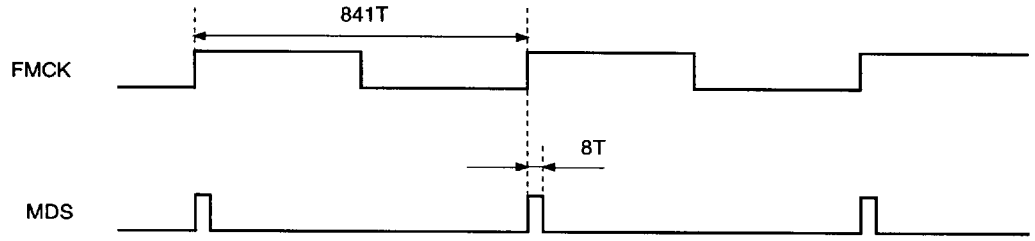
T_{MDS} = (FMCK cycle – 840T) × 8

Here, T = 1/5.6448MHz.

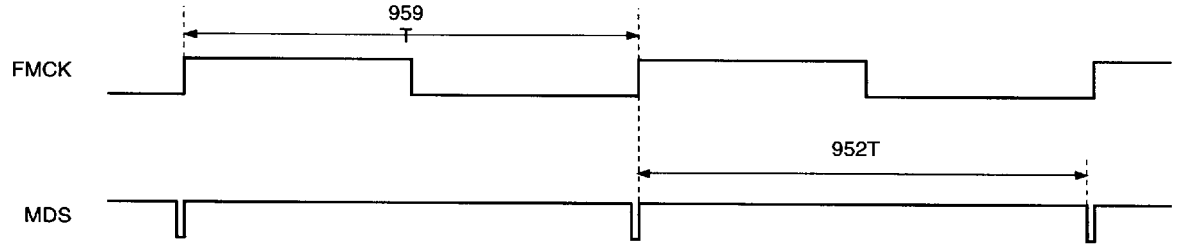
1) MDS pin output when rotating at prescribed speed (CLV gain = 0dB)



2) Example of MDS pin output when rotating at faster than prescribed speed (CLV gain = 0dB)



3) Example of MDS pin output when rotating at slower than prescribed speed (CLV gain = 0dB)



ADIP — CLVA1: Auto mode 1

When ADIP CRC check is OK twice in a row: ADIP — CLVP. If not OK once: ADIP — CLVS.

ADIP — CLVA2: Auto mode 2

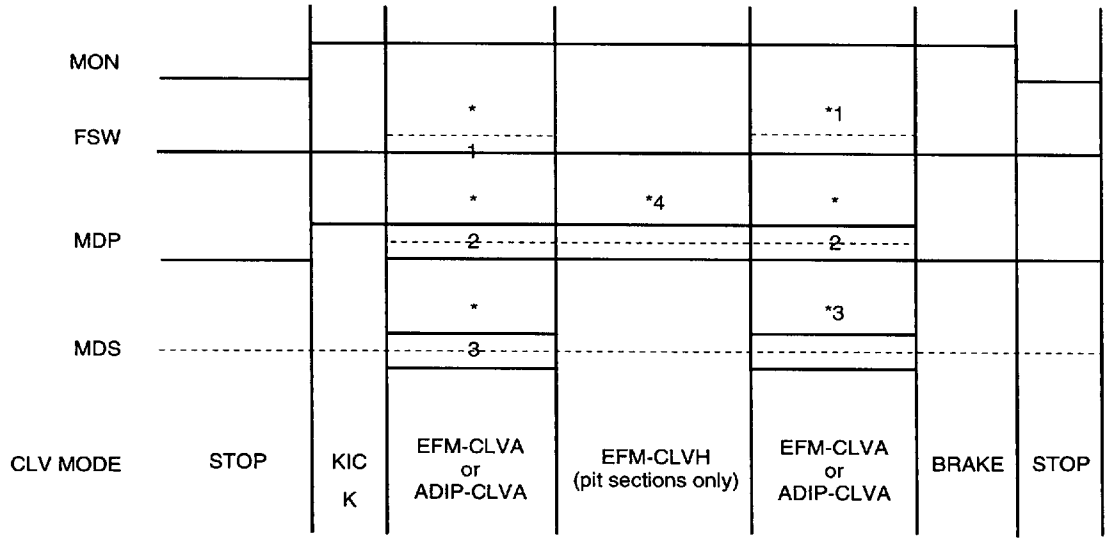
When ADIP CRC check is OK twice in a row: ADIP — CLVP. If not OK for four consecutive frames: ADIP — CLVS.

ADIP — CLVA3: Auto mode 3

When ADIP CRC check is OK twice in a row: ADIP — CLVP. If not OK for ten consecutive frames: ADIP — CLVS.

Note: Set the mode as desired.

Spindle Motor Control Example (when CLV gain is 0dB)



Note: The dotted lines indicate high impedance.

*1) Low for EFM — CLVS and ADIP — CLVS
High impedance for EFM — CLVP and ADIP — CLVP

*2) Low, high impedance and high for EFM — CLVS
Low or high for ADIP — CLVS
Low, high impedance, or high for EFM — CLVP and ADIP — CLVP

*3) High impedance for EFM — CLVS and ADIP — CLVS
Low or high for EFM — CLVP and ADIP — CLVP

*4) Low, high impedance, or high.

- Relationship between the CLV gain setting and the output waveforms of the MDP pin and the MDS pin
  The MDP and MDS pin outputs are of the PWM output format, consisting of high, low, and high impedance.

  When the CLV gain is 0dB, the output from the MDP and MDS pins is as shown in the address $83 (CLV mode) timing chart.
  If the CLV gain is changed, the time when the MDP and MDS pin outputs are high or low becomes shorter in proportion to the gain each 88.2kHz cycle. For the remainder of the time, the signal is high impedance.
  For example: in the case of STOP, when the CLV gain is –6dB, the MDP pin outputs a low signal for one-half the time of the 88.2kHz signal, and goes to high impedance for the other one-half the time.

- CLV lock status monitor
  The CLV lock status can be monitored through the LOCK pin, the SENS pin (note 1), or the microcomputer interface (note 2). High: locked; low: unlocked.
  Note 1: Refer to "§2. Description of SENS Pin."
  Note 2: Refer to "§1. Microcomputer Interface" ($90).

• CLV locked/unlocked judgment criteria

The criteria for making the CLV locked/unlocked judgment differ according to the CLV operation mode setting (microcomputer interface, address $83).

If the CLV operation mode is STOP, KICK, BRAKE, EFM — CLVS, EFM — CLVH, EFM — CLVP, or EFM — CLVA, the GFS signal is sampled at WFCK/16. When high: locked; when low for eight consecutive samples: unlocked.

For ADIP — CLVS, — CLVP, and — CLVA2:
If the result of the ADIP CRC check is "OK" twice in a row, locked; if not OK for four consecutive frames, unlocked.

For ADIP — CLVA1:
If the result of the ADIP CRC check is "OK" twice in a row, locked; if not OK for one frame: unlocked.

For ADIP — CLVA3:
If the result of the ADIP CRC check is "OK" twice in a row, locked; if not OK for ten consecutive frames, unlocked.

• DATA WRITE command ($88, $89, $8B)

$88 : Traverse counter set

WRITE DATA	ADRS	DATA1								DATA2							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Traverse counter set	$88	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Sets the number of track jumps when executing a track jump. For details on usage, refer to "§11. Using the Traverse Counter."

$89 : Setting the C bits in digital audio interface signal output (the DOUT pin)

WRITE DATA	ADRS	DATA1								DATA2							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
D. Out-Cbit	$89	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		Lbit	Category code							0	0	CONTROL					0

Of the digital output C bits (channel status), bit 0 to bit 15 must be set by the microcomputer. Support type 2, form 1 for home use. C bits from bit 16 on are all automatically set to "0".
Once the data is set, the values are held. Refer to "§10. Digital Audio Interface."

$8B : Sub Q setting (Settings differ for playback and recording.)

WRITE DATA	ADRS	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7	DATA8	DATA9	DATA10
		D7 to D0	D7 to D0	D7 to D0	D7 to D0	D7 to D0	D7 to D0	D7 to D0	D7 to D0	D7 to D0	D7 to D0
SubQ	$8B	00	00	00	00	00	00	00	*1	*2	00

Mode	*1	*2
Playback	INDEX	TNO
Recording	00	00

During playback (the REC pin is low): Sets the U bits of the digital audio interface signal output (DOUT pin). Aside from INDEX and TNO, all are set to "0". Refer to"§10. Digital Audio Interface."

During recording: (the REC pin is high): Sets the Sub Q recorded on the disc. The 80 bits are all set to "0". Refer to "§8. Subcodes."

Always set these bits at the start of playback and recording, respectively. Once set, those values are held, however, when switching from playback to recording or vice versa, these values must be set once again. The Sub Q CRC is automatically generated in the IC.

- SRDT pin output

A flag is output when an address is transferred to the SWDT pin and the XLAT pin falls. In addition, if the transfer clock is input, data is output from the SRDT pin.

- READ CTRL command ($90, $91, $93 to $95, $97)

$90: STATUS.

READ DATA	ADRS	DATA1								FLG
		D7	D6	D5	D4	D3	D2	D1	D0	
STATUS	$90	GFS	ENCPLL LOCK	DINPLL LOCK	$\overline{\text{COMPLT}}$	$\overline{\text{COUNT}}$	CLV LOCK	$\overline{\text{OV64}}$	0	READ OK

The data is set in the read register at the falling edge of the XLAT signal.

FLG: READ OK
Goes high at the falling edge of the XLAT signal.

GFS: When high: frame sync OK. Output from both the GFS pin and the SENS pin.

ENCPLL LOCK: Encoder PLL lock status monitor. High: locked; low: unlocked.

DINPLL LOCK: Digital in PLL lock status monitor.
Goes high when digital in PLL is locked and the parity is OK.
Goes low when digital in PLL is unlocked or the parity is not OK.

$\overline{\text{COMPLT}}$: Goes high when the internal traverse counter starts its count, and goes low when the set value is reached. Refer to "§11. Using the Traverse Counter."

$\overline{\text{COUNT}}$: Goes high when the internal traverse counter starts its count, and is toggled each time the set value is reached. The count then starts again. Refer to "§11. Using the Traverse Counter."

CLV LOCK: CLV lock status monitor. High: locked; low: unlocked. Output from both the LOCK pin and the SENS pin. Refer to "CLV lock status monitor" in "§1. Microcomputer Interface" ($83).

$\overline{\text{OV64}}$: Goes low when the disc rotation speed is 1/3 or less the prescribed level. Valid only for the pit sections of the disc; use the playback EFM signal (EFMI pin).

$91: ADIP address; valid only for the groove sections.

READ DATA	ADRS	DATA1	DATA2	DATA3	FLG
		D7 to D0	D7 to D0	D7 to D0	
ADIP	$91	MSB LSB SECTOR	MSB LSB CLUSTER L	MSB LSB CLUSTER H	ADIP CRCF

When the SYPL pin is low, the data is set in the read register at the falling edge of the ADSY signal. When the SYPL pin is high, the data is set at the rising edge of the signal.

FLG : ADIP CRCF

When high, ADIP CRCF is OK; when low, ADIP CRCF is not OK.

For the read data, refer to the previous page. Refer to "§9. ADIP Decoding."

$93 : "Digital in (the DIN pin) U bits. Categories are valid for CD or MD only.

READ DATA	ADRS	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7	DATA8	DATA9	DATA10		FLG
		D7 to D0	D7 to D0	D7 to D0	D7 to D0	D7 to D0	D7 to D0	D7 to D0	D7 to D0	D7 to D0	D7 to D0		
D. In-Ubit SubQ	$93	MSB LSB AFRAME	ASEC	AMIN	ZERO	FRAME	SEC	MIN	INDEX	TNO	CTRL	ADRS	SubQ CRCF

When the SYPL pin is low, the data is set in the read register at the falling edge of the DQSY signal.
When the SYPL pin is high, the data is set at the rising edge of the signal.

FLG : Sub Q CRCF

When high, CRCF is OK; when low, CRCF is not OK.

The read data differs depending on the category.
When the category is CD, the data is as shown in the above table.
When the category is MD, the data is all set to "0" except for INDEX and TNO.
Refer to "§10. Digital Audio Interface."

$94 : Digital in (DIN pin) C bits

READ DATA	ADRS	DATA1	DATA2	DATA3	DATA4	FLG
		D7 to D0	D7 to D0	D7 to D0	D7 to D0	
D. In-Cbit	$94	bit31 bit24	bit23 bit16	bit15 bit8	bit7 bit0	READ OK
		Channel status				

The data is set in the read register at the falling edge of the XLAT signal.

FLG: READ OK

When digital in PLL is locked and the parity is OK: high.
When digital in PLL is unlocked or the parity is not OK: low.

Of the "digital in" C bits, bits 0 to 31 can be read.
Refer to "§. Digital Audio Interface."

$95: Peak level detection of the audio data input from the DODT pin

READ DATA	ADRS	DATA1		DATA2	FLG
		D7	D6 to D0	D7 to D0	
PEAK-DATA	$95	L/$\overline{R}$	MSB bit8	bit7 LSB	READ OK
			PEAK DATA		

The data is set in the read register at the falling edge of the XLAT signal.

FLG: READ OK

Goes high at the falling edge of the XLAT signal.

When D7 = 1: left channel peak data. When D7 = 0: right channel peak data.
The peak level detection alternates between the left and right channels.
The peak level from the time address $95 is latched until the next time address $95 is latched is output.
Peak level detection is performed regardless of whether playback or recording is in progress.

$97 : Reading the Sub Q address in the pit sections

READ DATA	ADRS	DATA1	DATA2	DATA3	FLG
		D7 to D0	D7 to D0	D7 to D0	
Disc SubQ	$97	MSB LSB SECTOR	MSB LSB CLUSTER L	MSB LSB CLUSTER H	SubQ CRCF

When the SYPL pin is low, the data is set in the read register at the falling edge of the SQSY signal.
When the SYPL pin is high, the data is set at the rising edge of the signal.

FLG: Sub Q CRCF

When high, CRCF is OK; when low, CRCF is not OK.

Refer to "§8. Subcodes."

§2. Description of SENS Pin

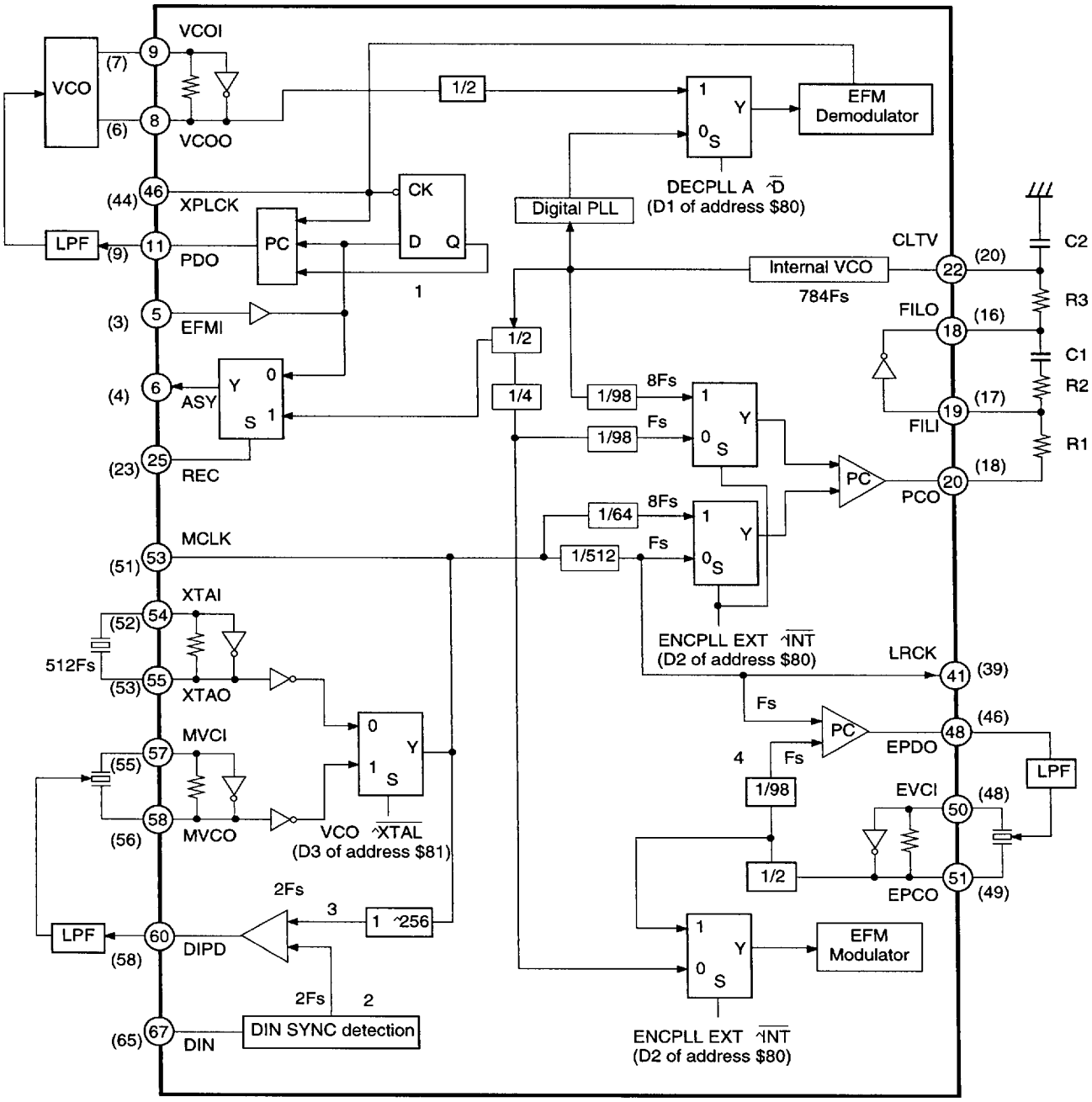
The SENS pin can be monitored simply by transferring the microcomputer interface address. Therefore, do not send the latch signal (the XLAT pin) and the transfer clock (the SCLK pin) from the point when the address of the SENS pin output to be monitored is sent until the point when the SENS pin output is monitored.
The SENS pin is high impedance except for the addresses shown in the following table.

ADRS	SENS pin output	Description
$80	GFS	High when the playback EFM frame sync was obtained with the correct timing. *1
$81	$\overline{OV64}$	Low when the disc rotation speed is 1/3 or less the prescribed level. Valid only for pit sections. *2
$82	$\overline{COUNT}$	High when the tracking counter starts a count; toggled each time the tracking counter reaches the set value. *3
$83	CLVLOCK	High when the spindle servo is locked; low when unlocked. *4
$88	$\overline{COMPLT}$	High when the tracking counter starts a count; low when the set value is reached. *3
$94	STID	High when the DAT start ID is input from the DIN pin. *5

*1) GFS: The GFS pin can be also monitored through D7 of microcomputer interface address $90.
*2) $\overline{OV64}$: Use the playback EFM signal (the EFMI pin). Can also be monitored through D1 of microcomputer interface address $90.
*3) $\overline{COUNT}$, $\overline{COMPLT}$: Can be also monitored through D3 and D4 of microcomputer interface address $90. Refer to "§11. Using the Traverse Counter."
*4) CLVLOCK: The LOCK pin can be also monitored through D2 of microcomputer interface address $90. Refer to "CLV lock status monitor" in "§1. Microcomputer Interface" ($83).
*5) STID: Read the channel status with the digital in C bits (microcomputer interface address $94), and then after confirming that the category is DAT, read STID from the SENS pin.

§3. PLL

§3-1. PLL Block Diagram



The numbers in circles are the QFP pin numbers, while the numbers in parentheses are the LQFP pin numbers.

A number in angle brackets (< >) indicates an internal signal of the IC. These numbers are used in the timing charts for the operation of the PDO, DIPD, and EPDO pins shown in §3-2.

The reference values for external circuits (R1 to R3, C1, and C2) are R1 = 3.3kΩ, R2 = 1.1kΩ, R3 = 1.2kΩ, C1 = 0.039μF, and C2 = 0.0027μF.

Because the internal VCO is always used for signal processing in the IC, the external circuits shown in the above diagram (R1 to R3, C1, and C2) are always required, regardless of the settings for recording, playback,

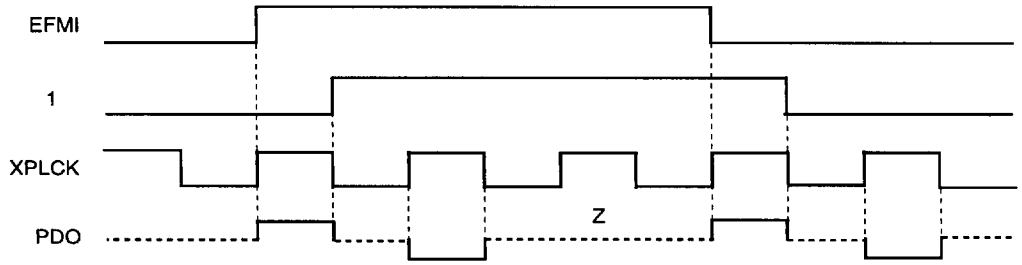
§3-2. PDO, DIPD, and EPDO Pin Operation

Note: The numbers in angle brackets (< >) in the timing charts indicate internal signals of the IC. Refer to "§3-1. PLL Block Diagram."

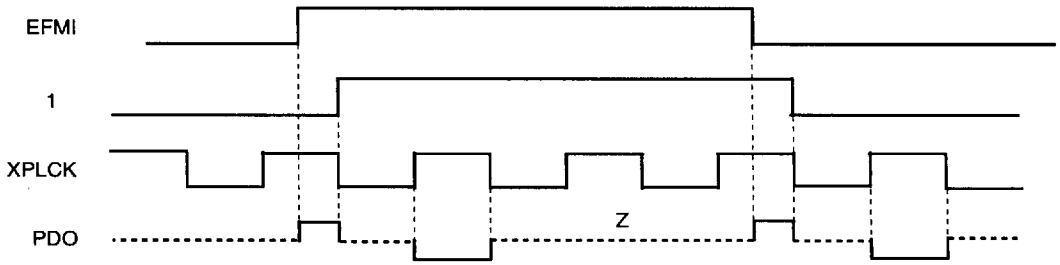
• PDO pin

Valid when decoder PLL = analog PLL (D1 of address $80 = 1)

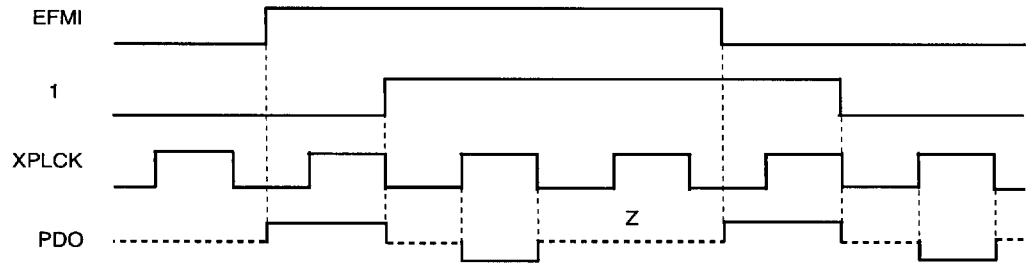
1) When the EFMI pin input signal is synchronized with the VCOI pin input signal



2) When the VCOI pin input signal has a higher frequency than the EFMI pin input signal

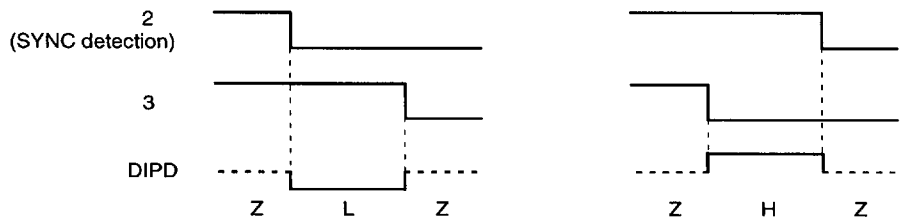


3) When the VCOI pin input signal has a lower frequency than the EFMI pin input signal



• DIPD pin

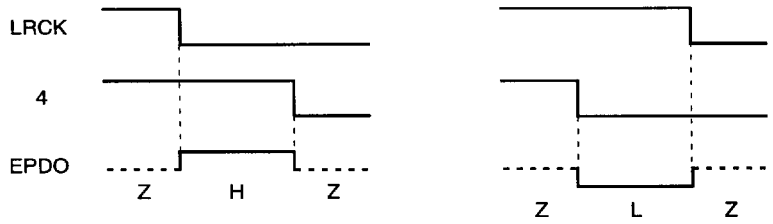
Valid when the master clock is the external VCO (D3 of address $81 = 1) of the digital in PLL



Note: The phase comparison frequency is 2Fs.

• EPDO pin

Valid when encoder PLL = external VCO (D2 of address $80 = 1).



Note: Phase comparison frequency is Fs.

§3-3. Channel Clock Regeneration by the Digital PLL Circuit

A channel clock is necessary in order to demodulate the EFM signal regenerated by the optical system. When T is the channel clock cycle, the EFM signal is modulated to an integer multiple of T from 3T to 11T. In order to read the information contained in the EFM signal, this integer value must be read correctly. Therefore, T, that is the channel clock is necessary.

PLL is needed to regenerate the channel clock because disparities in spindle rotation cause the EFM pulse width to change in an actual MD player.

The decoder digital PLL consists of a two-stage PLL.

The first-stage PLL generates the high-frequency clock (784Fs) required by the second-stage digital PLL.

The second-stage PLL is the digital PLL that regenerates the actual channel clock, and provides a capture range of approximately ±150kHz.

The digital PLL has a secondary loop, and is controlled by the primary loop (phase) and the secondary loop (frequency). When FLFC = 1, the secondary loop can be turned off. However, in this case the capture range becomes approximately ±50kHz.

Note: Refer to address $81 in "§1. Microcomputer Interface."

Due to imperfections in disc construction and other such factors, high-frequency components such as 3T, 4T, etc., may contain deviations. In such a case, turning the secondary loop off yields better playability.

FLFC setting example

Set FLFC as shown in 1 or 2 below, depending on the C1 and C2 error rate, system evaluation, etc.

1) When CLV is unlocked, FLFC = 0. When CLV is locked, FLFC = 1.
   For details on the CLV lock status monitor, refer to address $83 in "§1. Microcomputer Interface."
2) FLFC is always "0".

Note: Do not make that setting when the CLV is unlocked because the capture range is narrow when FLFC = 1.

§4. Frame Sync Protection

In MiniDisc, frame sync is recorded approximately every 136μs (7.35kHz).

Using this signal as a reference, what data is determined within a given frame. Conversely, if frame sync can not be recognized, the data is processed as error data because it is not recognized that what the data is.

As a result, proper recognition of frame sync is extremely important for excellent playability.

Window protection, forward protection and backward protection are used for frame sync protection in this IC. By adopting these, this IC has been provided with powerful frame sync protection capabilities.

• Window

The window is provided in order to prevent incorrect detection of the sync pattern.

During playback, the window operates approximately 136µs after frame detection. Only those sync signals detected within the window are valid; sync signals outside of the window are invalid.

In reality, the sync cycle fluctuates due to rotational disturbances, etc. Therefore, the window is wide enough to allow a little leeway in regards to the exact timing (approximately 136µs after). The window width can be selected for either cases where such rotational disturbances are small or when they are large.

When rotational disturbances are small	WSEL = 0: window ±6 clocks
When rotational disturbances are large	WSEL = 1: window ±26 clocks

When WSEL = 0, the possibility of incorrect sync detection is small.

When WSEL = 1, resistance to rotational disturbances (anti-rolling characteristics) is enhanced.

Note: Refer to D6 (WSEL) of address $80 in "§1. Microcomputer Interface."

• Forward protection

In cases where sync was being detected normally (within the window) but now cannot be detected due to a scratch on the disc or for a similar reason, sync signals are inserted for up to 13 frames. If sync could still not be detected within those inserted frames, window operation is halted and any sync signal with any timing becomes valid (resynchronization).

Although the number of frames can be selected to be either 13 or 4, 13 frames (GSEL = 0) are recommended since the larger number of insertion frames provides better playability.

Note: Refer to D7 (GSEL) of address $80 in "§1. Microcomputer Interface."

• Backward protection

When sync could not be detected during the forward protection insertion frames, window operation halts. However, if sync is detected window operation starts. If correct sync cannot be detected within three frames (within the window), window operation halts again and the resynchronization process is made.

§5. Error Correction

In the MiniDisc format, each piece of data (8 bits) is included in two error correction codes, C1 and C2. In C1 correction, the code is created from 28 bytes of information and four C1 parity bytes. In C2 correction, the code is created from 24 bytes of information and four C2 parity bytes. Both C1 and C2 are Reed Solomon code with a minimum distance of 5.

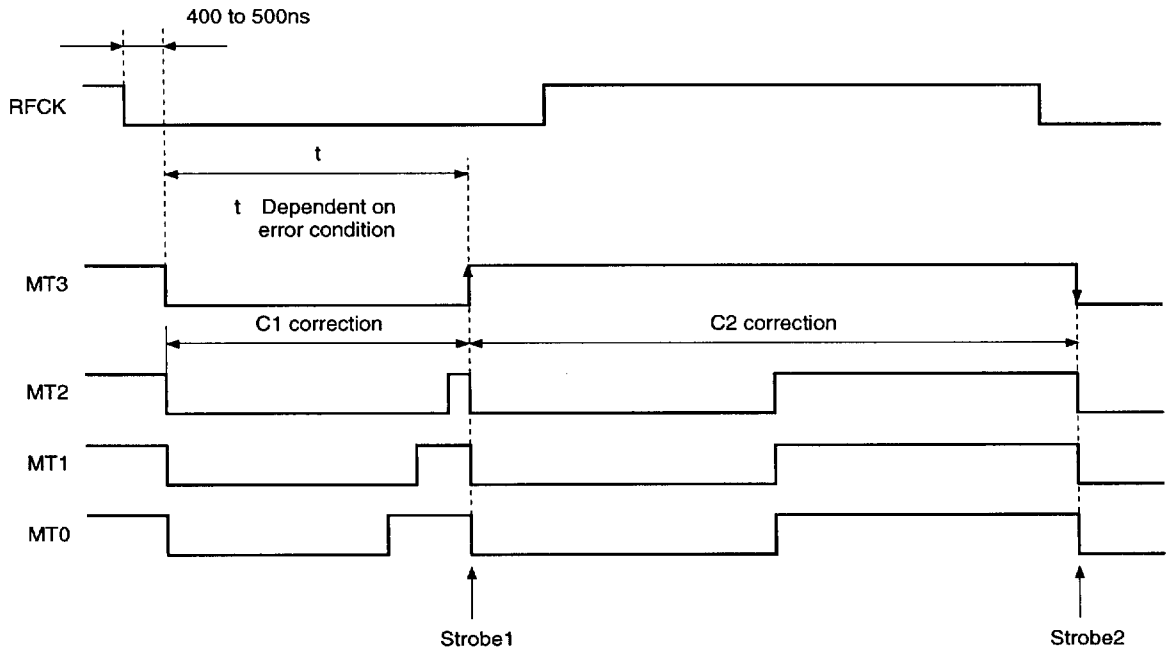
This IC implements double correction in C1 correction and quadruple correction in C2 correction (when D2 of address $81 in the microcomputer interface = 0) using a refined superstrategy . In addition, in order to prevent improper C2 error corrections, a C1 pointer is added for data after C1 correction in accordance with the C1 error status during C1 correction, the EFM signal regeneration status, and the player operating status.

MT3	MT2	MT1	MT0	Explanation	
0	0	0	0	C1: no errors	C1 pointer reset
0	0	0	1	C1: 1 error corrected	C1 pointer reset
0	0	1	0	*	
0	0	1	1	*	
0	1	0	0	C1: no errors	C1 pointer set
0	1	0	1	C1: 1 error corrected	C1 pointer set
0	1	1	0	C1: 2 errors corrected	C1 pointer set
0	1	1	1	C1: correction impossible	C1 pointer set
1	0	0	0	C2: no errors	C2: pointer reset
1	0	0	1	C2: 1 error corrected	C2 pointer reset
1	0	1	0	C2: 2 errors corrected	C2 pointer reset
1	0	1	1	C2: 3 errors corrected	C2 pointer reset
1	1	0	0	C2: 4 errors corrected	C2 pointer reset
1	1	0	1	C2: correction impossible	C1 pointer copied
1	1	1	0	C2: correction impossible	C2 pointer set
1	1	1	1	*	

Error Monitor Output Data

Note 1: There are a total of 13 error correction states. The four bits MT3 to MT0 are assigned to the expression of these states. The asterisks in the above table indicate that monitor data is not output.

Note 2: Valid only during playback. Error correction monitoring is not performed during recording.



Error Monitor Output Timing Example

- Monitoring method

  When the MT3 pin rises, the C1 correction status is output to the MT2 to MT0 pins.
  (Strobe 1)
  When the MT3 pin falls, the C2 correction status is output to the MT2 to MT0 pins.
  (Strobe 2)

  Note: The MT3 to MT0 change at roughly the same times because they operate according to a common internal clock. Therefore, when monitoring them, delay the MT2 to MT0 pins with R or C, and then latch the MT2 to MT0 pins at the rising or falling edge of MT3.

§6. Setting of Recording and Playback Modes

Mode	REC pin	VCO/$\overline{\text{XTAL}}$*
Playback	0	0
Analog REC	1	0
Digital REC	1	1

* Refer to D3 of address $81 in "§1. Microcomputer Interface."

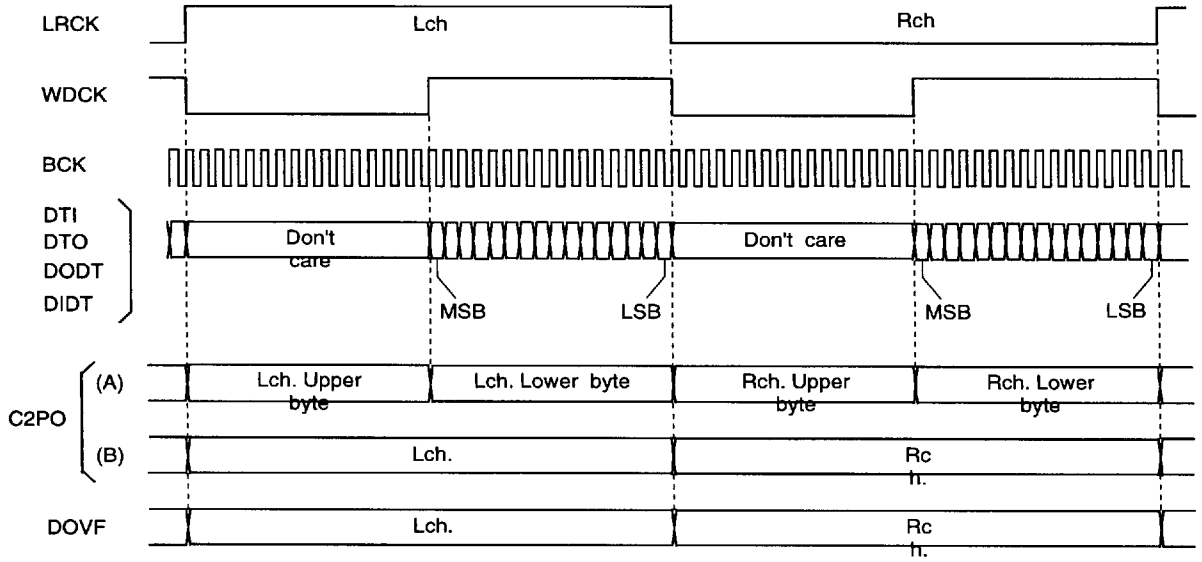
§7. Audio Interface

This interface includes 64 BCK clocks within one LRCK clock; the data (Note) format is MSB first, rearward truncation.

Note: The DTI, DTO, DODT, and DIDT pins. Refer to the timing chart shown below.

The output method of the C2PO pin differs for recording and playback. Refer to the timing chart and the table shown below.

• Audio Interface Timing Chart



Mode	C2PO	
	Contents	Output Timing
Playback	C2 pointer for playback data*	Refer to diagram above (A)
Analog REC	Always 0	—
Digital REC	Digital in V bits	Refer to diagram above (B)

Relationship between C2PO and Recording and Playback Modes

* When C2PO pin is high, error correction cannot be performed on that data.

§8. Subcodes

Subcode processing is different for recording and playback.

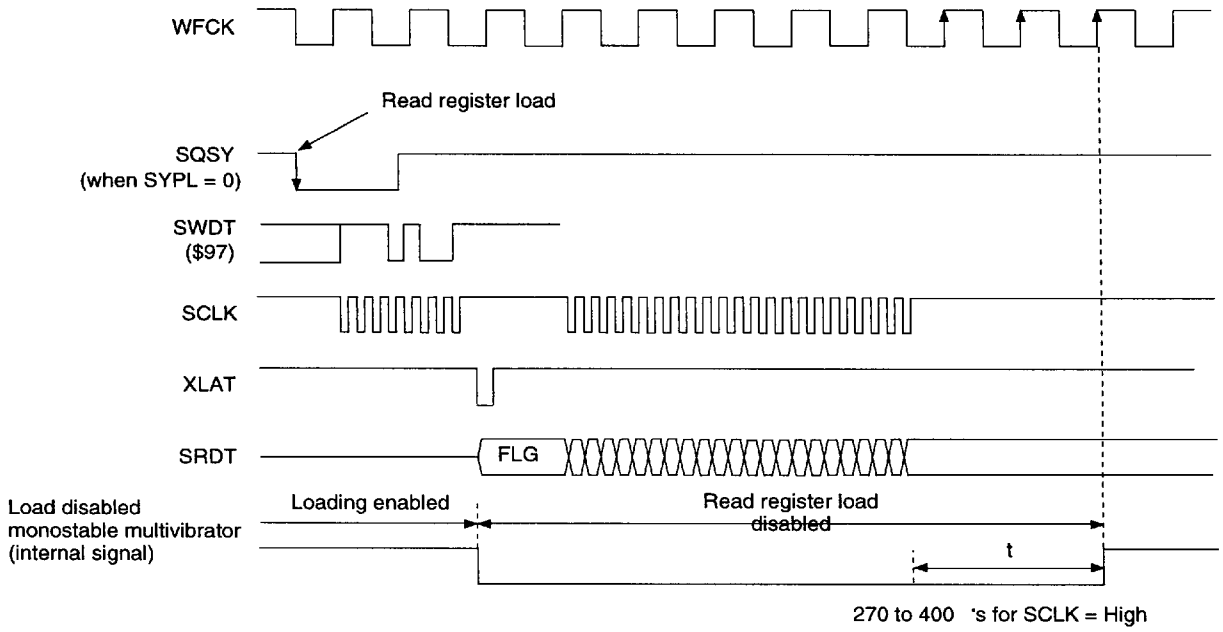
§8-1. During Playback

Sub Q is read from the disc. It is valid only for the pit sections of the disc.

In the MD format, the subcodes associated with he conventional CD format are used only for the pit sections of the disc. Moreover, aside from Sub Q, all subcodes (P, R, S, T, U, V, and W) are "0".

In this IC, after the 96-bit CRC check of Sub Q, a total of 24 bits for CLUSTER and SECTOR can be read through address $97 of the microcomputer interface. After being latched (at the falling edge of the XLAT pin), the CRC check results are output from the SRDT pin as a flag. If the flag is OK, the 24 bits of data are set in the internal read register at the front edge of the SQSY signal. In addition, clock input is detected, the retriggerable-type monostable multivibrator (time constant = 270 to 400µs) is triggered, and while a read is performed for a period shorter than the time constant, the read register is protected from being overwritten. A read should be paused for 270µs or less.

Ex.) The chart below shows that even though SCLK is temporarily halted due to microcomputer interrupt processing, the data in the internal register cannot be overwritten for a period of 270 to 400µs.



Disc Sub Q Read Timing

§8-2. During recording

Sub Q is written to the disc.

During recording, the EFM signal is written to the disc, but it is necessary to set all of the subcodes to "0" through address $8B of the microcomputer interface.

In this IC, the 80-bit register for Sub Q is also used for the digital out U bit register during playback, so that the Sub Q 80-bit register should be set to all "0" once at the start of recording.

§9. ADIP Decoding

The ADIP FM signal recorded by a recordable disc groove wobble is demodulated and the clock is regenerated by the CXA1380, and the FM signal is then input to the FMDT and FMCK pins. In this IC, bi-phase demodulation and ADIP decoding are performed, followed by an ADIP CRC check. After latching microcomputer interface address $91 (at the falling edge of XLAT), the ADIP CRC check results are output from the SRDT pin as a flag. If the flag is OK, the 24 bits of ADIP data are read.

Although loading of the data into the read register is performed at the front edge of the ADSY pin, it is still loaded even if the flag is not OK; do not read the ADIP data in this case. In addition, unlike with Sub Q, read register loading is not prohibited during the read, so avoid timing that would permit ADSY to be active during a read. If the ADIP sync pattern does not arrive within the window two times in a row, the window is released and sync detection is performed. Even if sync is not detected, sync signals are output from the ADSY pin according to the insertion timing. In addition, the read register is also loaded in this case.

§10. Digital Audio Interface

§10-1. Digital Out

Although the digital out is output from the DOUT pin, the data that is output differs according to the mode. Refer to the table shown below.

Mode	DOUT pin output				
	16-bit audio data	Vbit	Ubit	Cbit	Parity
Playback	Data input from the DODT pin	Data input from the DOVF pin	Written through the microcomputer interface		Generated in the IC
Analog REC			All "0"		
Digital REC	Signal input from the DIN pin is output as is				

Relationship between Mode and DOUT Pin Output

- C bits

  During playback and analog recording, the C bits must be set through the microcomputer interface. In setting, write to $89 according to the channel status type II, form I of the digital audio interface. Bits 16 and beyond are all automatically set to "0". Set the CONTROL and L bit according to the serial copy management system (SCMS). (Refer to the Rainbow Book.)

  During digital recording, the signal input from the DIN pin is output as is to the DOUT pin, so there is no need to set the C bits.

bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7	bit8	bit9	bit10	bit11	bit12	bit13	bit14	bit15
0	CONTROL					0	0	Category code							L bit
	Music/data	Copy bit	Emphasis	0	0										

→ Emphasis (1 = On, 0 = Off)
→ Copy bit ("0" = with Copy right)
→ Music/data ("0" = Music)

Mode	Source	Category code						
		bit8	bit9	bit10	bit11	bit12	bit13	bit14
Playback	MD	1	0	0	1	0	0	1
Analog REC	Actual A/D	0	1	1	0	0	×	×

C Bit Settings by the Microcomputer Interface ($89)

Note: Refer to EIAJ CP1201 for details on category code bits 13 and 14 during analog recording.

• U bits

During playback, subcodes are output from the DOUT pin as U bits in accordance with the MD format. Therefore, write to Sub Q through address $8B of the microcomputer interface. The contents to be written is TNO and INDEX; "0" is for data 1 to 6 and data 10. (Refer to the Rainbow Book.) CRC is generated within the IC. P and R through W are all set to "0". The written data is hold and output so that only TNO should be rewritten at the beginning of each tune during playback.

However, during recording, because Sub Q is written as all "0" in address $8B of the microcomputer interface, after recording it is necessary (for playback) to rewrite Sub Q. (note)

Note: In this IC, the U bit register used for playback is the same register as the one used as the Sub Q register for recording.

During analog recording, all U bits are automatically set to "0".

During digital recording, the signal input from the DIN pin is output as is from the DOUT pin, so there is no need to set the U bits.

§10-2. Digital In

During digital recording, the master clock is switched from a clock of the XTAI pin input to a PLL system synchronized with the digital in signal input from the DIN pin. Set D3 (VCO/$\overline{\text{XTAL}}$) of address $81 of the microcomputer interface to "1". The PLL lock status can be monitored through D5 (DINPLL LOCK) in address $90 of the microcomputer interface. When high, PLL is locked.

Of the digital in signals input from the DIN pin, the audio data is output from the DIDT pin in an MSB first, rearward truncation format, while the Vbits are output from the C2PO pin. Refer to"§7. Audio Interface." The C bits can be read for 32 bits (bit 0 to bit 31) in address $94 of the microcomputer interface.

When the category code in the C bits is CD or MD, the Sub Q of the U bit can be read for 80 bits in address $93 of the microcomputer interface. In this case, the results of the CRC check are output as a flag (Sub Q CRC). In addition, just as when reading disc Sub Q in address $97 of the microcomputer interface, data will not be overwritten during the read if the read is done in a period of 270µs or less. Refer to "§8. Subcodes."

When the category code in the C bits is DAT, STID is output from the SENS pin in address $94 of the microcomputer interface. When STID arrives, the SENS pin outputs a high signal. Refer to "§2. Description of the SENS Pin."

§11. Using the Traverse Counter

When performing a large track jump or a sled move, the traverse counter can be used to count the number of tracks crossed. The falling edges of the pulses input to the CNIN pin are counted as the number of tracks crossed.

A 16-bit counter is used in this IC, so that a maximum of 65,535 tracks can be counted for one time. Also, there are two methods of counting: once count mode and continuous count mode.

§11-1. Setting the Number of Tracks Counted

Set the number of tracks in address $88 of the microcomputer interface.

§11-2. Counter Operation

- Once count mode

  After setting the number of tracks, transfer address $88 of the microcomputer interface. The count starts once the latch signal is sent. There is no need to send data. When the counter reaches the set value, the count stops.

- Continuous count mode

  After setting the number of tracks, transfer data = 00 and address $82. The count starts once the latch signal is sent. When the counter reaches the set value, the counter is reset and the count starts again.

§11-3. Monitoring the Counter

There are two methods for monitoring the counter: using the microcomputer interface and using the SENS pin. After the count starts, the count continues even if other addresses of the microcomputer interface are used. When monitoring via the SENS pin, send only the address; do not send the latch signal.

- Once count mode (monitor signal name = $\overline{\text{COMPLT}}$)

  Either read D4 in address $90 of the microcomputer interface, or else monitor the SENS pin after transferring only address $88. D4 of address $90 and the SENS pin both go high at the start of the count, and both go low when the count ends.

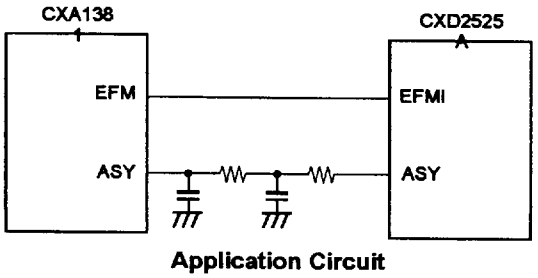
- Continuous count mode (monitor signal name = $\overline{\text{COUNT}}$)

  Either read D3 in address $90 of the microcomputer interface, or else monitor the SENS pin after transferring only address $82. D3 of address $90 and the SENS pin both go high at the start of the count, and both are inverted each time the counter resets.

§12. Asymmetry Compensation

An application circuit for asymmetry compensation is shown below.

Note: Refer to the CXA1381 specifications.



Application Circuit

§13. Reset Timing during Power On

After turning the power supply on and at least ten pulses of the master clock have been input to the XTAI pin, the XRST pin switches from low to high.

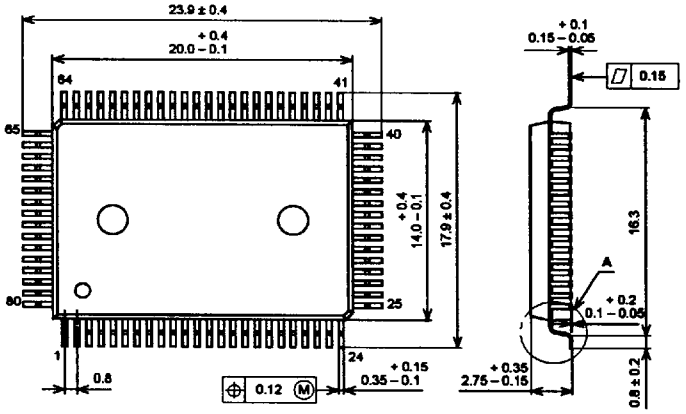
Note: In order to execute a reset when the XRST pin is low, at least 10 pulses of the master clock must be input to the XTAI pin.

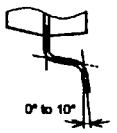
§14. Note on Power On/Off

V_{DD} and AV_{DD} should turned on and off simultaneously. If they are not simultaneous, a latchup may occur.

Package Outline Unit: mm

80PIN QFP (PLASTIC)





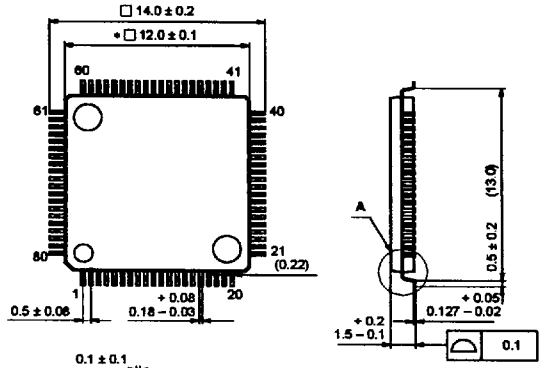
DETAIL A

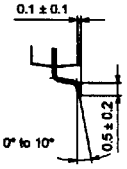
SONY CODE	QFP-80P-L01
EIAJ CODE	*QFP080-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g

80PIN LQFP (PLASTIC)





NOTE: Dimension "*" does not include mold protrusion.

DETAIL A

SONY CODE	LQFP-80P-L01
EIAJ CODE	*QFP080-P-1212-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g