SONY **CXD2550P**

Digital Filter for CD

Description

CXD2550P is a digital filter LSI with 4-times/8-times over sampling rate, developed for compact disc player.

Features

- Provide a 4-times/8-times sampling digital filter.
- Filter characteristics
  ripple within 0.05dB
  attenuation below −40dB
- De-emphasis function
- Attenuate function (Built-in 1st noise shaping)
- I/O Format
  Input: 2's complement MSB first (serial)
  Output: 2's complement MSB first (serial)
  (16 bit slot, 18 bit slot selection possible)

Application

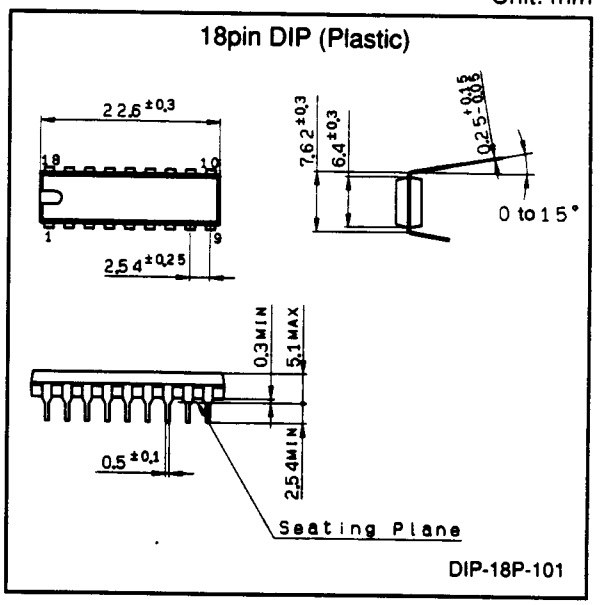
Compact disc player

Structure

Silicon gate CMOS IC

Package Outline

Unit: mm



Absolute Maximun Ratings (Ta= −20 to +75°C)

• Supply voltage	V_{DD}	−0.5 to +6.5	V
• Input voltage	V_I	−0.5 to V_{DD} +0.5	V
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	500	mW (Ta=75°C)

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	−20 to +75	°C
• OSC frequency	fx	10 to 20	MHz (duty 50 ±10%)

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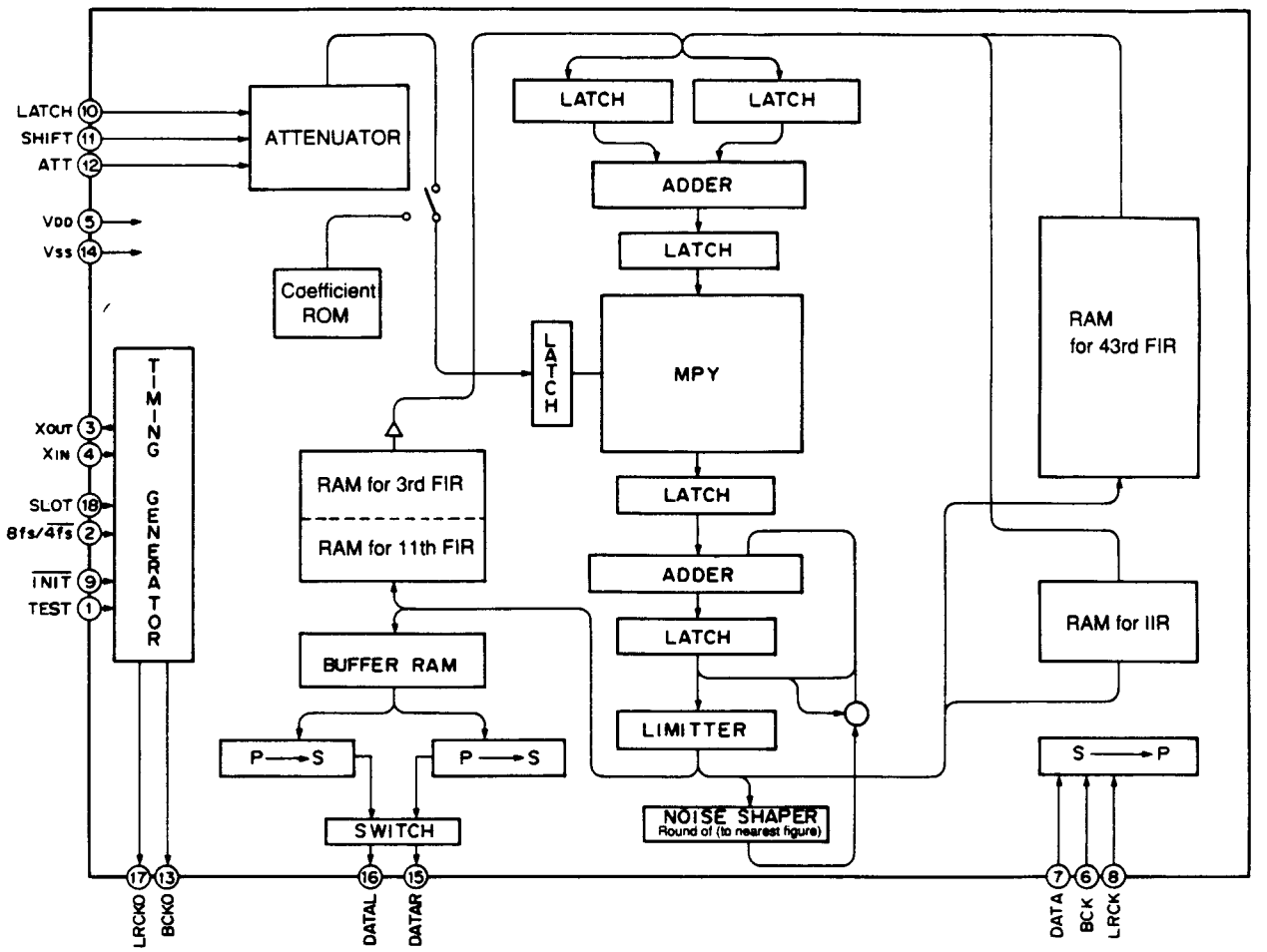
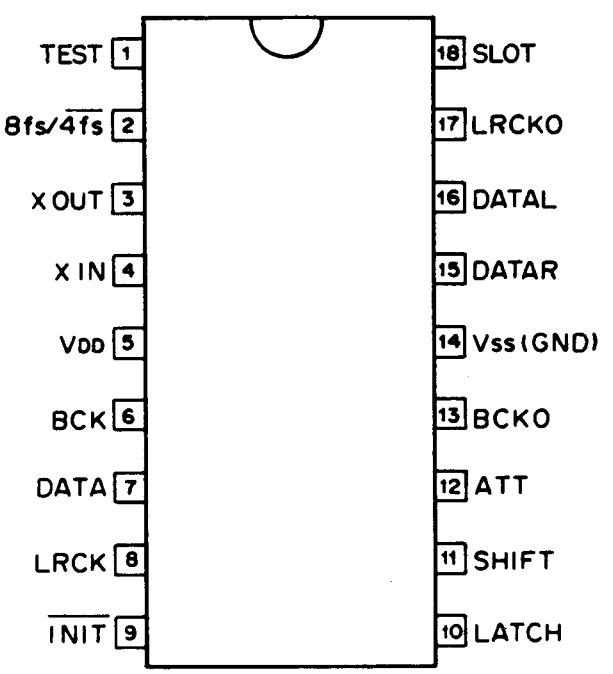
Block Diagram



Pin Configuration (Top View)



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Pin Description

No.	Symbol	I/O	Description
1	TEST	I	Test pin. For normal usage, fixed to 'L'
2	8fs/$\overline{4fs}$	I	FIR 3 selection, at 'H' 8fs at 'L' 4fs
3	X OUT	O	Master clock output (f=384fs)
4	X IN	I	Master clock input (f=384fs)
5	V_{DD}	—	+ Supply (5V)
6	BCK	I	BCK input
7	DATA	I	Serial data input (2's complement)
8	LRCK	I	LRCK input
9	$\overline{INIT}$	I	Resync with the rise of this signal
10	LATCH	I	Latch CLK input
11	SHIFT	I	Shift CLK input
12	ATT	I	Attenuate data input
13	BCKO	O	BCK output
14	Vss (GND)	—	- Supply (0V)
15	DATAR	O	At 4fs: WCK output At 8fs: RCH serial data output (2's complement)
16	DATAL	O	At 4fs: LCH, RCH Time-shared serial data output (2's complement) At 8fs: LCH serial data output (2's complement)
17	LRCKO	O	LRCK output
18	SLOT	I	Output slot selection at 'H' 18 bit slot at 'L' 16 bit slot

***Note)** TEST, 8fs/$\overline{4fs}$, SLOT pins: Pull down

Electrical characteristics

DC characteristics

V_{DD}=4.5 to 5.5 V, Ta=−20 to +75°C

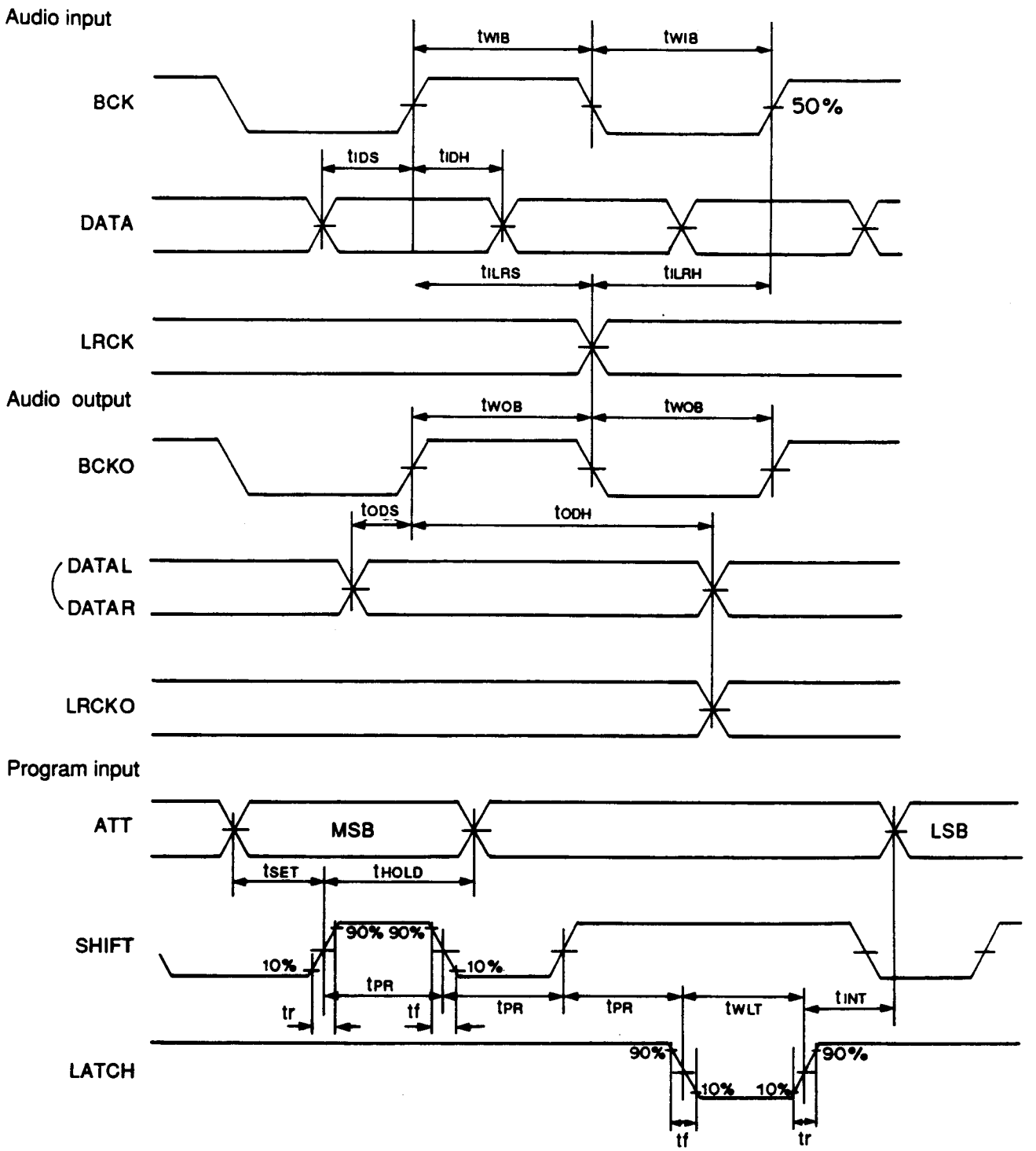
No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
All inputs except 4 XIN	Input capacitance	C_{IN}	———	—	3	5	pF
1, 2, 6, 7, 8, 9, 10, 11, 12, 18	'H' input voltage	V_{IN}	———	0.76V_{DD}	—	—	V
	'L' input voltage	V_{IL}	———	—	—	0.24V_{DD}	
6, 7, 8, 9, 10, 11, 12	Input leak current 1	I_{ILK1}	V_I=V_{DD}/0V	−5	—	5	μA
1, 2, 18	Pull down resistance	R_{PD}	———	7.5	15	30	KΩ
	'L' input leak current	I_{IL}	V_I=0V	—	—	5	μA
4	Input leak current 2	I_{ILK2}	V_I=V_{DD}/0V	−20	—	20	
13, 15, 16 ,17	'H' output voltage	V_{OH}	I_D=−4mA	V_{DD}-0.5	—	—	V
	'L' output voltage	V_{OL}	I_D=4mA	—	—	0.4	
	Consumption current	I_{DD}	No load V_I=V_{DD}/0V fx=16.9344MHz	—	—	40	mA

AC characteristics

V_{DD}=4.5 to 5.5 V, Ta=−20 to +75°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	fx	———	10	16.9344	20	MHz
Input BCK frequency	f_{BCK}		—	—	4.0	
Input BCK pulse width	t_{WIB}	———	100	—	—	ns
Input data set up time	t_{IDS}	———	20	—	—	
Input data hold time	t_{IDH}	———	20	—	—	
Input LRCK set up time	t_{ILRS}	———	50	—	—	
Input LRCK hold time	t_{ILRH}	———	50	—	—	
Output BCKO pulse width	t_{WOB}	8fs	40	—	—	
Output data set up time	t_{ODS}	fx=16.9344MHz	25	—	—	
Output data hold time	t_{ODH}	Cl=50pF	25	—	—	
Program input base time	t_{PR}	fx=16.9344MHz	250	—	—	
Latch input pulse width	t_{WLT}		500	—	—	
Rise time (SHIFT, LATCH)	tr		—	—	200	ns
Fall time (SHIFT, LATCH)	tf		—	—	200	
Set up time (ATT)	t_{SET}	———	500	—	—	
Hold time (ATT)	t_{HOLD}		500	—	—	
Interval (ATT)	t_{INT}		1000	—	—	

Timing Chart



Functions

1. Soft muting

The soft mute function mutes or demutes output data on the basis of a muting time of 1024/fs (fs=44.1kHz on CD).

2. Digital attenuator

The data trasferred from an external attenuator may be used to attenuate the output data. The ATT data comprises 8 bits. The D7 is the digital de-emphasis control bit, whereas the D6 through D0 constitute attenuator data.

1) Command and audio output
The attenuator data is in 7 bits, allowing selection of 127 different settings. The relation between a command and output is shown in the following table.

Attenuator data D_6 to D_0	Audio output
7F(H)	0 dB
7E(H) | 01(H)	−0.13 dB | −42.144 dB
00(H)	−∞

An attenuator value between 01(H) and 7E(H) can be given by the following equation.

$$ATT=20 \log \left[\frac{\text{Input data}}{128} \right] dB$$

Example)Suppose that the attenuator data is 7A.

$$ATT=20 \log \left[\frac{122}{128} \right] dB=-0.417dB$$

3. I/O synchronizing circuit

1) Theory of operation
The synchronizing cuircuit opens a window for six internal system clocks, CK2(fx/4) to monitor whether the differentiated signal of the rise of LRCK (LRCK $\int$) that may be input exists in it. If the LRCK is out of the window when the power supply is turned on, the synchronizing circuit holds the CK2 at the time it is in the center of the window, and lets it start as soon as the next LRCK $\int$ arrives. This operation synchronizes an external system and this IC and lines up the phases of serial input data.

2) Resynchronization by INIT
If the LRCK $\int$ is in the window when the power supply is turned ON, a fluctuation of LRCK could cause desynchronization during operation of the IC (particularly when it is either end of the window).
For this reason, resynchronization must always be achieved after the power supply has been turned ON. The operation for resynchronization is performed at the time the INIT rises. The operation initializes the synchronizing circuit to cause a temporary desynchronization and then achieves resynchronization, there by positioning the LRCK $\int$ in the center of the window.

4. Attenuator operation

Suppose that there are pieces of attenuator data ATT1, ATT2 and ATT3 and that ATT1> ATT3> ATT2 and that the piece of attenuator data ATT1 is transferred first and ATT2 transferred next. If ATT2 is transferred before the value of ATT1 is reached (during the state of A in Fig.1), the attenuation directly approaches the value of ATT2. If ATT3 is transferred before the value of ATT2 is reached (during the state of B or C in Fig.1) ,the attenuation is carried on from the value at the time(B or C) to approach the value of ATT3. Transition from one piece of attenuator data to another is the same as in the case of soft muting.

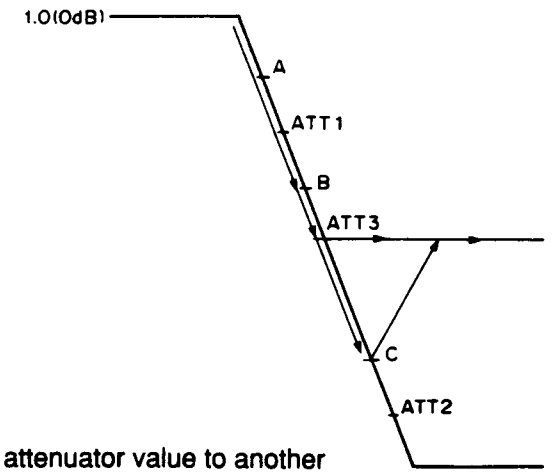


Fig.1 Transition from one attenuator value to another

5. Input data timing

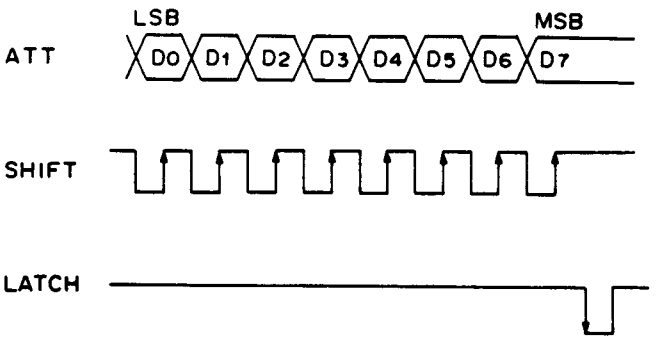


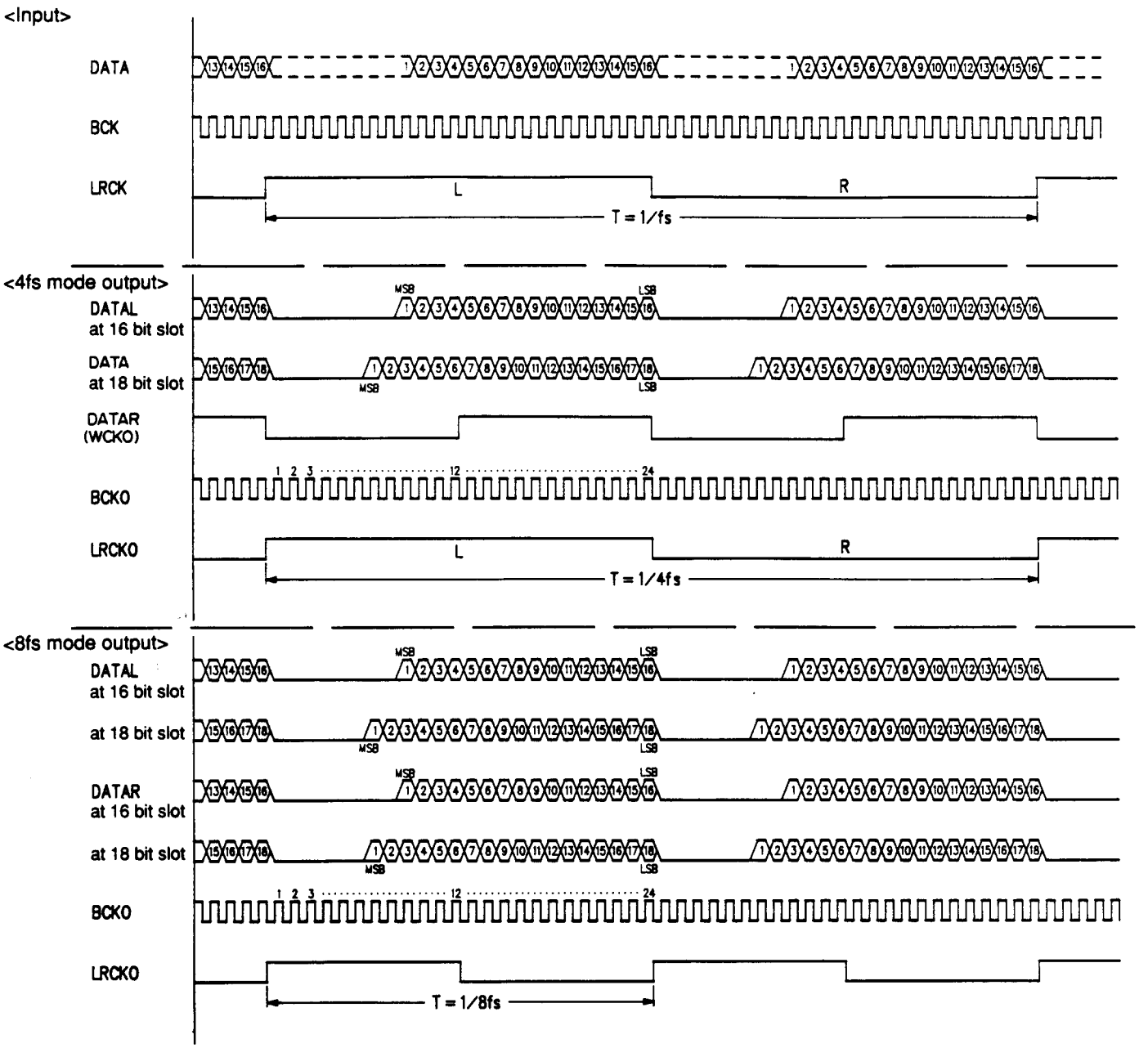
Fig.2 Timing of ATT, SHIFT and LATCH

1) The ATT data is LSB first.
2) About the ATT data
   D_7: Digital de-emphasis control bit
   H: De-emphasis ON
   L: De-emphasis OFF
   Note that the time constants of emphasis are $\tau1$=50μs and $\tau2$=15μs at fs=44.1kHz
   D_0 to D_6: Attenuator data

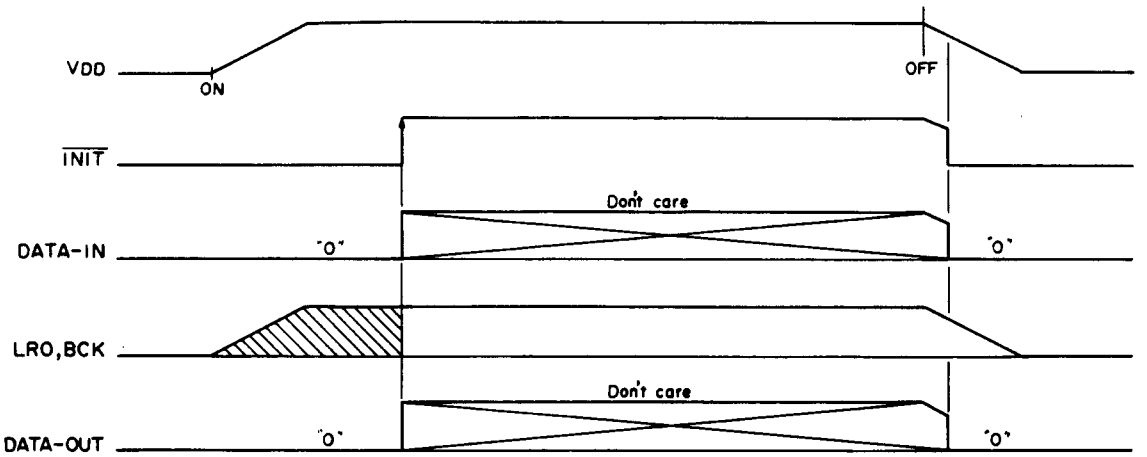
6. $\overline{\text{INIT}}$ pin

After $\overline{\text{INIT}}\downarrow$, the counters and registers for the attenuators in the IC are reset to all 0s(muted state). After $\overline{\text{INIT}}\downarrow$, therefore, a proper value(7F(H) (Full scale) for example) should be trasferred from the microcomputer to the ATT pins.

I/O Timing


<Input>
DATA
BCK
LRCK
L
R
T = 1/fs
<4fs mode output>
DATAL
at 16 bit slot
DATA
at 18 bit slot
DATAR
(WCKO)
BCKO
LRCKO
MSB
LSB
T = 1/4fs
<8fs mode output>
DATAL
at 16 bit slot
at 18 bit slot
DATAR
at 16 bit slot
at 18 bit slot
BCKO
LRCKO
T = 1/8fs

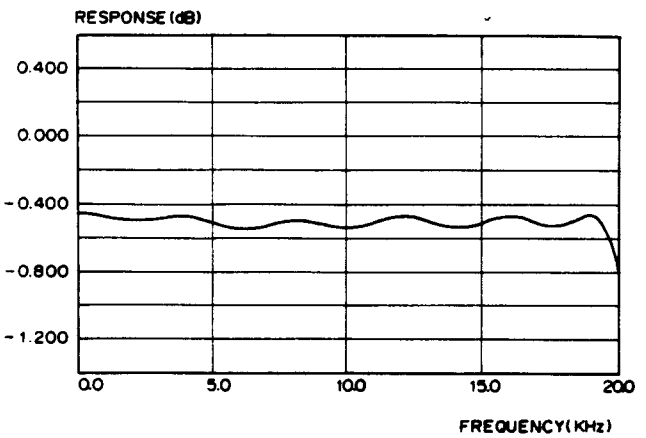
Operation at power ON/OFF



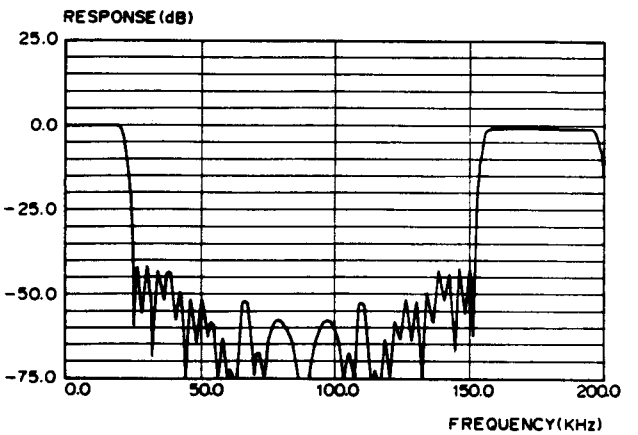
Filter Characteristics

Quadrupled over sampling mode

Frequency characteristics 1(Pass band)

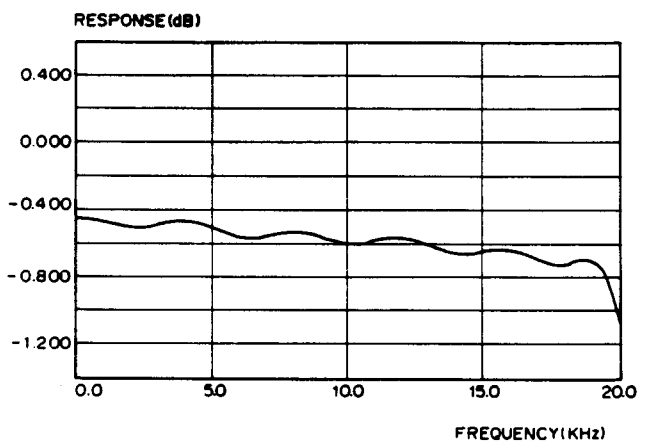


Frequency characteristics 2(Stop band)

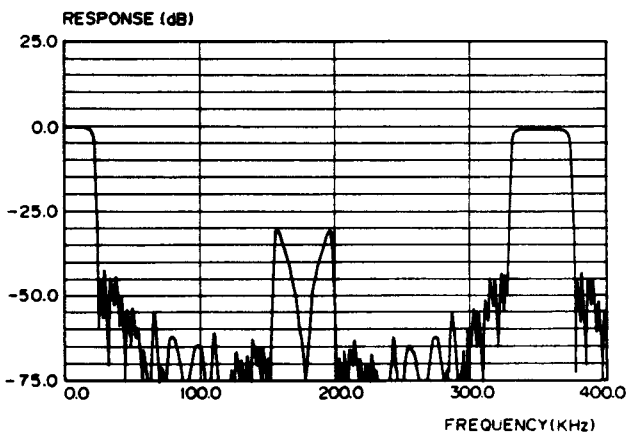


Octupled over sampling mode

Filter characteristics 1(Pass band)

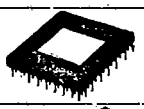
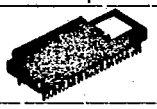


Filter characteristics 2(Stop band)



T-90-20

Sony Package Product Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	4-direction
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT PACKAGE		P	1.0mm 0.8mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull Wing	2-direction
	Standard chip carrier	PLCC	PLASTIC LEADED CHIP CARRIER		P	1.27mm (50MIL)	J-bend	4-direction
		LCC	LEAD LESS CHIP CARRIER		C	1.27mm (50MIL)	Lead less	Package side
	Shrink chip carrier	SPLCC (PLCC)	SHRINK PLASTIC LEADED CHIP CARRIER		P	1.27mm Max. (50MIL Max.)	J-bend	4-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEAD PACKAGE		P	1.27mm (50MIL)	J-bend	2-direction

*P……Plastic, C……Ceramic