

**SONY®****CXD2551M/P****Digital Filter for CD****Description**

The CXD2551M/P is a 4- and 8-times oversampling digital filter LSI for a compact disc player.

**Features**

- A 4- and 8-times digital filter
- Filter characteristics
  - Ripple:  $\pm 0.05$  dB or less
  - Attenuation:  $-40$  dB or less
- De-emphasis function
- Attenuating function (Built-in 1st noise shaper)
- Digital offset function
- I/O format
  - Input: 2's complement MSB first (serial)
  - Output: 2's complement MSB first (serial)
  - (16- or 18-bit slot selectable)

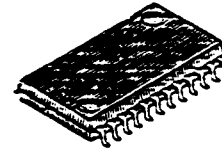
**Applications**

Compact disc player

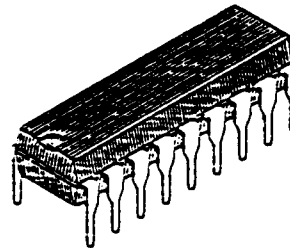
**Structure**

Silicon gate CMOS IC

CXD2551M 24 pin SOP (Plastic)



CXD2551P 18 pin DIP (Plastic)

**Absolute Maximum Ratings (Ta = -20 to +75°C)**

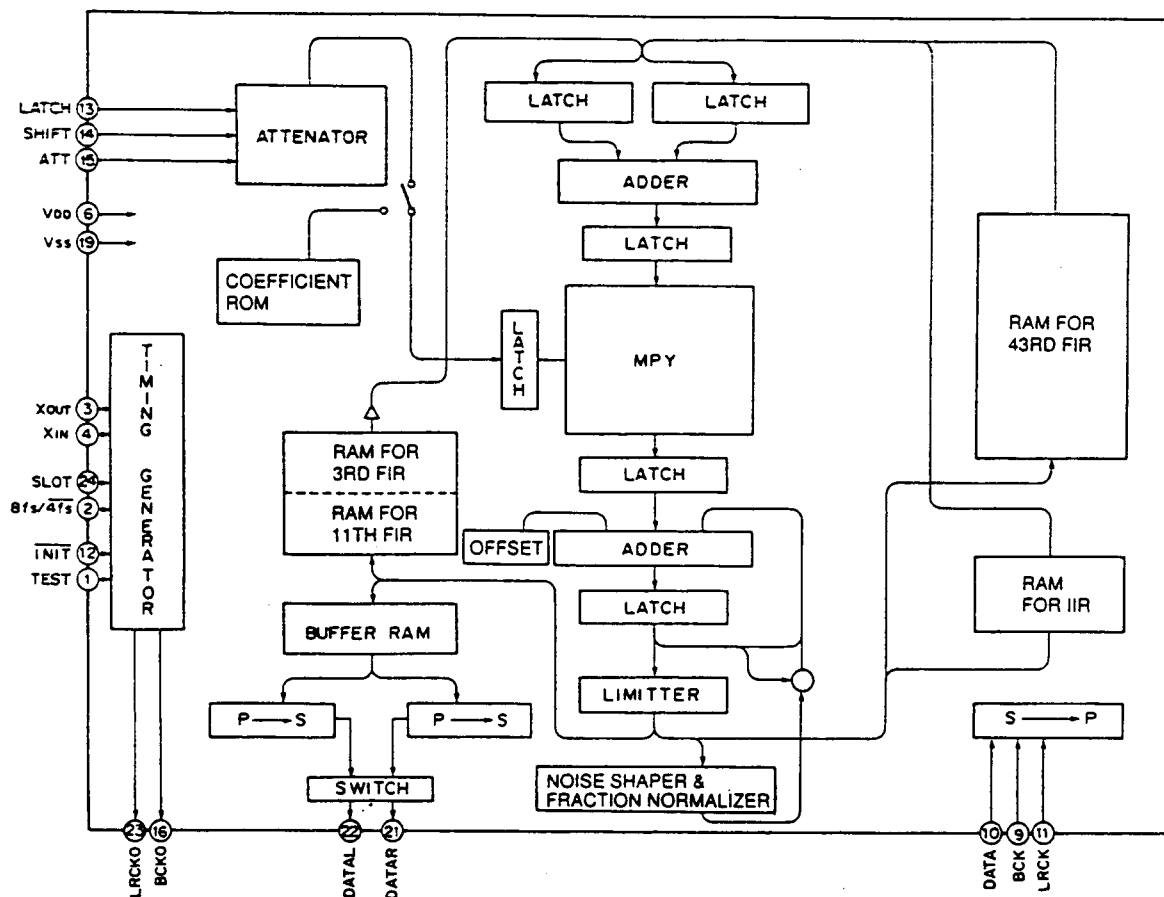
- |                               |          |                        |                |
|-------------------------------|----------|------------------------|----------------|
| • Supply voltage              | $V_{DD}$ | -0.5 to +6.5           | V              |
| • Input voltage               | $V_I$    | -0.5 to $V_{DD} + 0.5$ | V              |
| • Allowable power dissipation | $P_D$    | 500                    | mW (Ta = 75°C) |
| • Storage temperature         | Tstg     | -55 to +150            | °C             |

**Recommended Operating Conditions**

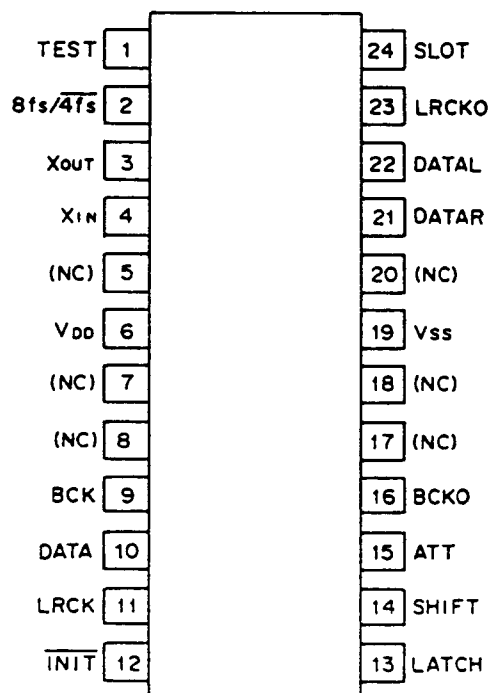
- |                         |          |            |                         |
|-------------------------|----------|------------|-------------------------|
| • Supply voltage        | $V_{DD}$ | 4.5 to 5.5 | V                       |
| • Operating temperature | Topr     | -20 to +75 | °C                      |
| • OSC frequency         | fx       | 10 to 20   | MHz (Duty 50 $\pm$ 10%) |

CXD2551M

Block Diagram

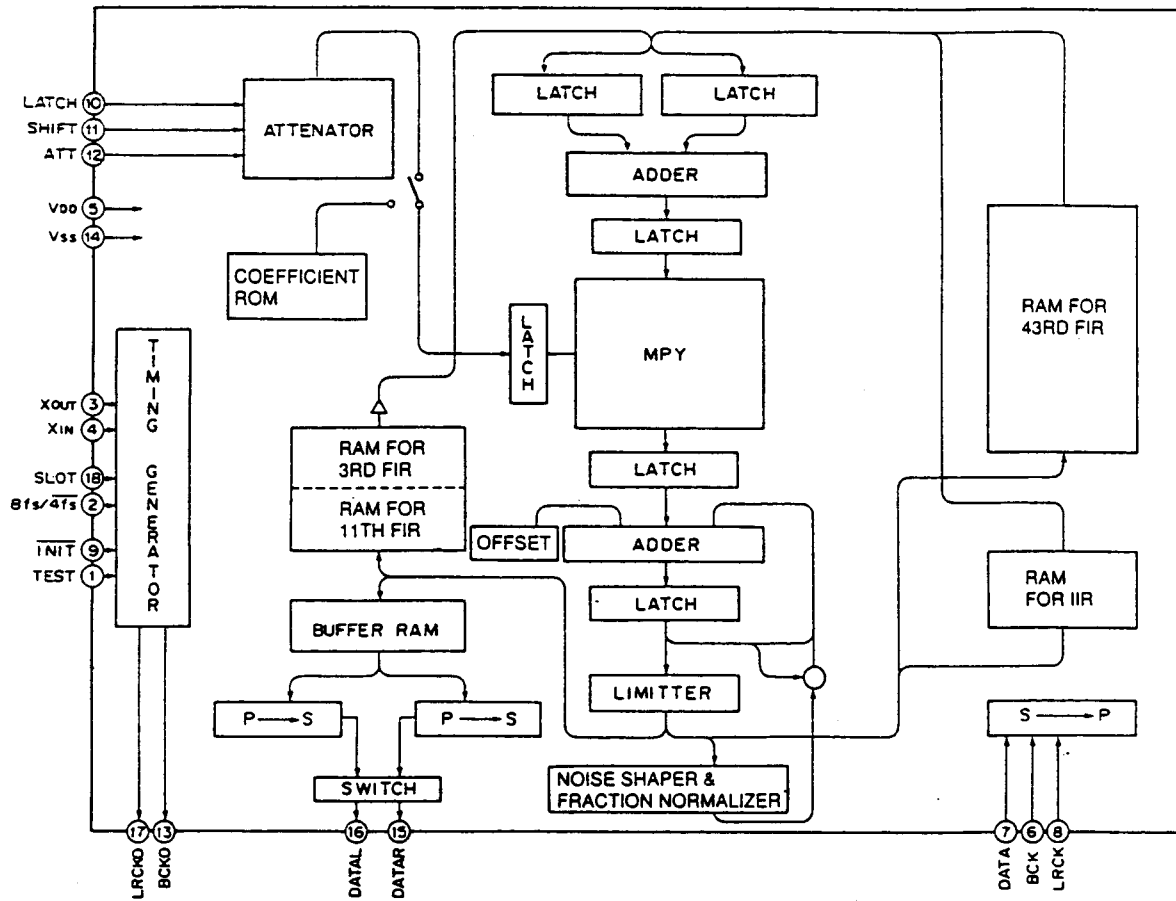


Pin Configuration

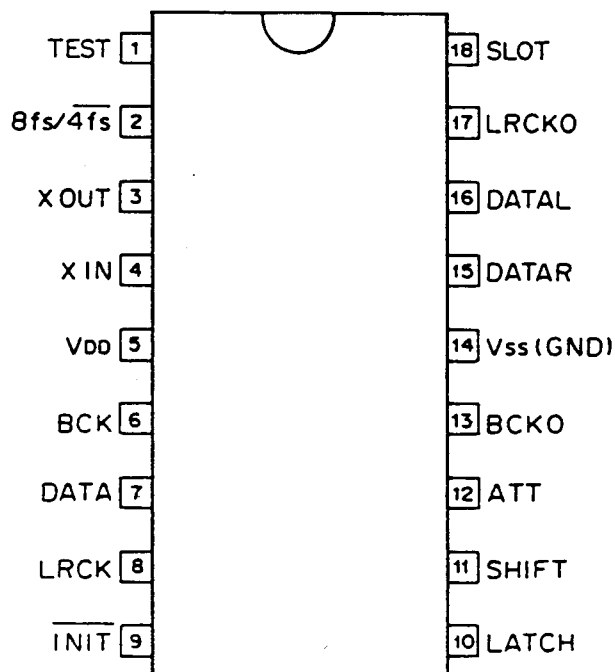


CXD2551P

Block Diagram



Pin Configuration



## Pin Description

Pin No.		Symbol	I/O	Description
CXD2551P	CXD2551M			
1	1	TEST	I	Test pin. Fixed at 'L' level in normal operation mode.
2	2	8fs / $\overline{4fs}$	I	To specify FIR 3. 'H': 8fs 'L': 4fs
3	3	XOUT	O	Master clock output (f = 384fs)
4	4	XIN	I	Master clock input (f = 384fs)
5	6	V <sub>DD</sub>	—	Power supply (+5 V)
6	9	BCK	I	BCK input
7	10	DATA	I	Serial data input (2's complement)
8	11	LRCK	I	LRCK input
9	12	$\overline{\text{INIT}}$	I	Re-synchronized by rising edge of this signal
10	13	LATCH	I	Latch clock input
11	14	SHIFT	I	Shift clock input
12	15	ATT	I	Attenuate data input
13	16	BCKO	O	BCK output
14	19	V <sub>SS</sub> (GND)	—	Power supply (0 v)
15	21	DATAR	O	4fs mode: WCK output 8fs mode: RCH serial data output (2's complement)
16	22	DATAL	O	4fs mode: LCH and RCH time division serial data output (2's complement) 8fs mode: LCH serial data output (2's complement)
17	23	LRCKO	O	LRCK output
18	24	SLOT	I	To specify output slot. 'H': 18-bit slot 'L': 16-bit slot
—	5, 7, 8, 17, 18, 20	(NC)	—	No connection

\* TEST, 8fs / $\overline{4fs}$  and SLOT pins: Pull down resistance

Electrical Characteristics

DC characteristics ( $V_{DD} = 4.5$  to  $5.5$  V,  $T_a = -20$  to  $+75^\circ\text{C}$ )

Pin	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
All inputs except XIN	Input capacitance	$C_{IN}$	—	—	3	5	pF
Note 1	"H" input voltage	$V_{IH}$	—	$0.76 V_{DD}$	—	—	V
	"L" input voltage	$V_{IL}$	—	—	—	$0.24 V_{DD}$	
Note 2	Input leak current 1	$I_{ILK1}$	$V_i = V_{DD}/0V$	—	—	$\pm 5$	$\mu\text{A}$
TEST, $\overline{8fs}$ , $\overline{4fs}$ , SLOT	Pull down resistance	$R_{PD}$	—	7.5	15	30	$k\Omega$
	"L" input leak current	$I_{IL}$	$V_i = 0V$	—	—	5	$\mu\text{A}$
XIN	Input leak current 2	$I_{ILK2}$	$V_i = V_{DD}/0V$	—	—	$\pm 20$	
BCKO, DATAR, DATAL, LRCKO	"H" output voltage	$V_{OH}$	$I_D = -4$ mA	$V_{DD}-0.5$	—	—	V
	"L" output voltage	$V_{OL}$	$I_D = 4$ mA	—	—	0.4	
	Consumption current	$I_{DD}$	When no load is placed $V_i = V_{DD}/0V$ $f_x = 16.9344$ MHz	—	—	40	mA

Note 1) TEST,  $\overline{8fs}$ ,  $\overline{4fs}$ , BCK, DATA, LRCK,  $\overline{INIT}$ , LATCH, SHIFT, ATT, SLOT

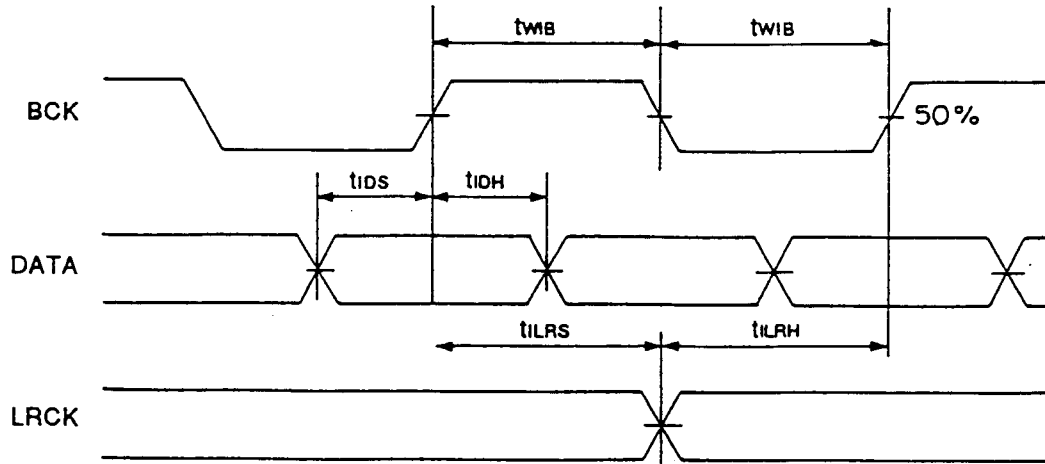
Note 2) BCK, DATA, LRCK,  $\overline{INIT}$ , LATCH, SHIFT, ATT

AC characteristics ( $V_{DD} = 4.5$  to  $5.5$  V,  $T_a = -20$  to  $+75^\circ\text{C}$ )

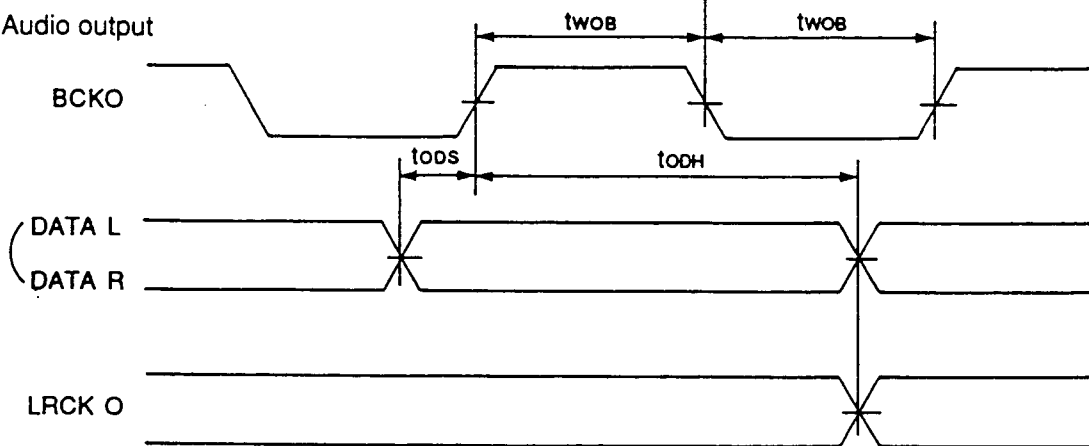
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	$f_x$	—	10	16.9344	20	MHz
Input BCK frequency	$f_{BCK}$	—	—	—	4.0	
Input BCK pulse width	$t_{WIB}$	—	100	—	—	ns
Input data set-up time	$t_{IDS}$	—	20	—	—	
Input data hold time	$t_{IDH}$	—	20	—	—	
Input LRCK set-up time	$t_{ILRS}$	—	50	—	—	
Input LRCK hold time	$t_{ILRH}$	—	50	—	—	
Output BCKO pulse width	$t_{WOB}$	8fs	40	—	—	
Output data set-up time	$t_{ODS}$	$f_x = 16.9344$ MHz	25	—	—	
Output data hold time	$t_{ODH}$	$C1 = 50$ pF	25	—	—	
Program input base time	$t_{PR}$	$f_x = 16.9344$ MHz	250	—	—	
Latch input pulse width	$t_{WLT}$	$f_x = 16.9344$ MHz	500	—	—	
Rise time (SHIFT, LATCH)	$t_r$	—	—	—	200	ns
Fall time (SHIFT, LATCH)	$t_f$	—	—	—	200	
Set-up time (ATT)	$t_{SET}$	—	500	—	—	
Hold time (ATT)	$t_{HOLD}$	—	500	—	—	
Interval	$t_{INT}$	—	1000	—	—	

Timing Chart

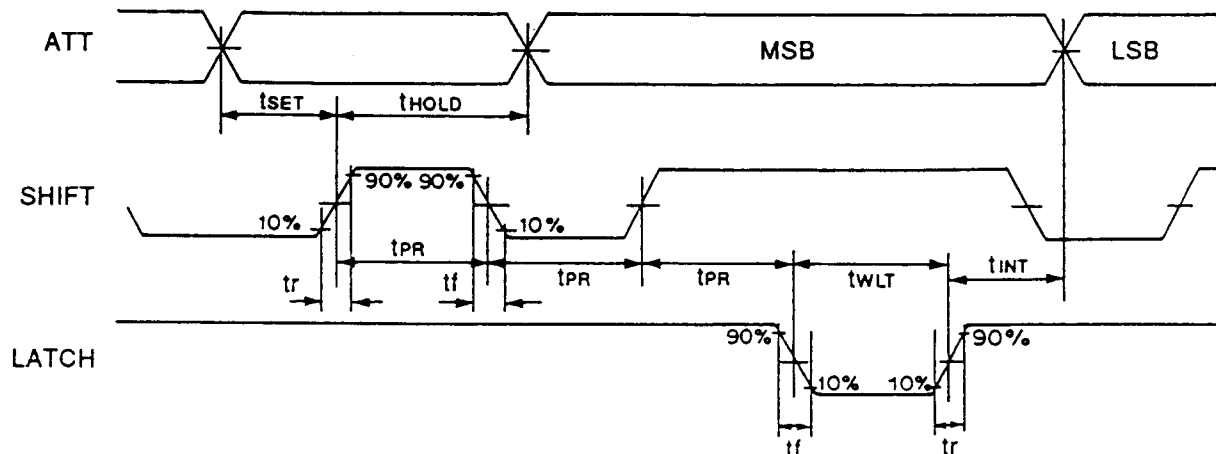
Audio input



Audio output



Program input



**Description of Functions**

**A. Soft muting**

The soft mute function mutes or demutes output data on the basis of a muting time of 1024/fs (CD: fs = 44.1 kHz).

**B. Digital attenuator**

Output data can be attenuated by use of data transferred from an external micro computer. The ATT data comprises 8 bits. Bit D<sub>7</sub> is the digital de-emphasis control bit, whereas bits D<sub>6</sub> through D<sub>0</sub> constitute attenuator data.

**(1) Command input and audio output**

The attenuator data is in 7 bits, allowing selection of 127 different settings. The relation between a command and output is shown in the following table.

Attenuator data D <sub>6</sub> to D <sub>0</sub>	Audio output
7F <sub>(H)</sub>	0 dB
7E <sub>(H)</sub> to 01 <sub>(H)</sub>	-0.13 dB to -42.144dB
00 <sub>(H)</sub>	-∞

An attenuator value between 01<sub>(H)</sub> and 7E<sub>(H)</sub> can be calculated by the following equation.

$$ATT = 20 \log \left( \frac{\text{Input data}}{128} \right) \text{dB}$$

Example) Suppose that attenuator data is 7A.

$$ATT = 20 \log \left( \frac{122}{128} \right) \text{dB} = -0.417 \text{ dB}$$

**C. I/O synchronizing circuit**

**1) Theory of operation**

The synchronizing circuit opens a window for six internal system clocks, CK2 (fx/4), to monitor whether the differentiated signal of the rise of LRCK (LRCK f) that may be input exists in it. If the LRCK f is out of the window when the power supply is turned on, the synchronizing circuit holds the CK2 at the time it is in the center of the window, and lets it start as soon as the next LRCK f arrives. This operation synchronizes an external system and this IC, and lines up the phases of serial input data.

**2) Re-synchronization by  $\overline{\text{INIT}}$**

If the LRCK f is in the window when the power supply is turned on, a fluctuation of LRCK could cause de-synchronization during operation of the IC (particularly when it is at either end of the window).

For this reason, re-synchronization must always be achieved after the power supply has been turned on. The operation for re-synchronization is performed at the time the  $\overline{\text{INIT}}$  rises. The operation initializes the synchronizing circuit to cause a temporary de-synchronization and then achieves re-synchronization, thereby positioning the LRCK f in the center of the window.

**D. Attenuator operation**

Suppose that there are three pieces of attenuator data, ATT1, ATT2 and ATT3 and that their relations are  $ATT1 > ATT3 > ATT2$ . Assume that ATT1 is transferred first, followed by ATT2.

If ATT2 is transferred before the value of ATT1 is reached (during the state of A in Fig. 1), the attenuation directly approaches the value of ATT2. If ATT3 is transferred before the value of ATT2 is reached (during the state of B or C in Fig. 1), the attenuation is carried on from the value at the time (B or C) to approach the value of ATT3. Transition from one piece of attenuator data to another is the same as in the case of soft muting.

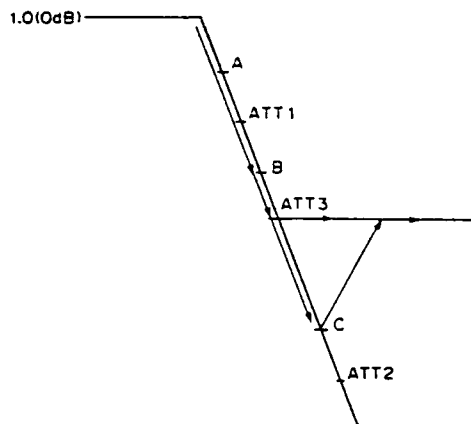


Fig. 1 Transition from one attenuator value to another

**E. Input data timing**

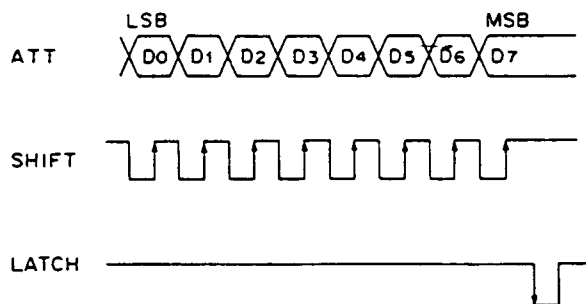


Fig. 2 Timing of ATT, SHIFT and LATCH

① ATT data is configured on the LSB first basis.

② ATT data

D7 : Digital de-emphasis control bit

H: Emphasis ON

L: Emphasis OFF

Note that emphasis time constants are  $\tau_1 = 50 \mu s$  and  $\tau_2 = 15 \mu s$  at  $f_s = 44.1 \text{ kHz}$ .

D<sub>0</sub> to D<sub>6</sub>: Attenuator data

**F. About  $\overline{INIT}$  pin is  $f$**

After  $\overline{INIT}$  is  $f$ , the counters and registers for the attenuators in the IC are set at  $7F_{(H)}$ .

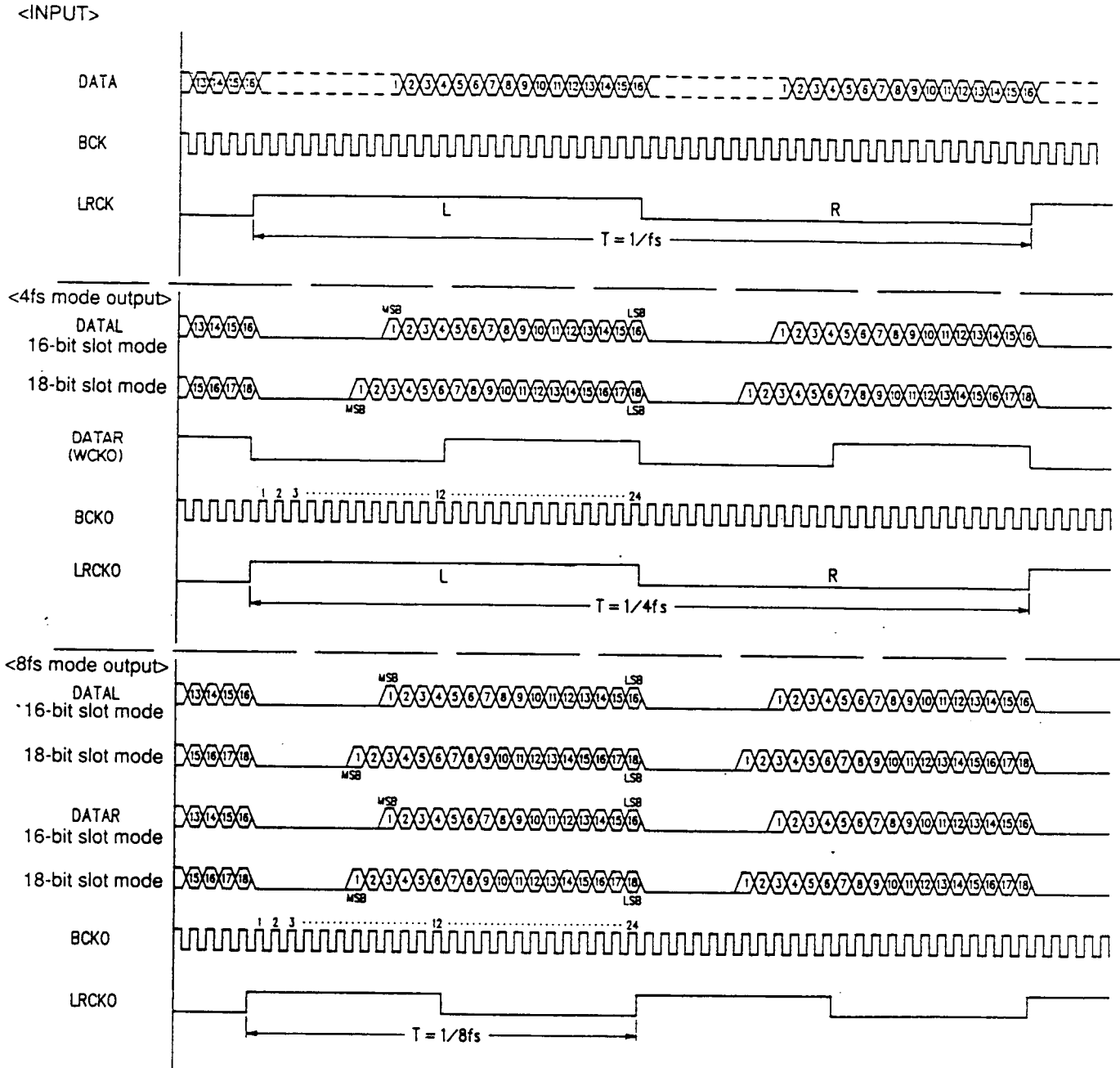


G. Digital offset

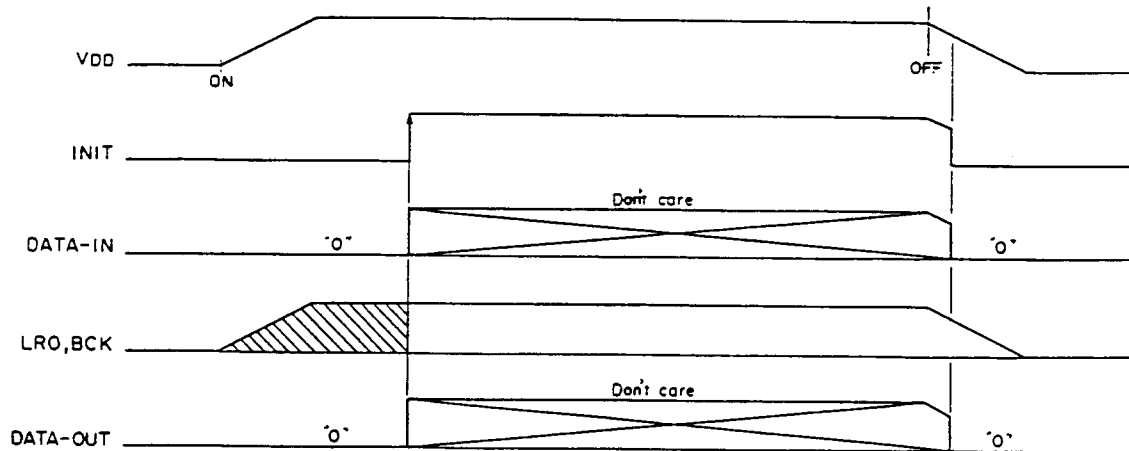
An offset value is added to the digital filter output. The value is 02AA<sub>(H)</sub> in the 16-bit slot mode and 02AA0<sub>(H)</sub> in the 18-bit slot mode.

In the muting mode, this offset value triggers muting.

I/O timing



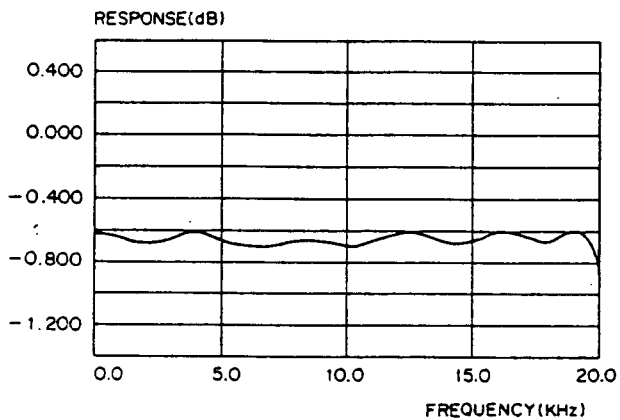
Operation in POWER ON/OFF state



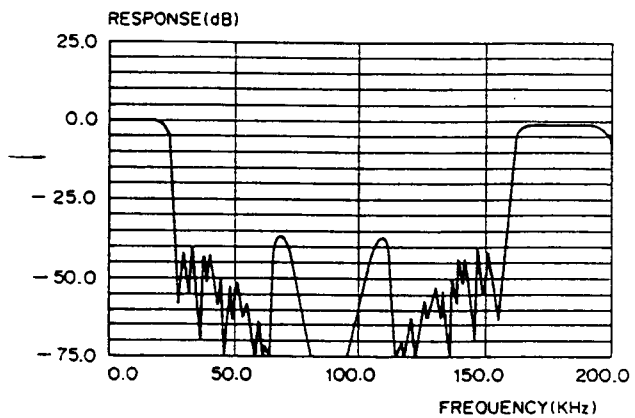
Filter Characteristics

Quadrupled oversampling mode

Frequency Characteristics 1 (Pass band)

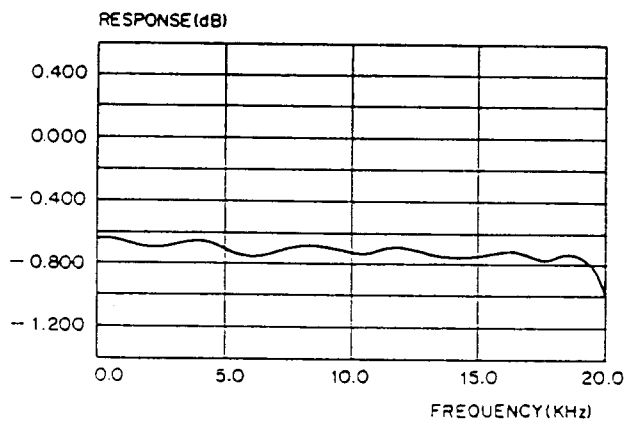


Frequency Characteristics 2 (Stop band)

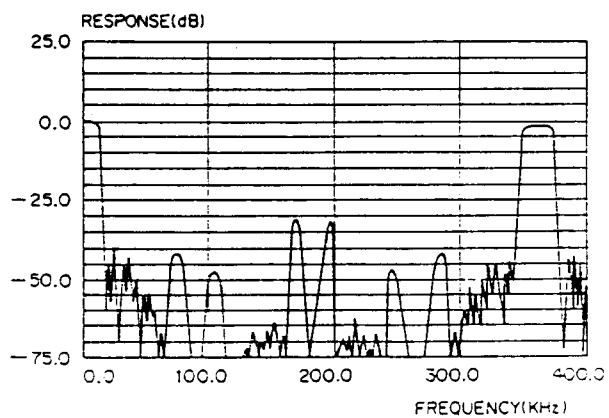


Octupled oversampling mode

Frequency Characteristics 1 (Pass band)

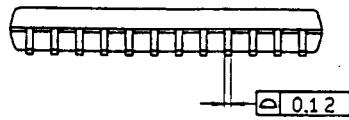
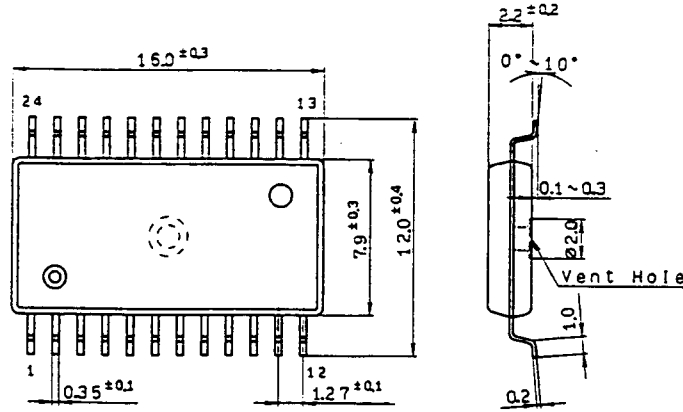


Frequency Characteristics 2 (Stop band)



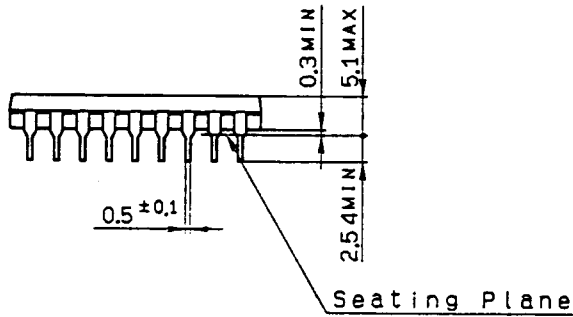
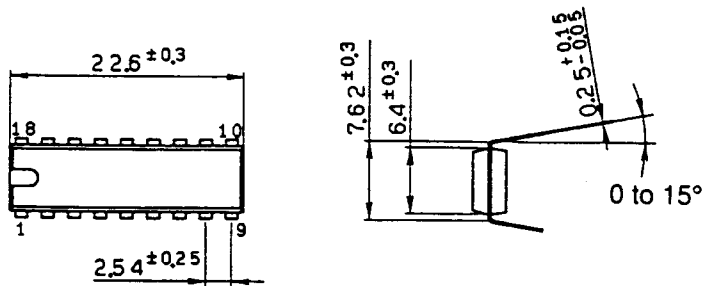
Package Outline Unit: mm

CXD2551M 24 pin SOP (Plastic) 450 mil



SOP-24P-L101

CXD2551P 18 pin DIP (Plastic) 300 mil



DIP-18P-101

T-90-20

**Sony Package Product Name**

Type	Package name		Package	Features				
	Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction	
Inserted	Standard	DIP	DUAL IN LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	4-direction
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
Shrink	SDIP	SHRINK DUAL IN LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction	
Surface mounted	Standard flat package	QFP	QUAD FLAT PACKAGE		P	1.0mm 0.8mm	Gull-Wing	4-direction
		SOP	SMALL-OUTLINE PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull Wing	2-direction
	Standard chip carrier	PLCC	PLASTIC LEADED CHIP CARRIER		P	1.27mm (50MIL)	J-bend	4-direction
		LCC	LEAD LESS CHIP CARRIER		C	1.27mm (50MIL)	Lead less	Package side
	Shrink chip carrier	SPLCC (PLCC)	SHRINK PLASTIC LEADED CHIP CARRIER		P	1.27mm Max. (50MIL Max.)	J-bend	4-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEAD PACKAGE		P	1.27mm (50MIL)	J-bend	2-direction



\*P.....Plastic, C.....Ceramic