SONY

CXD3152AR

Signal Processor LSI for Single-chip CCD B/W Camera

Description

The CXD3152AR is a digital signal processor LSI for CCD black-and-white cameras. In addition to the CDS and AGC circuits of conventional analog signal processor LSI, this chip also features the ease of use and functions of digital signal processing.

Features

- Supports 510H/760H system CCD image sensors
- Supports EIA/CCIR modes
- Built-in CDS and AGC circuits
- Built-in 10-bit A/D converter
- Built-in 9-bit D/A converter
- Analog and digital signal output
- Right/left inverted (mirror image) output function
- Horizontal and vertical aperture correction function
- Gamma correction curve variable function
- Serial communication function (I^2C bus)
- Supports external sync functions (when using the CXD2463R)
  — Line lock/Vreset HPLL
- Supports backlight compensation functions (when using the CXD2463R)
- Character input pin
- Blemish detection and compensation function

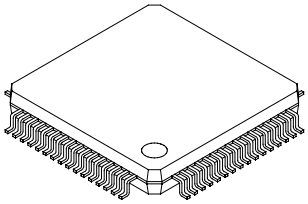
Absolute Maximum Ratings

• Supply voltage	V_{DD} (3.3V)	V_{SS} – 0.3 to +4.6	V
	V_{DD} (5.0V)	V_{SS} – 0.3 to +6.0	V
• Input voltage	V_I (3.3V)	V_{SS} – 0.3 to $V_{DD}3$ + 0.3	V
	V_I (5.0V)	V_{SS} – 0.3 to $V_{DD}5$ + 0.3	V
• Output voltage	V_O (3.3V)	V_{SS} – 0.3 to $V_{DD}3$ + 0.3	V
	V_O (5.0V)	V_{SS} – 0.3 to $V_{DD}5$ + 0.3	V
• Operating temperature			
	Topr	–20 to +75	°C
• Storage temperature			
	Tstg	–55 to +125	°C

Recommended Operating Conditions

• Supply voltage	V_{DD} (3.3V)	3.0 to 3.6	V
	V_{DD} (5.0V)	4.75 to 5.25	V

64 pin LQFP (Plastic)



Applications

Various CCD black-and-white cameras

Applicable CCD Image Sensors*

510H system CCDs (Type 1/3, 1/4 EIA/CCIR)
760H system CCDs (Type 1/2, 1/3, 1/4 EIA/CCIR)

Supported Related LSIs

TG : CXD2463R
EEPROM : S-24C01B
(Seiko Instruments Co., Ltd.)
or equivalent product

* Applicable CCD Image Sensors are applicable products as of preparing this data sheet. They may be changed according to the version up and production stop of CCD image sensor.

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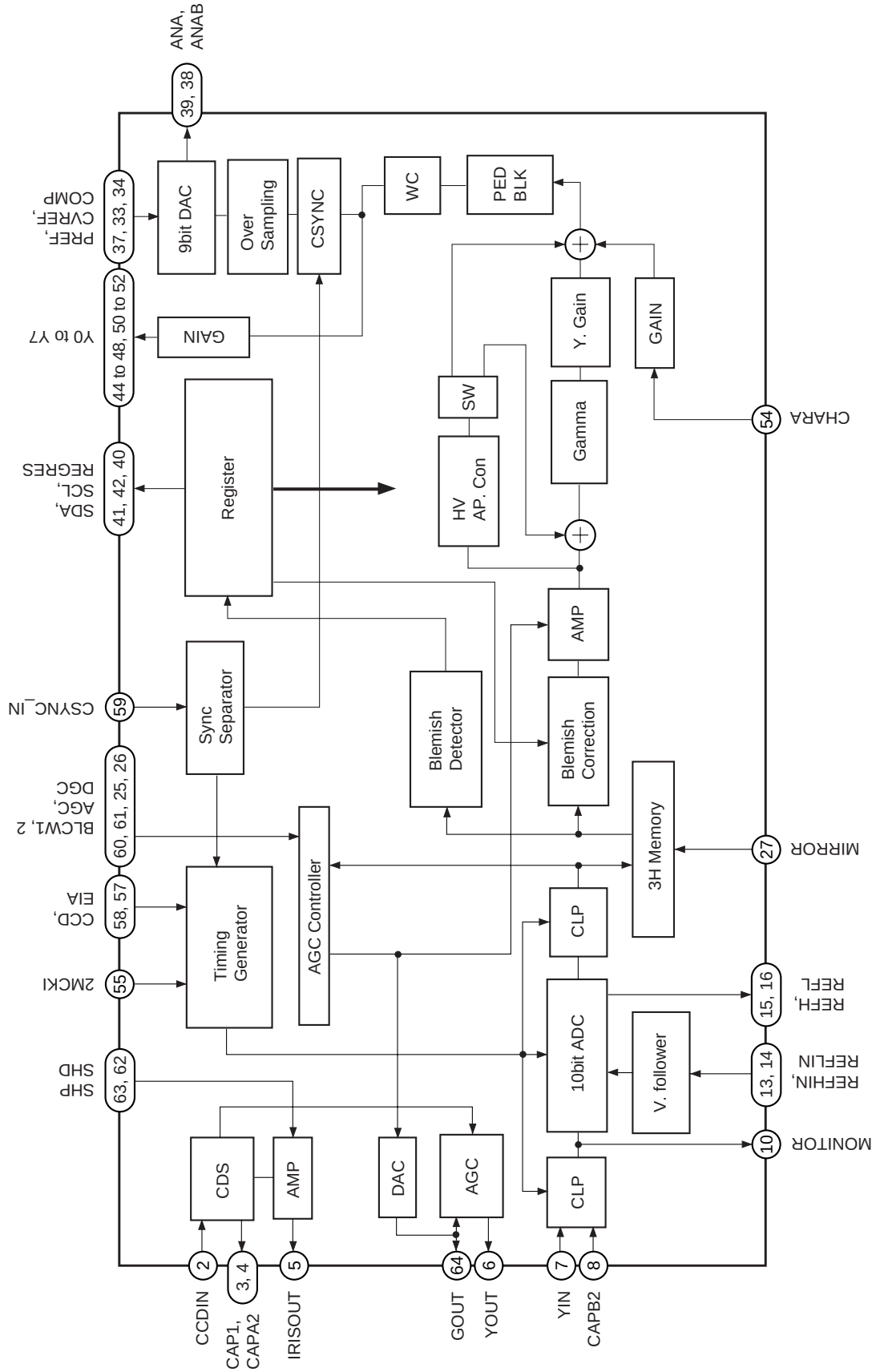
Block Diagram



Description of Functions by Block

CDS & AGC

- **CDS**
  $V_{DD}1$ = 5.0V
  SHD/SHP external input: <SHD/SHP>
  Brightness signal output for iris detection: <IRISOUT>
- **AGC**
  $V_{DD}2$ = 5.0V
  AGC gain variable range: 6 to 19dB (typ.)
  The gain is controlled by the 8-bit DAC for DC voltage generation.
  Manual setting possible by the register

A/D Converter

- **ADC**
  10 bits
  $V_{DD}3$ = 3.3V
  The input block clamp circuit pulse is generated internally, and external input is impossible.
  Built-in voltage follower for the reference voltage

Digital Signal Processing

- **DGC**
  DGC (digital gain control) operates at the maximum AGC (analog gain control) gain.
  The gain can be controlled from 0 to approximately 8 times.
  The aperture signal coring level is automatically controlled in conjunction with the gain.
- **MIRROR**
  Right/left inverted output possible <MIRROR>
- **APCON**
  Horizontal and vertical aperture correction circuit
  The circuit can be turned on and off by the setting pin. <APCON>
  Fine adjustment possible by the register
  The position at which the aperture correction signal is added can be switched to before or after gamma.
- **Gamma correction**
  4 patterns can be selected by the setting pins. <GAMMA1, GAMMA2>
  7-line approximation
  Adjustable by the register
- **Oversampling**
  Sampling frequency selectable from 2MCKI or (2MCKI/2)
- **PED**
  Standard setting: 7.5 IRE
  Adjustable by the register
- **Character input**
  A 1-bit signal from an external pin can be added to the luminance signal. <CHARA>
  The gain can be set by the register.
- **Blemish detection and compensation function**
  Up to a total of 10 white point blemishes can be detected and compensated during dark signal.
  Blemish addresses can be read out by serial communication.
- **Digital output**
  8-bit digital signal output

D/A Converter

- **DAC**

9 bits

$V_{DD}6$ = 3.3V

Supports –40 to +130 IRE output

Timing Generation

- **Timing**

Generation of various DSP internal signal processing pulses

Input clock frequencies:

EIA (510 × 492) : 19.06993MHz

CCIR (500 × 582) : 18.9375MHz

EIA (768 × 494) : 28.63636MHz

CCIR (752 × 582) : 28.375MHz

Slave operation according to the sync signal <CSYNC_IN> from an external TG: Composite sync input

Gain Control

Built-in auto gain control circuit

The maximum AGC (analog gain control) and DGC (digital gain control) gains can be set individually by the registers.

AGC and DGC can be turned on and off individually by external pins. <AGC, DGC>

The gain control time constants can be set by the registers.

Supports backlight compensation

Registers

- **I^2C bus**

Various register settings: <SCL, SDA, REGRES>

Slave address: [A6:A0] = 0011111 (b)

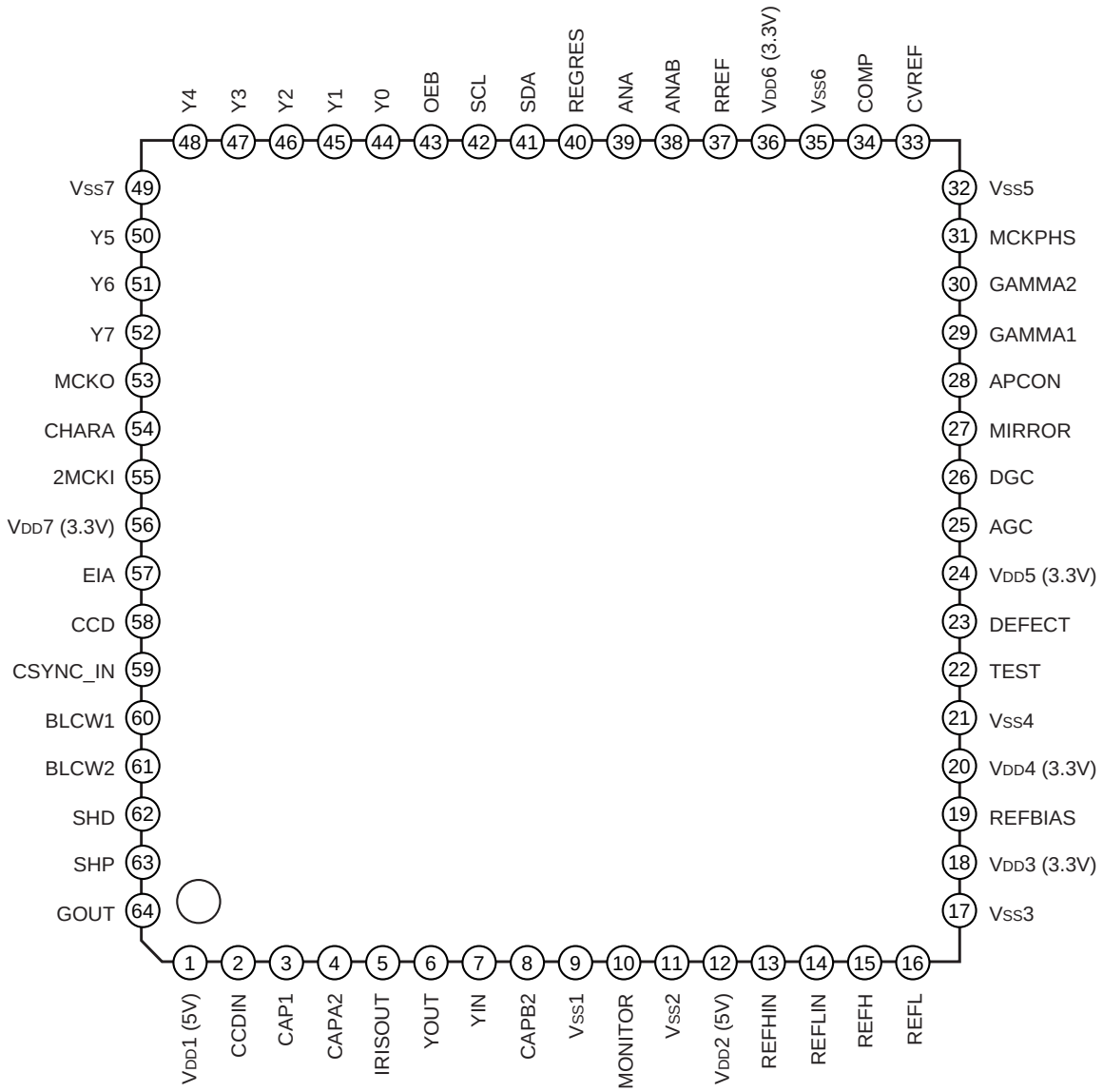
Related pins: <SCL, SDA, REGRES>

- **External EEPROM**

An EEPROM which supports the I^2C bus can be connected.

Register values can be automatically read out during power-on.

Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	$V_{DD}1$	P	Analog power supply (5.0V)
2	CCDIN	I	Image signal input from CCD
3	CAP1	O(A)	CDS DC bias output Connect to GND via an approximately 0.1µF capacitor.
4	CAPA2	O(A)	Gain control amplifier DC bias output Connect to GND via an approximately 0.1µF capacitor.
5	IRISOUT	O(A)	Image signal output for iris detection
6	YOUT	O(A)	AGC image signal output
7	YIN	I(A)	Image signal input to ADC Normally input YOUT via an approximately 0.1µF capacitor.
8	CAPB2	I(A)	ADC input clamp level (DC) input High reference (REFHIN) reference level
9	$V_{SS}1$	P	Analog GND
10	MONITOR	O(A)	Output for monitoring the signal input to ADC
11	$V_{SS}2$	P	Analog GND
12	$V_{DD}2$	P	Analog power supply (5.0V)
13	REFHIN	I(A)	ADC high reference input
14	REFLIN	I(A)	ADC low reference input
15	REFH	O(A)	ADC high reference output Connect to GND via an approximately 0.1µF capacitor.
16	REFL	O(A)	ADC low reference output Connect to GND via an approximately 0.1µF capacitor.
17	$V_{SS}3$	P	Analog GND
18	$V_{DD}3$	P	Analog power supply (3.3V)
19	REFBIAS	O(A)	ADC DC bias output Connect to GND via an approximately 0.1µF capacitor.
20	$V_{DD}4$	P	Digital power supply (3.3V)
21	$V_{SS}4$	P	Digital GND
22	TEST	I	Test pin. Normally fix high.
23	DEFECT	I	Blemish compensation function switching 0: Off, 1: On
24	$V_{DD}5$	P	Digital power supply (3.3V)
25	AGC	I	Analog gain switching 0: Fixed, 1: Auto
26	DGC	I	Digital gain switching 0: Fixed, 1: Auto
27	MIRROR	I	Mirror inversion switching 0: Standard, 1: Mirror
28	APCON	I	Aperture correction switching 0: Off, 1: On
29	GAMMA1	I	Gamma correction characteristics switching 00: 0.45, 01: 0.6 (register setting), 10: 1.0, 11: S curve
30	GAMMA2	I	

Pin No.	Symbol	I/O	Description
31	MCKPHS	I	2MCKI input polarity switching 0: Through, 1: Inverted
32	$V_{SS}5$	P	Digital GND
33	CVREF	O(A)	DAC reference voltage output Connect to GND via 0.1µF.
34	COMP	O(A)	DAC phase compensation. Connect to GND via 0.1µF.
35	$V_{SS}6$	P	Digital GND
36	$V_{DD}6$ (3.3V)	P	Digital power supply (3.3V)
37	RREF	O(A)	DAC reference voltage generation Normally connect to GND via 3.3kΩ.
38	ANAB	O(A)	DAC negative output. Normally connect to GND via 200Ω.
39	ANA	O(A)	DAC positive output. Normally connect to GND via 200Ω.
40	REGRES	I*	Register reset. All registers reset to the default when low.
41	SDA	I/O*	I^2C bus data line
42	SCL	I/O*	I^2C bus clock line
43	OEB	I	Digital output (Y0 to Y7) control. 0: Output, 1: Hi-Z
44	Y0	O	Digital signal output (LSB)
45	Y1	O	Digital signal output
46	Y2	O	Digital signal output
47	Y3	O	Digital signal output
48	Y4	O	Digital signal output
49	$V_{SS}7$	P	Digital GND
50	Y5	O	Digital signal output
51	Y6	O	Digital signal output
52	Y7	O	Digital signal output (MSB)
53	MCKO	O	Y0 to Y7 latch clock output
54	CHARA	I*	Character signal input
55	2MCKI	I*	Reference clock input
56	$V_{DD}7$	P	Digital power supply (3.3V)
57	EIA	I*	TV mode switching 0: EIA, 1: CCIR
58	CCD	I*	CCD number of horizontal pixels switching 0: 510H system, 1: 760H system
59	CSYNC_IN	I*	Composite sync input
60	BLCW1	I*	Backlight compensation window switching 00: Full-screen photometry, 01: Bottom photometry 10: Center photometry, 11: Bottom + center photometry
61	BLCW2	I*	
62	SHD	I*	Data block sampling pulse input

Pin No.	Symbol	I/O	Description
63	SHP	I*	Precharge block sampling pulse input
64	GOUT	O(A)	AGC gain control voltage output (DAC output) Connect to GND via an approximately 0.1µF capacitor.

Note 1) Asterisks (*) indicate that either 3.3V or 5.0V input is possible.

Note 2) The I/O column symbol meanings are as follows.

I : Digital input
O : Digital output
I/O : Digital input/output
I(A) : Analog input
O(A) : Analog output
P : Power supply/GND

Logic Block Electrical Characteristics

DC Characteristics

3.3V Block (V_{DD} = 3.0 to 3.6V, V_{SS} = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input high level voltage	V_{IH}	CMOS supported	0.7V_{DD}	—	—	V	*1
Input low level voltage	V_{IL}		—	—	0.2V_{DD}	V	
Input high level voltage	V_{IH}	CMOS Schmitt supported	0.75V_{DD}	—	—	V	*2, *4
Input low level voltage	V_{IL}		—	—	0.15V_{DD}	V	
Output low level voltage	V_{OL}	I_{OL} = 4mA	—	—	0.4	V	*4
Output high level voltage	V_{OH}	I_{OH} = –4mA	V_{DD} – 0.8	—	—	V	*3
Output low level voltage	V_{OL}	I_{OL} = 4mA	—	—	0.4	V	
Input leak current	I_{IL}	V_I = V_{DD}, V_{SS}	–10	—	+10	µA	*1, *2, *4
Output leak current	I_{OZ}	At high impedance output	–10	—	+10	µA	*3, *4

Note 1) The applicable pins correspond to the following symbols.

*1 AGC, APCON, BLCW1, BLCW2, CCD, CHARA, MCKPHS, CSYNC_IN, DEFECT, DGC, EIA, GAMMA1, GAMMA2, 2MCKI, MIRROR, TEST, OEB (input)

*2 REGRES

*3 MCKO, Y0 to Y7 (output)

*4 SCL, SDA (I/O)

Note 2) The ANA, ANAB, COMP, CVREF, REFBIAS, REFH, REFL and RREF pins are not included in the DC characteristics.

5.0V Block (V_{DD} = 4.75 to 5.25V, V_{SS} = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input high level voltage	V_{IH}	CMOS supported	0.7V_{DD}	—	—	V	*5
Input low level voltage	V_{IL}		—	—	0.3V_{DD}	V	
Input leak current	I_{IL}	V_I = V_{DD}, V_{SS}	–10	—	+10	µA	*5

Note 1) The applicable pins correspond to the following symbols.

*5 SHD, SHP (input)

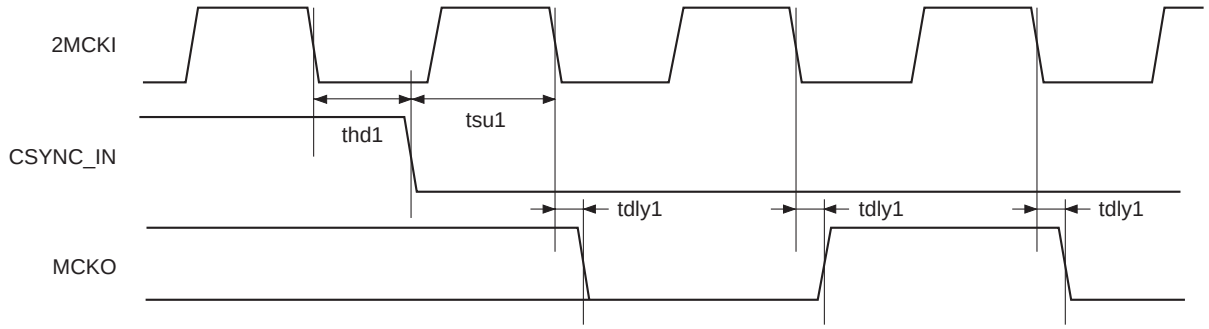
Note 2) The CAP1, CAPA2, CAPB2, CCDIN, REFHIN, REFLIN, YIN, GOUT, IRISOUT, MONITOR and YOUT pins are not included in the DC characteristics.

AC Characteristics (Output load: C_L = 50pF)

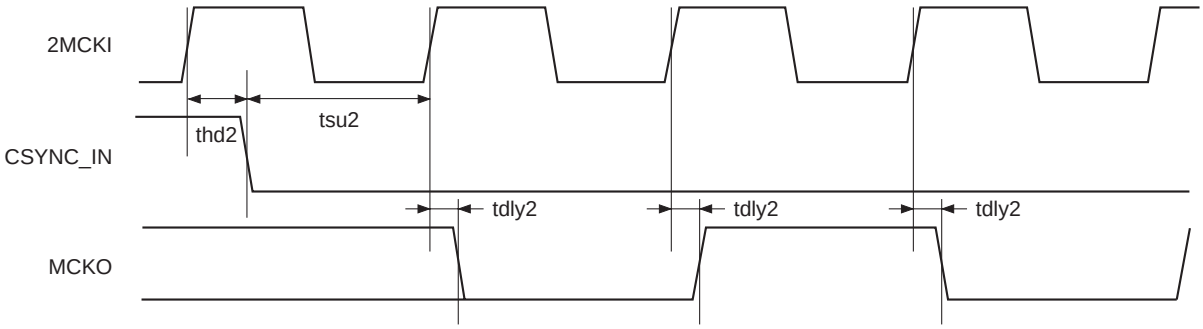
Item	Symbol	Min.	Typ.	Max.	Unit
CSYNC_IN fall setup time, activated by the falling edge of 2MCKI	tsu1	10	—	—	ns
CSYNC_IN fall hold time, activated by the falling edge of 2MCKI	thd1	10	—	—	ns
Delay time from the falling edge of 2MCKI to MCKO output	tdly1	—	—	20	ns
CSYNC_IN fall setup time, activated by the rising edge of 2MCKI	tsu2	10	—	—	ns
CSYNC_IN fall hold time, activated by the rising edge of 2MCKI	thd2	10	—	—	ns
Delay time from the rising edge of 2MCKI to MCKO output	tdly2	—	—	20	ns
CHARA setup time, activated by the falling edge of MCKO	tsu3	0	—	—	ns
CHARA hold time, activated by the falling edge of MCKO	thd3	20	—	—	ns
Delay time from the falling edge of MCKO to Y0 to Y7 output	tdly3	—	—	15	ns
Power-on reset time	tpor	1	—	—	µs
Reset pulse width	trst	1	—	—	µs
SCL clock frequency	fscl	—	—	500	kHz
SCL clock high level width	thigh	700	—	—	ns
SCL clock low level width	tlow	700	—	—	ns
SDA setup time, activated by the rising edge of SCL	tsu4	30	—	—	ns
SDA hold time, activated by the falling edge of SCL	thd4	0	—	—	ns
Delay time from the falling edge of SCL to SDA low level output	tdly4	—	—	20	ns
Delay time from the falling edge of SCL to SDA output floating	tdly5	—	—	15	ns
SHP rise time, activated by the falling edge of 2MCKI	tdly6	—	—	—	ns
SHD rise time, activated by the falling edge of 2MCKI	tdly7	0	—	30	ns

Master Clock Generation Timing

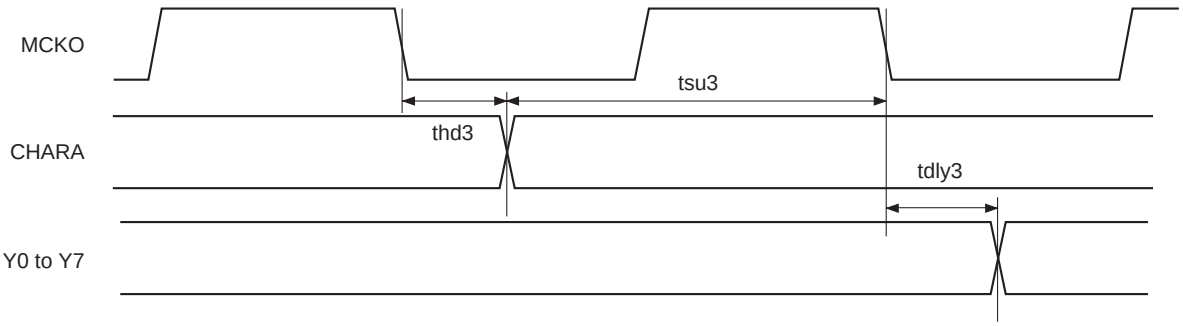
(1) MCKPHS = Low



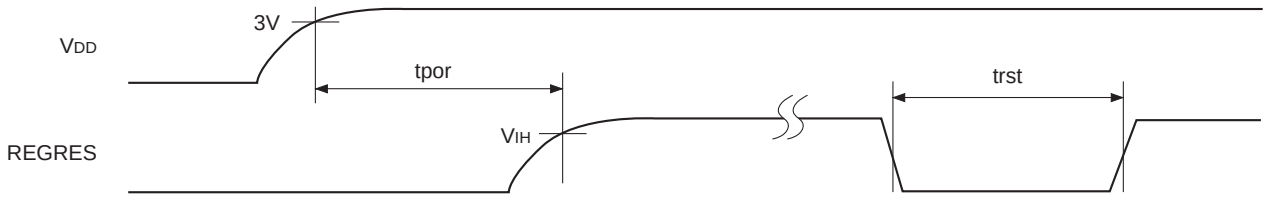
(2) MCKPHS = High



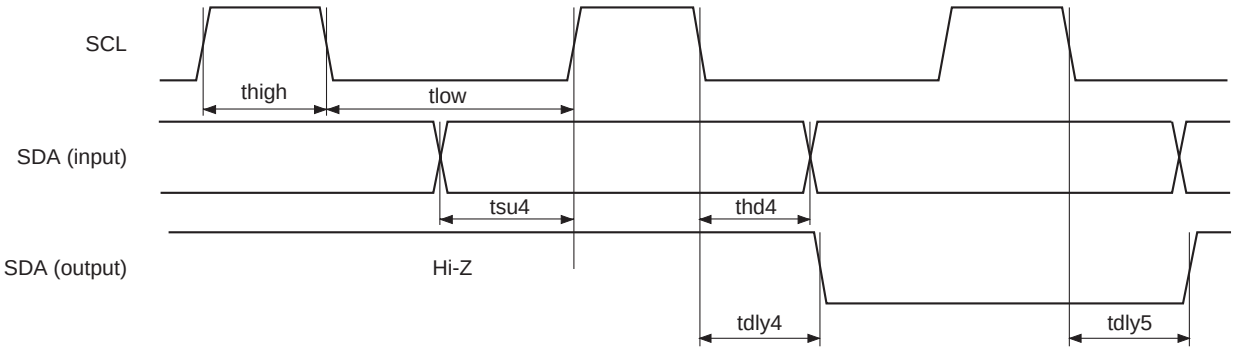
Video Signal Related Input/Output Timing



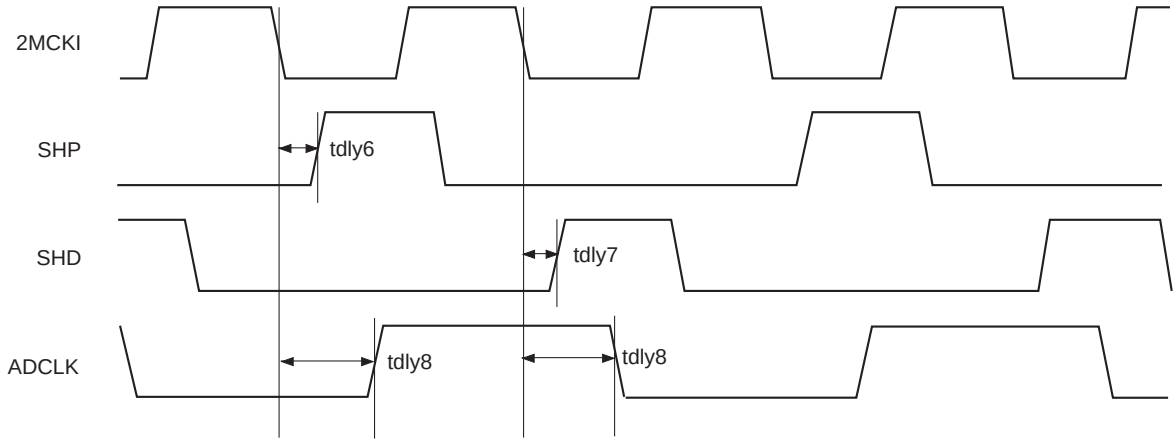
Reset Timing



I²C bus Timing



Analog Signal Processing Sampling Pulse Timing



Note 1) When MCKPHS = Low

Analog Block Electrical Characteristics

10-bit A/D Converter Electrical Characteristics

($V_{DD}3$ = 3.3V, V_{SS} = 0V, Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Resolution	RES	—	—	10	Bits	
Conversion frequency	Fs	—	15	20	MSPS	
Nonlinearity error	I.L.	—	—	±2.0	LSB	DC accuracy
Differential nonlinearity error	D.L.	—	—	±1.0	LSB	DC accuracy

* For the power supply names, refer to the symbols in the Pin Description.

9-bit D/A Converter Electrical Characteristics

($V_{DD}6$ = 3.3V, V_{SS} = 0V, Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Resolution	RES	—	—	10	Bits	
Conversion frequency	Fs	—	—	20.0	MSPS	
Zero scale output voltage	V_{ZERO}	–15	0	15	mW	
Full scale output voltage	V_{FULL}	1.21	1.30	1.43	V	
Full scale output current	I_{FULL}	0	6.6	16.5	mA	
Nonlinearity error	I.L.	—	—	±2.0	LSB	DC accuracy
Differential nonlinearity error	D.L.	—	—	±1.0	LSB	DC accuracy

* For the power supply names, refer to the symbols in the Pin Description.

CDS-AGC Electrical Characteristics ($V_{DD}1, 2$ = 5.0V, $V_{DD}3$ = 3.3V, V_{SS} = 0V, Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test conditions
CAP1 DC level	CAP1	1.5	1.6	1.7	V	CAP1 output DC level CCDIN = 1.6V (DC) GOUT = 1.5V
CAPA2 DC level	CAPA2	2.5	3.0	3.5	V	CAPA2 output DC level CCDIN = 1.6V (DC) GOUT = 1.5V
CDS DC level	CDSDC	2.9	3.4	3.9	V	YOUT output DC level CCDIN = 1.6V (DC) GOUT = 2.5V
AGC DC offset 1	GCOF1	–0.2	0	0.2	mV	GCOF1 = V4 – CDSDC V4 = YOUT output DC level CCDIN = 1.6V (DC) GOUT = 1.5V
AGC DC offset 2	GCOF2	–0.4	0	0.4	mV	GCOF2 = V5 – CDSDC V5 = YOUT output DC level CCDIN = 1.6V (DC) GOUT = 0.5V
AGC minimum gain characteristics **(Note 1)**	AGCG1	3.3	6.4	8.7	dB	YOUT output gain CCDIN = S1 **(Note 2)** GOUT = 3.3V
AGC maximum gain characteristics **(Note 1)**	AGCG2	15.7	18.8	21.1	dB	YOUT output gain CCDIN = S1 **(Note 2)** GOUT = 0V
AGC D range 1	AGCD1	1.9	2.2	2.7	V	YOUT output AC level CCDIN = S1 **(Note 3)** GOUT = 0.5V
AGC D range 2	AGCD2	1.6	2.0	2.7	V	YOUT output AC level CCDIN = S1 **(Note 3)** GOUT = 2.5V
IRIS DC level	IRISDC	1.6	2.2	2.6	V	IRISOUT DC level CCDIN = 1.6V (DC) GOUT = 3.3V
IRIS gain	IRISG	8.3	9.5	10.7	dB	IRISOUT gain CCDIN = S2 **(Note 4)** GOUT = 3.3V
IRIS D range	IRISDR	1.6	2.1	2.7	V	IRISOUT AC level CCDIN = S2 **(Note 5)** GOUT = 3.3V

* For the power supply names, refer to the symbols in the Pin Description.

Note 1) Refer to the AGC Gain Characteristics.
Note 2) S1: Va = 100 to 400mV, Vb = 1.6V (Va = peak to peak, Vb = peak to GND)
Note 3) S1: Va = 1000mV, Vb = 1.6V
Note 4) S2: Va = 400mV, Vb = 1.6V
Note 5) S2: Va = 1000mV, Vb = 1.6V

CLP Electrical Characteristics ($V_{DD}1, 2$ = 5.0V, $V_{DD}3$ = 3.3V, V_{SS} = 0V, Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test conditions
CAPB2 DC level	CAPB2	2.6	2.7	2.8	V	CAPB2 output DC level SW1 = A, SW2 = A
CLP DC level	CLPDC1	2.6	2.7	2.8	V	MONITOR output DC level CLP = "H" SW1 = A, SW2 = A
CLP gain	CLPG	0	0.6	1.2	dB	MONITOR output gain SW1 = B, SW2 = B YIN = S4 **(Note 1)**
CLP D range	CLPD	2.0	2.4	2.7	V	MONITOR output AC level SW1 = B, SW2 = A YIN = S3 **(Note 2)**

* For the power supply names, refer to the symbols in the Pin Description.

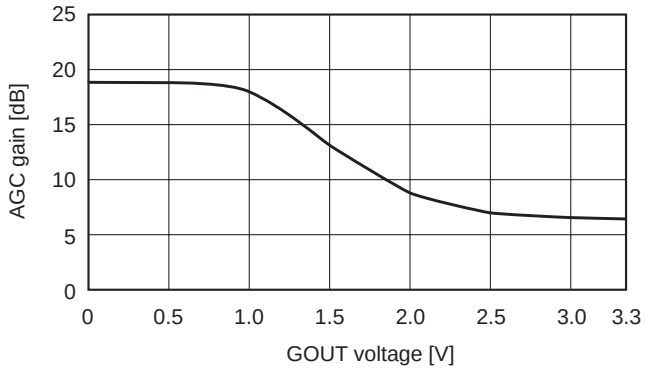
Note 1) S4: Va = 1000mV, Vb = 2.75V (Va = peak to peak, Vb = peak to GND)
Note 2) S3: Va = 2000mV, Vb = 3.6V

OPAMP Electrical Characteristics ($V_{DD}1, 2$ = 5.0V, $V_{DD}3$ = 3.3V, V_{SS} = 0V, Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test conditions
OPAMP DC H	OPH	2.8	2.9	3.0	V	REFH output DC level SW1 = A, SW2 = A
OPAMP DC L	OPL	0.8	0.9	1.0	V	REFL output DC level SW1 = A, SW2 = A

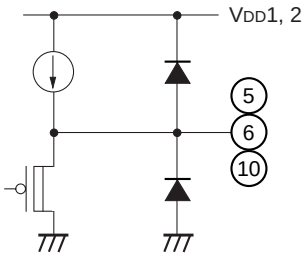
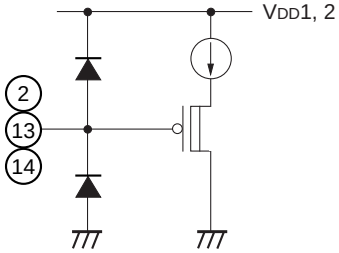
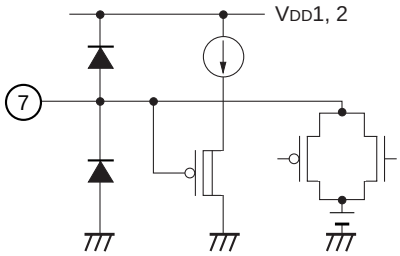
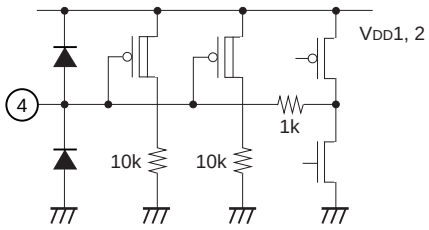
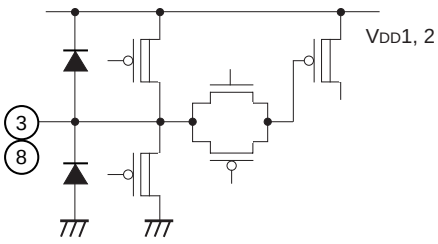
* For the power supply names, refer to the symbols in the Pin Description.

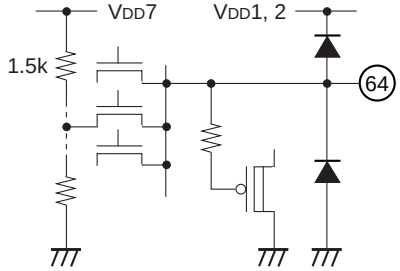
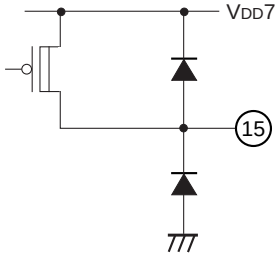
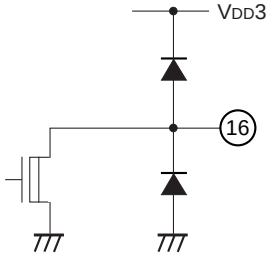
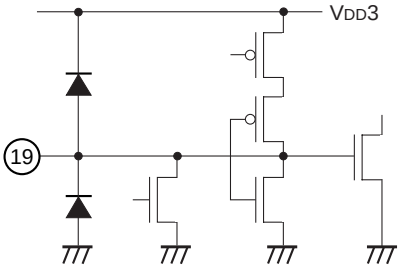
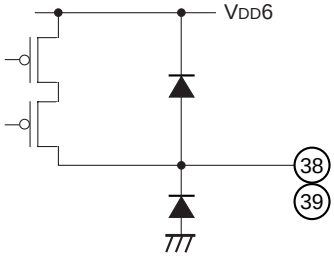
AGC Gain Characteristics ($V_{DD}1, 2$ = 5.0V, $V_{DD}3$ = 3.3V, V_{SS} = 0V, Ta = 25°C)

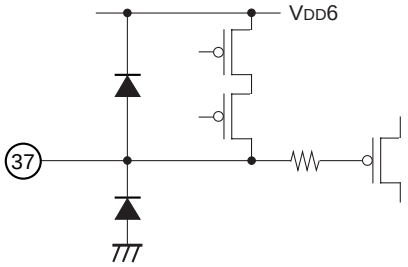
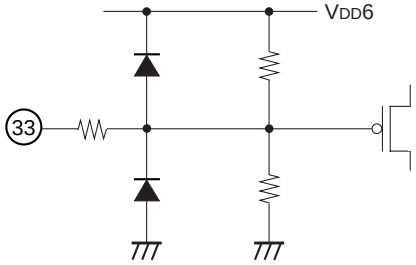
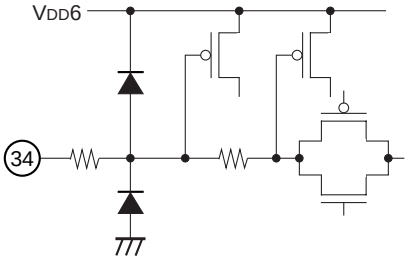


AGC Gain Characteristics

Analog Input/Output Pin Equivalent Circuits

Pin No.	Symbol	I/O	Equivalent circuit	Description
5	IRISOUT	O		Video signal output pin for iris detection Maximum output amplitude = 2.10Vp-p (typ.)
6	YOUT	O		Video signal output pin of gain control amplifier (AGC) Maximum output amplitude = 2.25Vp-p (typ.) Black level = 3.40V DC (typ.)
10	MONITOR	O		Video signal output of analog clamp circuit Monitor pin for input signal to ADC Black level = 2.75V DC (typ.)
2	CCDIN	I		Maximum input amplitude = 3.40Vp-p (Maximum video signal amplitude from precharge level = 2.00Vp-p) DC input bias = 1.80 ± 0.1V
13	REFHIN	I		High reference input pin for ADC 2.92V DC input (typ.)
14	REFLIN	I		Low reference input pin for ADC 0.82V DC input (typ.)
7	YIN	I		Input pin for video signal to undergo A/D conversion Maximum input amplitude = 2.30Vp-p (typ.) Black level = 2.73V DC (typ.)
4	CAPA2	O		DC bias output pin of the gain control amplifier 3.00V DC output (typ.)
3	CAP1	O		DC bias output pin of the CDS circuit 1.58V DC output (typ.)
8	CAPB2	I		Clamp level (DC) input pin of the clamp circuit for A/D conversion 2.73V DC input (typ.)

Pin No.	Symbol	I/O	Equivalent circuit	Description
64	GOUT	O		Gain control signal (8-bit DAC for gain control) output pin for AGC
15	REFH	O		High reference output pin for ADC Voltage follower output 2.90V DC output (typ.)
16	REFL	O		Low reference output pin for ADC Voltage follower output 0.80V DC output (typ.)
19	REFBIAS	O		DC bias output pin for ADC 1.55V DC output (typ.)
38	ANAB	O		D/A converter negative output 0 to 1.24V output
39	ANA	O		D/A converter positive output 0 to 1.24V output

Pin No.	Symbol	I/O	Equivalent circuit	Description
37	RREF	O		DAC reference voltage generation pin 1.32V DC output (typ.)
33	CVREF	O		DAC reference voltage output pin 1.32V DC output (typ.)
34	COMP	O		DAC phase compensation pin 2.18V DC output (typ.)

Note) For the power supply names in the equivalent circuits, refer to the symbols in the Pin Description.

Timing Chart

Horizontal Direction Timing

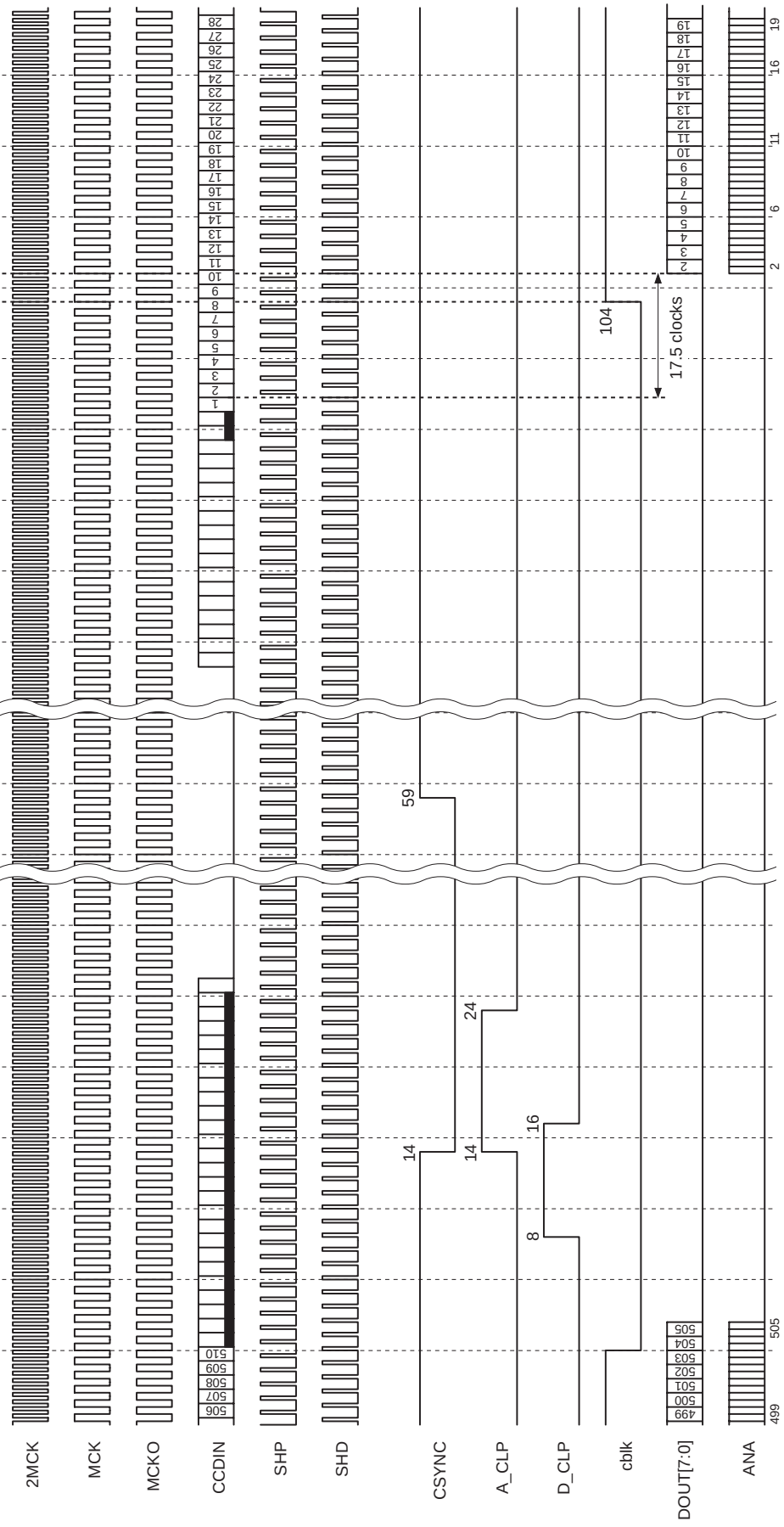
2MCK:	Master clock input for the CXD3152AR
MCK:	Internal reference clock produced by dividing the input reference clock (2MCK) in half.
MCKO:	Latch clock for digital output signal (Inverted MCK signal)
CCDIN:	Imaging signal from CCD
SHP:	Precharge level sampling pulse input
SHD:	Video level sampling pulse input
cblk:	Internal composite blanking pulse (for VIDEO output signal)
CSYNC:	Composite sync pulse input (in phase for CSYNC_IN and the VIDEO output signal)
A_CLP:	Internal pulse for analog clamp
D_CLP:	Internal pulse for digital clamp
DOUT[7:0]:	8-bit digital output signal
ANA:	Analog output signal

Vertical Direction Timing

HD:	Internal horizontal sync signal
cblk:	Internal composite blanking pulse (for VIDEO output signal)
CSYNC:	Composite sync pulse input (in phase for CSYNC_IN and the VIDEO output signal)
A_CLP:	Internal pulse for analog clamp
D_CLP:	Internal pulse for digital clamp
CCDIN:	Video signal from the CCD
DOUT[7:0]:	8-bit digital output signal

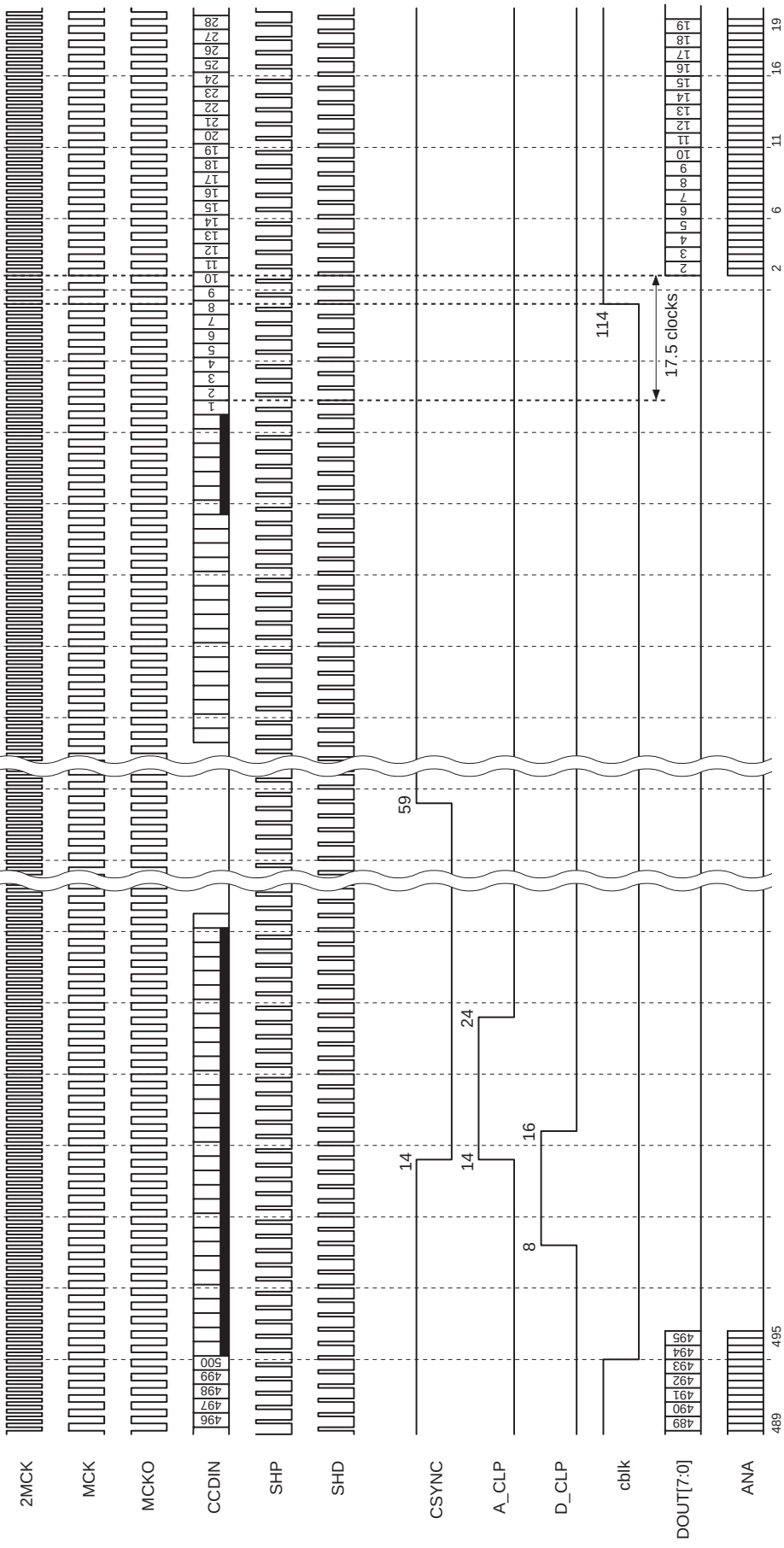
Horizontal Direction Timing Chart EIA 510H System

Count CLK = 606fH = 19.0699/2MHz



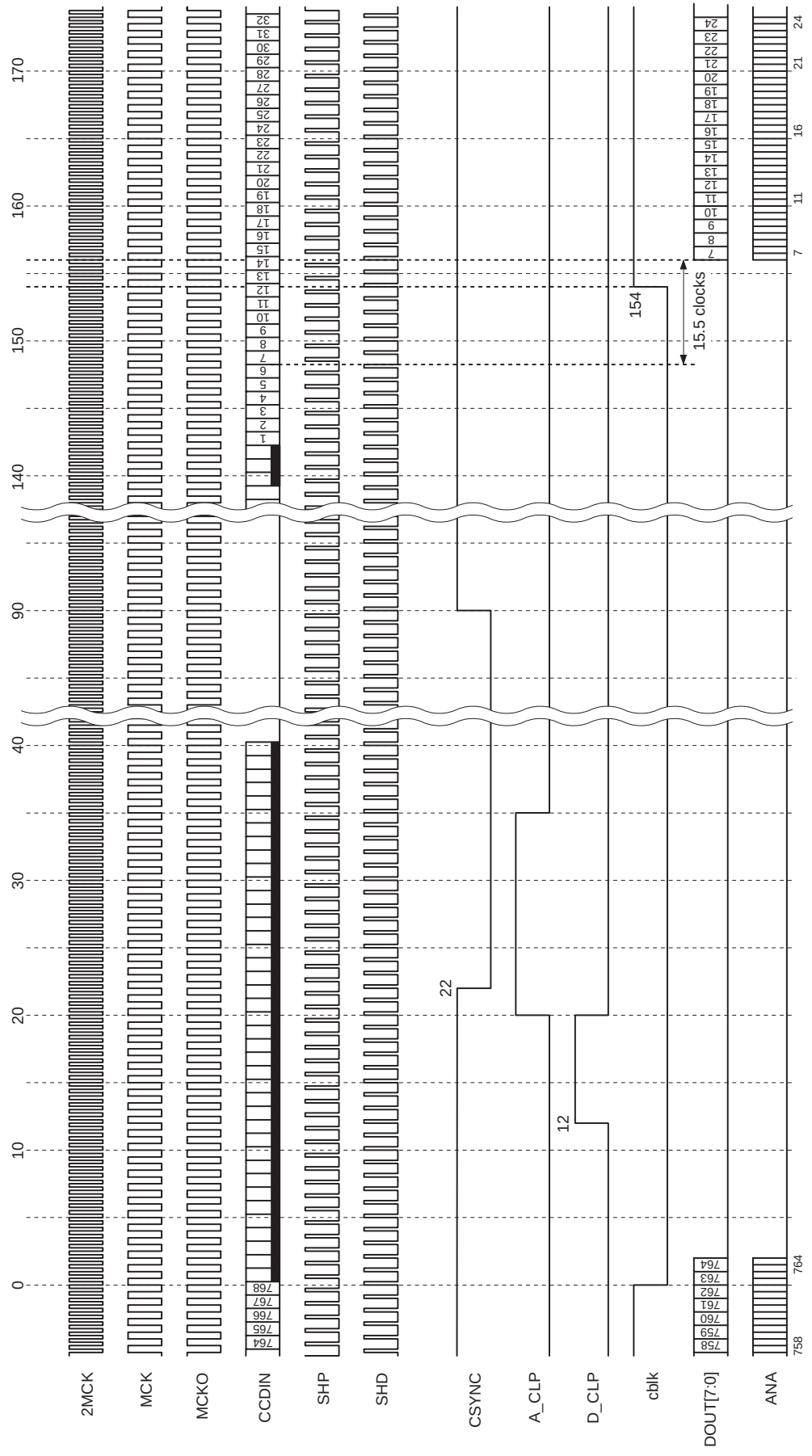
Horizontal Direction Timing Chart CCIR 510H System

Count CLK = 606fH = 18.9375/2MHz



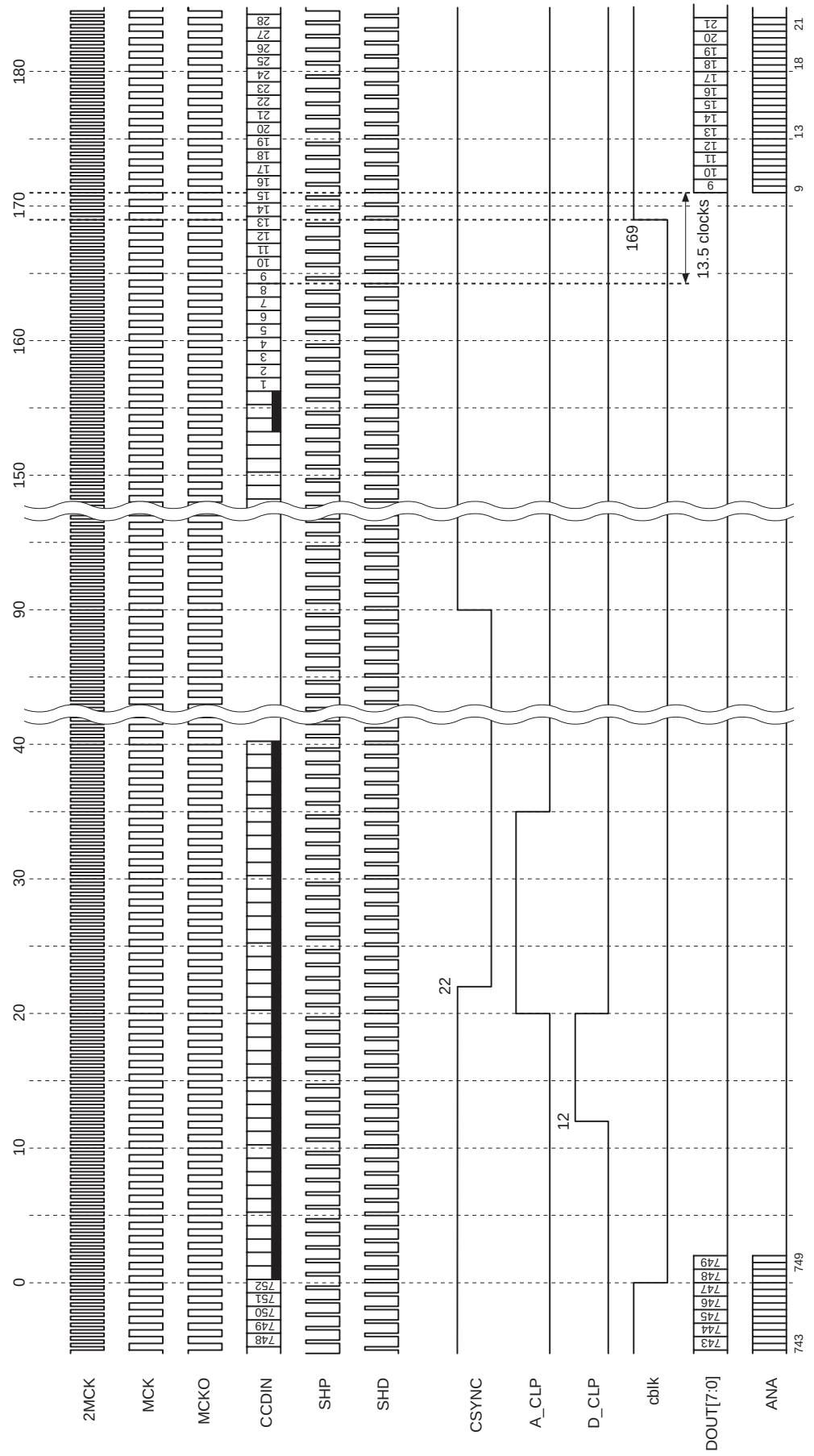
Horizontal Direction Timing Chart EIA 760H System

Count CLK = 910fH = 28.63636/2MHz

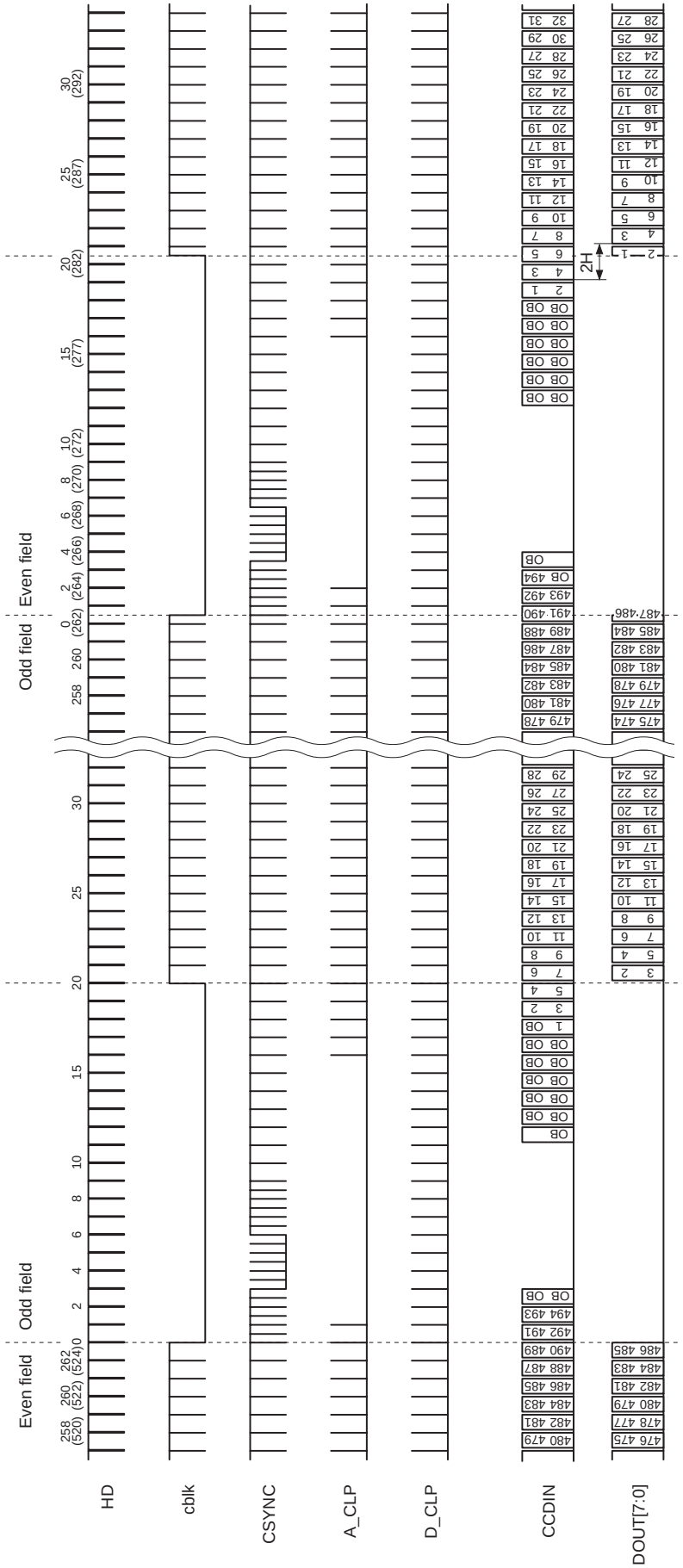


Horizontal Direction Timing Chart CCIR 760H System

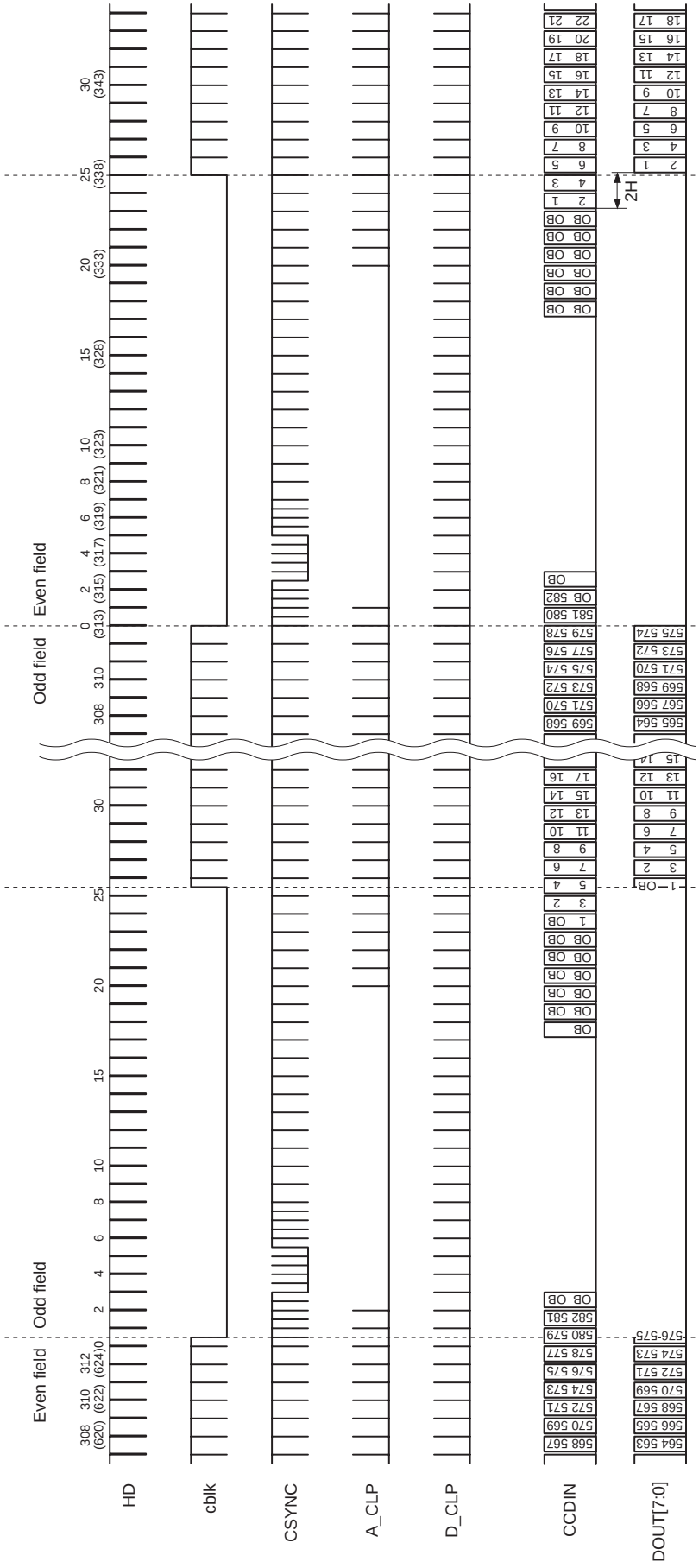
Count CLK = 908fH = 28.375/2MHz



Vertical Direction Timing Chart EIA 510H/760H System



Vertical Direction Timing Chart CCIR 510H/760H System



I²C Serial Communication

1. Description of communication

The CXD3152AR performs serial communication between a PC or an external EEPROM via the I²C bus. In communication with a PC, the PC is the master device and the CXD3152AR is the slave device. On the other hand, in communication with an EEPROM, the CXD3152AR is the master device and the EEPROM is the slave device. Communication is performed using two signal lines: SDA and SCL. SDA is a bidirectional serial data transfer line, and is used to transfer addresses from master to slave and to transfer data between master and slave. SDA is normally pulled up to V_{DD} by external resistance of several kΩ. (Therefore, SDA is high at high impedance.) SCL is a bidirectional serial clock transfer line, and is used as the data transfer synchronization clock. SCL is driven by the master device, and like SDA is pulled up to V_{DD} by external resistance of several kΩ.

2. Slave address

The CXD3152AR I²C slave address is as follows.

[A6:A0] = 0011111 (b)

3. I²C protocol

Communication conforms to the I²C bus protocol. Data transfer is started when the bus is not in the busy status. During the data transfer period, the data line must be kept stable while the clock line is high. Otherwise, data line changes while the clock line is high are interpreted as START or STOP conditions.

- **START condition**

  The START condition occurs before all commands to the device, and is defined as SDA changing from high to low when SCL is high.

- **STOP condition**

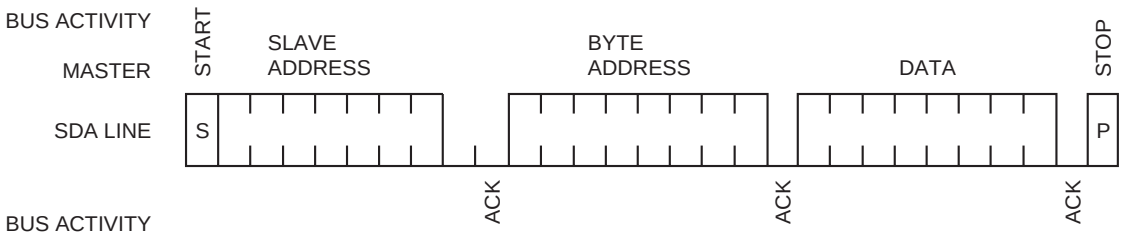
  The STOP condition is defined as SDA changing from low to high when SCL is high. All operations must end in the stop condition.

4. Communication timing

During read, the SDA data is taken in sync with the falling edge of SCL. During write, the data is output to SDA after a certain delay time from the falling edge of SCL. The communication data is MSB first. An overview of the byte-write and byte-read timings are described below.

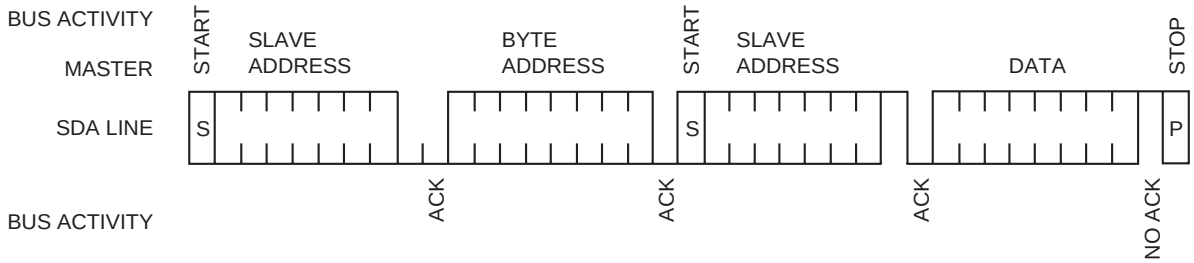
- **Byte-write timing**

  In the byte-write mode, the master device transmits the START condition and the slave address information (the R/W bit is set to 0) to the slave device. After the slave returns an acknowledgement, the master transmits the byte address to be written in the slave address pointer. After receiving the next acknowledgement from the slave, the master transfers the data to be written to the preceding address. The slave device returns an acknowledgement again, and the master generates the STOP condition.



• **Byte-read timing**

In the byte-read mode, the master device first transmits the START condition, the slave address, and the byte address of the position to be read to the slave device as a write operation. After the slave returns an acknowledgement, the master transmits the START condition and slave address (at this time the R/W bit is set to 1) again. After that, the slave issues an acknowledgement and transfers the read data. The master generates the STOP condition without transmitting an acknowledgement.



Note 1) The upper 7 bits of the slave address indicate the device address, while the lowermost bit indicates the R/W mode. (Read mode when this bit is high, and write mode when it is low.)

Note 2) The CXD3152AR slave address is [A6:A0] = 0011111 (b).

Note 3) ACK is the response acknowledgement signal, and the slave device goes to low.

Note 4) NO ACK means that a response acknowledgement signal is not returned.

Note 5) S: START condition, P: STOP condition

Description of Registers

Address	Symbol	Part symbol	bit	Description	Default	R/W
00 (h)	REGRES	REGRES	0	Register reset 0: Reset, 1: Normal (The REGRES pin (Pin 40) has precedence.)	—	W
		dummy	1			
			2			
			3			
			4			
			5			
			6			
			7			
0F (h)	WSTART	WSTART	0	Horizontal timing for write start to line memory Set in MCKI clock units 0x00 : Earliest (advanced) position 0xFE : Latest (delayed) position 0xFF : Internal fixed value EIA510 system = 67 (h) CCIR510 system = 71 (h) EIA760 system = 95 (h) CCIR760 system = A3 (h)	FF (h)	W
			1			
			2			
			3			
			4			
			5			
			6			
			7			
10 (h)	RSTART	RSTART	0	Horizontal timing for read start from line memory Set in MCKI clock units 0x00 : Earliest (advanced) position 0xFE : Latest (delayed) position 0xFF : Internal fixed value EIA510 system = 5C (h) CCIR510 system = 66 (h) EIA760 system = 89 (h) CCIR760 system = 96 (h)	FF (h)	W
			1			
			2			
			3			
			4			
			5			
			6			
			7			
14 (h)	YGAM1	YGAM1	0	Gamma correction curve adjustment-1 Sets the intersection between the 1st approximation line (slope = 1) and the 2nd approximation line (slope = 3). Setting range: 00 (h) to 1F (h)	00 (h)	W
			1			
			2			
			3			
			4			
		dummy	5			
			6			
			7			

Address	Symbol	Part symbol	bit	Description	Default	R/W
15 (h)	YGAM2	YGAM2	0	Gamma correction curve adjustment-2 Sets the intersection between the 2nd approximation line (slope = 3) and the 3rd approximation line (slope = 3/2). Setting range: 00 (h) to 3F (h)	0A (h)	W
			1			
			2			
			3			
			4			
			5			
		dummy	6			
			7			
16 (h)	YGAM3	YGAM3	0	Gamma correction curve adjustment-3 Sets the intersection between the 3rd approximation line (slope = 3/2) and the 4th approximation line (slope = 1). Setting range: 00 (h) to 7F (h)	20 (h)	W
			1			
			2			
			3			
			4			
			5			
			6			
		dummy	7			
17 (h)	YGAM4	YGAM4	0	Gamma correction curve adjustment-4 Sets the intersection between the 4th approximation line (slope = 1) and the 5th approximation line (slope = 3/4). Setting range: 00 (h) to 7F (h)	2E (h)	W
			1			
			2			
			3			
			4			
			5			
			6			
		dummy	7			
18 (h)	YGAM5	YGAM5	0	Gamma correction curve adjustment-5 Sets the intersection between the 5th approximation line (slope = 3/4) and the 6th approximation line (slope = 1/2). Setting range: 00 (h) to 7F (h)	36 (h)	W
			1			
			2			
			3			
			4			
			5			
			6			
		dummy	7			

Address	Symbol	Part symbol	bit	Description	Default	R/W
19 (h)	YGAM6	YGAM6	0 1 2 3 4 5 6	Gamma correction curve adjustment-6 Sets the intersection between the 6th approximation line (slope = 1/2) and the 7th approximation line (slope = 1/8). Setting range: 00 (h) to 7F (h) The 7th approximation line is used for knee processing.	41 (h)	W
		dummy	7			
1A (h)	HAPGAIN	HAPGAIN	0 1 2 3	Horizontal aperture correction signal gain setting The gain changes linearly from 0 (h) to 7 (h). 0 (h): ×0 F (h): Maximum gain	09 (h)	W
		dummy	4 5 6 7			
1B (h)	HAPCORE	HAPCORE1	0 1 2 3 4 5	Horizontal aperture correction signal noise suppression (coring) characteristics setting OUTPUT = INPUT – HAPCORE1 If (OUTPUT < 0), OUTPUT = 0 00 (h): Noise suppression off 3F (h): Maximum noise suppression level	02 (h)	W
		HAPCORE2	6 7	Horizontal aperture correction signal noise suppression (coring) characteristics setting OUTPUT = INPUT If (OUTPUT ≤ HAPCORE2), OUTPUT = 0 00 (h): Noise suppression off 03 (h): Maximum noise suppression level	00 (h)	
1C (h)	VAPGAIN	VAPGAIN	0 1 2 3	Vertical aperture correction signal gain setting The gain changes linearly from 0 (h) to F (h). 0 (h): ×0 F (h): Maximum gain	04 (h)	W
		dummy	4 5 6 7			

Address	Symbol	Part symbol	bit	Description	Default	R/W
1D (h)	VAPCORE	VAPCORE1	0 1 2 3 4 5	Vertical aperture correction signal noise suppression (coring) characteristics setting OUTPUT = INPUT – VAPCORE1 If (OUTPUT < 0), OUTPUT = 0 00 (h): Noise suppression off 3F (h): Maximum noise suppression level	02 (h)	W
		VAPCORE2	6 7	Vertical aperture correction signal noise suppression (coring) characteristics setting OUTPUT = INPUT If (OUTPUT ≤ VAPCORE2), OUTPUT = 0 00 (h): Noise suppression off 03 (h): Maximum noise suppression level	00 (h)	
1E (h)	APCLIP	LCLIP	0 1 2 3	Aperture correction signal minus side clip level setting OUTPUT = INPUT If (INPUT ≤ LCLIP), OUTPUT = LCLIP 0 (h): Maximum clip level F (h): Minimum clip level	04 (h)	W
		HCLIP	4 5 6 7	Aperture correction signal plus side clip level setting OUTPUT = INPUT If (INPUT ≥ HCLIP), OUTPUT = HCLIP 0 (h): Maximum clip level F (h): Minimum clip level	06 (h)	
1F (h)	AT_APCORE	AT_APCORE	0 1 2 3 4	Aperture correction signal coring level DGC link setting 0x0: Coring off 0x1F: Maximum coring level	1F (h)	W
		dummy	5 6 7			
20 (h)	YGAIN1	YGAIN1	0 1 2 3 4 5	Signal gain setting when GAMMA1 and GAMMA2 are set to 00 (gamma = 0.45)	3C (h)	W
		dummy	6 7			

Address	Symbol	Part symbol	bit	Description	Default	R/W
21 (h)	YGAIN2	YGAIN2	0	Signal gain setting when GAMMA1 and GAMMA2 are set to 10 (gamma = 0.6)	1F (h)	W
			1			
			2			
			3			
			4			
			5			
		dummy	6			
			7			
22 (h)	YGAIN3	YGAIN3	0	Signal gain setting when GAMMA1 and GAMMA2 are set to 01 (gamma = 1.0)	18 (h)	W
			1			
			2			
			3			
			4			
			5			
		dummy	6			
			7			
23 (h)	YGAIN4	YGAIN4	0	Signal gain setting when GAMMA1 and GAMMA2 are set to 11 (gamma = S)	3A (h)	W
			1			
			2			
			3			
			4			
			5			
		dummy	6			
			7			
24 (h)	PED	PED	0	Pedestal level setting The pedestal level changes linearly from 0 (h) to F (h). 00 (h): Low 17 (h): 7.5 IRE 3F (h): High	17 (h)	W
			1			
			2			
			3			
			4			
			5			
			6			
		dummy	7			

Address	Symbol	Part symbol	bit	Description	Default	R/W
25 (h)	LOWCLIP	LCLIP	0	Clip level setting for the black level and lower 0: –20 IRE, 1: Pedestal level	00 (h)	W
		dummy	1			
			2			
			3			
			4			
			5			
			6			
			7			
27 (h)	CHARA_G	CHARA_G	0	Externally input 1-bit character signal gain setting 00 (h): –85 IRE 20 (h): ±0 3F (h): +85 IRE	32 (h)	W
			1			
			2			
			3			
			4			
			5			
		dummy	6			
			7			
28 (h)	WT_CLIP	WT_CLIP	0	White clip level setting	C4 (h)	W
			1			
			2			
			3			
			4			
			5			
			6			
			7			
29 (h)	BK_CLIP	BK_CLIP	0	Video signal minus component clip level setting	1D (h)	W
			1			
			2			
			3			
			4			
			5			
		dummy	6			
			7			

Address	Symbol	Part symbol	bit	Description	Default	R/W
2A (h)	APGAM1	APGAM1	0	Aperture signal gamma correction characteristics setting Sets the intersection of the 1st approximation line (slope = 2) which passes through the origin and the 2nd approximation line (slope = 1). Setting range: 00 (h) to 3F (h)	3F (h)	W
			1			
			2			
			3			
			4			
			5			
		dummy	6			
			7			
2B (h)	APGAM2	APGAM2	0	Aperture signal gamma correction characteristics setting Sets the intersection of the 2nd approximation line (slope = 1) and the 3rd approximation line (slope = 1/2). Setting range: 00 (h) to 7F (h)	7F (h)	W
			1			
			2			
			3			
			4			
			5			
			6			
		dummy	7			
2C (h)	APSW	APSW	0	Aperture correction signal added position setting 0: After gamma correction, 1: Before gamma correction	01 (h)	W
		dummy	1			
			2			
			3			
			4			
			5			
			6			
			7			
32 (h)	AGC_REF	AGC_REF	0	Reference level setting for auto gain control integral value	18 (h)	W
			1			
			2			
			3			
			4			
			5			
			6			
		dummy	7			

Address	Symbol	Part symbol	bit	Description	Default	R/W
33 (h)	DGCMIN	DGCMIN	0 1 2 3 4 5 6 7	Digital gain control (DGC) minimum gain limiter setting Valid when DGC = 1 When DGC = 0, this is the digital gain manual setting register. 20 (h) : ×1.0 times (1F (h) and lower settings are prohibited) FF (h) : ×8.0 times	20 (h)	W
34 (h)	DGCMAX	DGCMAX	0 1 2 3 4 5 6 7	Digital gain control (DGC) maximum gain limiter setting Valid when DGC = 1 20 (h) : ×1.0 times (1F (h) and lower settings are prohibited) 0xA0 : ×5.0 times 0xFF : ×8.0 times	A0 (h)	W
35 (h)	AGCMIN	AGCMIN	0 1 2 3 4 5 6	Analog gain control (AGC) minimum gain limiter setting (Sets the upper 7 bits for gain signal generating 8-bit DAC. The lowest digit is "0".) Valid when AGC = 1 When AGC = 0, this is the analog gain manual setting register. 00 (h) : Min. 7F (h) : Max.	00 (h)	W
		dummy	7			
36 (h)	AGCMAX	AGCMAX	0 1 2 3 4 5 6	Analog gain control (AGC) maximum gain limiter setting (Sets the upper 7 bits for gain signal generating 8-bit DAC. The lowest digit is "0".) Valid when AGC = 1 00 (h) : Min. 7F (h) : Max.	59 (h)	W
		dummy	7			

Address	Symbol	Part symbol	bit	Description	Default	R/W
37 (h)	AGCWAIT	AGCWAIT	0	Auto gain control time constant setting Hold time (Hold_time) or feedback time (FB_time) can be selected by the SW setting. Hold_time = (AGCWAIT × 2 + 2) × Vt Vt: 1/60 (EIA), 1/50 (CCIR) (FB_time also uses the above formula.)	1D (h)	W
			1			
			2			
			3			
			4			
		SW	5	Hold time/feedback time selection 0: Hold_time, 1: FB_time	00 (h)	
		dummy	6			
			7			
38 (h)	AGCTM	AGCTM	0	Auto gain control feedback time setting 0: Low speed, 1: High speed	00 (h)	W
		dummy	1			
			2			
			3			
			4			
			5			
			6			
			7			
39 (h)	AGCHD	AGCHD	0	Auto gain control hold setting 0: Normal operation, 1: Hold	00 (h)	W
		dummy	1			
			2			
			3			
			4			
			5			
			6			
			7			
3A (h)	DCLP	DCLP	0	Time constant setting (00: Short, 11: Long)	3 (h)	W
			1			
			2	Insensitive range setting (0: Narrow, 1: Wide)	0	
			3	Digital clamp operation mode setting (011: V period, 100: H period) 6 bit* is also used.	1	
			4		1	
			5	Digital clamp function ON/OFF (= 1)	0	
			6*	Digital clamp operation mode setting	0	
		dummy	7			

Address	Symbol	Part symbol	bit	Description	Default	R/W
3B (h)	NEWCLPH	NEWCLPH	0	Clamp system changing (1 = New system)	1	W
		dummy	1			
			2			
			3			
			4			
			5			
			6			
			7			
3C (h)	CLPCYCL	CLPCYCL	0	Period setting (effective more than 000111) of digital clamp data renewal (setting value + one field)	1	W
			1		1	
			2		0	
			3		0	
			4		1	
			5		0	
		dummy	6			
			7			
3D (h)	HLDAREA	HLDAREA	0	Digital clamp insensitive range setting	0	W
			1		1	
			2		0	
		dummy	3			
			4			
			5			
			6			
			7			
4C (h)	MAX_N_DEF	MAX_N_DEF	0	Maximum number of registered blemishes setting Maximum 10 points	0A (h)	W
			1			
			2			
			3			
		dummy	4			
			5			
			6			
			7			

Address	Symbol	Part symbol	bit	Description	Default	R/W
5A (h)	DEFRES	DEFRES	0	Blemish detection operation reset 0: Reset, 1: Normal	01 (h)	W
		dummy	1			
			2			
			3			
			4			
			5			
			6			
			7			
64 (h)	DEF01	X[0:7]	0	Lower 8 bits of blemish pixel X address	00 (h)	R/W
			1			
			2			
			3			
			4			
			5			
			6			
			7			
65 (h)	DEF02	X[8:9]	0	Upper 2 bits of blemish pixel X address	00 (h)	R/W
			1			
		Y[0:5]	2	Lower 6 bits of blemish pixel Y address	00 (h)	
			3			
			4			
			5			
			6			
			7			
66 (h)	DEF03	Y[6:8]	0	Upper 3 bits of blemish pixel Y address	00 (h)	R/W
			1			
			2			
		D[0:4]	3	D0: EVEN Y address offset data relative to ODD 0: Offset value 0, 1: Offset value 1	00 (h)	
			4	Fixed to 1		
			5	D2: Valid data/invalid data 0: Invalid data, 1: Valid data		
			6	D3: Internal data/external data 0: External, 1: Internal		
			7	dummy		

Address	Symbol	Part symbol	bit	Description	Default	R/W
67 (h)	DEF11	Omitted: Same as DEF01				
68 (h)	DEF12	Omitted: Same as DEF02				
69 (h)	DEF13	Omitted: Same as DEF03				
6A (h)	DEF21	Omitted: Same as DEF01				
6B (h)	DEF22	Omitted: Same as DEF02				
6C (h)	DEF23	Omitted: Same as DEF03				
6D (h)	DEF31	Omitted: Same as DEF01				
6E (h)	DEF32	Omitted: Same as DEF02				
6F (h)	DEF33	Omitted: Same as DEF03				
70 (h)	DEF41	Omitted: Same as DEF01				
71 (h)	DEF42	Omitted: Same as DEF02				
72 (h)	DEF43	Omitted: Same as DEF03				
73 (h)	DEF51	Omitted: Same as DEF01				
74 (h)	DEF52	Omitted: Same as DEF02				
75 (h)	DEF53	Omitted: Same as DEF03				
76 (h)	DEF61	Omitted: Same as DEF01				
77 (h)	DEF62	Omitted: Same as DEF02				
78 (h)	DEF63	Omitted: Same as DEF03				
79 (h)	DEF71	Omitted: Same as DEF01				
7A (h)	DEF72	Omitted: Same as DEF02				
7B (h)	DEF73	Omitted: Same as DEF03				
7C (h)	DEF81	Omitted: Same as DEF01				
7D (h)	DEF82	Omitted: Same as DEF02				
7E (h)	DEF83	Omitted: Same as DEF03				
7F (h)	DEF91	Omitted: Same as DEF01				
80 (h)	DEF92	Omitted: Same as DEF02				
81 (h)	DEF93	Omitted: Same as DEF03				

Address	Symbol	Part symbol	bit	Description	Default	R/W
96 (h)	ADGC	DGC	0	Digital gain switching (Same function as DGC pin) 0: Fixed, 1: Auto	00 (h)	W
		AGC	1	Analog gain switching (Same function as AGC pin) 0: Fixed, 1: Auto	00 (h)	
		SW	2	Register setting/pin setting selection 0: Pin setting, 1: Register setting	00 (h)	
		dummy	3			
			4			
			5			
			6			
			7			
97 (h)	GAMMA	GAM1	0	Gamma correction characteristics switching (Same function as GAMMA1 and GAMMA2 pins) 00: 0.45, 01: 0.6, 10: 1, 11: S curve	00 (h)	W
		GAM2	1			
		SW	2	Register setting/pin setting selection 0: Pin setting, 1: Register setting	00 (h)	
		dummy	3			
			4			
			5			
			6			
			7			
98 (h)	BLCW	BLCW1	0	Backlight compensation window switching (Same function as BLCW1 and BLCW2 pins) 00: Full-screen photometry, 01: Lower photometry 10: Center photometry, 11: Lower + center photometry	00 (h)	W
		BLCW2	1			
		SW	2	Register setting/pin setting selection 0: Pin setting, 1: Register setting	00 (h)	
		dummy	3			
			4			
			5			
			6			
			7			

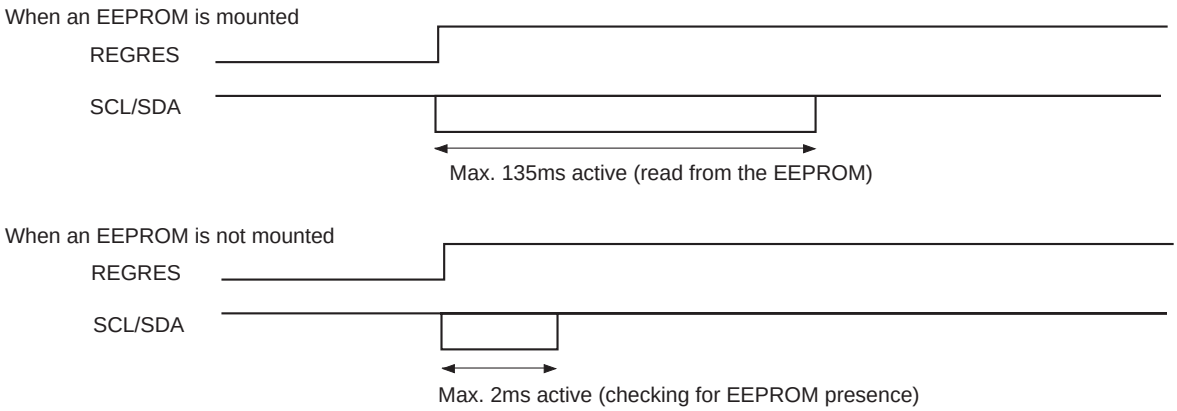
Address	Symbol	Part symbol	bit	Description	Default	R/W
99 (h)	EIA	EIA	0	TV mode switching (Same function as EIA pin) 0: EIA, 1: CCIR	00 (h)	W
		SW	1	Register setting/pin setting selection 0: Pin setting, 1: Register setting	00 (h)	
		dummy	2			
			3			
			4			
			5			
			6			
			7			
9A (h)	CCD	CCD	0	CCD number of horizontal pixels switching (Same function as CCD pin) 0: 510H system, 1: 760H system	00 (h)	W
		SW	1	Register setting/pin setting selection 0: Pin setting, 1: Register setting	00 (h)	
		dummy	2			
			3			
			4			
			5			
			6			
			7			
9B (h)	MIRROR	MIR	0	Mirror inversion switching (Same function as MIRROR pin) 0: Standard, 1: Mirror	00 (h)	W
		SW	1	Register setting/pin setting selection 0: Pin setting, 1: Register setting	00 (h)	
		dummy	2			
			3			
			4			
			5			
			6			
			7			

Address	Symbol	Part symbol	bit	Description	Default	R/W
9C (h)	APCON	APCON	0	Aperture correction switching (Same function as APCON pin) 0: Off, 1: On	00 (h)	W
		SW	1	Register setting/pin setting selection 0: Pin setting, 1: Register setting	00 (h)	
		dummy	2			
			3			
			4			
			5			
			6			
			7			
9D (h)	OVSA	DACSW	0	DA conversion frequency setting 0: 2MCKI/2, 1: 2MCKI	01 (h)	W
		dummy	1			
			2			
			3			
			4			
			5			
			6			
			7			
9E (h)	DEFECT	DEFECT	0	Blemish compensation function switching (Same function as DEFECT pin) 0: Off, 1: On	00 (h)	W
		SW	1	Register setting/pin setting selection 0: Pin setting, 1: Register setting	00 (h)	
		dummy	2			
			3			
			4			
			5			
			6			
			7			
9F (h)	DACSW	DSCSW	0	Video output DAC on/off 0: On, 1: Off	00 (h)	W
		dummy	1			
			2			
			3			
			4			
			5			
			6			
			7			

Address	Symbol	Part symbol	bit	Description	Default	R/W
A0 (h)	OEB	OEB	0	Digital output (Y0 to Y7) switching (Same function as OEB pin) 0: Output, 1: Hi-Z	00 (h)	W
		SW	1	Register setting/pin setting selection 0: Pin setting, 1: Register setting	00 (h)	
		dummy	2			
			3			
			4			
			5			
			6			
			7			
A1 (h)	CHARA	CHARA	0	1-bit character signal input switching (Same function as CHARA pin)	00 (h)	W
		SW	1	Register setting/pin setting selection 0: Pin setting, 1: Register setting	00 (h)	
		dummy	2			
			3			
			4			
			5			
			6			
			7			

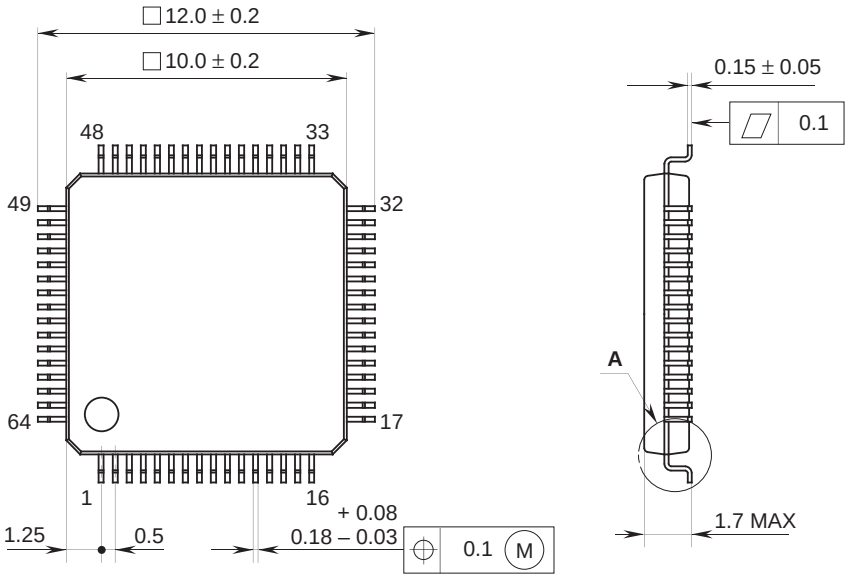
Using the EEPROM

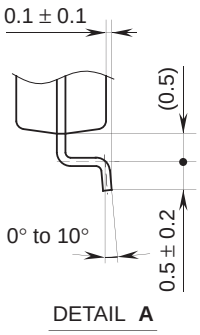
The CXD3152AR can connect an external EEPROM which supports the I^2C bus. Normally, read and write to and from the EEPROM are performed from the PC master via the I^2C bus to the slave EEPROM. Also, this IC can automatically read the user-set register values during power-on by writing the addresses and setting values for up to 64 registers in the EEPROM. (At this time this IC is the master device and the EEPROM is the slave device.)
The serial EEPROM S-24C01B made by Seiko Instruments Co., Ltd. or equivalent product can be used as the external EEPROM.
The external EEPROM load timing during power-on or register reset is shown below for when an EEPROM is mounted and not mounted. The I^2C bus is occupied by the EEPROM load at this period, so when using the I^2C bus, other communication by the master device is prohibited for the following times from the rising edge of REGRESS.



Package Outline Unit: mm

64PIN LQFP (PLASTIC)





DETAIL **A**

SONY CODE	LQFP-64P-L061
EIAJ CODE	LQFP064-P-1010-AY
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.3g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi
PLATING THICKNESS	5-18µm