SONY

CXD4017R

Reception Digital Signal Processor IC for Infrared Spatial Digital Audio Communication

Description

The CXD4017R is an IC that processes the received digital signals used for infrared spatial digital audio communication (based on the IEC61603-8-1 standard) in consumer products. This IC contains the analog-to-digital converter (ADC) for RF signal applications and a PLL circuit for audio applications.

Features

- Performs all the received digital signal processing on a single chip.
- Supports the infrared spatial digital audio communication system formats for consumer uses.
- Direct input of RF signals enabled by on-chip ADC.
- External RAM and PLL circuit not required.

Demodulator Block

- Digital processing throughout enables the received RF signals in the infrared spatial digital audio communication system formats to be processed directly.
- External analog circuit can be simplified by digital filter and on-chip ADC for RF signal applications.
- Reproduction of subcarrier processed digitally.

Error Corrector Block

- Enables error correction for infrared spatial digital audio communication system formats.

Output Interface Block

- Digital-to-analog converter (DAC) for various audio applications can be connected directly.

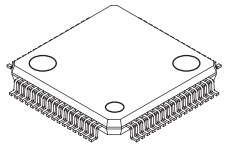
Controller Block

- Simple pin setting mode
- Serial interface provided by serial bus
- Enables output of error correction state.

PLL Block

- On-chip PLL circuit for reproducing the clock signals required by the infrared spatial digital audio communication system formats.

64 pin LQFP (Plastic)



Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

• Supply voltage	V_{DD1}	–0.5 to +3.0	V
	V_{DDE}	–0.5 to +3.0	V
• Input voltage	V_I	–0.5 to V_{DDE} + 0.5 (≤ 3.0V)	V
• Output voltage	V_O	–0.5 to V_{DDE} + 0.5 (≤ 3.0V)	V
• Storage temperature	Tstg	–55 to +125	°C

Recommended Operating Conditions

• Supply voltage	V_{DDI}	1.5 ± 0.1	V
	V_{DDE}	2.5 ± 0.2	V
• A/D supply voltage	V_{AD}	2.5 ± 0.2	V
• PLL supply voltage	V_{PLL}	1.5 ± 0.1	V
• Operating temperature	Topr	–40 to +85	°C

Input/Output Capacitance

• Input capacitance	C_{IN}	16 (max.)	pF
• Output capacitance	C_{OUT}	16 (max.)	pF

Note: Measurement conditions:

Tj = 25°C, V_{DD} = V_I = 0V, f = 1MHz

• Analog input capacitance	C_{AD}	12 (typ.)	pF

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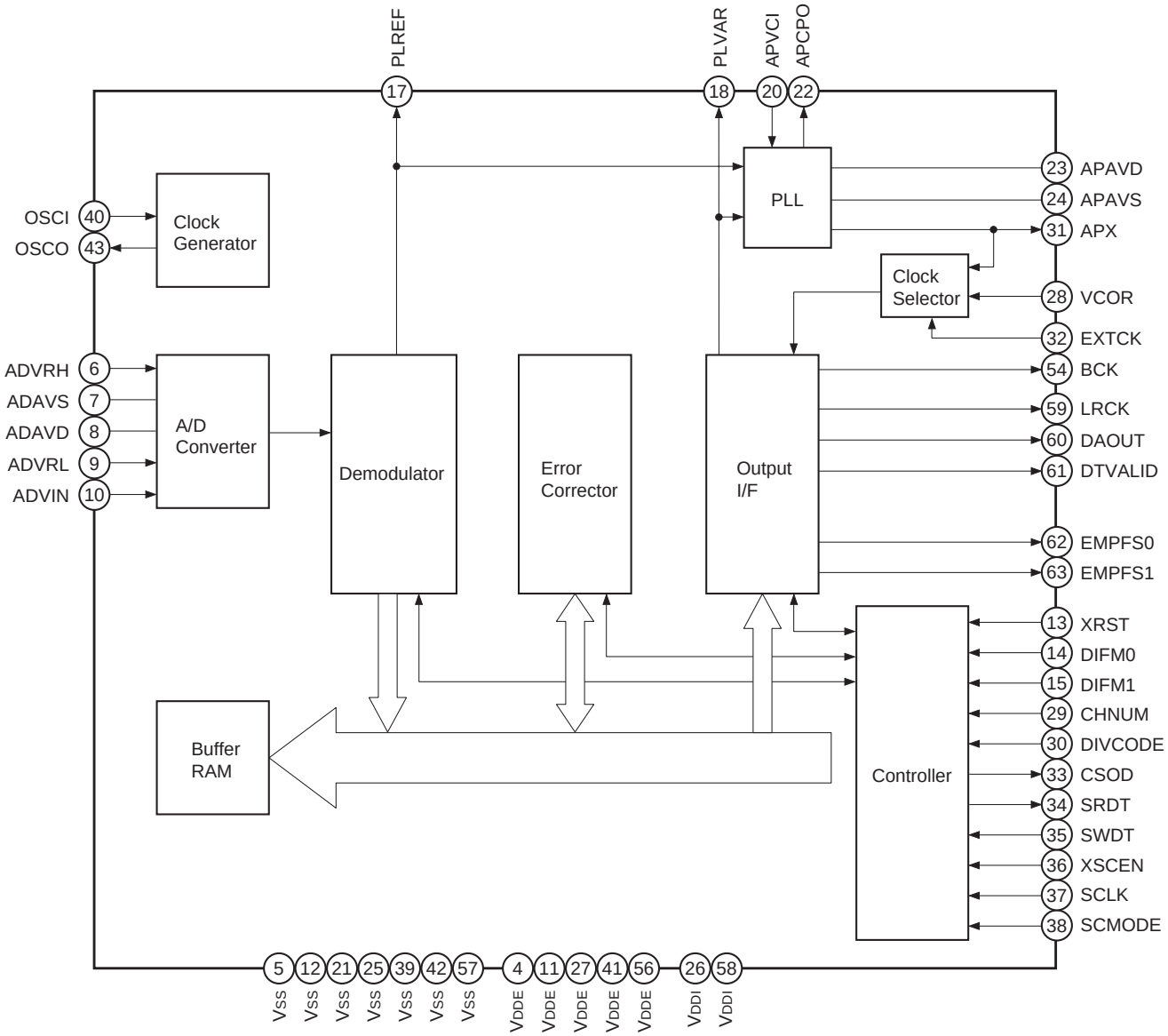
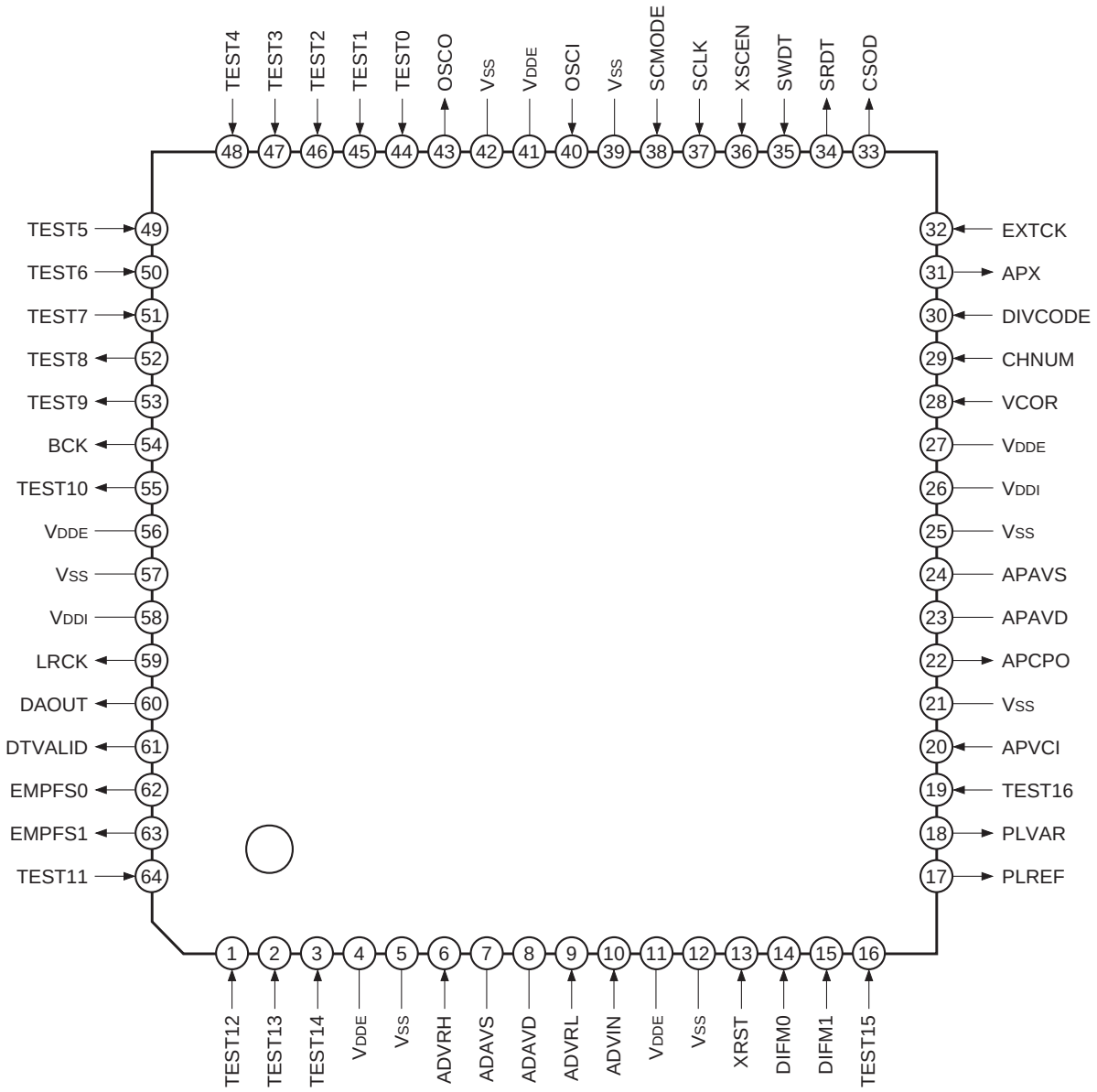
Block Diagram



* Test pins not shown.

Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	TEST12	I	Test pin, normally fixed at low
2	TEST13	I	Test pin, normally fixed at high
3	TEST14	I	Test pin, normally fixed at high
4	V_{DDE}	—	Digital I/O power supply
5	V_{SS}	—	Digital GND
6	ADVRH	I	RF ADC reference voltage input (high)
7	ADAVS	—	RF ADC analog GND
8	ADAVD	—	RF ADC analog power supply
9	ADVRL	I	RF ADC reference voltage input (low)
10	ADVIN	I	RF ADC input
11	V_{DDE}	—	Digital I/O power supply
12	V_{SS}	—	Digital GND
13	XRST	I	Reset (negative logic)
14	DIFM0	I	Audio output format selection
15	DIFM1	I	
16	TEST15	I	Test pin, normally fixed at low
17	PLREF	O	PLL reference output (fs)
18	PLVAR	O	PLL frequency-divided output (APX output or VCOR input divided by 256)
19	TEST16	I	Test pin, normally fixed at low
20	APVCI	I	PLL VCO control voltage input
21	V_{SS}	—	Digital GND
22	APCPO	O	PLL charge pump output
23	APAVD	—	PLL VCO power supply
24	APAVS	—	PLL VCO GND
25	V_{SS}	—	Digital GND
26	V_{DDI}	—	Digital internal power supply
27	V_{DDE}	—	Digital I/O power supply
28	VCOR	I	Data output clock input
29	CHNUM	I	Channel number selection (low: Ch0, high: Ch1)
30	DIVCODE	I	Full/half-band mode selection (low: full-band, high: half-band)
31	APX	O	PLL VCO output
32	EXTCK	I	Data output clock selection (low: APX internal connection, high: VCOR pin input)
33	CSOD	O	Chapter start delay output
34	SRDT	O	Serial interface data read output
35	SWDT	I	Serial interface data write output
36	XSCEN	I	Serial interface data enable input (negative logic)
37	SCLK	I	Serial interface data clock input

Pin No.	Symbol	I/O	Description
38	SCMODE	I	Control mode selection (low: pin setting, high: serial setting)
39	V_{SS}	—	Digital GND
40	OSCI	I	Crystal oscillator circuit input (12.288MHz)
41	V_{DDE}	—	Digital I/O power supply
42	V_{SS}	—	Digital GND
43	OSCO	O	Crystal oscillator circuit output (12.288MHz)
44	TEST0	I	Test pin, normally fixed at low
45	TEST1	I	Test pin, normally fixed at low
46	TEST2	I	Test pin, normally fixed at low
47	TEST3	I	Test pin, normally fixed at low
48	TEST4	I	Test pin, normally fixed at low
49	TEST5	I	Test pin, normally fixed at low
50	TEST6	I	Test pin, normally fixed at low
51	TEST7	I	Test pin, normally fixed at low
52	TEST8	O	Test pin, normally open
53	TEST9	O	Test pin, normally open
54	BCK	O	Bit clock output
55	TEST10	O	Test pin, normally open
56	V_{DDE}	—	Digital I/O power supply
57	V_{SS}	—	Digital GND
58	V_{DDI}	—	Digital internal power supply
59	LRCK	O	Audio sample clock output
60	DAOUT	O	Output data for audio DAC
61	DTVALID	O	Data valid flag output (DTVALID, low: invalid, high: valid)
62	EMPFS0	O	Emphasis, fs information output
63	EMPFS1	O	
64	TEST11	I	Test pin, normally fixed at high

Electrical Characteristics

1. DC characteristics

(V_{DDE} = 2.5 ± 0.2V, V_{DDI} = 1.5 ± 0.1V, V_{SS} = 0V, Topr = –40 to +85°C)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
High level input voltage		V_{IH}		1.7	—	V_{DDE} + 0.3	V	*1
Low level input voltage		V_{IL}		–0.3	—	0.7		
High level output voltage		V_{OH}	I_{OH} = –100µA	V_{DD} – 0.2	—	V_{DDE}		*2, 3, 4
Low level output voltage		V_{OL}	I_{OL} = 100µA	0	—	0.2		
High level output current		I_{OH}	V_{OH} = V_{DDE} – 0.4V	–4.0	—	—	mA	*2, 3
				–8.0	—	—		*4
Low level output current		I_{OL}	V_{OL} = 0.4V	4.0	—	—		*2, 3
				8.0	—	—		*4
Input leakage current		I_L		—	—	±5	µA	*1
Crystal connection pin	High level	V_{IH}		1.7		V_{DDE} + 0.3	V	*5
	Low level	V_{IL}		–0.3		0.7	V	*5
PLL supply voltage		V_{PLL}		1.4	1.5	1.6	V	*6
PLL charge pump output voltage		V_{CPO}		0		V_{PLL}	V	*7
PLL VCO control voltage		V_{VCI}		0		V_{PLL}	V	*8
ADC supply voltage		V_{AD}		2.3	2.5	2.7	V	*9
ADC reference voltage (high)		V_{RH}		1.0	2.0	V_{AD}	V	*10
ADC reference voltage (low)		V_{RL}		0.0	—	V_{AD} – 1.0	V	
ADC reference potential difference (1)		V_{RW}		1.0	2.0	2.1	V	
ADC reference input resistance (2)		R_{RW}		140	280		Ω	
ADC input voltage		V_{IA}		V_{RL}	—	V_{RH}	V	*11
ADC input capacitance		C_{AD}			12		pF	
ADC offset		V_{OFF}			20		mV	
Digital block supply current internal logic		I_{DDI}	V_{DDI} = 1.5V		7.5		mA	*12
Digital block supply current I/O		I_{DDE}	V_{DDE} = 2.5V		3.2			*13
ADC block supply current		I_{AD}	V_{AD} = 2.5V		6.7			*9
PLL block supply current		I_{PLL}	V_{PLL} = 1.5V		0.5			*6
Reference voltage pin current of A/D block		I_{REF}	V_{RW} = 2.0V		7.2	14.3		*10

Note 1: $V_{RW} = V_{RH} – V_{RL}$

Note 2: A current of approximately 7.2mA (typ.), 14.3mA (max.) flows between the ADVRH pin and ADVRL pin (when V_{RW} is 2.0V). Ensure that the drive capacity of the supply power concerned is adequate.

Applicable pins

*1 XRST, DIFM0, DIFM1, VCOR, CHNUM, DIVCODE, EXTCK, SWDT, XSCEN, SCLK, SCMODE, TEST0 to TEST7, TEST11 to TEST16
*2 CSOD, LRCK, DAOUT, DTVALID, EMPFS0, EMPFS1, TEST8
*3 SRDT
*4 PLREF, PLVAR, APX, BCK, TEST9, TEST10
*5 OSCI, OSCO
*6 APAVD, APAVS
*7 APCPO
*8 APVCI
*9 ADAVD, ADAVS
*10 ADVRL, ADVRH
*11 ADVIN
*12 V_{DDI}
*13 V_{DDE}

2. AC characteristics

(1) OSCI, OSCO pins

(a) When using self-excited oscillation

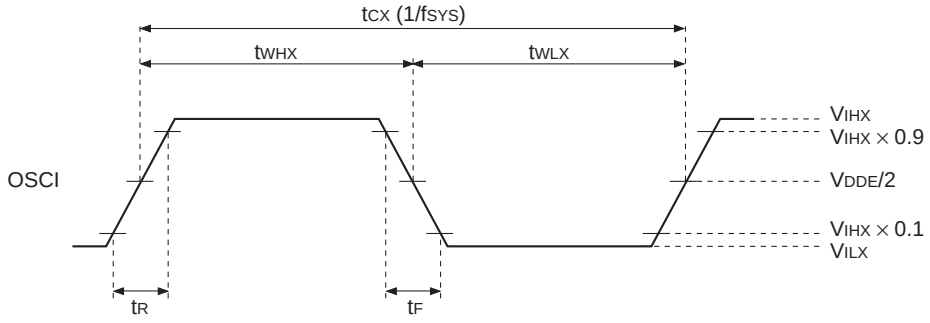
(V_{DDE} = 2.5 ± 0.2V, V_{DDI} = 1.5 ± 0.1V, V_{SS} = 0V, Topr = –40 to +85°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{SYS}	—	12.288	—	MHz

(b) When inputting pulses to OSCI

(V_{DDE} = 2.5 ± 0.2V, V_{DDI} = 1.5 ± 0.1V, V_{SS} = 0V, Topr = –40 to +85°C)

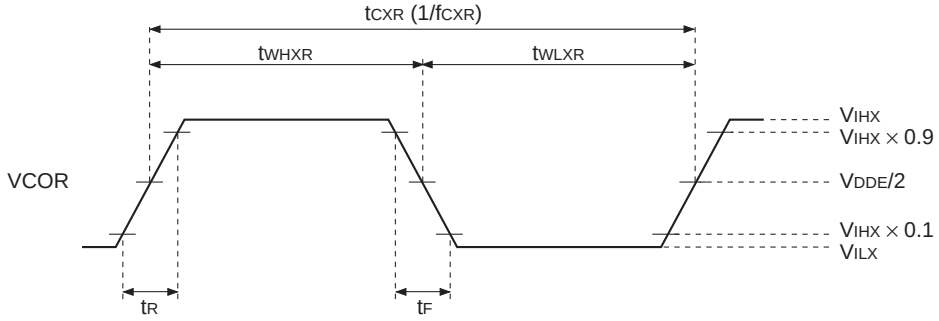
Item	Symbol	Min.	Typ.	Max.	Unit
Pulse frequency	f_{SYS}	—	12.288	—	MHz
High level pulse width	t_{WHX}	—	40.69	—	ns
Low level pulse width	t_{WLX}	—	40.69	—	ns
Rise time/fall time	t_R, t_F			5	ns



(2) VCOR pin

(V_{DDE} = 2.5 ± 0.2V, V_{DDI} = 1.5 ± 0.1V, V_{SS} = 0V, Topr = –40 to +85°C)

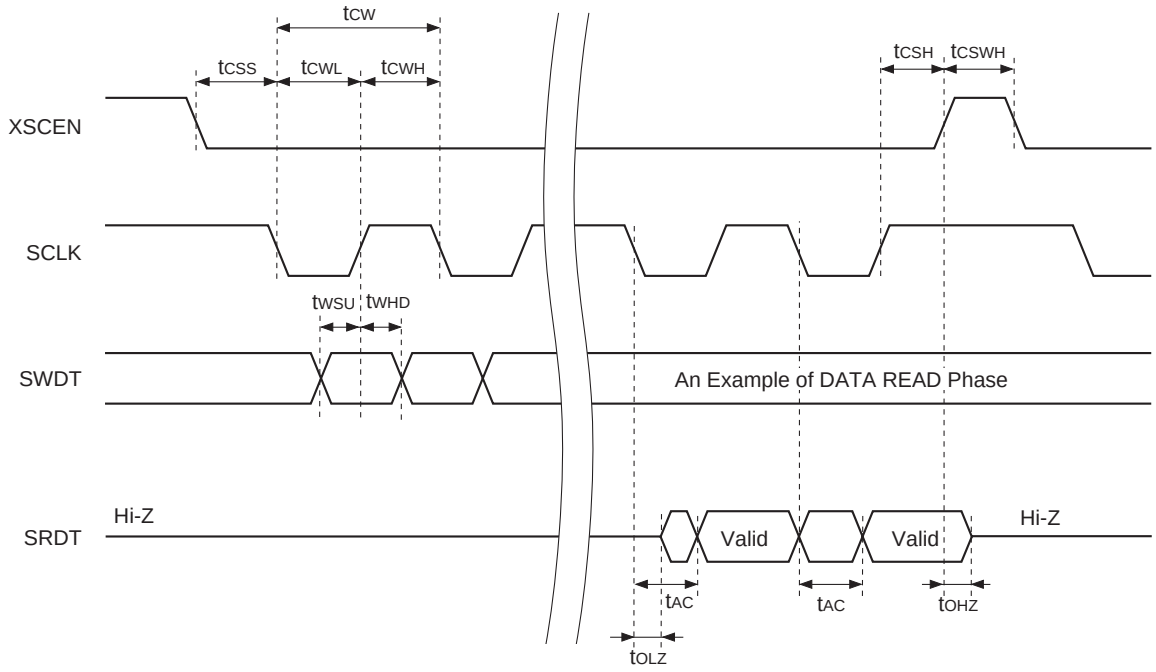
Item	Symbol	Min.	Typ.	Max.	Unit
Pulse frequency	f_{CXR}	8.176	—	12.31	MHz
High level pulse width	t_{WHXR}	t_{CXR} × 0.4	—	t_{CXR} × 0.6	ns
Low level pulse width	t_{WLXR}	t_{CXR} × 0.4	—	t_{CXR} × 0.6	ns



(3) SCLK, XSCEN, SWDT, SRDT pins

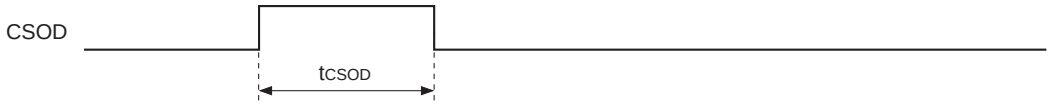
(V_{DDE} = 2.5 ± 0.2V, V_{DDI} = 1.5 ± 0.1V, V_{SS} = 0V, Topr = –40 to +85°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock period	t_{CW}	800	—	—	ns
Clock pulse width, high	t_{CWH}	400	—	—	ns
Clock pulse width, low	t_{CWL}	400	—	—	ns
Enable signal pulse width	t_{CSWH}	170	—	—	ns
Enable signal setup time	t_{CSS}	0	—	—	ns
Enable signal hold time	t_{CSH}	400	—	—	ns
Setup time	t_{WSU}	350	—	—	ns
Hold time	t_{WHD}	350	—	—	ns
Access time	t_{AC}	—	—	345	ns
Enable time	t_{OLZ}	162	—	—	ns
Disable time	t_{OHZ}	—	—	80	ns



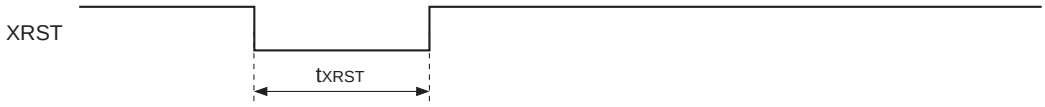
(4) CSOD pin (V_{DDE} = 2.5 ± 0.2V, V_{DDI} = 1.5 ± 0.1V, V_{SS} = 0V, Topr = –40 to +85°C)

Item	Symbol	Min.	Typ.	Max.	Unit
CSOD pulse width	t_{CSOD}	30	—	—	µs



(5) XRST pin (V_{DDE} = 2.5 ± 0.2V, V_{DDI} = 1.5 ± 0.1V, V_{SS} = 0V, Topr = –40 to +85°C)

Item	Symbol	Min.	Typ.	Max.	Unit
XRST pulse width	t_{XRST}	10.0	—	—	ns



Description of Functions

1. Description of clock generator

(1) This LSI chip can generate the system clock pulse by connecting a 12.288MHz crystal oscillator to the OSCI pin and OSCO pin.

(2) It functions as the system clock by inputting a 12.288MHz external oscillation clock pulse to the OSCI pin while keeping the OSCO pin open.

2. Description of PLL circuit

(1) In addition to supplying the system clock pulse using the OSCI pin, this LSI requires the reproduction clock pulse which is provided by the PLL circuit. The PLL circuit provided on the LSI chip can be used for this purpose.

(2) If the sampling frequency of the digital audio signals which contain the input RF signal is fs, then the reproduction clock pulse provided by the PLL circuit has a frequency of 256fs.

(3) When the PLL circuit on the LSI is used, input a low level to the EXTCK pin and VCOR pin. Furthermore, an external lag-lead filter must be connected to the LSI between the charge pump output APCPO pin and the VCO control voltage input APVCI pin of the PLL circuit. Ensure that the wiring involved is kept as short as possible.

(4) When the PLL circuit on the LSI is not used, the LSI chip must be provided with an external PLL circuit. Input a high level to the EXTCK pin and the reproduction clock pulse to the VCOR pin. The reference signal of the PLL circuit for generating the clock pulses is output to the PLREF pin, and its frequency is set to fs. At this time, the frequency of the clock pulse which has been input to the VCOR pin is divided by 256 inside the LSI, and the pulse with the resulting frequency is output to the PLVAR pin.

3. Pin setting/serial setting mode

The setting modes of this LSI can be broadly classified into two: the pin setting mode and the serial setting mode. Switching between these modes is achieved by the SCMODE pin.

Pin	Signal level	Operation
SCMODE	Low	Pin setting mode
	High	Serial setting mode

The pins of this LSI that become not significant in serial setting mode are listed below:

DIVCODE pin, CHNUM pin, DIFM0 pin, DIFM1 pin

In the serial setting mode, these pins can be set by serial setting. The rated values of the parameters which cannot be changed in pin setting mode (they can be changed in serial setting mode) are given below.

Parameter	Rated value	Operation
CRCCK	1	CRC checked.
XMUTE	1	Not muted

CRCCK is valid only when crc_flag on Source_Info is set to "1", and when the CRC check is performed, the CRC errors affect the output data.

(1) Pin setting mode

In the pin setting mode (SCMODE = low), this LSI enables the various LSI operations to be changed by the DIVCODE pin, CHNUM pin, DIFM0 pin and DIFM1 pin.

(2) Serial setting mode

In serial setting mode (SCMODE = high), this LSI enables the various LSI operations to be changed by the serial interface.

4. Description of serial interface

(1) Serial interface timings

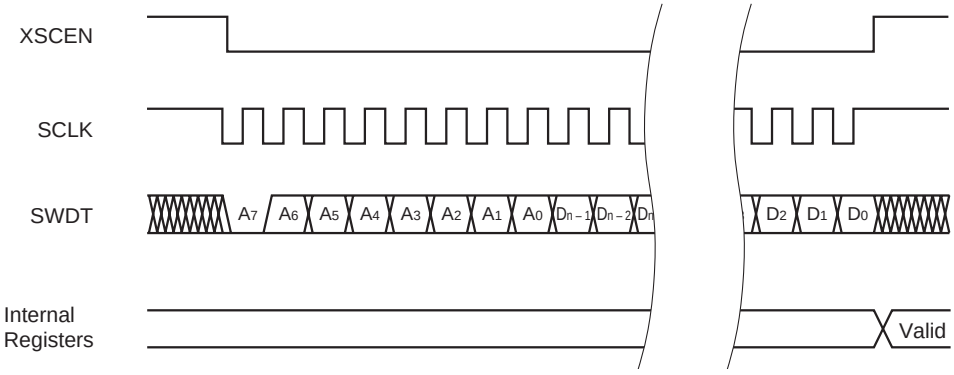
This LSI enables the various LSI operations to be changed by the SCLK pin, SWDT pin, XSCEN pin and SRDT pin. The serial interface is divided into two code groups called the write code and read code. The interface timing chart for each code group is presented below.

(2) XRST pin

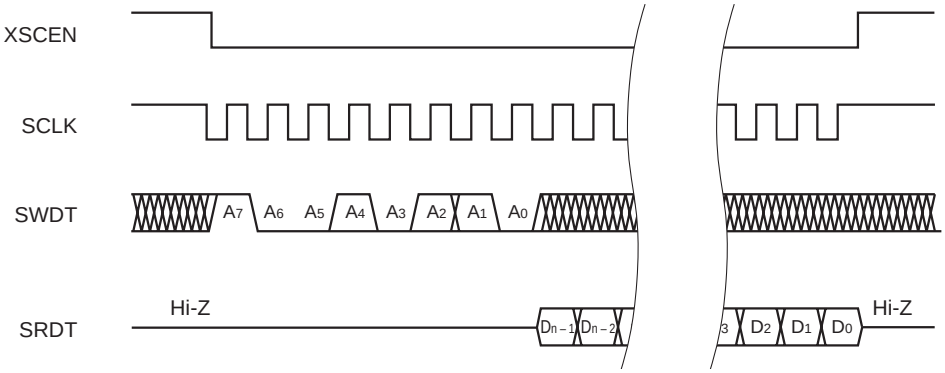
All the internal registers are initialized to "0" when reset by setting the XRST pin to low.

(3) SRDT pin

SRDT is the tri-state output pin. In order to use this pin as a quasi open drain output, the external pull-up supply voltage must be set to less than V_{DDE}. Furthermore, the external pull-up resistance must be set to a value which is within the output drive capacity (I_{OL} = 4mA).



Write Code



Read Code

(4) Serial setting command table

Address [A_7 to A_0]	Code	Command bit width	Name [D_{n-1} to D_0]	Bit width	Value	Effect
0000_0000 (00h)	Write	8	DIVCODE	1	0 1	Full-band mode Half-band mode
			CHNUM	1	0 1	Lower band Higher band
			XMUTE	1	0 1	Muted Not muted
			CRCCK*1	1	0 1	CRC not checked CRC checked
			DIFM	3	—	DAOUT output format selected
			res.	1		Reserved
1000_0110 (86h)	Read	8	CORNUM*2	8	—	Number of corrections in chapter

*1 CRCCK is valid only when crc_flag on Source_Info is set to "1", and when the CRC check is performed, the CRC errors affect the output data.

*2 This is the number of corrections in one chapter obtained from ECC.

5. Description of audio DAC interface

(1) In this LSI, the audio DAC can be directly coupled. If the on-chip PLL circuit is used, a 256fs clock pulse is output to the APX pin.

DAOUT: DAC data
BCK: DAC bit clock pulse
LRCK: DAC sample clock pulse
DTVALID: Data valid flag (low: invalid, high: valid)

(2) The emphasis and sampling frequency information is output to the EMPFS0 pin and EMPFS1 pin.

EMPFS1	EMPFS0	Emphasis	Sampling frequency
Low	Low	Not provided	No information
Low	High	Provided	44.1kHz
High	Low	Provided	48kHz
High	High	Provided	32kHz

(3) The data valid flag DTVALID indicates the valid_flag contained in the Source_Info and the errors in communication. When this pin is low, it indicates that the valid_flag is "0" or that some kind of error, including any errors in the input signals at the transmission end, has occurred at some point after these signals were input.

(4) Sixty-four BCK cycles are contained in one LRCK cycle.

(5) The DAOUT output format can be changed by the DIFM register (3 bits) with address 00h when SCMODE is high (serial setting mode) and by the DIFM1 pin and DIFM0 pin when SCMODE is low (pin setting mode).

Output mode	SCMODE = High	SCMODE = Low	
	DIFM	DIFM1	DIFM0
Mode-0	000	Low	Low
Mode-1	001	Low	High
Mode-2	010	High	Low
Mode-3	011	High	High
Mode-4	100	No settings possible	
Mode-5	101		
Mode-6	110		
Mode-7	111		

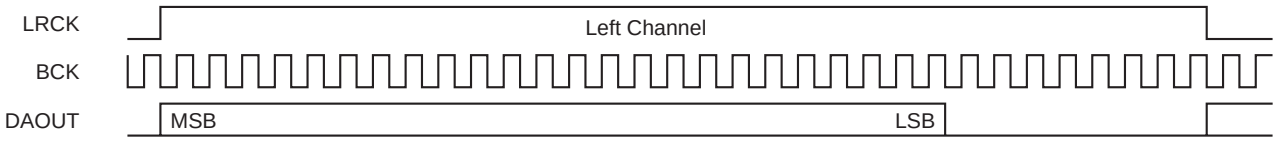
Output mode	Data output format	
	Full-band	Half-band
Mode-0	MSB first, Left Justified	MSB first, Left Justified
Mode-1	I^2S	I^2S
Mode-2	MSB first, 16 bits, Right Justified	MSB first, 16 bits, Right Justified
Mode-3	MSB first, 24 bits, Right Justified	MSB first, 16 bits + 8 bits (zero data), Right Justified
Mode-4	MSB first, 20 bits, Right Justified	MSB first, 16 bits + 4 bits (zero data), Right Justified
Mode-5	LSB first, Right Justified	LSB first, Right Justified
Mode-6	—*1	LSB first, Right Justified
Mode-7	—*1	

*1 Connection cannot be made to the DAC since these are special formats.

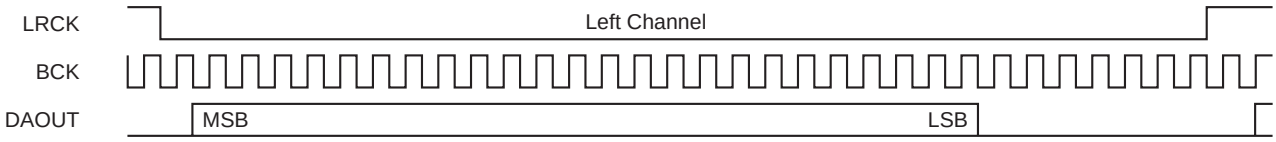
*2 In modes 0 to 5, the data is output only when pcm_id on the Source_Info is output.

Timing charts covering what has been described above are presented below.

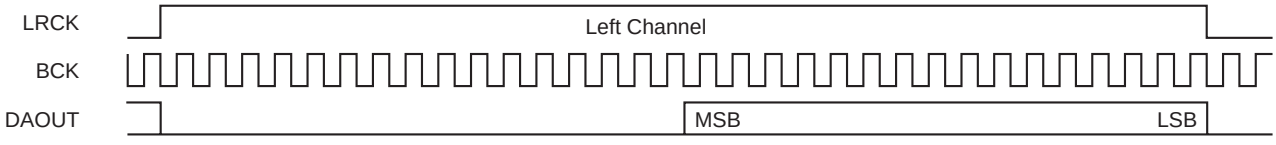
Audio DAC interface timing charts



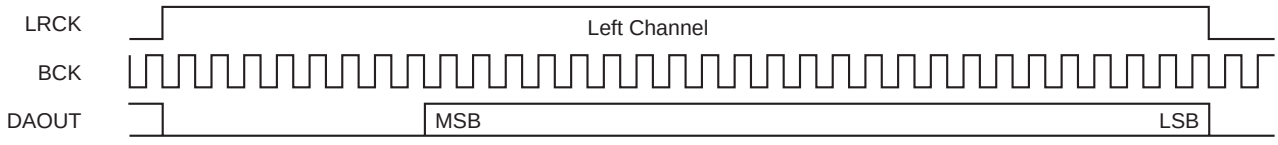
Full-band, Mode-0



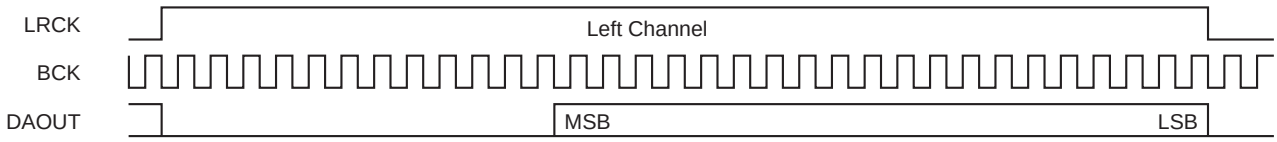
Full-band, Mode-1



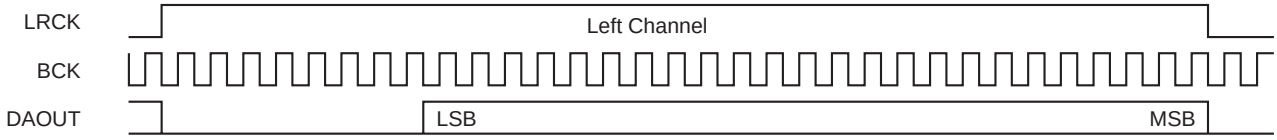
Full-band, Mode-2



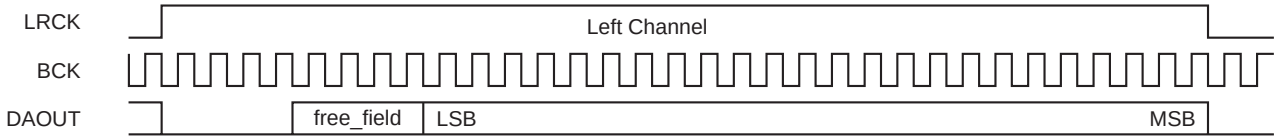
Full-band, Mode-3



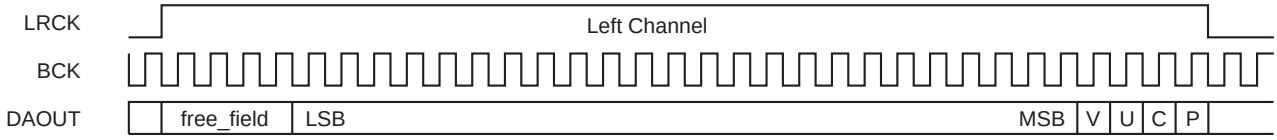
Full-band, Mode-4



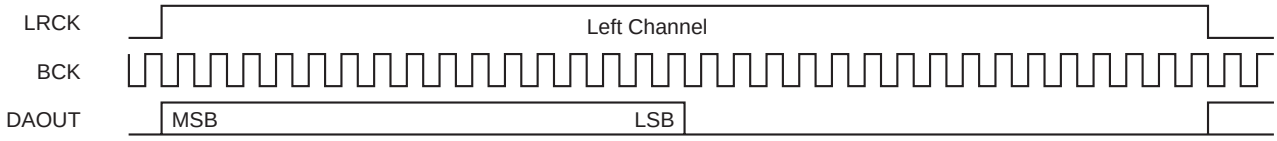
Full-band, Mode-5



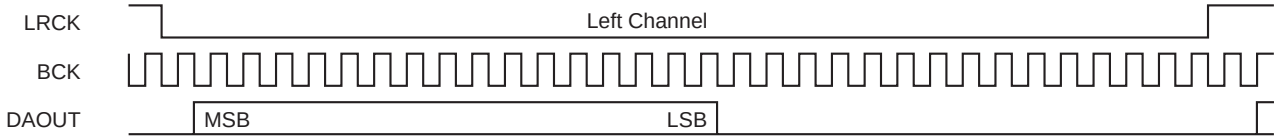
Full-band, Mode-6



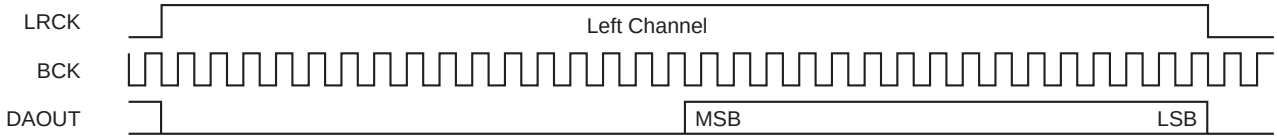
Full-band, Mode-7



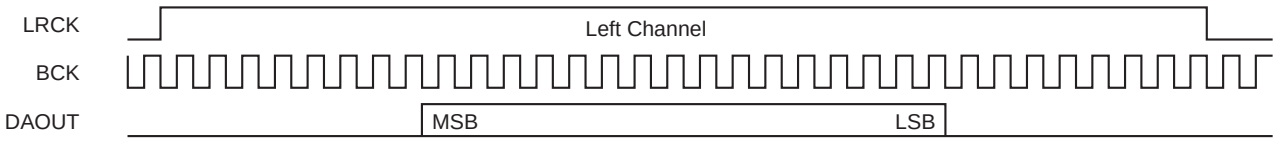
Half-band, Mode-0



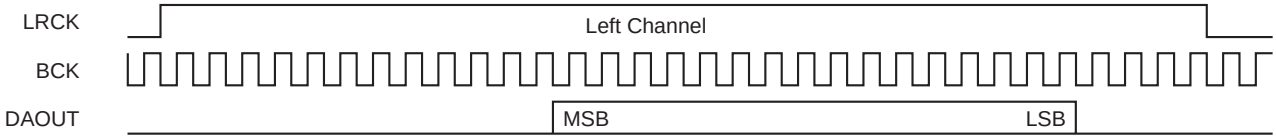
Half-band, Mode-1



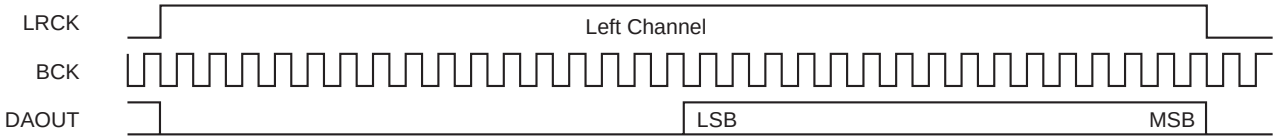
Half-band, Mode-2



Half-band, Mode-3



Half-band, Mode-4



Half-band, Mode-5, 6, 7

6. Description of other functions

(1) Mute conditions

The conditions under which muting occurs are more or less as listed below.

- When the RF signal cannot be received due to cutoff or some other such reason
  In this case, the signal is muted as soon as it could not be received.
- When many errors have occurred due to poor reception
  In this case, the signal is muted as soon as it is deemed that a high number of errors have occurred.
- When the prescribed time has not elapsed after the signal was muted due to cutoff or some other such reason
  In this case, the muting is released after the prescribed time has elapsed since it was deemed that the RF signal received is problem-free.
- When the PLL lock was not applied
  The muting is released after the prescribed time has elapsed since the PLL lock was applied.
- When the XMUTE pin was set to "0" at address 00h
  In this case, the signal is instantly muted immediately after the setting. The muting is instantly released immediately after the XMUTE pin is set to "1".

(2) CSOD

The read parameters of the Read Code based on the serial interface are updated on a chapter by chapter basis in the infrared spatial digital audio communication system format. The CSOD pin output indicates a break in the chapter in response to the issue of this command. Access the Read Code within 3ms after the CSOD pin has changed from high to low.

(3) CORNUM

Feed forward errors are corrected in the infrared spatial digital audio communication system format. At the reception end, the errors are corrected using this parity. The number of symbols (bytes) whose errors have been corrected this way can be counted up. The number obtained by the countup for each chapter is output as the CORNUM. CORNUM takes the following values.

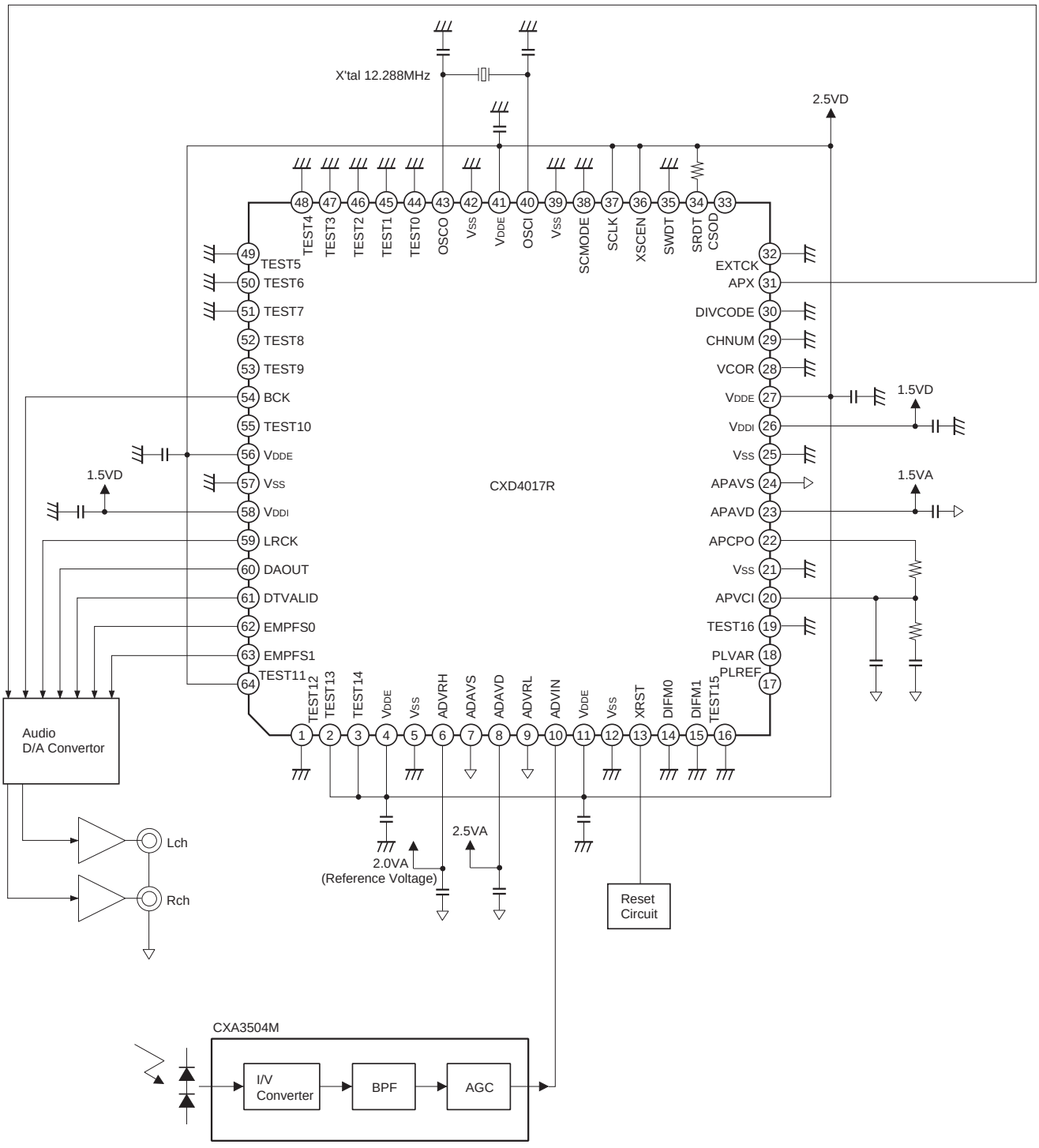
Name	Value	
CORNUM	Min.	Max.
	0	165

(4) DTVALID

This signal, which is the data valid flag, is set to high when all of the following conditions have been met.

- The number of times errors cannot be corrected in a chapter in the error correction circuit must not exceed 2.
- No CRC errors must have occurred. (Operation can be changed by serial interface address 00h and CRCCK.)
- The SYNC pattern of the received signals must have been detected properly.
- The digital audio sample frequency must be locked.
- The header signals among the received signals must coincide in multiple ways.
- The synchronization timing in the output interface block must be locked to the start of the chapter of the received signals.
- The XMUTE internal signal described above must be set to "1" (XMUTE is "1" when SCMODE is at low, and its setting can be changed by the serial interface when SCMODE is at high).

7. Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

- The loop filter portion of the PLL block is important for the characteristics. Therefore, the loop filter should be located as close to the IC pin as possible and surrounded by AGND. In addition, temperature compensation parts should be used for the loop filter capacitor and resistor.

- The CXD4017R generates a delay during reception. Labeling the sampling frequency as fs, the delay time is 384/fs [s] in full-band mode. For example, when fs = 48kHz, the delay time is 8ms. In addition, in half-band mode the delay time is 768/fs [s]. In this case for example, when fs = 48kHz, the delay time is 16ms. Note that a delay is also generated during transmission by the transmission side IC CXD4016R. See the CXD4016R data sheet for details.

CXD4017R Evaluation Board

Description

The CXD4017R evaluation board is a dedicated board designed to allow easy evaluation of the CXD4017R which was developed for reception of infrared spatial digital audio communication.
An infrared spatial digital audio communication system format RF signal which is input from a SMB connecter is demodulated to a digital audio signal, and is converted to an analog audio signal by an internal audio DAC, then is output as pin jack or headphone output.
The number of corrections can be displayed on the LED, so the receiving state can be confirmed visually.

Features

- Supply voltage: ±5V power supply
- Displays the number of corrections on the LED
- 2 audio outputs; pin jack and headphone output

Operating Conditions

- Supply voltage: ±5V (typ.)
- Current consumption: +5V: 180mA (typ.), –5V: 10mA (typ.)

Operation Method

The CXD4017R evaluation board allows easy evaluation simply by providing the power supply and inputting an infrared spatial digital audio communication system format RF signal. The evaluation procedure is as follows.

(1) Connect the power supply to the power supply connection pin J6.
(2) SW1 is the manual reset switch. A reset is applied automatically during power-on, but this switch is used to perform reset manually.
(3) The DIVCODE pin can be set by DIP switch S1-1. The DIVCODE pin is set low when this switch is OFF, and high when ON.
(4) The CHNUM pin can be set by DIP switch S1-2. The CHNUM pin is set low when this switch is OFF, and high when ON.
(5) The SCMODE pin can be set by DIP switch S1-3. The SCMODE pin is set low when this switch is OFF, and high when ON
(6) The DIFM2 pin can be set by DIP switch S1-4. The DIFM2 pin is set low when this switch is OFF, and high when ON
(7) The DIFM1 pin can be set by DIP switch S1-5. The DIFM1 pin is set low when this switch is OFF, and high when ON
(8) The DIFM0 pin can be set by DIP switch S1-6. The DIFM0 pin is set low when this switch is OFF, and high when ON

(9) Always set DIP switches other than noted above to OFF. The above contents are listed in the tables below for reference.

S1	Mode
1	OFF: DIVCODE = L, ON: DIVCODE = H
2	OFF: CHNUM = L, ON: CHNUM = H
3	OFF: SCMODE = L, ON: SCMODE = H
4	OFF: DIFM2 = L, ON: DIFM2 = H
5	OFF: DIFM1 = L, ON: DIFM1 = H
6	OFF: DIFM0 = L, ON: DIFM0 = H
7	Always OFF
8	Always OFF

S2	Mode
1	Always OFF
2	Always OFF
3	Always OFF
4	Always OFF
5	Always OFF
6	Always OFF
7	Always OFF
8	Always OFF

(10) Light emitting diode D1 is off when DIVCODE is low, and lighted when DIVCODE is high.

(11) Light emitting diode D2 is off when CHNUM is low, and lighted when CHNUM is high.

(12) Light emitting diodes D3 and D4 indicate the sampling frequency of the audio signal. This relationship is shown in the table below.

D3, D4	Sampling frequency
Off, off	44.1kHz
Off, lighted	48kHz
Lighted, lighted	32kHz
Flashing, flashing	Unlock

(13) Light emitting diodes D5 to D8 are not used.

(14) Light emitting diodes D9 to D15 display the number of error corrections. This is the total error correction numbers during time for 48 chapters. The relationship between lighting of light emitting diodes and the number of error corrections is shown in the table below.

D9	Lighted with 1 error correction or more
D10	Lighted with 3 error corrections or more
D11	Lighted with 9 error corrections or more
D12	Lighted with 27 error corrections or more
D13	Lighted with 81 error corrections or more
D14	Lighted with 243 error corrections or more
D15	Lighted with 729 error corrections or more

(15) Light emitting diode D16 is off when DTVALID is high, and lighted when DTVALID is low.

(16) Connection pins J3,J4, J7 and J9 are not used.

(17) Audio signal outputs LINE OUT and Headphone OUT are available. For headphone OUT, the output level can be adjusted by RV1.

CXD4017R EVB Semiconductor Parts List

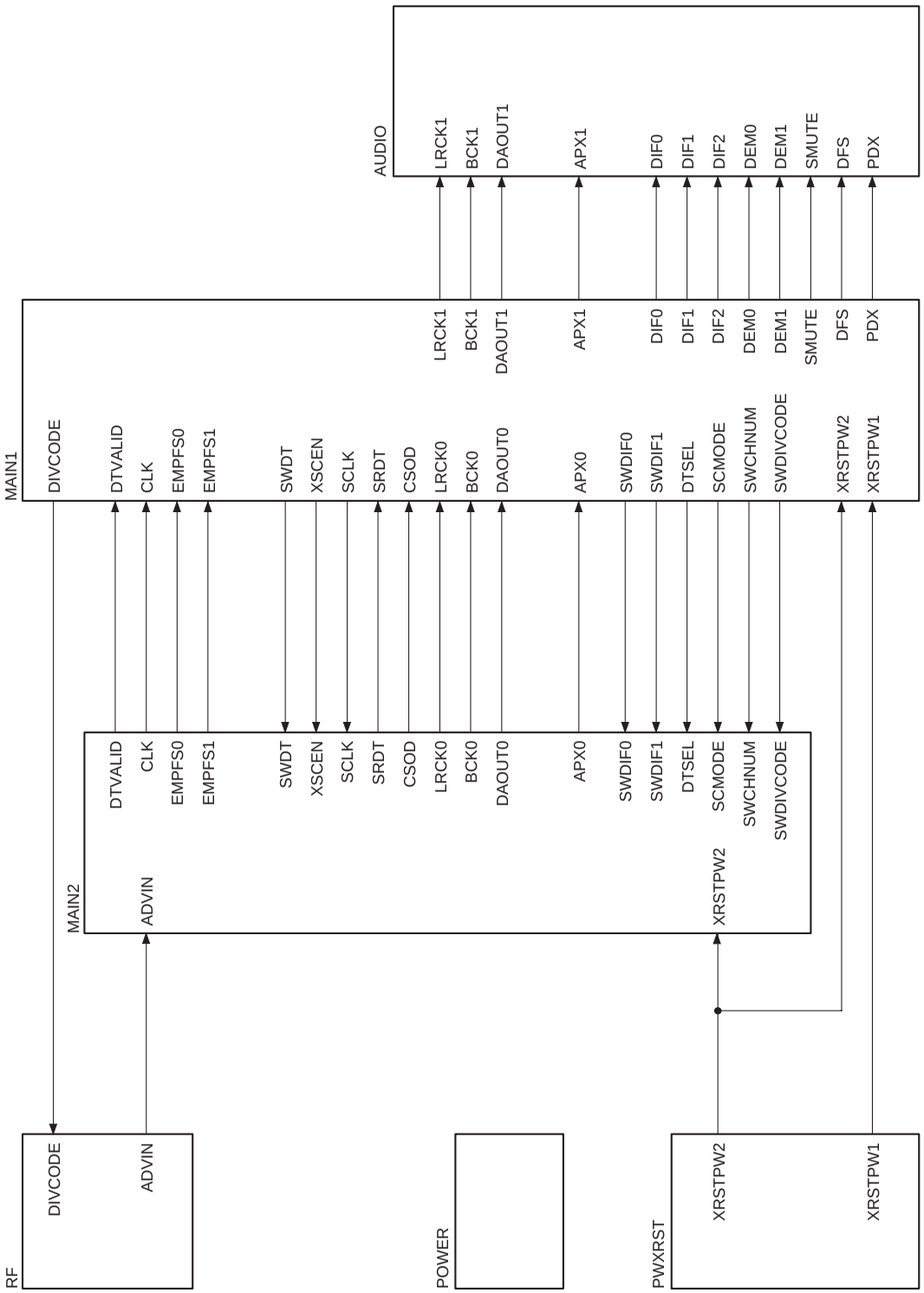
Parts No.	Product name	Manufacturer
U1, 5	NJM5532M	New Japan Radio
U2, 4	TC74HCT541F	Toshiba
U3	AK4393VF	Asahi Kasei Microsystems
U6	EP1K100QI208-2	ALTERA
U7	EPC2LI20	ALTERA
U8	CXD4017R	SONY
U9, 10, 11	LM317T	National Semiconductor
U12, 13	TL7705CP	Texas Instruments
U14	TC74LCX541F	Toshiba
Q1	2SC2223L	NEC
D1, 2, 9, 10	TLG124	Toshiba
D3, 4, 11, 12	TLY124	Toshiba
D5, 6, 13, 14	TLO124	Toshiba
D7, 8, 15, 16	TLR124	Toshiba
D17 to 22	1S1588	Toshiba

FPGA Operation

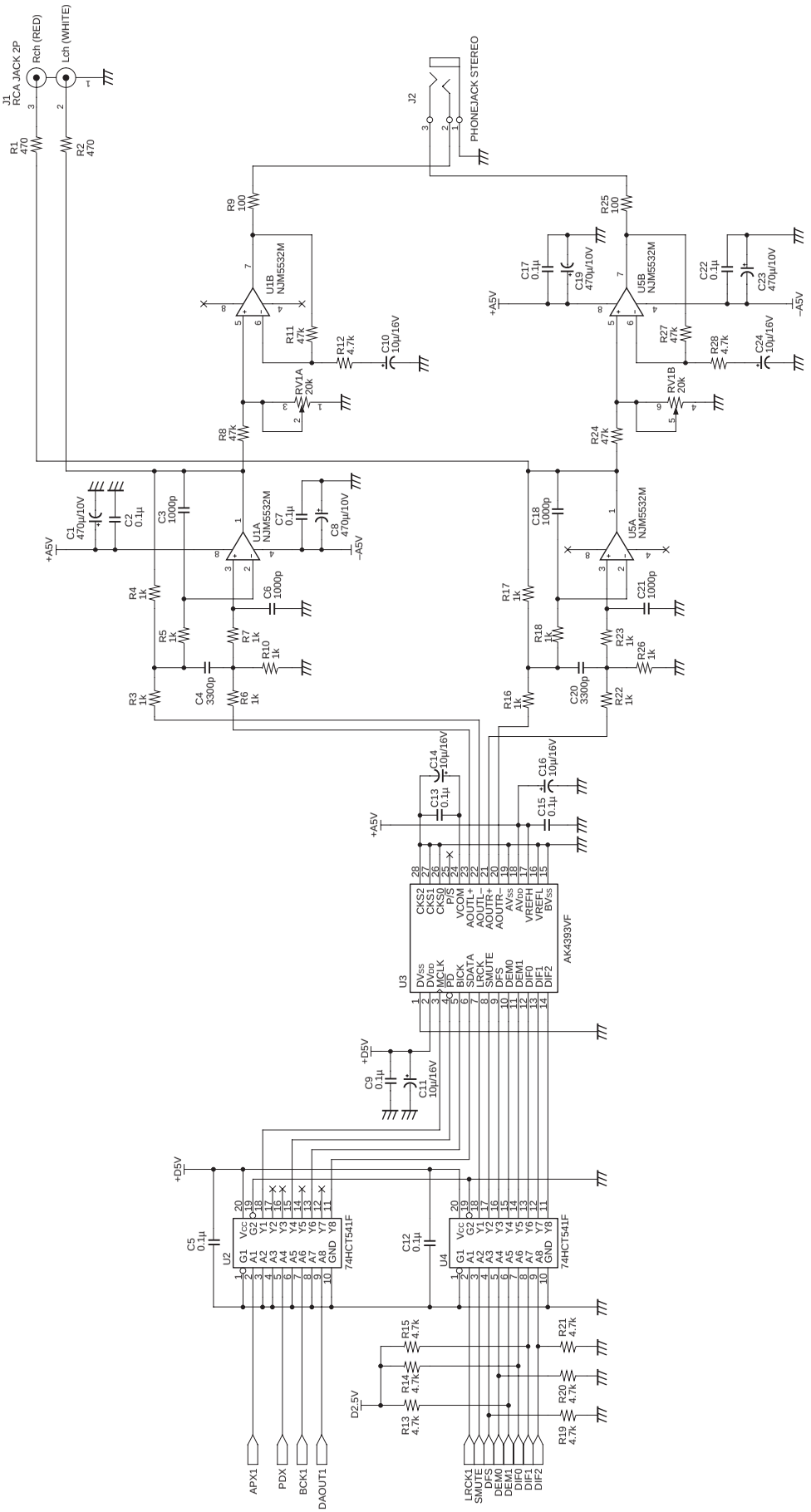
(1) Accumulates the number of error corrections, and displays.

(2) Detects the sampling frequency.

Circuit Diagram

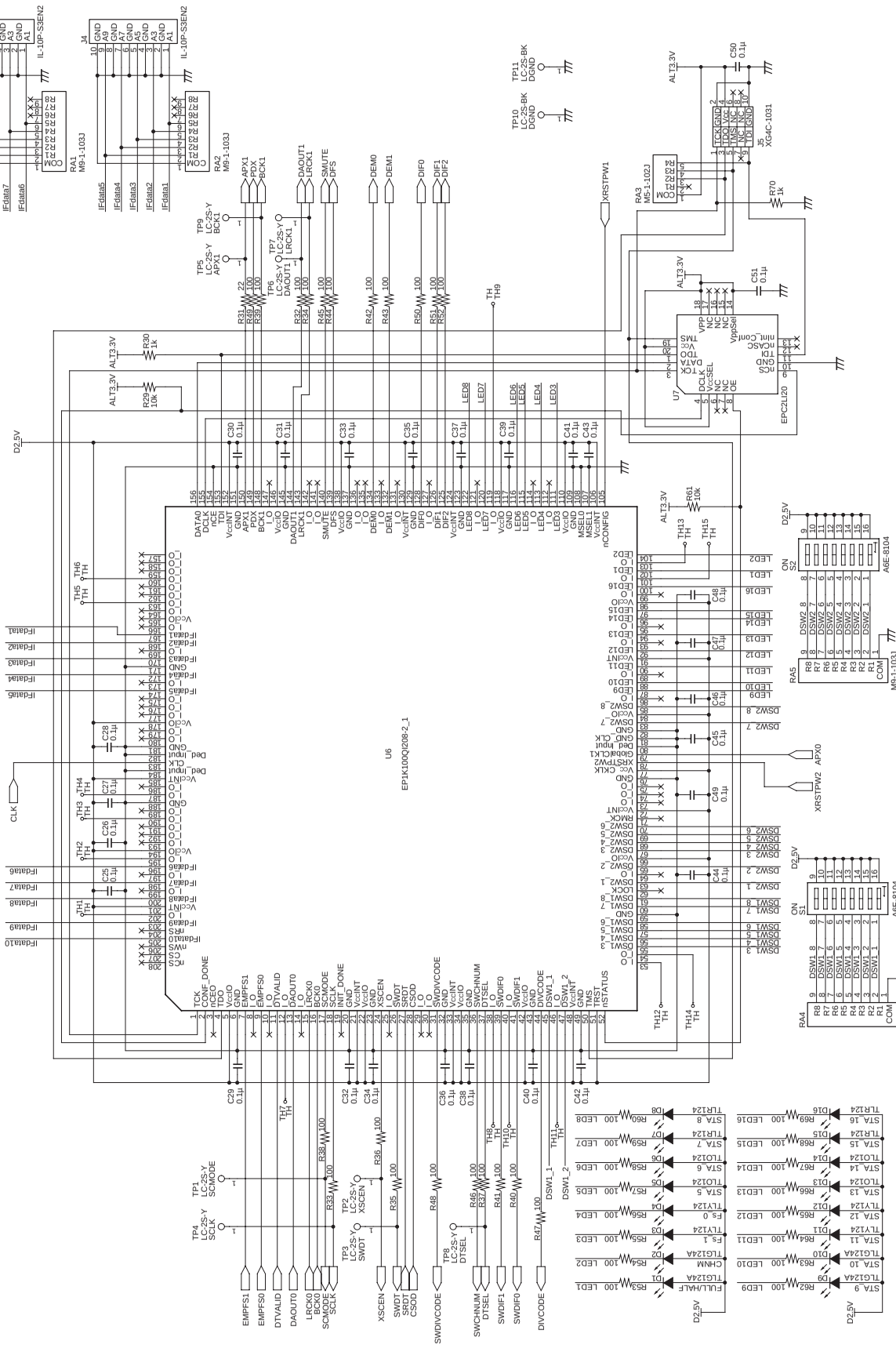


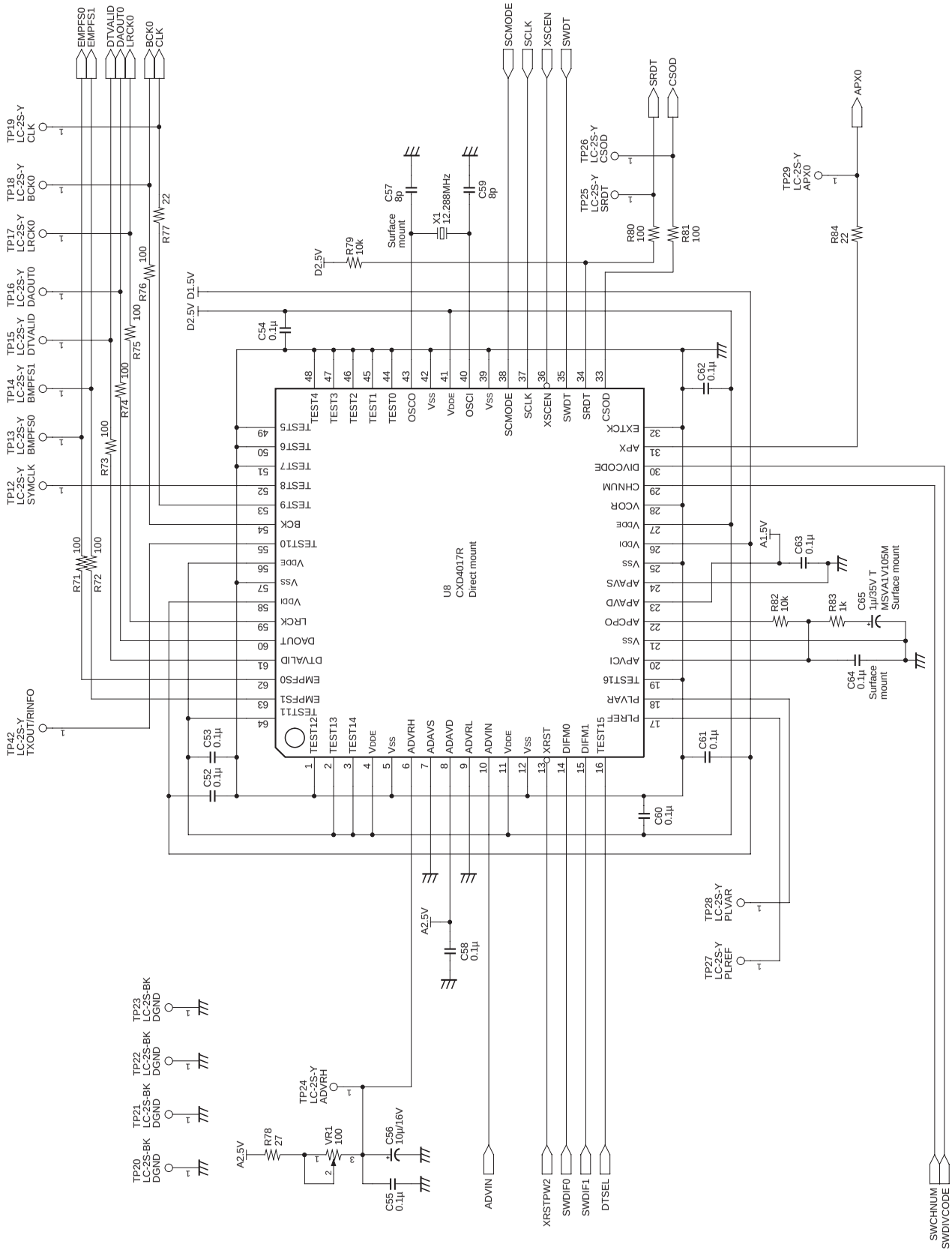
CXD4017R EVB Circuit Diagram (TOP)



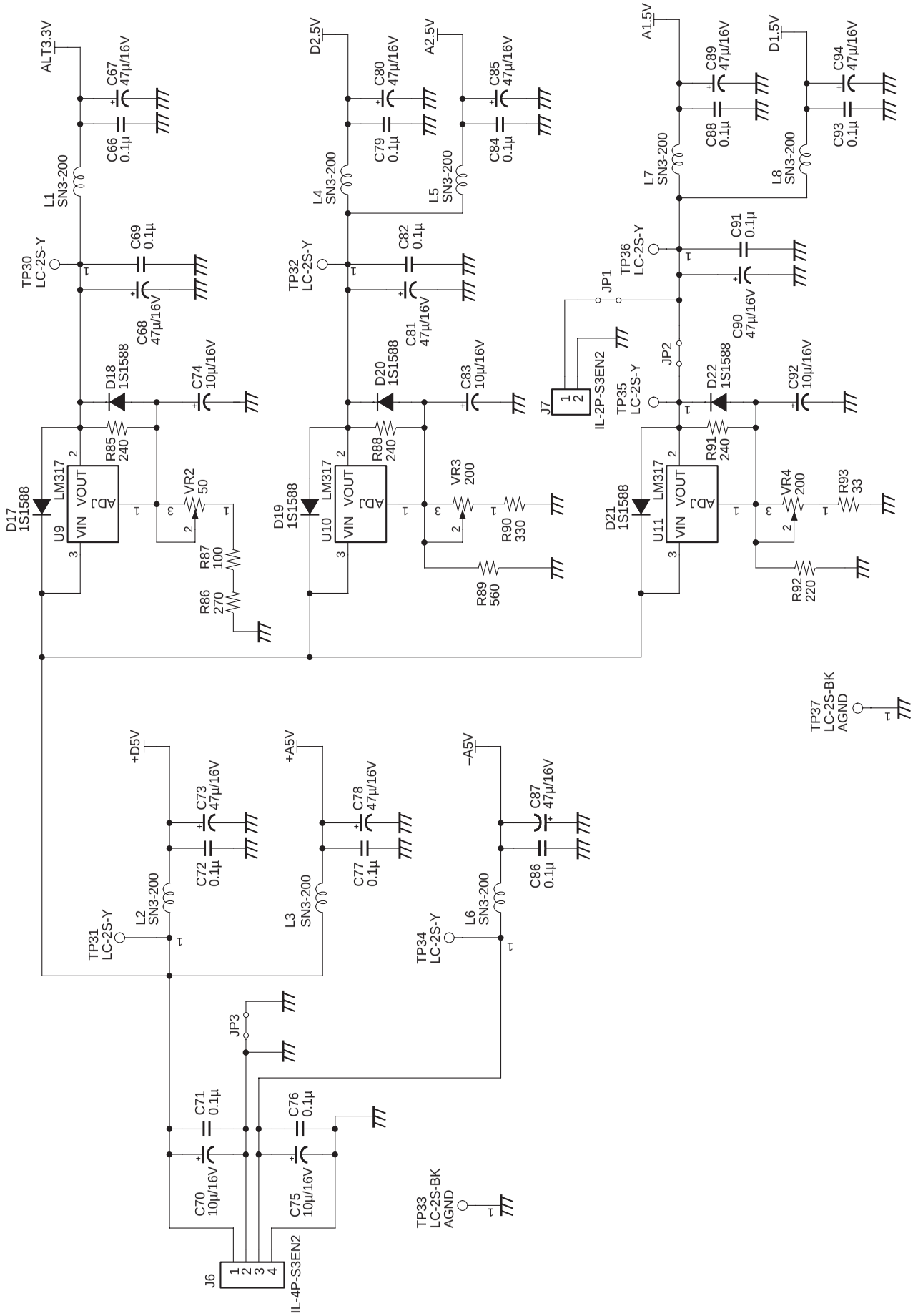
CXD4017R EVB Circuit Diagram (AUDIO)

CXD4017R EVB Circuit Diagram (PLD)

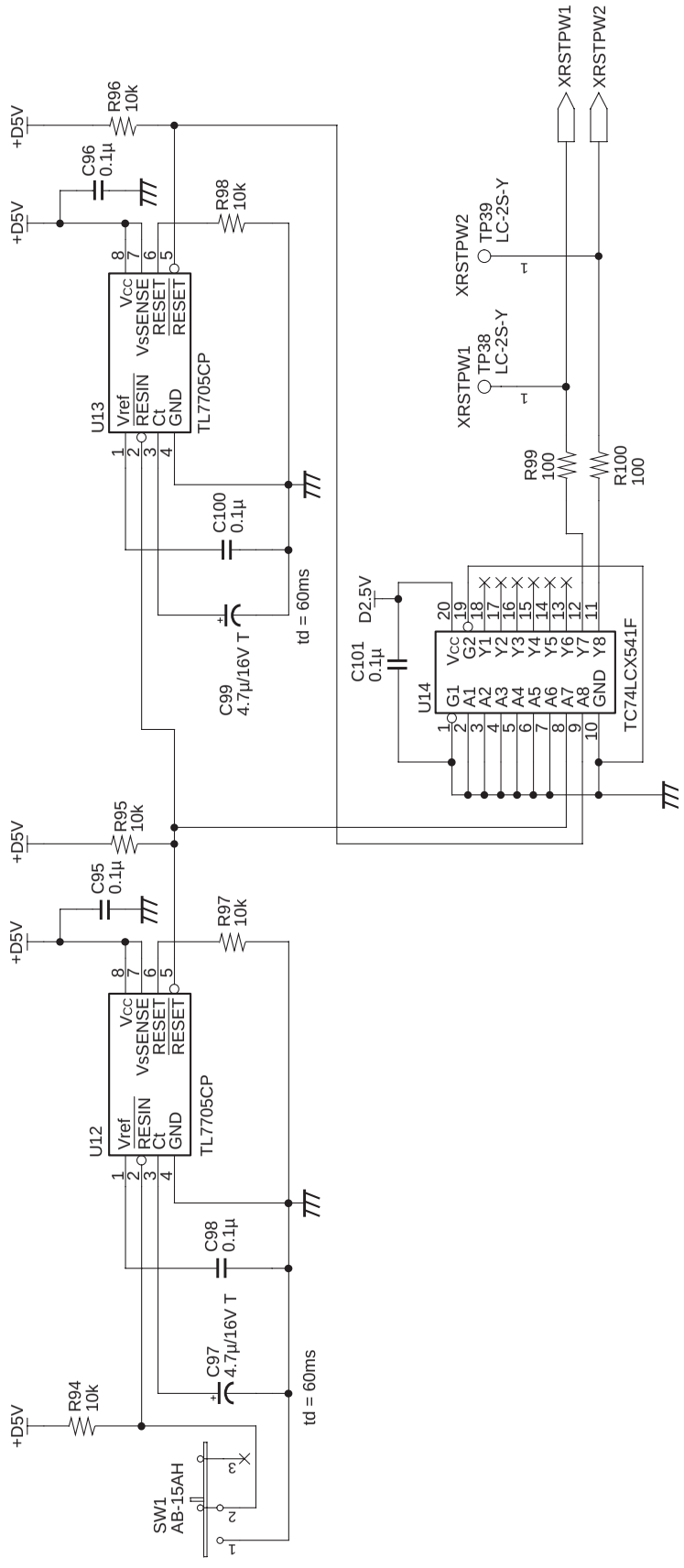




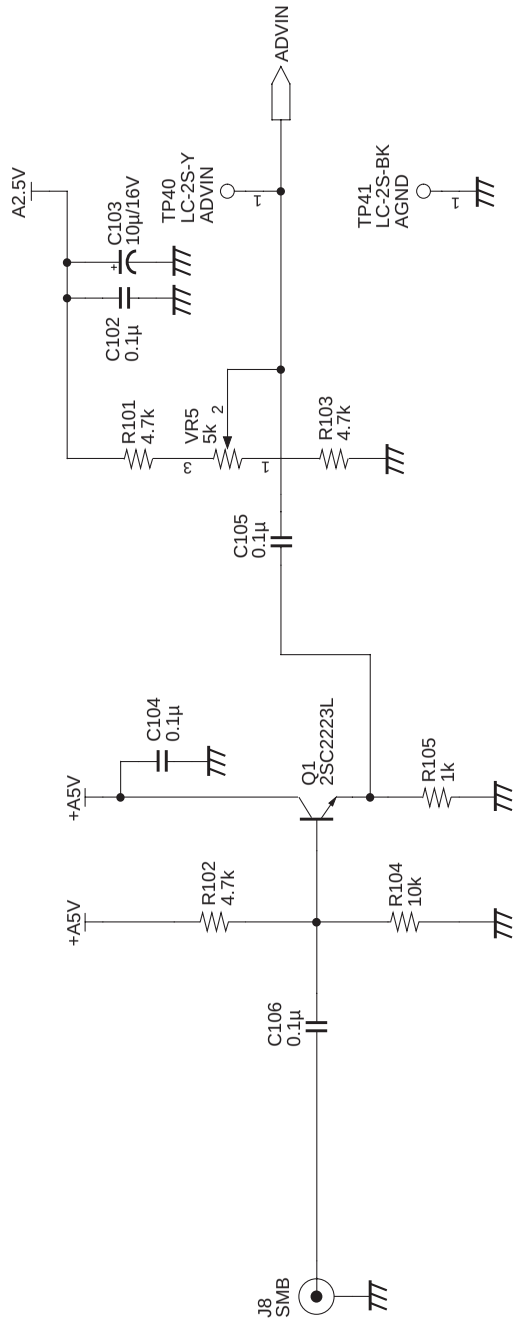
CXD4017R EVB Circuit Diagram (MAIN)



CXD4017R EVB Circuit Diagram (POWER)

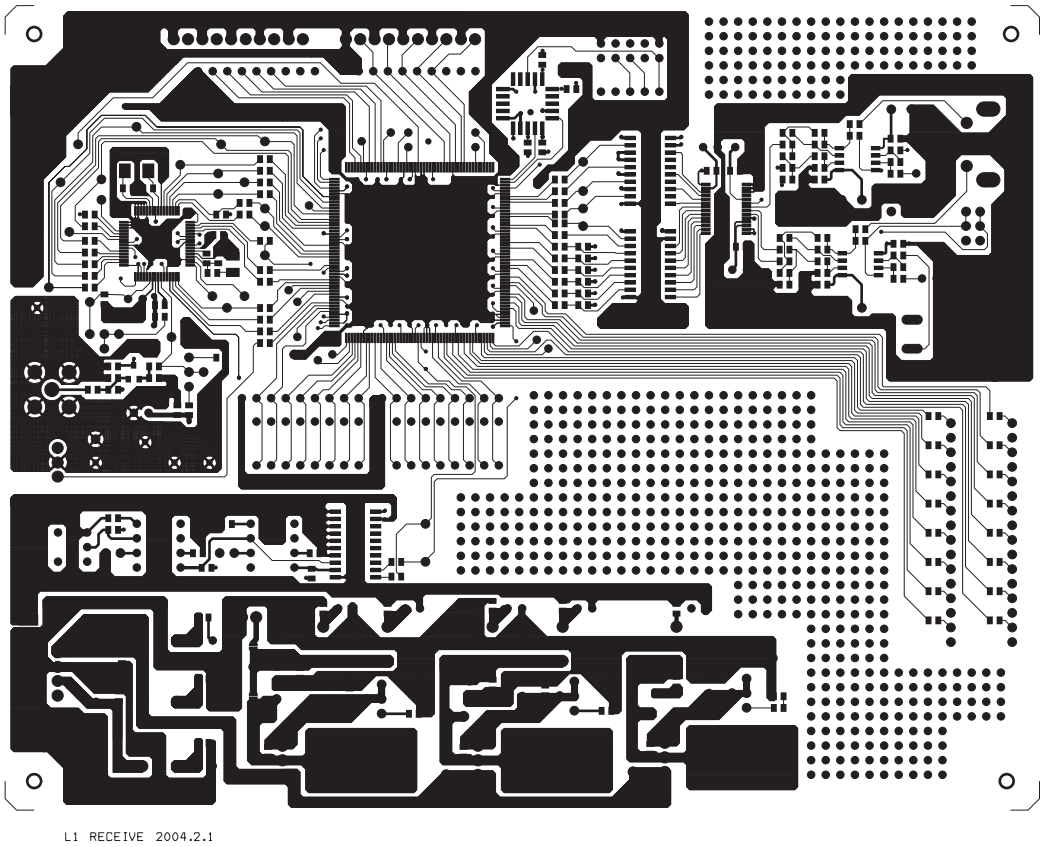


CXD4017R EVB Circuit Diagram (RESET)

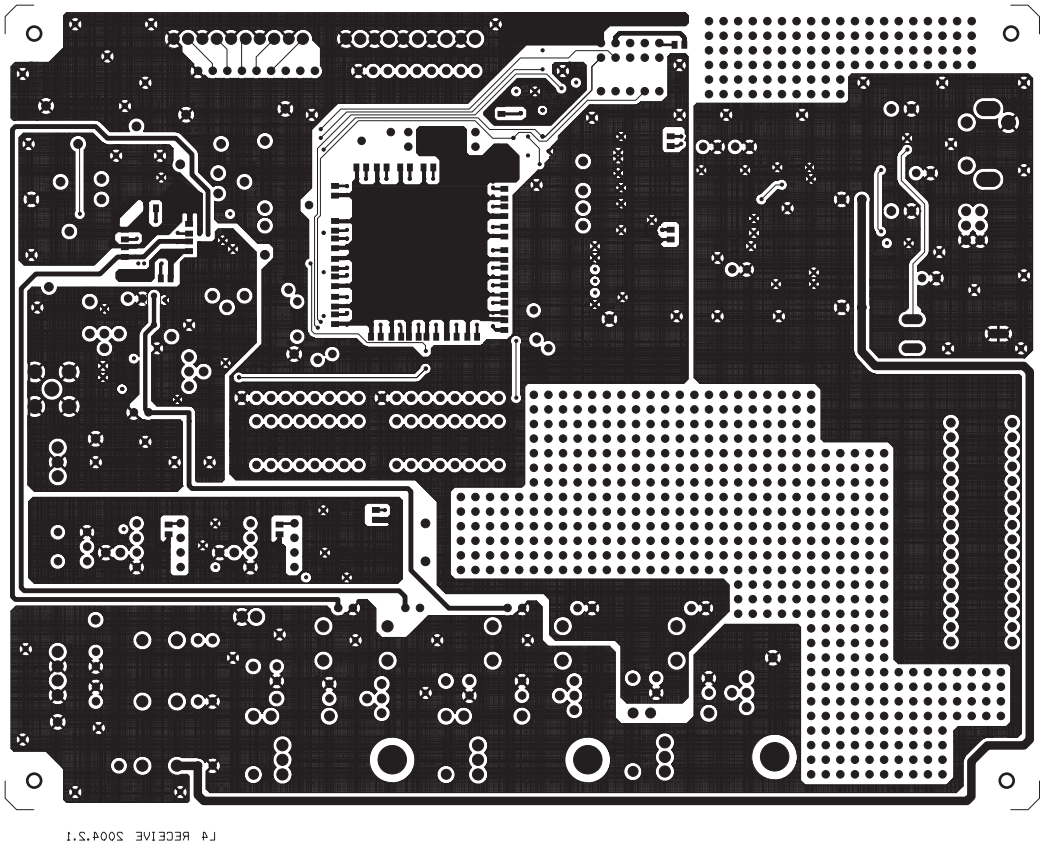


CXD4017R EVB Circuit Diagram (RFIN)

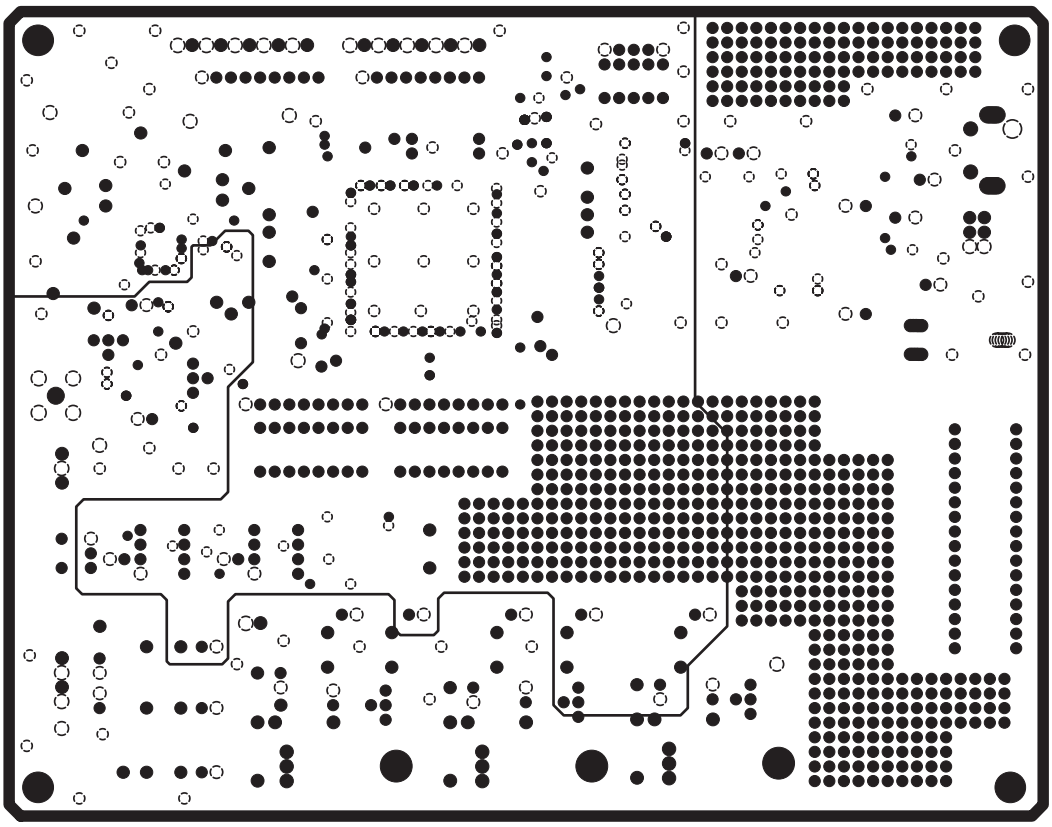
Pattern Diagram



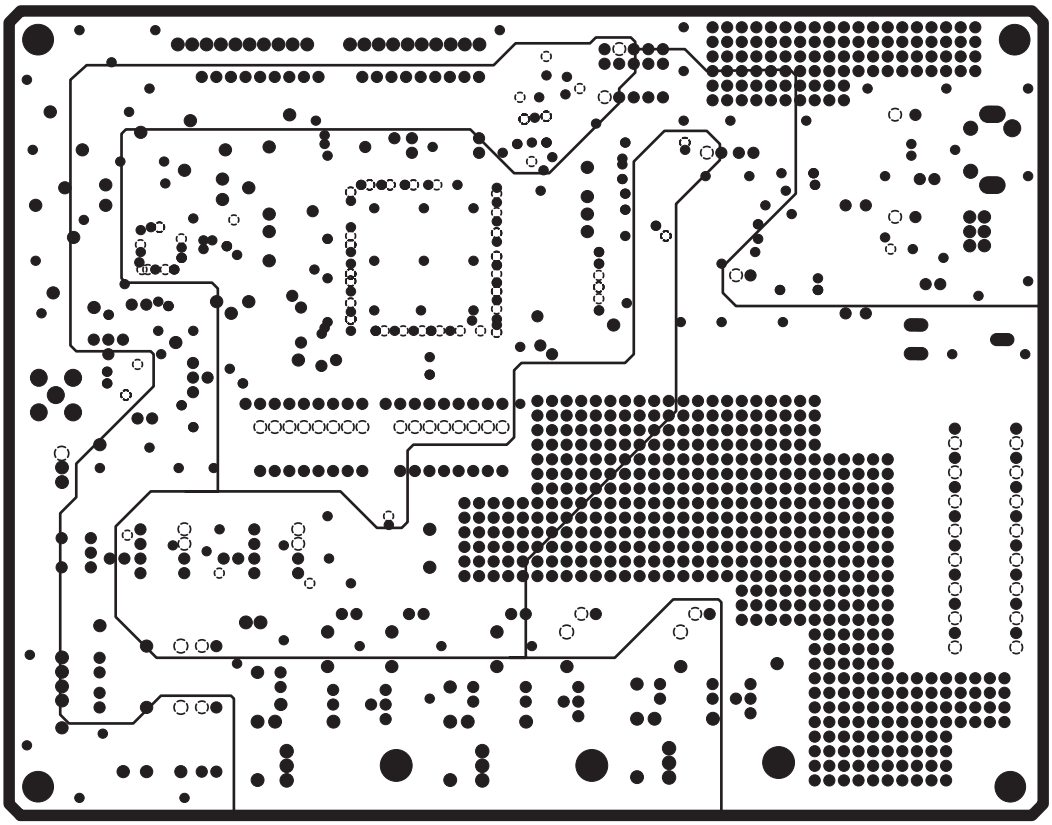
CXD4017R EVB A Side Pattern Diagram



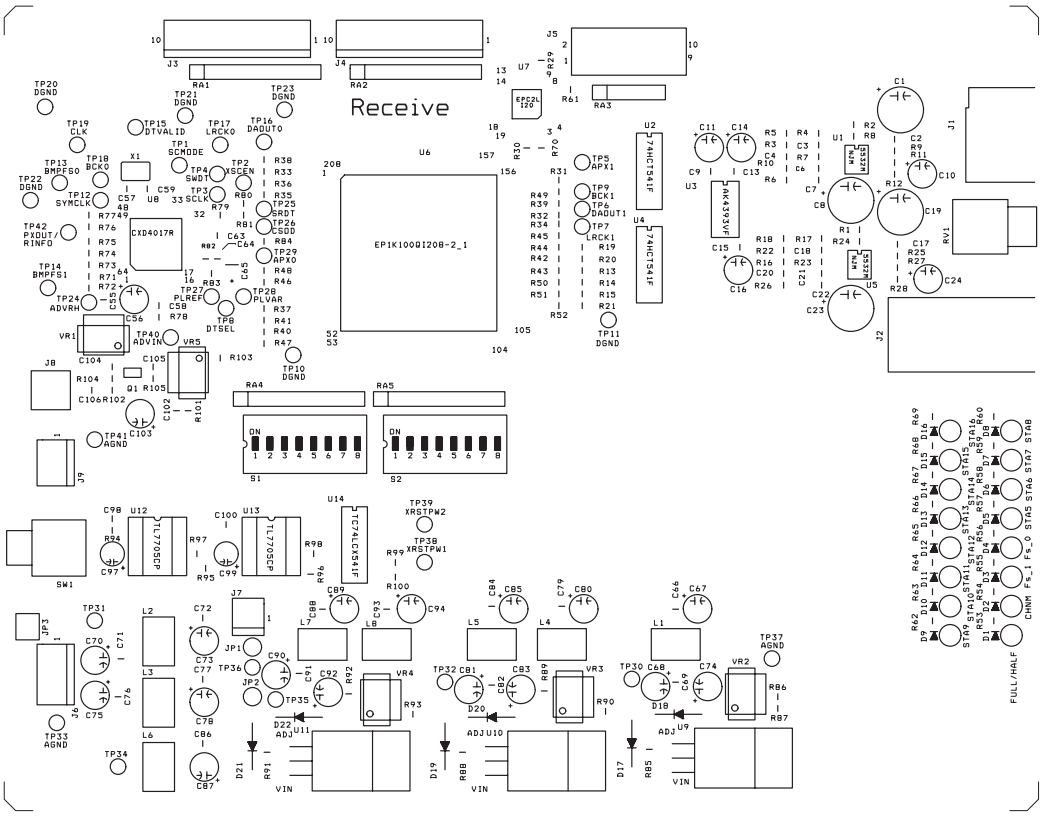
CXD4017R EVB B Side Pattern Diagram



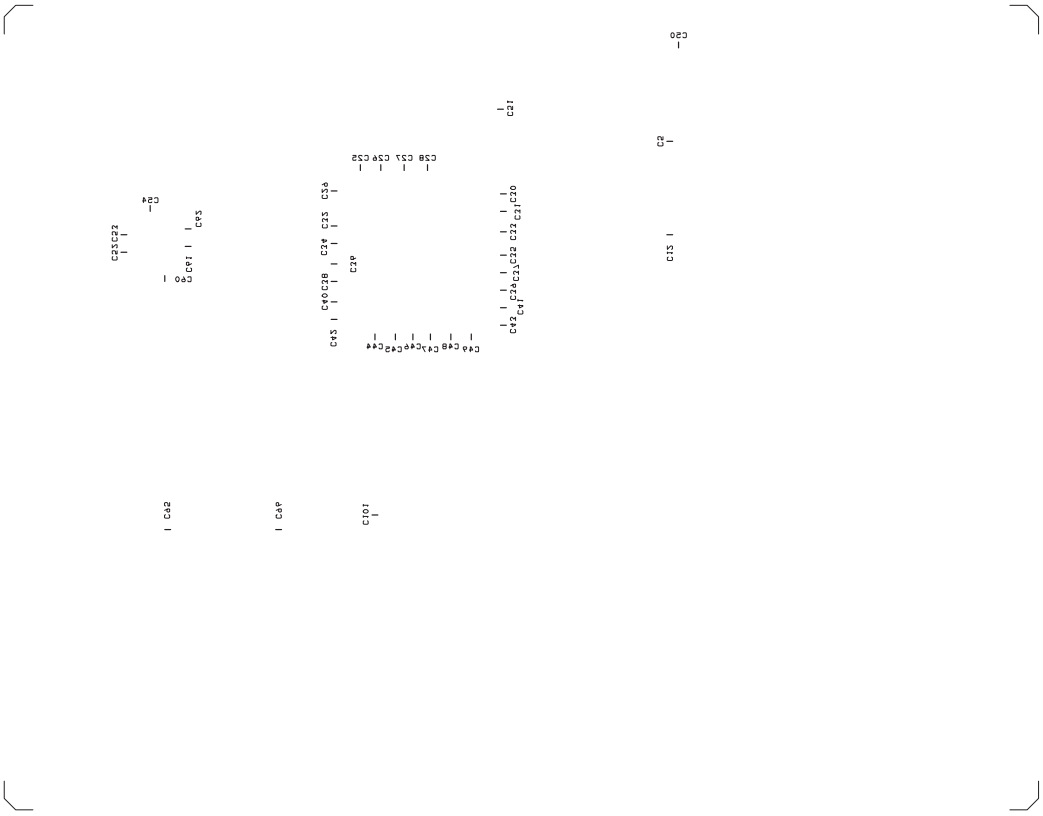
CXD4017R EVB GND Layer Pattern Diagram



CXD4017R EVB Power Supply Layer Pattern Diagram



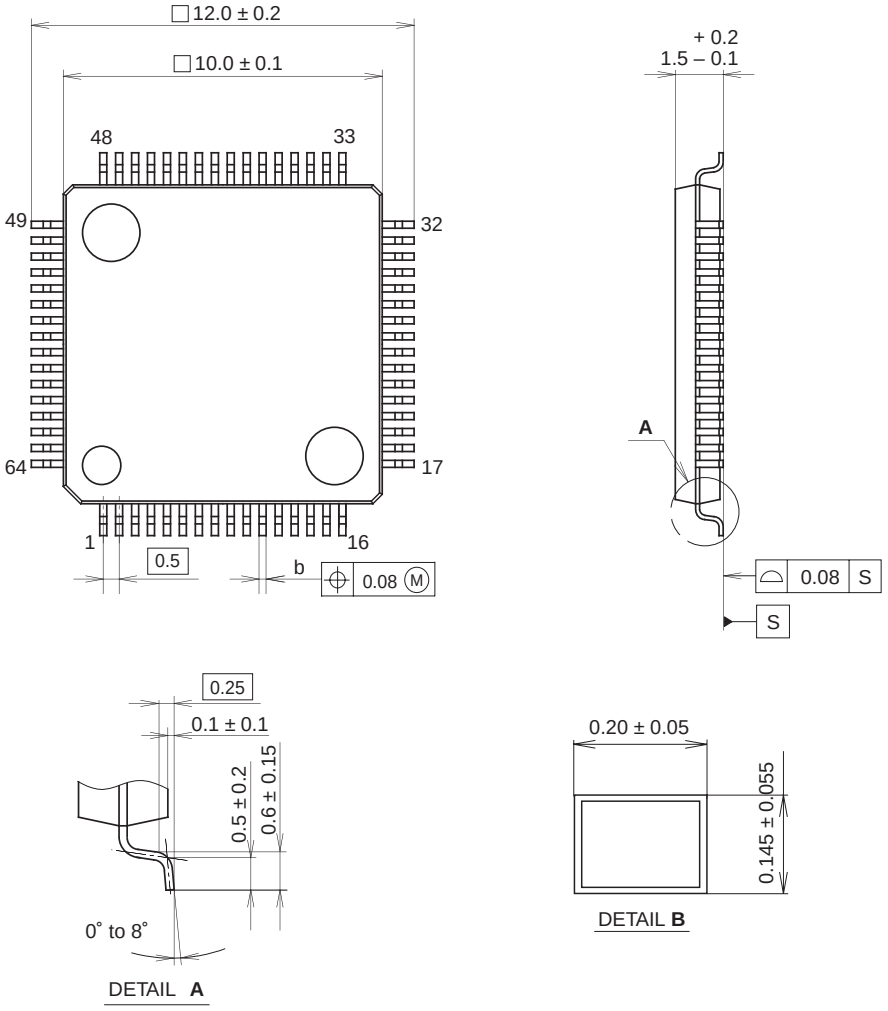
CXD4017R EVB A Side Silk Diagram



CXD4017R EVB B Side Silk Diagram

Package Outline Unit: mm

64PIN LQFP (PLASTIC)



SONY CODE	LQFP-64P-L023
JEITA CODE	P-LQFP64-10X10-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	SOLDER PLATING
TERMINAL MATERIAL	42 ALLOY
PACKAGE MASS	0.32g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-2%Bi
PLATING THICKNESS	5-20µm