SONY

Distribution Restraint	Internal	Outside
	Limited	Limited

Signal Processor LSI for Single CCD Color Camera

CXD4103R

Description

The CXD4103R is a signal processor LSI for Ye, Cy, Mg and G single CCD color cameras. In addition to basic camera signal processing functions, it includes an AE/AWB detection circuit, a sync signal generation circuit and an external sync circuit, etc. This chip also has a built-in microcontroller to realize basic camera control functions such as AE/AWB without an external microcomputer.
(Applications : Industrial CCD cameras (Surveillance/FA/image input cameras), Multimedia CCD cameras (Teleconferencing/personal computer cameras))

Features

- ◆ Generates timing pulses to drive the single CCD image sensor
  Built-in H driver for CCD image sensor
  Luminance/chroma signal processing
- ◆ Supports NTSC/PAL modes
- ◆ Supports 510H/760H system CCD image sensor
- ◆ Built-in 10-bit A/D converter
- ◆ Built-in EVR (3ch)
- ◆ Analog composite output
  Built-in digital encoder
  10-bit D/A converter output
- ◆ Digital output
  Conforms to ITU-REC656 format
- ◆ Supports external sync functions
  Built-in phase comparator
- ◆ Built-in AE/AWB detector
- ◆ Block control functions with a built-in microcontroller
  AE/AWB/CLAMP/Blemish detection and compensation
- ◆ Peripheral IC control function
  EEPROM communication control
- ◆ Serial communication function (2-mode selection)
  Microcomputer communication/start-stop synchronous system communication (RS-232C)
- ◆ Blemish detection and compensation function
- ◆ Mirror inversion function

E05949-CR

Absolute Maximum Ratings

◆ Supply voltage	DVDD	DVSS – 0.5 to + 2.5	V
	VDE	VSS – 0.5 to + 4.5	V
	AVD	AVS – 0.5 to + 4.5	V
◆ Input voltage	VI	VSS – 0.3 to VDE + 0.3	V
◆ Output voltage	VO	VSS – 0.3 to VDE + 0.3	V
◆ Operating temperature	Topr	– 20 to + 75	℃
◆ Storage temperature	Tstg	– 55 to + 150	℃

Recommended Operating Conditions

◆ Supply voltage	DVDD	1.65 to 1.95	V
	VDE	3.0 to 3.6	V
	AVD	3.0 to 3.6	V
◆ Operating temperature	Topr	– 20 to + 75	℃

Applicable CCD Image Sensors*

◆ 510H color CCDs
(Type 1/3, 1/4, NTSC/PAL)

◆ 760H color CCDs
(Type 1/3, 1/4, NTSC/PAL)

* When using 1/3 types, an external buffer circuit (3.3V → 5.0V voltage step-up) is required.
* Applicable CCD image sensors are applicable products as of preparing this data sheet. They may be changed according to the version up and production discontinuation of CCD image sensors.

Supported Related LSI

V-Driver	CXD1267AN
AGC	CXA2096N
EEPROM	AK6480A (Asahi Kasei Microsystems Co., Ltd.)
	BR9080A (ROHM Co., Ltd.)

Notes On Handling

Use Restrictions

- The Products are intended for incorporation into such general electronic equipment as general CCTV surveillance, image input cameras, FA cameras, teleconferencing cameras and personal computer cameras in accordance with the terms and conditions set forth in this specifications book and otherwise notified by Sony from time to time.
- You should not use the Products for critical applications, as car use products, which may pose a life- or injury- threatening risk or are highly likely to cause significant property damage in the event of failure of the Products. In addition, you should not use the Products in weapon or military equipment.
- Sony disclaims and does not assume any liability and damages arising out of misuse, improper use, modification, use of the Products for the above-mentioned critical applications, weapon and military equipment, or any deviation from the requirements set forth in this specifications book.

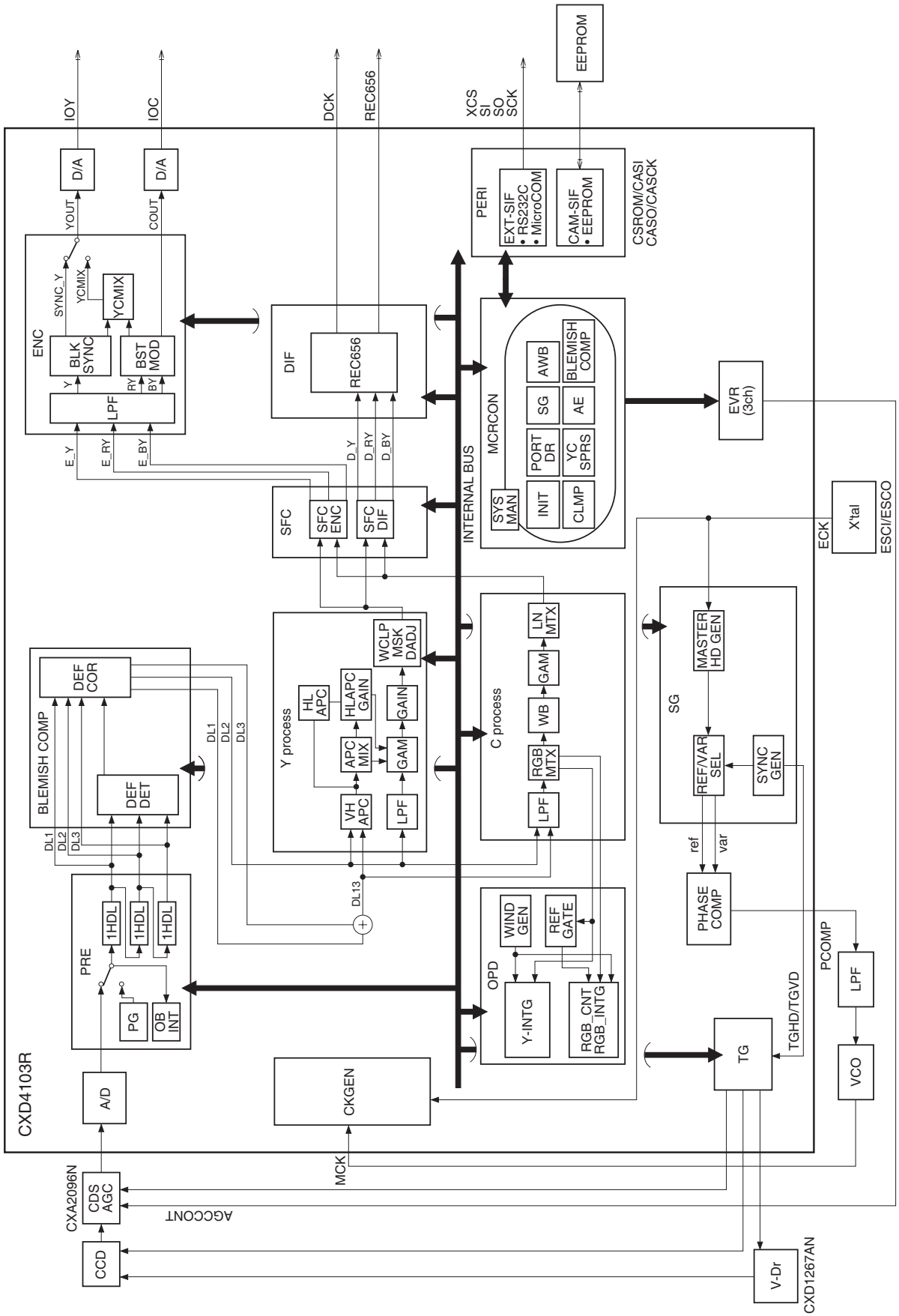
Design for Safety

- Sony is making continuous efforts to further improve the quality and reliability of the Products; however, failure of a certain percentage of the Products is inevitable. Therefore, you should take sufficient care to ensure the safe design of your products such as component redundancy, anti-conflagration features, and features to prevent mis-operation in order to avoid accidents resulting in injury or death, fire or other social damage as a result of such failure.

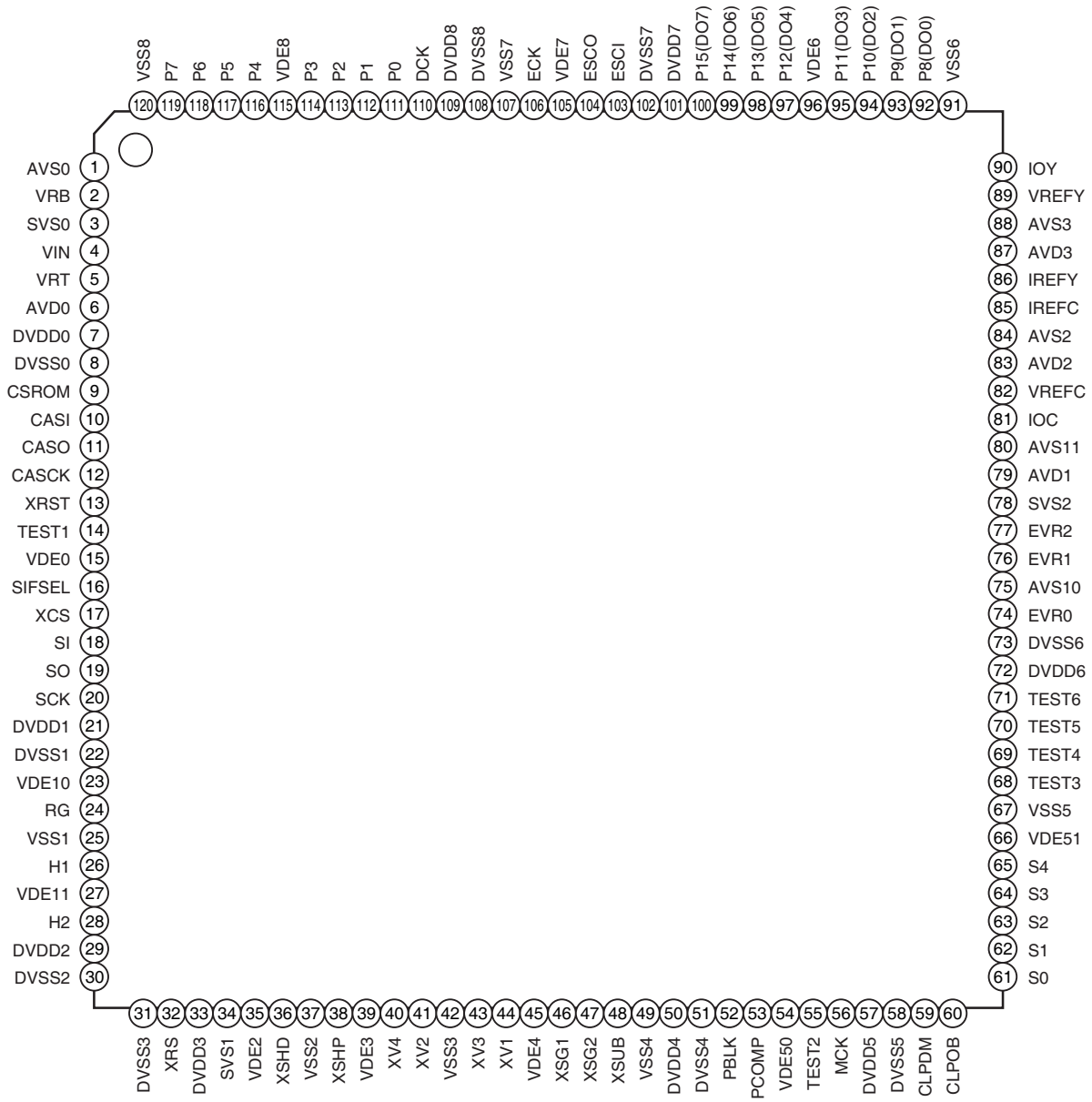
Other Applicable Terms and Conditions

- The terms and conditions in the Sony additional specifications, which will be made available to you when you order the Products, shall also be applicable to your use of the Products as well as to this specifications book. You should review those terms and conditions when you consider purchasing and/or using the Products.

Block Diagram



Pin Configuration



Note) Symbols in parentheses are the signal names when the function is switched by the communication parameter settings.

Pin Description

Pin No.	Symbol	I/O	Description	Power supply
1	AVS0	—	GND	Analog 1
2	VRB	I	A/D converter reference voltage (bottom) input.	
3	SVS0	—	Sub GND	
4	VIN	I	A/D converter analog signal input.	
5	VRT	I	A/D converter reference voltage (top) input.	
6	AVD0	—	Power supply for analog (3.3V).	
7	DVDD0	—	Power supply for logic (1.8V).	Logic 1
8	DVSS0	—	GND	
9	CSROM	O	EEPROM chip select output	
10	CASI	I	Serial data input for system communication.	
11	CASO	O	Serial data output for system communication.	
12	CASCK	O	Serial clock output for system communication.	
13	XRST	I	Reset input.	
14	TEST1	I	Test	
15	VDE0	—	Power supply for input/output (3.3V).	
16	SIFSEL	I	Serial interface mode switching input. 0 : microcomputer (3 wires) 1 : RS-232C	
17	XCS	I	Chip select input for 3-wire serial interface. (when SIFSEL = 0)	
18	SI	I	Serial data input for 3-wire serial interface. (when SIFSEL = 0)	
19	SO	O	Serial data output for 3-wire serial interface. (when SIFSEL = 0)	
20	SCK	I	Serial clock input for 3-wire serial interface. (when SIFSEL = 0)	
21	DVDD1	—	Power supply for logic (1.8V).	
22	DVSS1	—	GND	

Pin No.	Symbol	I/O	Description	Power supply
23	VDE10	—	Power supply for input/output (3.3V).	Driving pulse
24	RG	O	Reset gate pulse output.	
25	VSS1	—	GND	
26	H1	O	CCD horizontal register transfer pulse output.	
27	VDE11	—	Power supply for input/output (3.3V).	
28	H2	O	CCD horizontal register transfer pulse output.	
29	DVDD2	—	Power supply for logic (1.8V).	
30	DVSS2	—	GND	
31	DVSS3	—	GND	
32	XRS	O	Resampling pulse output.	
33	DVDD3	—	Power supply for logic (1.8V).	
34	SVS1	—	Sub GND	
35	VDE2	—	Power supply for input/output (3.3V).	
36	XSHD	O	Data sample-and-hold pulse output.	
37	VSS2	—	GND	
38	XSHP	O	Precharge level sample-and-hold pulse output.	
39	VDE3	—	Power supply for input/output (3.3V).	
40	XV4	O	CCD vertical register transfer pulse output.	
41	XV2	O	CCD vertical register transfer pulse output.	
42	VSS3	—	GND	
43	XV3	O	CCD vertical register transfer pulse output.	
44	XV1	O	CCD vertical register transfer pulse output.	
45	VDE4	—	Power supply for input/output (3.3V).	
46	XSG1	O	Sensor gate readout pulse output.	
47	XSG2	O	Sensor gate readout pulse output.	
48	XSUB	O	CCD electronic shutter pulse output.	
49	VSS4	—	GND	

Pin No.	Symbol	I/O	Description	Power supply
50	DVDD4	—	Power supply for logic (1.8V).	Logic 2
51	DVSS4	—	GND	
52	PBLK	O	Preblanking pulse output.	
53	PCOMP	O	Phase comparator output.	
54	VDE50	—	Power supply for input/output (3.3V).	
55	TEST2	I	Test	
56	MCK	I	System drive clock input.	
57	DVDD5	—	Power supply for logic (1.8V).	
58	DVSS5	—	GND	
59	CLPDM	O	Dummy data clamp pulse output.	
60	CLPOB	O	Optical black clamp pulse output.	
61	S0	I/O	Sync signal input/output.	
62	S1	I/O	Sync signal input/output.	
63	S2	I/O	Sync signal input/output.	
64	S3	I/O	Sync signal input/output.	
65	S4	O	Sync signal output.	
66	VDE51	—	Power supply for input/output (3.3V).	
67	VSS5	—	GND	
68	TEST3	O	Test	
69	TEST4	I	Test	
70	TEST5	I	Test	
71	TEST6	I	Test	
72	DVDD6	—	Power supply for logic (1.8V).	
73	DVSS6	—	GND	

Pin No.	Symbol	I/O	Description	Power supply
74	EVR0	O	EVR0 analog output.	
75	AVS10	—	GND	
76	EVR1	O	EVR1 analog output.	
77	EVR2	O	EVR2 analog output.	
78	SVS2	—	Sub GND	
79	AVD1	—	Power supply for analog (3.3V).	
80	AVS11	—	GND	
81	IOC	O	Analog chroma output.	
82	VREFC	I	Reference voltage setting for chroma signal D/A converter.	Analog 2
83	AVD2	—	Power supply for analog (3.3V).	
84	AVS2	—	GND	
85	IREFC	O	Reference current setting for chroma signal D/A converter.	
86	IREFY	O	Reference current setting for luminance signal D/A converter.	
87	AVD3	—	Power supply for analog (3.3V).	
88	AVS3	—	GND	
89	VREFY	I	Reference voltage setting for luminance signal D/A converter.	
90	IOY	O	Analog Y output/composite video output.	
91	VSS6	—	GND	
92	P8 (DO0)	I/O	Port 8 input/output or digital signal output.	
93	P9 (DO1)	I/O	Port 9 input/output or digital signal output.	
94	P10 (DO2)	I/O	Port 10 input/output or digital signal output.	
95	P11 (DO3)	I/O	Port 11 input/output or digital signal output.	
96	VDE6	—	Power supply for input/output (3.3V).	
97	P12 (DO4)	I/O	Port 12 input/output or digital signal output.	
98	P13 (DO5)	I/O	Port 13 input/output or digital signal output.	
99	P14 (DO6)	I/O	Port 14 input/output or digital signal output.	Logic 3
100	P15 (DO7)	I/O	Port 15 input/output or digital signal output.	
101	DVDD7	—	Power supply for logic (1.8V).	
102	DVSS7	—	GND	
103	ESCI	I	Oscillation cell input.	
104	ESCO	O	Oscillation cell output.	
105	VDE7	—	Power supply for input/output (3.3V).	
106	ECK	I	Encoder clock input	
107	VSS7	—	GND	

Pin No.	Symbol	I/O	Description	Power supply
108	DVSS8	—	GND	
109	DVDD8	—	Power supply for logic (1.8V).	
110	DCK	O	Clock output for digital signal output.	
111	P0	I/O	Port 0 input/output.	
112	P1	I/O	Port 1 input/output.	
113	P2	I/O	Port 2 input/output.	
114	P3	I/O	Port 3 input/output.	Logic 4
115	VDE8	—	Power supply for input/output (3.3V).	
116	P4	I/O	Port 4 input/output or OPD frame pulse output.	
117	P5	I/O	Port 5 input/output or VD output.	
118	P6	I/O	Port 6 input/output or HD output.	
119	P7	I/O	Port 7 input/output.	
120	VSS8	—	GND	

Electrical Characteristics

DC Characteristics

(within the recommended operating range)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	VDE		3.0	3.3	3.6	V
	DVDD		1.65	1.8	1.95	V
	AVD		3.0	3.3	3.6	V
Output voltage 1	$V_{OH}1$*1	I_{OH} = 1.0mA	VDE – 0.4			V
	$V_{OL}1$*1	I_{OL} = 1.0mA			0.4	V
Output voltage 2	$V_{OH}2$*2	I_{OH} = 4.0mA	VDE – 0.4			V
	$V_{OL}2$*2	I_{OL} = 4.0mA			0.4	V
Input voltage 1	V_{T+} *1		2.0			V
	V_{T-} *1				0.8	V
Input voltage 2	V_{T+} *3, *5		2.3			V
	V_{T-} *3, *5				0.7	V
Hysteresis	$V_{T+} - V_{T-}$ *3, *5			0.5		V
Input voltage 3	LV_{TH}*4			0.5VDE		V
	V_{IH}*4		0.7VDE			V
	V_{IL}*4				0.2VDE	V
	V_{IN}*4	f_{MAX} = 90MHz	0.3			V_{P-P}
Input leakage current 1	I_{I}*1 (input), *3, *4	V_{IN} = VSS or VDE	– 10		10	μA
Input leakage current 2	I_{IH}*5	V_{IN} = VDE	40	100	240	μA

*1 S0, S1, S2, S3, P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15

*2 CSROM, CASCK, XV1, XV2, XV3, XV4, XSG1, XSG2, XSUB, CLPDM, CLPOB, PBLK, S4, TEST3, DCK, CASO, SO

*3 CASI, XRST, SIFSEL, XCS, SI, SCK, TEST2, TEST4, TEST5, TEST6

*4 MCK, ECK

*5 TEST1

Input/Output Capacitance

(VDE = V_I = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}			7	pF
Output pin capacitance	C_{OUT}			7	pF
I/O pin capacitance	$C_{I/O}$			7	pF

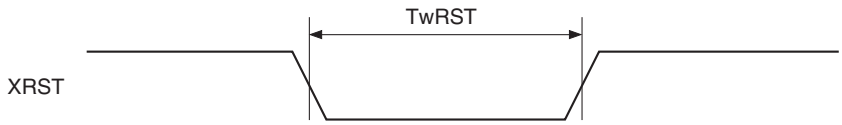
AC Characteristics

(Within the recommended operating range)

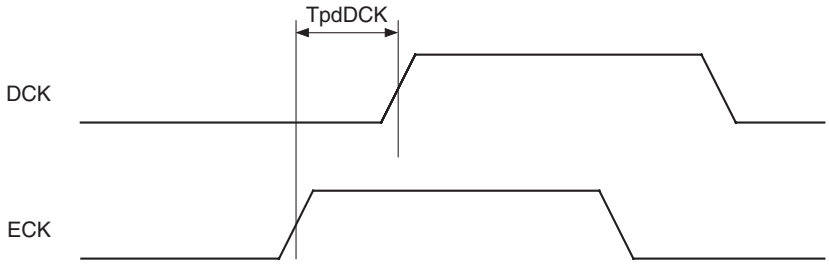
Classification	Item	Symbol	Min.	Typ.	Max.	Unit
Reset input	Minimum Low period of XRST pin reset operation	TwRST	500	—	—	ns
Digital output	P0 to P15 output delay time against DCK ↑	TpdP	0.4	—	20	ns
	S0 output delay time against DCK ↑	TpdS0	0.4	—	28	ns
	S1 output delay time against DCK ↑	TpdS1	0.4	—	30	ns
	DCK output delay time against ECK ↑	TpdDCK	7	—	29	ns
SYNC block sync output	HD, VD, FLD and SYNC output delay time against ECK ↑	TpdSY	10	—	45	ns
Serial communication I/O	SCK input pulse width (High period)	TwHSCK	—	580	—	ns
	SCK input pulse width (Low period)	TwLSCK	—	580	—	ns
	XCS input setup time against SCK ↓	TsuXCS	580	—	—	ns
	XCS input hold time against SCK ↑	ThXCS	580	—	—	ns
	SI input setup time against SCK ↑	TsuSI	0	—	—	ns
	SI input hold time against SCK ↑	ThSI	0	—	—	ns
	SO output transition time against XCS ↓ (Hi-Z → Data active)	TzdSO	0	—	—	ns
	SO transition time against XCS ↑ (Data active → Hi-Z)	TdzSO	0	—	—	ns
	SO output delay time against SCK ↓	TpdSO	—	—	580	ns

AC Characteristics Diagram

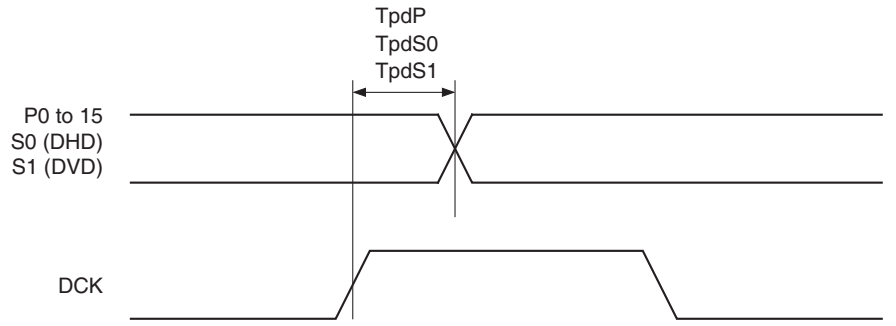
1. Reset input



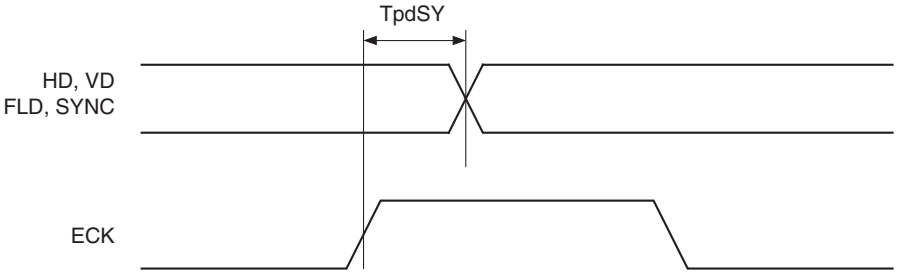
2. DCK output



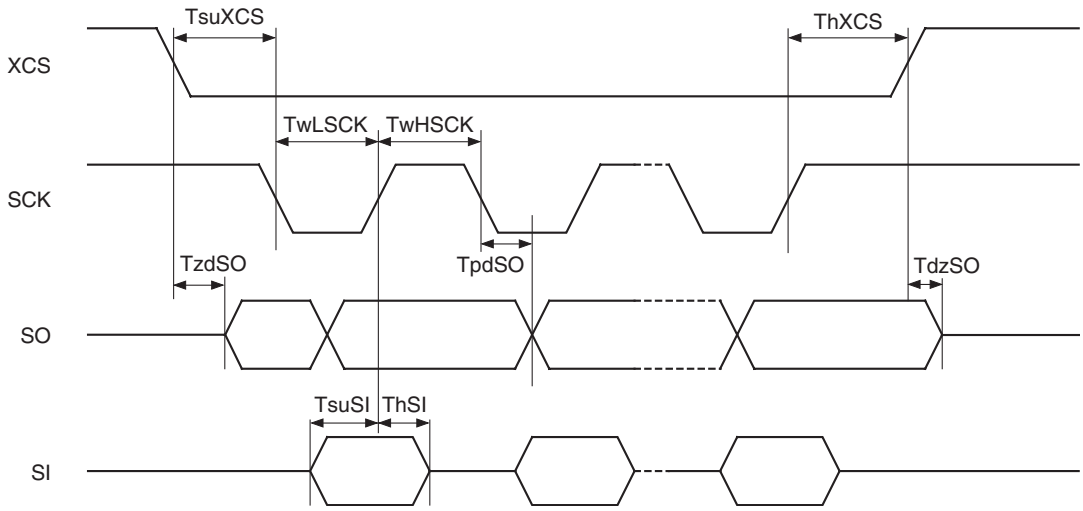
3. Digital output



4. SYNC block output



5. Serial communication I/O



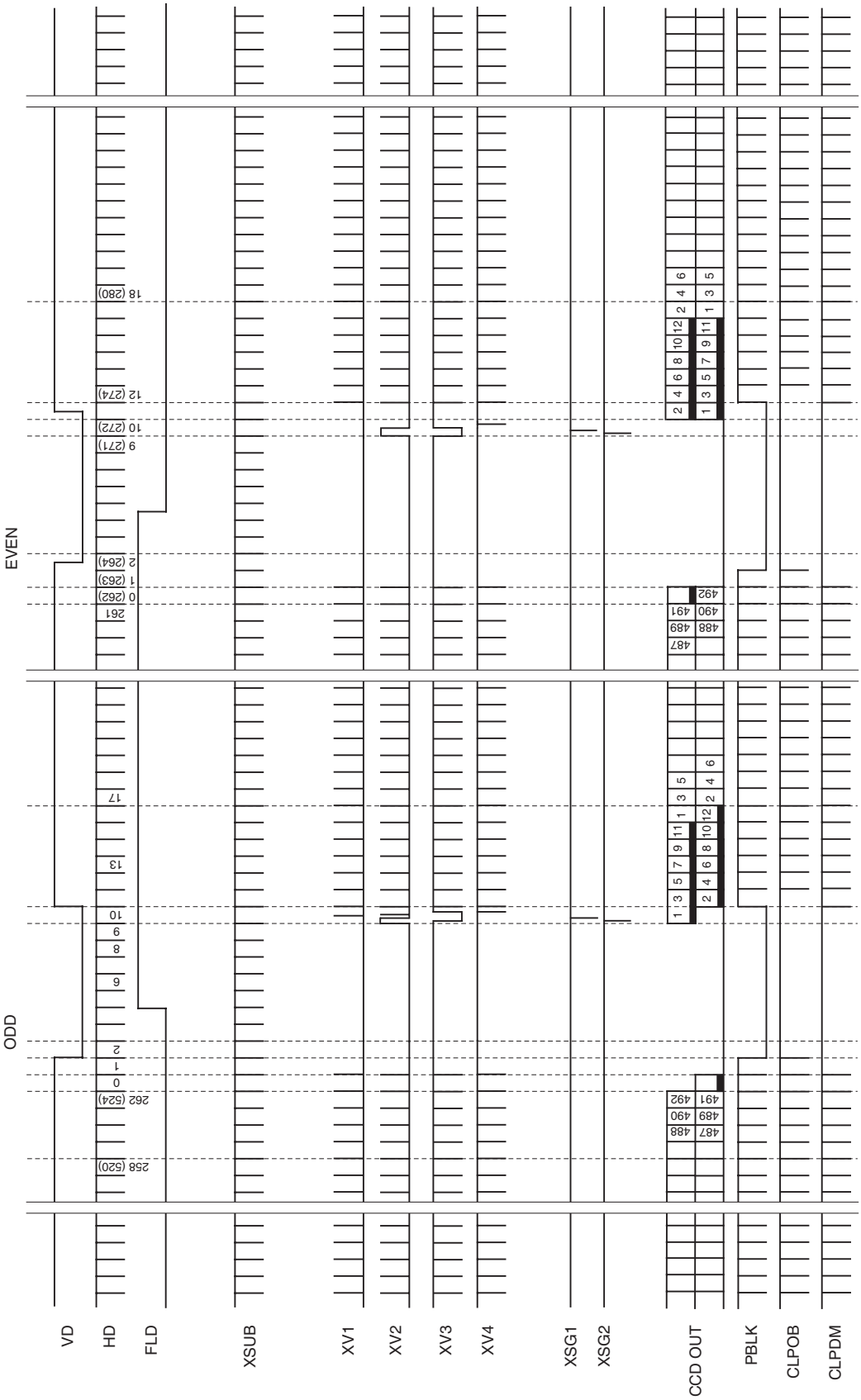
Relationship between MODESEL and Each Clock

TV system	CCD type	MODESEL	ECK	MCK	DSPCK*1	Remarks
NTSC	510H	0	38.13986MHz	(ECK = MCK)	MCK/4	ECK and MCK are connected internally.
		2	27.00000MHz	38.13986MHz		
	760H	6	28.63636MHz	(ECK = MCK)	MCK/2	ECK and MCK are connected internally.
		8	27.00000MHz	28.63636MHz		
PAL	510H	3	37.87500MHz	(ECK = MCK)	MCK/4	ECK and MCK are connected internally.
		5	27.00000MHz	37.87500MHz		
	760H	9	28.37500MHz	(ECK = MCK)	MCK/2	ECK and MCK are connected internally.
		B	27.00000MHz	28.37500MHz		

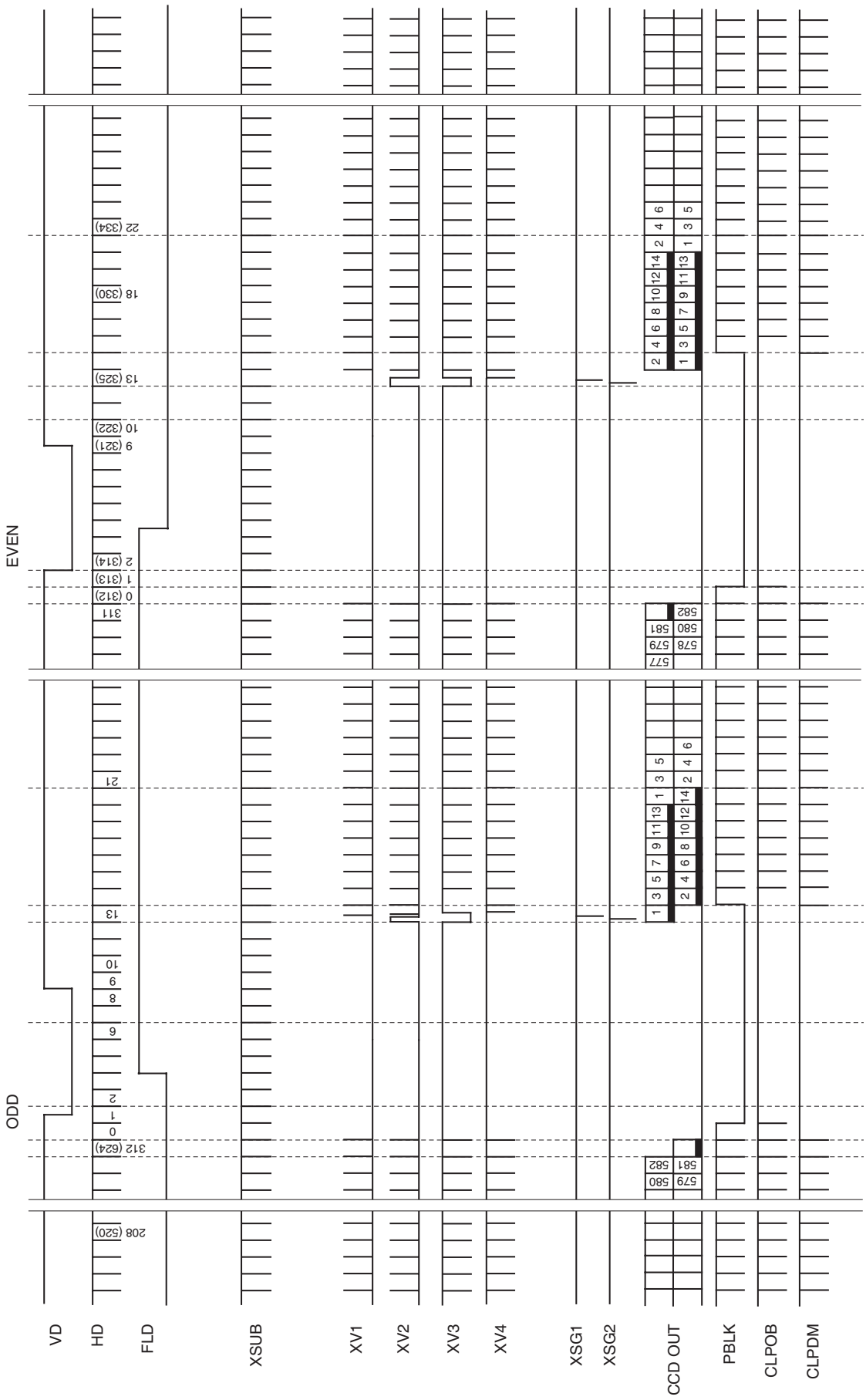
*1 DSPCK : clock which is not output by external pins.
See the above table for the relationship between the encoder clock (ECK) and the system drive clock (MCK).

Timing Chart

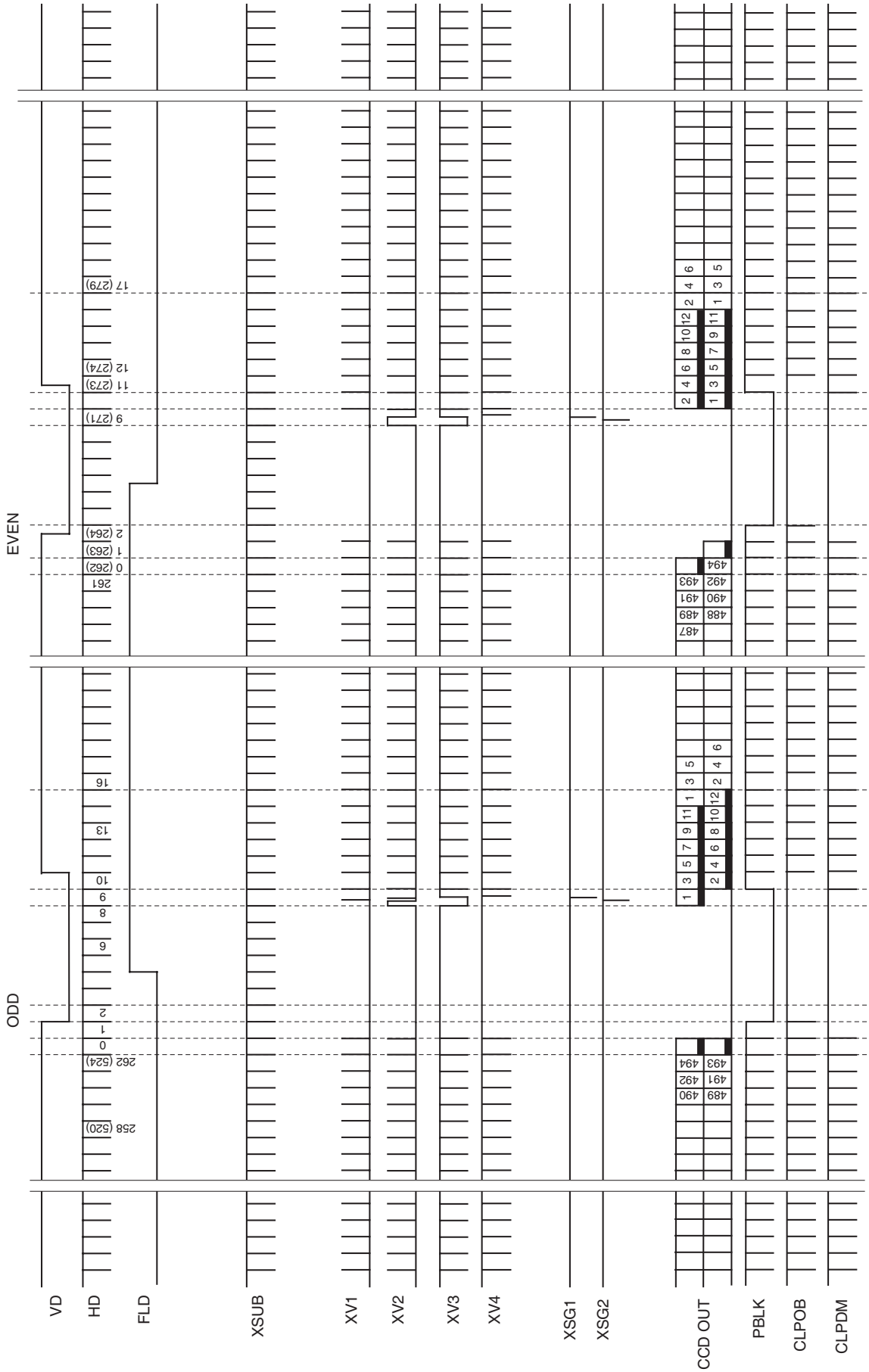
Vertical Timing Chart MODESEL 0, 2 [510H NTSC]



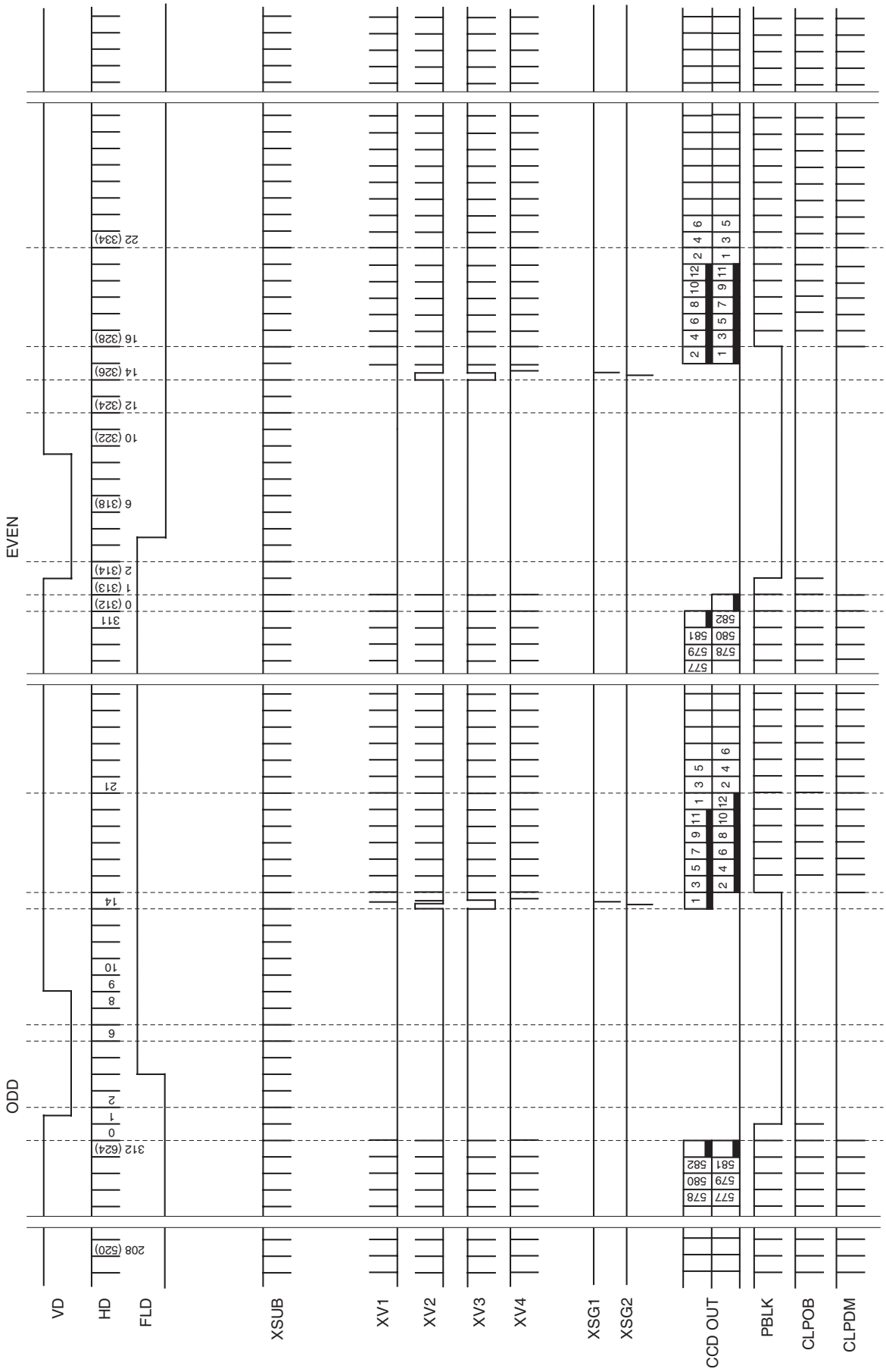
Vertical Timing Chart MODESEL 3, 5 [510H PAL]



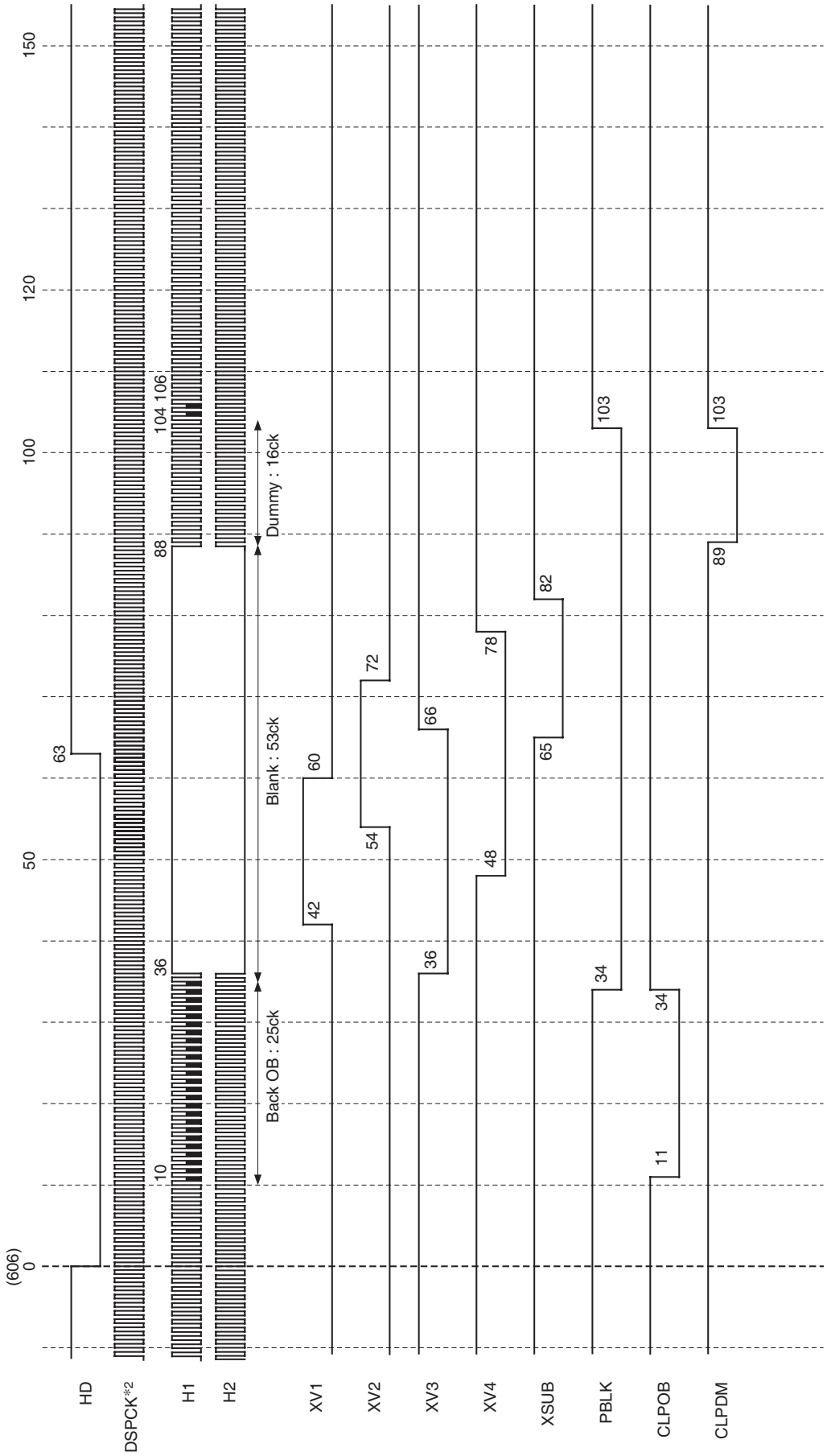
Vertical Timing Chart MODESEL 6, 8 [760H NTSC]



Vertical Timing Chart MODESEL 9, B [760H PAL]

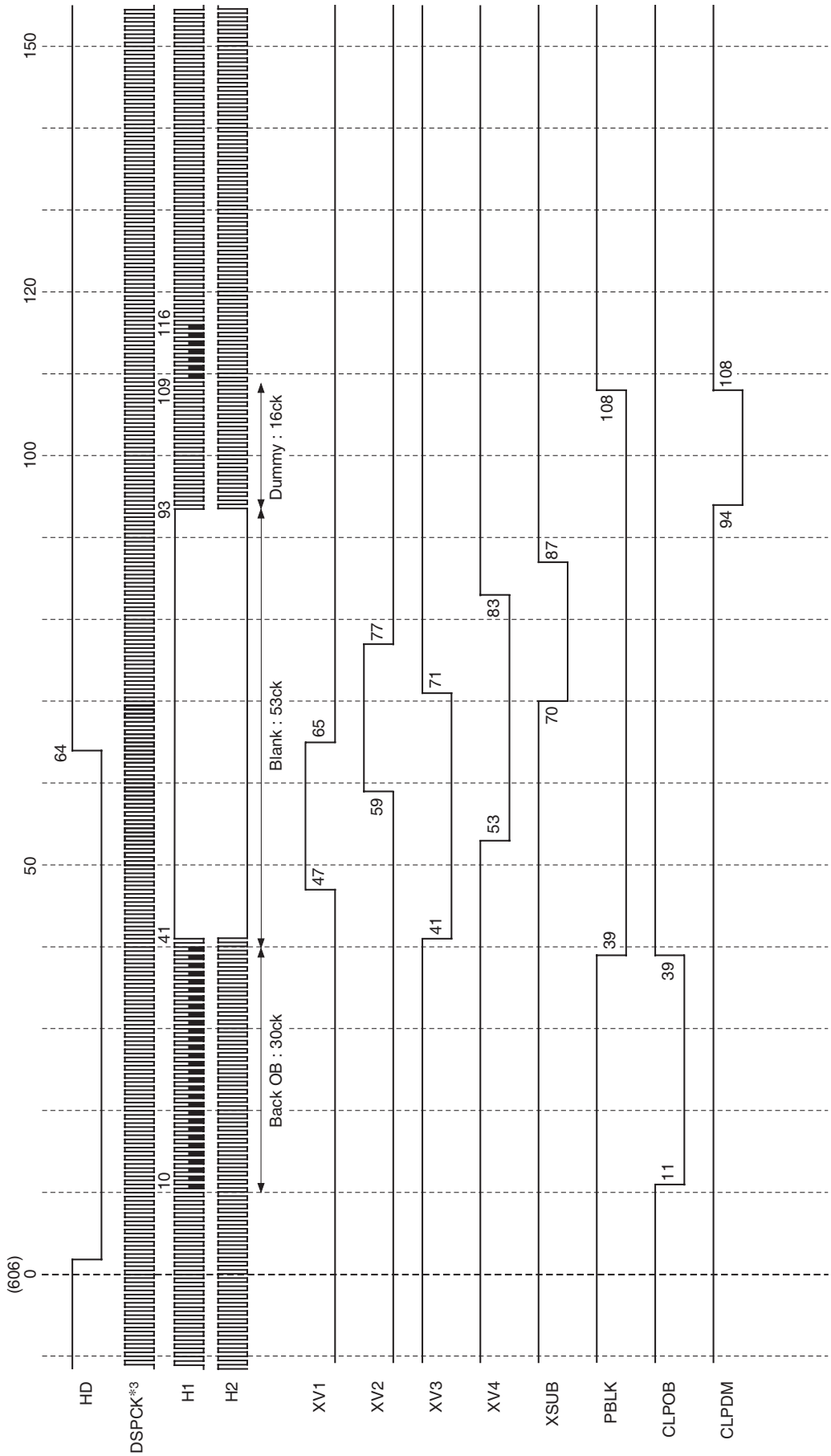


Horizontal Timing Chart MODESEL 0, 2 [510H NTSC] DSPCK : 606fH (9.534965MHz : 104.88ns)



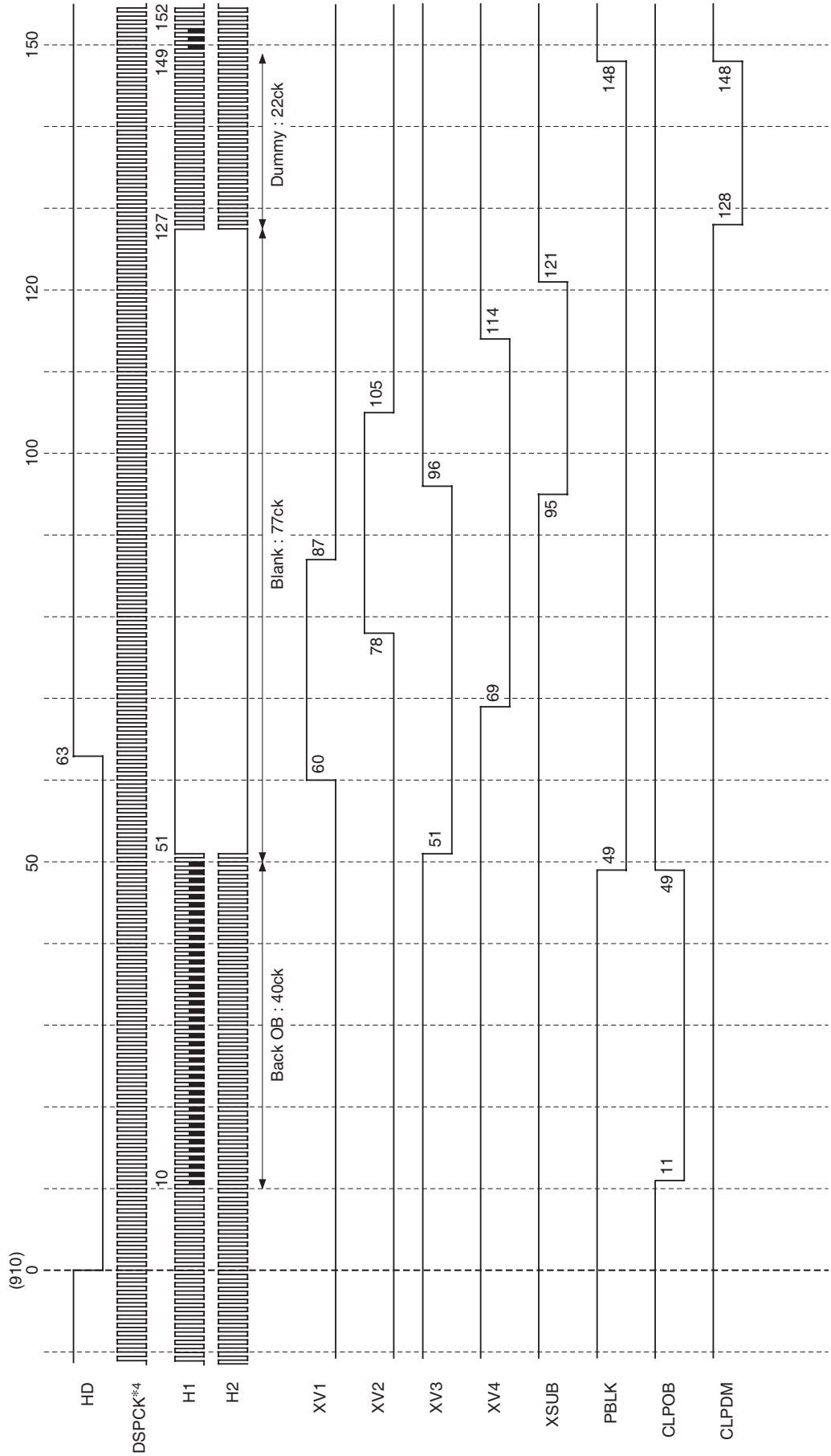
*2 DSPCK is a clock which is not output by external pins. See the previously described table (Relationship between MODESEL and Each Clock).

Horizontal Timing Chart MODESEL 3, 5 [510H PAL] DSPCK : 606fH (9.46875MHz : 105.60ns)



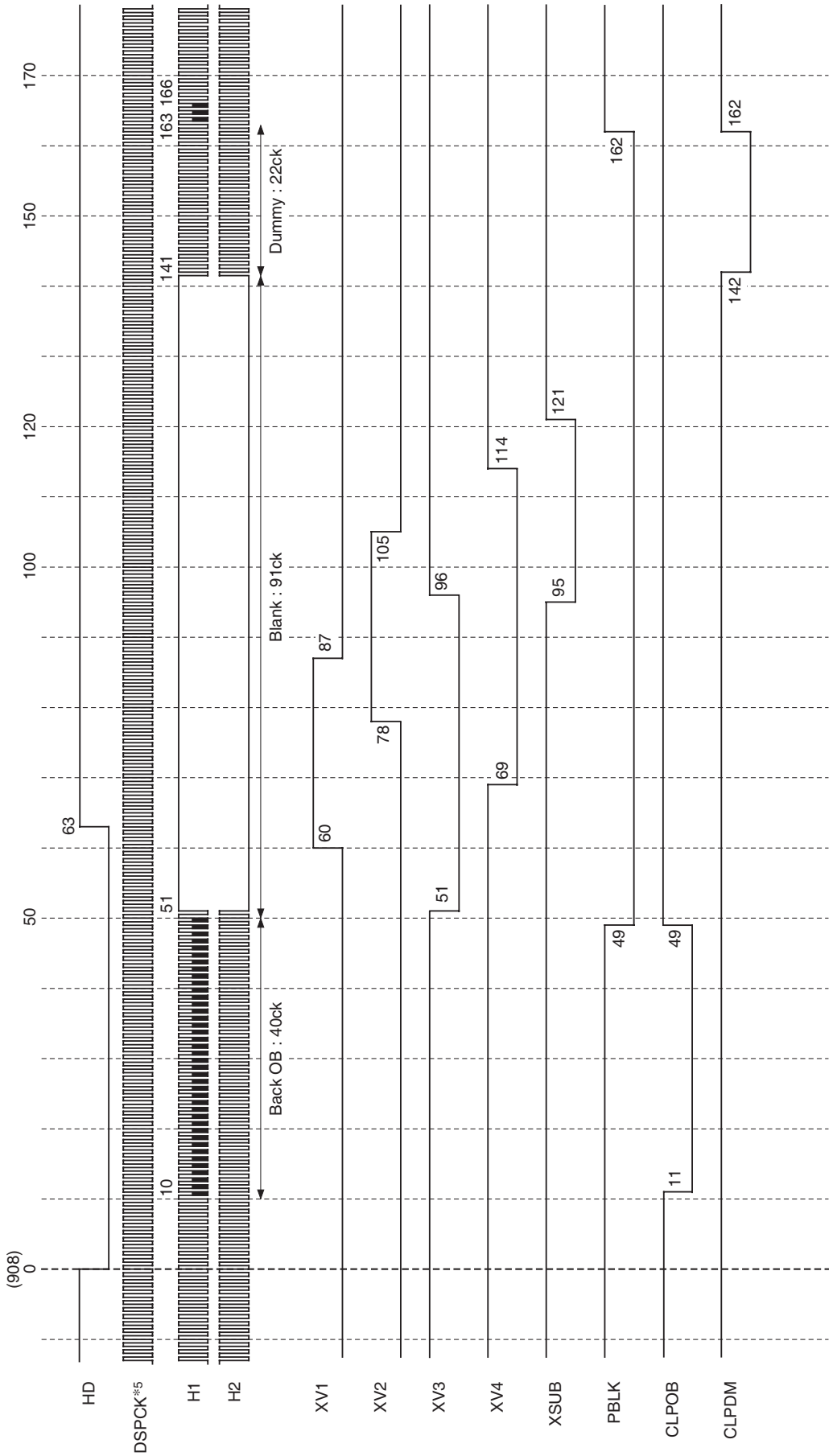
*3 DSPCK is a clock which is not output by external pins. See the previously described table (Relationship between MODESEL and Each Clock).

Horizontal Timing Chart MODESEL 6, 8 [760H NTSC] DSPCK : 910fH (14.31818MHz : 69.84ns)



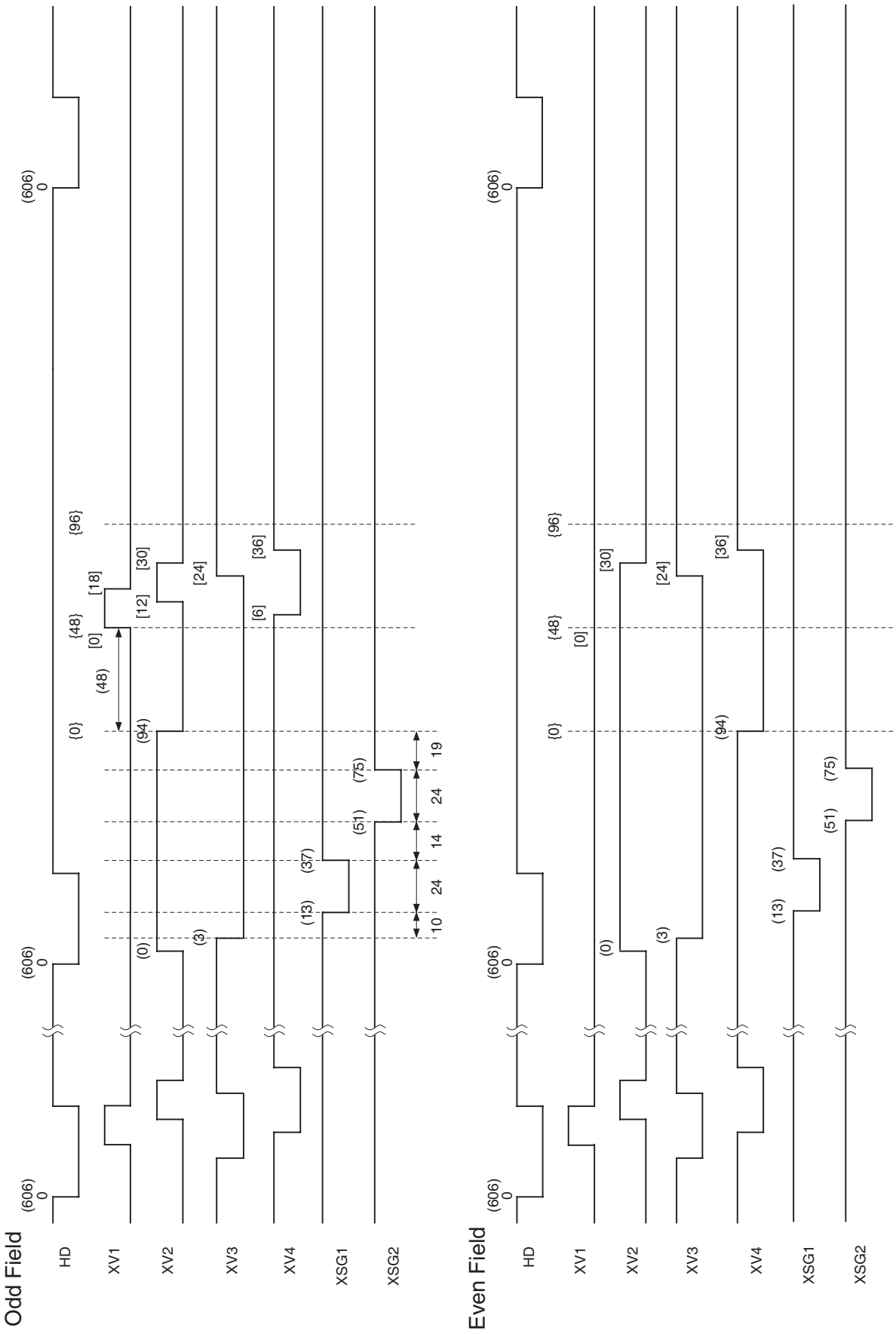
*4 DSPCK is a clock which is not output by external pins. See the previously described table (Relationship between MODESEL and Each Clock).

Horizontal Timing Chart MODESEL 9, B [760H PAL] DSPCK : 908fH (14.1875MHz : 70.48ns)

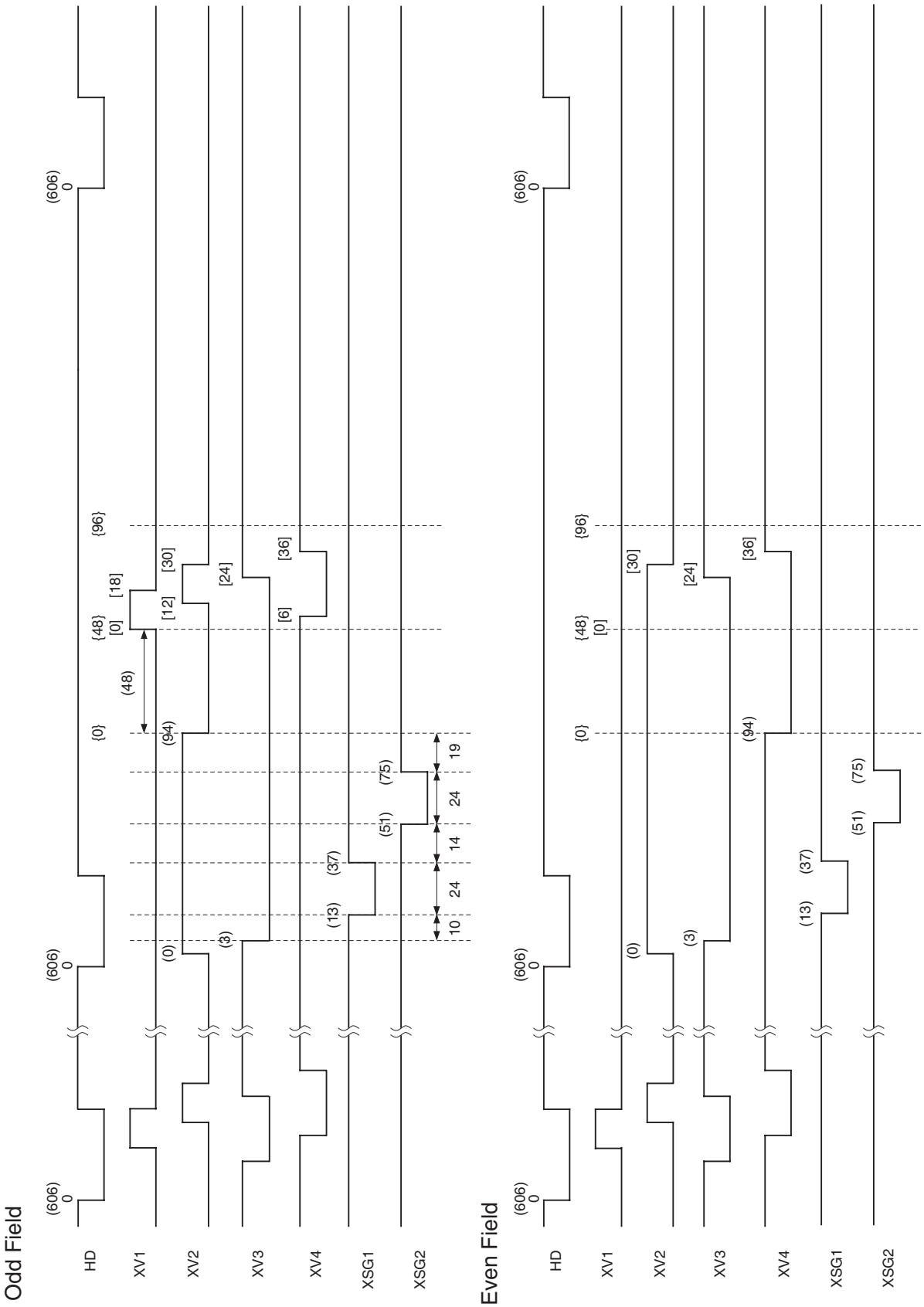


*5 DSPCK is a clock which is not output by external pins. See the previously described table (Relationship between MODESEL and Each Clock).

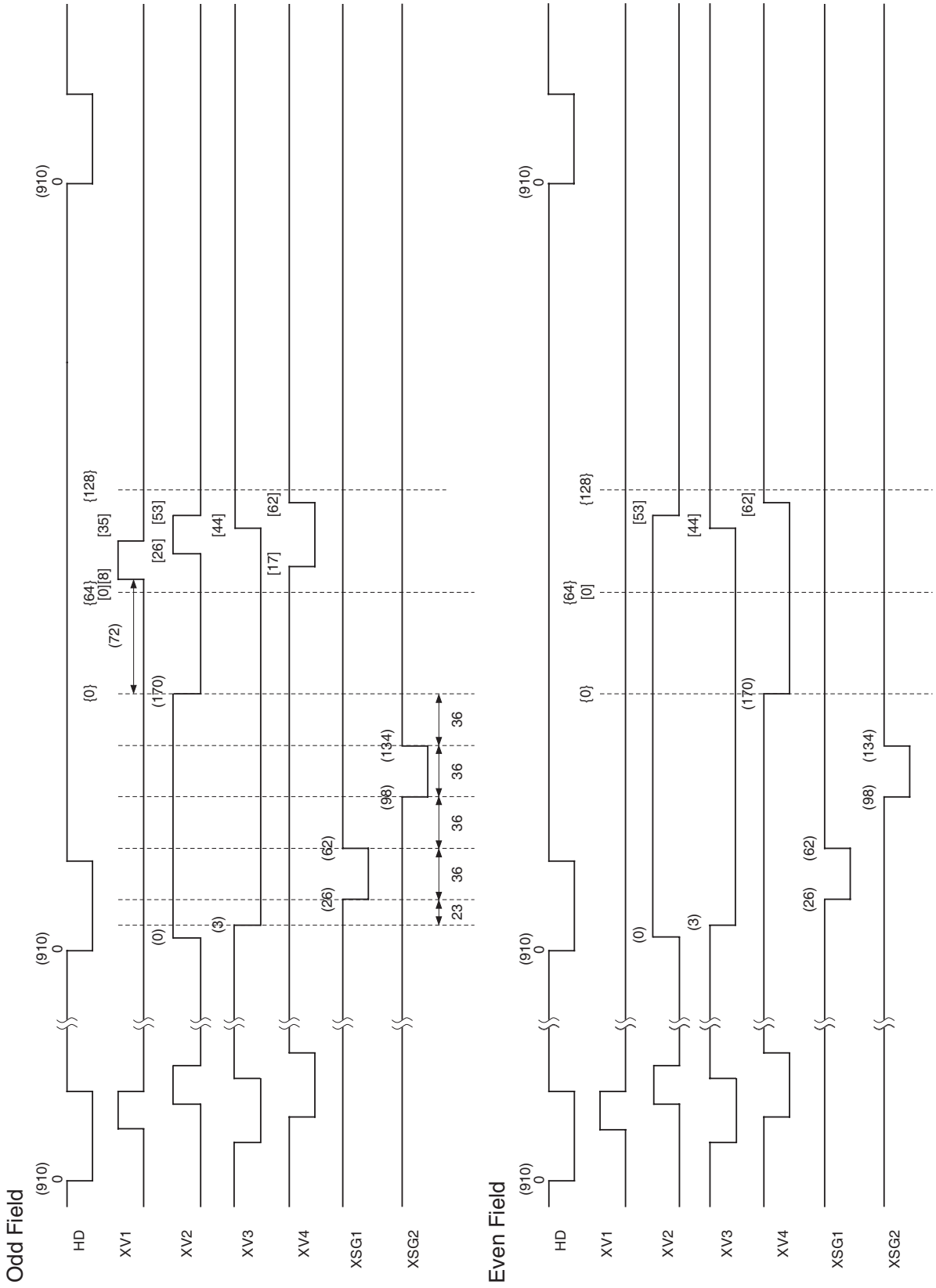
Horizontal Timing Chart MODESEL 0, 2 [510H NTSC]



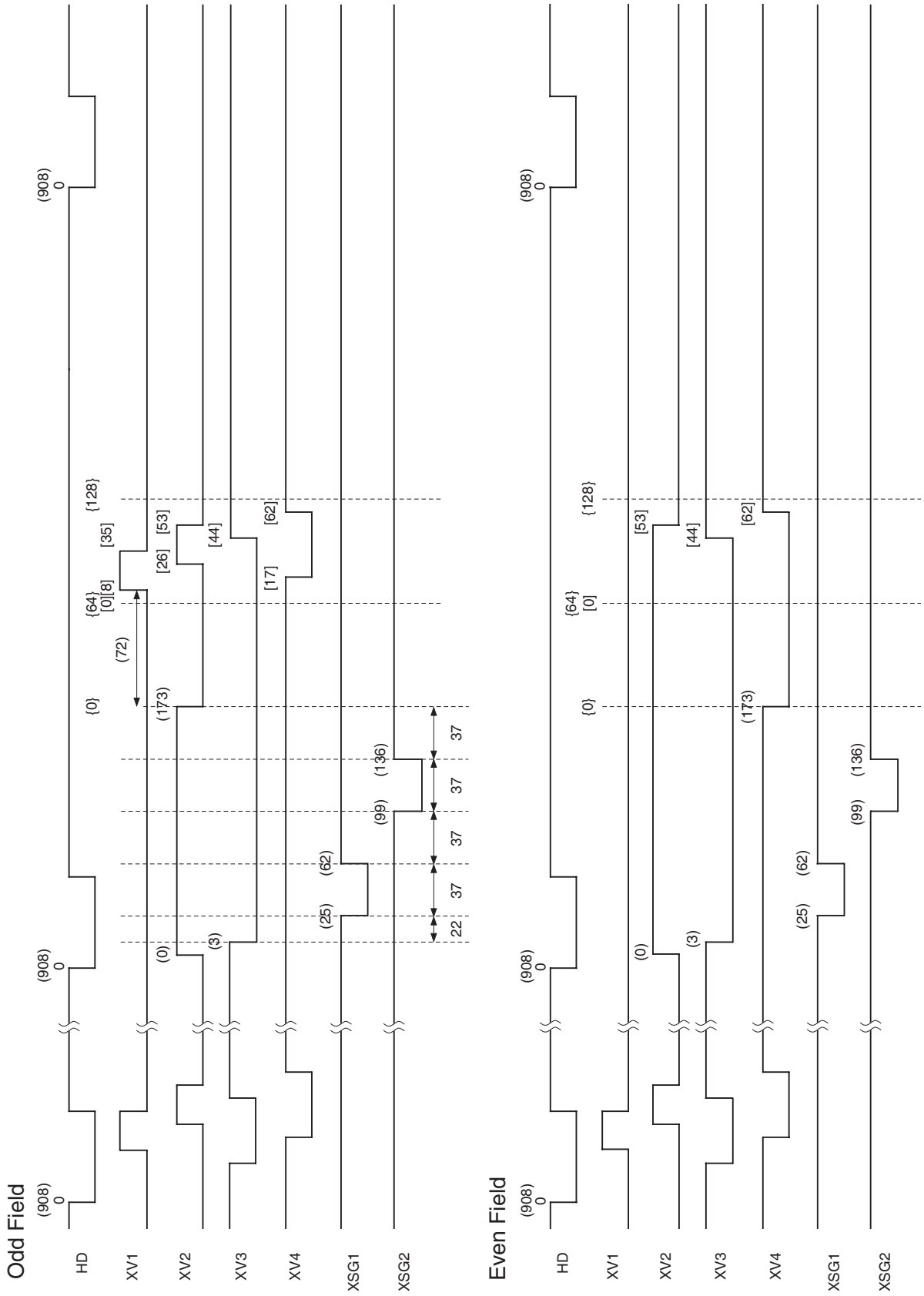
Horizontal Timing Chart MODESEL 3, 5 [510H PAL]



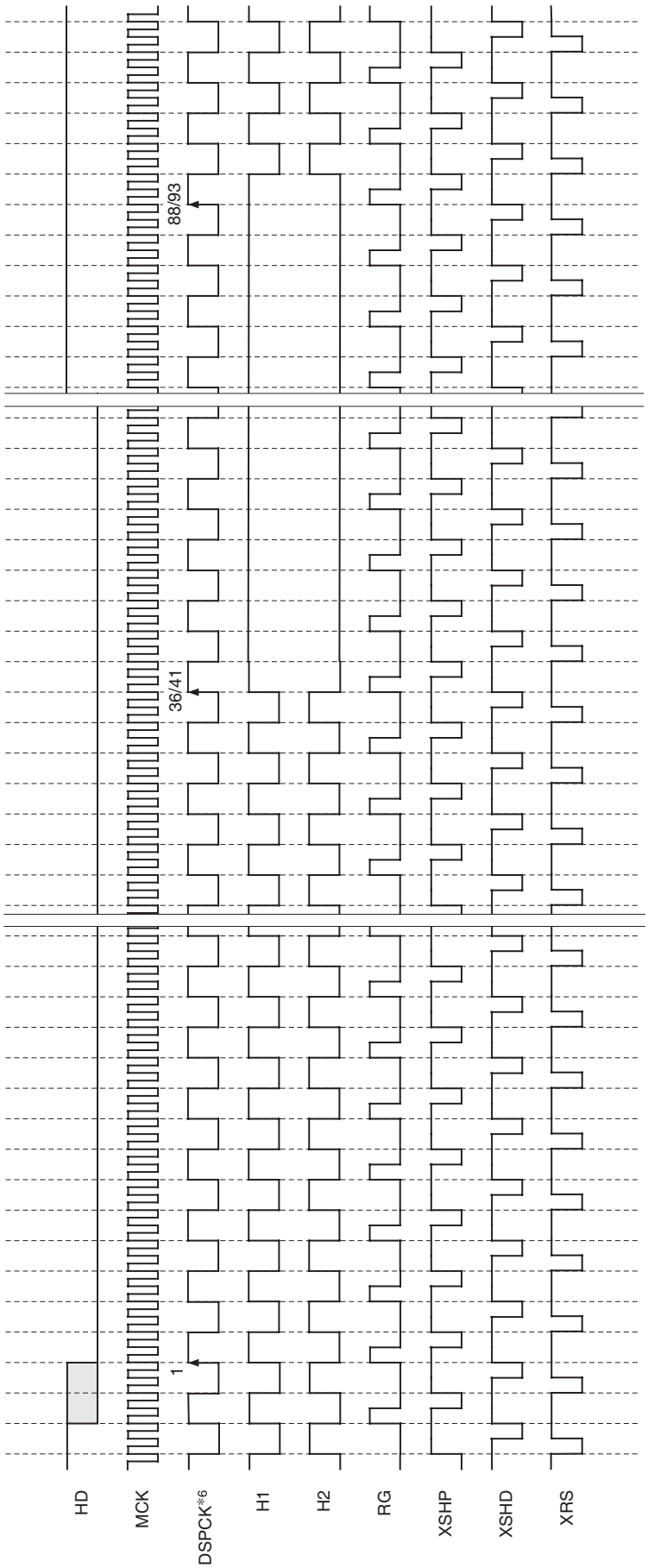
Horizontal Timing Chart MODESEL 6, 8 [760H NTSC]



Horizontal Timing Chart MODESEL 9, B [760H PAL]

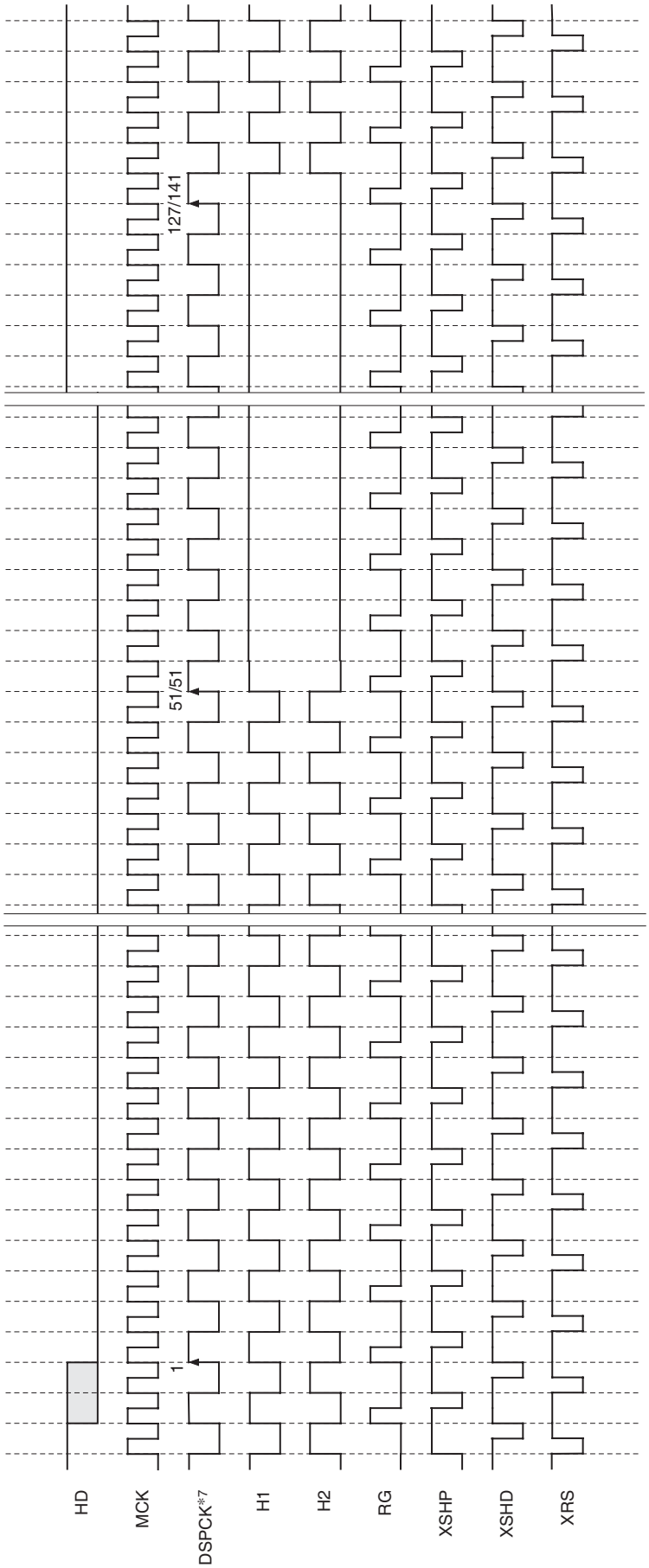


High-Speed Waveform Pulse MODESEL 0, 2, 3, 5 [510H NTSC/PAL]



*6 DSPCK is a clock which is not output by external pins. See the previously described table (Relationship between MODESEL and Each Clock).
* The phase relationship of each pulse shows the logical position relationship. For the actual output, a delay is added to each pulse.
* The high-speed pulse pin setting shown above indicates the state of initial setting of the parameter (Category 6 : TG)

High-Speed Waveform Pulse MODESEL 6, 8, 9, B [760H NTSC/PAL]



*7 DSPCK is a clock which is not output by external pins. See the previously described table (Relationship between MODESEL and Each Clock).
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Serial Communication Parameter

Communication Category Details

Category Classification	Description
CAT1 : SYSCON	System related parameters
CAT2 : PICT1	Image quality settings related parameters
CAT3 : FIX	Fix parameters
CAT4 : AWB1	AWB related parameters
CAT5 : OPDWND1	Nondisclosure parameters
CAT6 : TG	High-speed phase adjustment related parameters
CAT7 : EXTSYNC1	External sync related parameters
CAT8 : FEADJ (EVRI)	Internal EVR related parameters
CAT9 : MASKPG	Mask function and PG related parameters
CAT10 : DIF	Digital interface related parameters
CAT11 : BLMDETS1	Blemish detection related parameters
CAT12 : CPU	CPU related parameters
CAT13 : PICT2	Image quality setting related parameters
CAT14 : AE2	AE related parameters
CAT15 : AWB2	AWB related parameters
CAT16 : OPDWND2	OPD window related parameters
CAT17 : EXTSYNC2	External sync related parameters
CAT18 : FIX	Fix parameters
CAT19 : PREADJ	Adjustment related parameters
CAT20 : PORT	Port driver setting parameters
CAT21 : BLMDET2	Blemish detection related parameters
CAT22 : SOUT1	Serial output setting parameters
CAT23 : SOUT2	Serial output setting parameters
CAT24 : TEST	Test related parameters

Category 1 : SYSCON

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	MODEPARA1	MODESEL control parameter	0h	132h
	1	Fix	“0h” fixed	0h	
	2	MODEPARA2	MODESEL control parameter	1h	
	3	Fix	“0h” fixed	0h	
	4	MIRROR	Mirror switching 0h : Normal, 1h : Mirror	0h	
	5	Fix	“0h” fixed	0h	
	6	DEFON	Blemish compensation function ON/OFF 0h : OFF, 1h : ON	1h	
	7	DYNDETON	Dynamic blemish detection mode switching 0h : OFF, 1h : ON	1h	
2	0	Fix	“0h” fixed	0h	133h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
3	0	MODEPARA3	MODESEL control parameter	1h	134h
	1				
	2	DACMODE	DAC Out mode select (DAC1, DAC2) 0h : DAC1 = composite, DAC2 = not used, 1h : DAC1 = component Y, DAC2 = component C	0h	
	3	Fix	“0h” fixed	0h	
	4	SGPARA1	SGMODE control parameter	1h	
	5				
	6	MODEPARA4	MODESEL control parameter	2h	
	7				
4	0	Fix	“0h” fixed	0h	135h
	1				
	2				
	3				
	4				
	5				
	6	MODEPARA5	MODESEL control parameter	1h	
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	SYNCLV	Sync level setting NTSC : 9h, PAL : 7h	9h	136h
	1				
	2				
	3				
	4				
	5	CCLPOFF	Chroma clipping switching 0h : ON, 1h : OFF	0h	
	6	HILLIM	High luminance limit level setting (Limit level of the 10-bit DAC output range) 0h : OFF, 1h : 96%, 2h : 93%, 3h : 90%	0h	
	7				
6	0	PEDLIM	Pedestal limit level setting (Limit level of the 10-bit DAC output range) 0h : – 40IRE, 1h : – 25IRE, 2h : – 9IRE, 3h : 7IRE	0h	137h
	1				
	2	Fix	“0h” fixed	0h	
	3	Fix	“1h” fixed	1h	
	4	Fix	“3h” fixed	3h	
	5				
	6	Fix	“0h” fixed	0h	
	7	Fix	“1h” fixed	1h	
7	0	Fix	“0h” fixed	0h	138h
	1				
	2	Fix	“1h” fixed	1h	
	3	Fix	“0h” fixed	0h	
	4	YDSEL	Port 8 to Port 15/Digital signal output switching 0h : Port driver [15 : 8], 1h : YUV out	0h	
	5	Fix	“0h” fixed	0h	
	6	S0IN	SGMODE control parameter S0 pin I/O setting switching 0h : DHD OUT, 1h : VRI IN	1h	
	7	S1IN	SGMODE control parameter S1 pin I/O setting switching 0h : DVD OUT, 1h : “H” fixed (TEST input)	1h	
8	0	S2SEL	SGMODE control parameter S2 pin I/O setting switching 0h : TEST output, 1h : DHD, 2h : DVD, 3h : SYNC 4h : TEST output, 5h : TEST output, 6h : FLD 7h : Setting prohibited (TEST input)	0h	139h
	1				
	2				
	3	S3SEL	SGMODE control parameter S3 pin I/O setting switching 0h : DHD, 1h : DVD, 2h : HD, 3h : VD 4h : TEST output, 5h : TEST output, 6h : FLD 7h : Setting prohibited (TEST input)	0h	
	4				
	5				
	6	S4SEL	SGMODE control parameter S4 pin output setting switching 0h : TEST output, 1h : TEST output, 2h : HD, 3h : VD	0h	
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	Fix	“0h” fixed	0h	13Ah
	1				
	2				
	3				
	4				
	5				
	6				
	7				
10	0	Fix	“0h” fixed	0h	13Bh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
11	0	Fix	“0h” fixed	0h	13Ch
	1	Fix	“1h” fixed	1h	
	2	YDACSTB	Y D/A converter (DAC1) standby switching 0h : Normal operation, 1h : Standby	0h	
	3	CDACSTB	C D/A converter (DAC2) standby switching 0h : Normal operation, 1h : Standby	0h	
	4	Fix	“0h” fixed	0h	
	5	Fix	“0h” fixed	0h	
	6	VHOUT	VD/HD output setting switching 0h : Port driver [6 : 5], 1h : P5 = VD, P6 = HD output	0h	
	7	ADCKINV	AD clock inversion control 0h : Normal, 1h : Inverted	0h	
12	0	ADCKDL	AD clock delay control 0h : 0ns, 1h : 5ns, 2h : 10ns, 3h : 15ns	0h	13Dh
	1				
	2	YDACCKSEL	SGMODE control parameter Clock select for YDAC and Y encoder part 0h : ECK, 1h : MCK	0h	
	3	Fix	“0h” fixed	0h	
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0	BSTLV	Burst level setting NTSC : 38h, PAL : 3Ah	38h	13Eh
	1				
	2				
	3				
	4				
	5				
	6				
	7	AD6DBUP	Built-in AD 6dB up 0h : 0dB, 1h : 6dB up	0h	

Category 2 : PICT1

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	Fix	"1h" fixed	1h	13Fh
	1	Fix	"0h" fixed	0h	
	2				
	3	YLPFOFF	Y-LPF processing 0h : ON, 1h : OFF	0h	
	4	HAPGH	H aperture compensation high frequency gain setting 0h : × 0, 1h : × 1, 2h : × 2, 3h : × 4	2h	
	5				
	6	HAPGL	H aperture compensation low frequency gain setting 0h : × 0, 1h : × 1/2, 2h : × 1, 3h : × 2	2h	
	7				
2	0	VAPG	V aperture compensation gain setting 0h to Fh : × 0 to × 1	Ah	140h
	1				
	2				
	3				
	4	VAPSL	V aperture compensation slice level setting 0h to 7h : Min. (OFF) to Max.	2h	
	5				
	6				
	7	Fix	"0h" fixed	0h	
3	0	Fix	"Ch" fixed	Ch	141h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
4	0	Fix	"0h" fixed	0h	142h
	1				
	2	VHAPG	Aperture compensation gain 0h to Fh : × 0 to × 2	6h	
	3				
	4				
	5				
	6	HLAPG	Highlight aperture compensation total gain 0h : × 0, 1h : × 1/4, 2h : × 1/2, 3h : × 1	2h	
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	VHAPSL	Aperture compensation slice level setting 0h to Fh : Min. to Max.	4h	143h
	1				
	2				
	3				
	4	Fix	"3h" fixed	3h	
	5				
	6	Fix	"3h" fixed	3h	
	7				
6	0	Fix	"3h" fixed	3h	144h
	1				
	2	HLAPDS	Highlight aperture compensation reference level detection point selection 0h : Before gamma, 1h : After gamma	0h	
	3	HLAPSL	Highlight aperture compensation slice level setting	4h	
	4				
	5				
	6				
	7	YGAMSON	Luminance signal gamma curve compression function for low luminance areas 0h : OFF, 1h : ON	0h	
7	0	YGAMSLV	Luminance signal gamma curve compression level switching for low luminance areas 0h : Strong, 1h : Weak	0h	145h
	1	Fix	"1h" fixed	1h	
	2	YGAMSEL	Luminance signal variable gamma setting	4h	
	3				
	4				
	5	YKNEESEL	Luminance signal variable knee setting	3h	
	6				
	7				
8	0	YGAIN	Luminance signal gain setting 0h to FFh : × 0 to × 2	80h	146h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	YSPRSTH	Highlight suppression threshold value selection 0h : 100IRE, 1h : 105IRE, 2h : 111IRE, 3h : 116IRE	0h	147h
	1				
	2	YSPRSLV	Gain control value with suppression 0h : × 1, 1h : × 1/2, 2h : × 1/4, 3h : × 0	0h	
	3				
	4	WCLIP	White clip level setting 0h : 78% 1h : 89% 2h : 100% 3h : 105% 4h : 111% 5h : 116% 6h : 122% 7h : 153% (Max)	6h	
	5				
	6				
	7	Fix	“0h” fixed	0h	
10	0	SETUP	Setup level setting 0h to 3Fh : 0IRE to 39.5IRE (6-bit gradation) (Ch : 7.5IRE)	Ch	148h
	1				
	2				
	3				
	4				
	5				
	6	POSNEG	Positive/Negative inversion 0h : Positive, 1h : Negative	0h	
	7	DEON	Detail enhancement 0h : OFF, 1h : ON	1h	
11	0	DELVSEL	Emphasis level of detail enhancement 0h : Weak, 1h : Strong	0h	149h
	1	YDLY	System delay adjustment of Y main signal (0 to 15)	5h	
	2				
	3				
	4				
	5	Fix	“1h” fixed	1h	
	6				
	7				
12	0	Fix	“D1” fixed	D1h	14Ah
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0 1 2 3 4 5 6 7	Fix	“11h” fixed	11h	14Bh
14	0 1 2 3 4 5 6 7	Fix	“F4h” fixed	F4h	14Ch
15	0 1 2 3 4 5 6 7	Fix	“Fh” fixed	Fh	14Dh
16	0 1 2 3 4 5 6 7	Fix	“FFh” fixed	FFh	14Eh

Byte	Bit	Parameter name	Description	Initial value	E2P address
17	0 1 2 3 4 5 6 7	Fix	“FFh” fixed	FFh	14Fh
18	0 1 2 3 4 5 6 7	Fix	“10h” fixed	10h	150h
19	0 1 2 3 4 5 6 7	MIRRST	Mirror reset timing adjustment (Uses when MIRROR = 1)	0h	151h
20	0 1 2 3 4 5 6 7	CLS1RL	Complementary color pixel clip level S1R (LSB)	FFh	152h

Byte	Bit	Parameter name	Description	Initial value	E2P address
21	0	CLS1BL	Complementary color pixel clip level S1B (LSB)	FFh	153h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
22	0	CLS2RL	Complementary color pixel clip level S2R (LSB)	FFh	154h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
23	0	CLS2BL	Complementary color pixel clip level S2B (LSB)	FFh	155h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
24	0	Fix	“8h” fixed	8h	156h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
25	0	CLS1RM	Complementary color pixel clip level S1R (MSB)	7h	157h
	1				
	2				
	3	Fix	“0h” fixed	0h	
	4	CLS1BM	Complementary color pixel clip level S1B (MSB)	7h	
	5				
	6				
	7	Fix	“0h” fixed	0h	
26	0	CLS2RM	Complementary color pixel clip level S2R (MSB)	7h	158h
	1				
	2				
	3	Fix	“0h” fixed	0h	
	4	CLS2BM	Complementary color pixel clip level S2B (MSB)	7h	
	5				
	6				
	7	Fix	“0h” fixed	0h	
27	0	Fix	“2h” fixed	2h	159h
	1				
	2				
	3	Fix	“0h” fixed	0h	
	4	HLEDDL13	Highlight edge color compensation : DL13 line horizontal edge compensation 0h : OFF, 1h : ON	0h	
	5	HLEDDL2	Highlight edge color compensation : DL2 line horizontal edge compensation 0h : OFF, 1h : ON	0h	
	6	HLEDV	Highlight edge color compensation : V-edge compensation 0h : OFF, 1h : ON	0h	
	7	Fix	“0h” fixed	0h	
28	0	Fix	“0h” fixed	0h	15Ah
	1				
	2				
	3				
	4				
	5	CDLY	Chroma signal system delay adjustment 0h to 3h : 0 to + 3 pixels delay, 4h to 7h : – 4 to – 1 pixels delay	0h	
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
29	0	Fix	"1h" fixed	1h	15Bh
	1				
	2	Fix	"3h" fixed	3h	
	3				
	4				
	5	CLSOFF	Complementary color pixel clip function OFF 0h : ON, 1h : OFF	1h	
	6	Fix	"1h" fixed	1h	
	7	RBQUADON	Four-quadrant independent control switching of GAIN/HUE 0h : Simultaneous four quadrants, 1h : Independent four quadrants	0h	
30	0	CGAMMA	Chroma variable gamma parameter 0h to 7h : gamma small (line) to gamma large	4h	15Ch
	1				
	2				
	3	Fix	"0h" fixed	0h	
	4				
	5	CKNEE	Chroma variable knee parameter	3h	
	6				
	7				
31	0	RMATY	Primary color separation matrix constant for Red (complementary color mosaic) × – 0.5 (80h) to × 0.0 (00) to × 0.5 (7Fh)	2Fh	15Dh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
32	0	RMATC	Primary color separation matrix constant for Red (complementary color mosaic) × – 0.5 (80h) to × 0.0 (00) to × 0.5 (7Fh)	14h	15Eh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
33	0 1 2 3 4 5 6 7	BMATY	Primary color separation matrix constant for Blue (complementary color mosaic) × – 0.5 (80h) to × 0.0 (00) to × 0.5 (7Fh)	28h	15Fh
34	0 1 2 3 4 5 6 7	BMATC	Primary color separation matrix constant for Blue (complementary color mosaic) × – 0.5 (80h) to × 0.0 (00) to × 0.5 (7Fh)	DCh	160h
35	0 1 2 3 4 5 6 7	Fix	“80h” fixed	80h	161h
36	0 1 2 3 4 5 6 7	Fix	“80h” fixed	80h	162h

Byte	Bit	Parameter name	Description	Initial value	E2P address
37	0 1 2 3 4 5 6 7	RYGAIN1	First quadrant, R-Y gain × – 1 (80h) to × 0 (00) to × 1 (7Fh)	3Fh	163h
38	0 1 2 3 4 5 6 7	BYGAIN1	First quadrant, B-Y gain × – 1 (80h) to × 0 (00) to × 1 (7Fh)	21h	164h
39	0 1 2 3 4 5 6 7	RYHUE1	First quadrant, R-Y hue × – 1 (80h) to × 0 (00) to × 1 (7Fh)	80h	165h
40	0 1 2 3 4 5 6 7	BYHUE1	First quadrant, B-Y hue × – 1 (80h) to × 0 (00) to × 1 (7Fh)	FFh	166h

Byte	Bit	Parameter name	Description	Initial value	E2P address
41	0 1 2 3 4 5 6 7	RYGAIN2	Second quadrant, R-Y gain × – 1 (80h) to × 0 (00) to × 1 (7Fh)	3Fh	167h
42	0 1 2 3 4 5 6 7	BYGAIN2	Second quadrant, B-Y gain × – 1 (80h) to × 0 (00) to × 1 (7Fh)	21h	168h
43	0 1 2 3 4 5 6 7	RYHUE2	Second quadrant, R-Y hue × – 1 (80h) to × 0 (00) to × 1 (7Fh)	80h	169h
44	0 1 2 3 4 5 6 7	BYHUE2	Second quadrant, B-Y hue × – 1 (80h) to × 0 (00) to × 1 (7Fh)	FFh	16Ah

Byte	Bit	Parameter name	Description	Initial value	E2P address
45	0 1 2 3 4 5 6 7	RYGAIN3	Third quadrant, R-Y gain × – 1 (80h) to × 0 (00) to × 1 (7Fh)	3Fh	16Bh
46	0 1 2 3 4 5 6 7	BYGAIN3	Third quadrant, B-Y gain × – 1 (80h) to × 0 (00) to × 1 (7Fh)	21h	16Ch
47	0 1 2 3 4 5 6 7	RYHUE3	Third quadrant, R-Y hue × – 1 (80h) to × 0 (00) to × 1 (7Fh)	80h	16Dh
48	0 1 2 3 4 5 6 7	BYHUE3	Third quadrant, B-Y hue × – 1 (80h) to × 0 (00) to × 1 (7Fh)	FFh	16Eh

Byte	Bit	Parameter name	Description	Initial value	E2P address
49	0 1 2 3 4 5 6 7	RYGAIN4	Fourth quadrant, R-Y gain × – 1 (80h) to × 0 (00) to × 1 (7Fh)	3Fh	16Fh
50	0 1 2 3 4 5 6 7	BYGAIN4	Fourth quadrant, B-Y gain × – 1 (80h) to × 0 (00) to × 1 (7Fh)	21h	170h
51	0 1 2 3 4 5 6 7	RYHUE4	Fourth quadrant, R-Y hue × – 1 (80h) to × 0 (00) to × 1 (7Fh)	80h	171h
52	0 1 2 3 4 5 6 7	BYHUE4	Fourth quadrant, B-Y hue × – 1 (80h) to × 0 (00) to × 1 (7Fh)	FFh	172h

Byte	Bit	Parameter name	Description	Initial value	E2P address
53	0	Fix	“84h” fixed	84h	173h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
54	0	6DBDWN	6dB minus gain	0h	174h
	1	Fix	“0h” fixed	0h	
	2				
	3				
	4	Fix	“2h” fixed	2h	
	5				
	6	Fix	“0h” fixed	0h	
	7				
55	0	BLACKS1	Digital clamp black level setting (S1)	80h	175h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
56	0	BLACKS2	Digital clamp black level setting (S2)	80h	176h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
57	0	Fix	“40h” fixed	40h	177h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
58	0	Fix	“40h” fixed	40h	178h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
59	0	Fix	“40h” fixed	40h	179h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
60	0	Fix	“40h” fixed	40h	17Ah
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
61	0	Fix	“0h” fixed	0h	17Bh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
62	0	Fix	“0h” fixed	0h	17Ch
	1				
	2				
	3				
	4				
	5				
	6				
	7				
63	0	Fix	“0h” fixed	0h	17Dh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
64	0	Fix	“0h” fixed	0h	17Eh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Category 3 : FIX

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	Fix	“Fh” fixed	Fh	17Fh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
2	0	Fix	“0h” fixed	0h	180h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
3	0	Fix	“0h” fixed	0h	181h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
4	0	Fix	“0h” fixed	0h	182h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	Fix	“0h” fixed	0h	183h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Category 4 : AWB1

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	WBR	White balance gain R	37h	184h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
2	0	WBG	White balance gain G	26h	185h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
3	0	WBB	White balance gain B	39h	186h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
4	0	Fix	“0h” fixed	0h	187h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	Fix	“0h” fixed	0h	188h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
6	0	WBYUP	Integration range (upper luminance limit) 0h to FFh	D0h	189h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
7	0	WBYDWN	Integration range (lower luminance limit) 0h to FFh	4h	18Ah
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Category 5 : OPDWND1

The parameters in CAT5 (OPDWND1) is not opened.
* The parameters in CAT5 (OPDWND1) is overwritten by those in CAT16 (OPDWND2).

Category 6 : TG

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	Fix	“0h” fixed	0h	18Bh
	1	SGPARA2	SGMODE control parameter	1h	
	2	Fix	“0h” fixed	0h	
	3				
	4				
	5				
	6				
	7				
2	0	SGPARA3	SGMODE control parameter	2h	18Ch
	1				
	2				
	3				
	4	SGPARA4	SGMODE control parameter	2h	
	5				
	6				
	7				
3	0	SGPARA5	SGMODE control parameter	0h	18Dh
	1				
	2				
	3				
	4				
	5				
	6				
	7	Fix	“0h” fixed	0h	
4	0	SGPARA6	SGMODE control parameter	0h	18Eh
	1				
	2				
	3				
	4				
	5				
	6				
	7	Fix	“0h” fixed	0h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	Fix	“0h” fixed	0h	18Fh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
6	0	SGPARA7	SGMODE control parameter	0h	190h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
7	0	SGPARA8	SGMODE control parameter	0h	191h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
8	0	SGPARA9	SGMODE control parameter	0h	192h
	1				
	2	SGPARA10	SGMODE control parameter	0h	
	3				
	4	Fix	“0h” fixed	0h	
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	DEH1	H1 pulse delay adjustment 0h to 7h : – 8ns to – 1ns, 8h to Fh : 0ns to + 7ns	8h	193h
	1				
	2				
	3				
	4	DEH2	H2 pulse delay adjustment 0h to 7h : – 8ns to – 1ns, 8h to Fh : 0ns to + 7ns	8h	
	5				
	6				
	7				
10	0	DERG	RG pulse delay adjustment 0h to 7h : – 8ns to – 1ns, 8h to Fh : 0ns to + 7ns	Fh	194h
	1				
	2				
	3				
	4	DESHP	XSHP pulse delay adjustment 0h to 7h : – 8ns to – 1ns, 8h to Fh : 0ns to + 7ns	7h	
	5				
	6				
	7				
11	0	DESHD	XSHD pulse delay adjustment 0h to 7h : – 8ns to – 1ns, 8h to Fh : 0ns to + 7ns	0h	195h
	1				
	2				
	3				
	4	DERS	XRS pulse delay adjustment 0h to 7h : – 8ns to – 1ns, 8h to Fh : 0ns to + 7ns	Eh	
	5				
	6				
	7				
12	0	DUH1	H1 pulse duty adjustment 0h to 7h : 0ns to + 7ns (falling edge), 8h to Fh : 0ns to + 7ns (rising edge)	Ah	196h
	1				
	2				
	3				
	4	DUH2	H2 pulse duty adjustment 0h to 7h : 0ns to + 7ns (falling edge), 8h to Fh : 0ns to + 7ns (rising edge)	Ah	
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0	DURG	RG pulse duty adjustment 0h to 7h : 0ns to + 7ns (falling edge), 8h to Fh : 0ns to + 7ns (rising edge)	8h	197h
	1				
	2				
	3				
	4	DUSHP	XSHP pulse duty adjustment 0h to 7h : 0ns to + 7ns (falling edge), 8h to Fh : 0ns to + 7ns (rising edge)	0h	
	5				
	6				
	7				
14	0	DUSHD	XSHD pulse duty adjustment 0h to 7h : 0ns to + 7ns (falling edge), 8h to Fh : 0ns to + 7ns (rising edge)	1h	198h
	1				
	2				
	3				
	4	DURS	XRS pulse duty adjustment 0h to 7h : 0ns to + 7ns (falling edge), 8h to Fh : 0ns to + 7ns (rising edge)	0h	
	5				
	6				
	7				
15	0	Fix	“0h” fixed	0h	199h
	1				
	2				
	3				
	4	DRBH1	H1 drive capability adjustment 0h to 6h : Max. to Min., 7h : OFF	3h	
	5				
	6				
	7	Fix	“0h” fixed	0h	
16	0	DRBH2	H2 drive capability adjustment 0h to 6h : Max. to Min., 7h : OFF	3h	19Ah
	1				
	2				
	3	DRBRG	RG drive capability adjustment 0h to 6h : Max. to Min., 7h : OFF	3h	
	4				
	5				
	6	Fix	“0h” fixed	0h	
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
17	0	DRBSHD	XSHD drive capability adjustment 0h to 6h : Max. to Min., 7h : OFF	3h	19Bh
	1				
	2				
	3	DRBSHP	XSHP drive capability adjustment 0h to 6h : Max. to Min., 7h : OFF	3h	
	4				
	5				
	6	Fix	“0h” fixed	0h	
	7				
18	0	DRBRS	XRS drive capability adjustment 0h to 6h : Max. to Min., 7h : OFF	3h	19Ch
	1				
	2				
	3	Fix	“0h” fixed	0h	
	4				
	5				
	6				
	7				
19	0	H1INV	H1 signal inversion control 0h : Normal, 1h : Inverted	0h	19Dh
	1	H2INV	H2 signal inversion control 0h : Normal, 1h : Inverted	0h	
	2	RGINV	RG signal inversion control 0h : Normal, 1h : Inverted	0h	
	3	SHDINV	XSHD signal inversion control 0h : Normal, 1h : Inverted	0h	
	4	SHPINV	XSHP signal inversion control 0h : Normal, 1h : Inverted	0h	
	5	RSINV	XRS signal inversion control 0h : Normal, 1h : Inverted	0h	
	6	Fix	“0h” fixed	0h	
	7				
20	0	10NSDEH1	H1 pulse delay 10ns adjustment 0h : 0ns, 1h : + 5ns, 2h : + 10ns, 3h : –	0h	19Eh
	1				
	2	10NSDEH2	H2 pulse delay 10ns adjustment 0h : 0ns, 1h : + 5ns, 2h : + 10ns, 3h : –	0h	
	3				
	4	10NSDERG	RG pulse delay 10ns adjustment 0h : 0ns, 1h : + 5ns, 2h : + 10ns, 3h : –	0h	
	5				
	6	10NSDESHD	XSHD pulse delay 10ns adjustment 0h : 0ns, 1h : + 5ns, 2h : + 10ns, 3h : –	0h	
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
21	0	10NSDESHP	XSHP pulse delay 10ns adjustment 0h : 0ns, 1h : + 5ns, 2h : + 10ns, 3h : –	0h	19Fh
	1				
	2	10NSDERS	XRS pulse delay 10ns adjustment 0h : 0ns, 1h : + 5ns, 2h : + 10ns, 3h : –	0h	
	3				
	4	Fix	“0h” fixed	0h	
	5				
	6				
	7				

Category 7 : EXTSYNC1

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	SGPARA11	SGMODE control parameter	0h	1A0h
	1	HVPLL	SGMODE control : H/V-PLL selector (Equivalent to EXSTAT signal) 0h : H-PLL, 1h : V-PLL	0h	
	2	SGPARA12	SGMODE control parameter	0h	
	3	SGPARA13	SGMODE control parameter	0h	
	4	SGPARA14	SGMODE control parameter	0h	
	5	SGPARA15	SGMODE control parameter	0h	
	6	SGPARA16	SGMODE control parameter	0h	
	7	MODEPARA7	MODESEL control parameter	0h	
2	0	Fix	“0h” fixed	0h	1A1h
	1	VDETOFF	Invalidates external vertical sync signal detection 0h : Validated, 1h : Invalidated	0h	
	2	Fix	“0h” fixed	0h	
	3	Fix	“0h” fixed	0h	
	4	PCMPINV	Phase comparator input ref/var inverted 0h : Normal, 1h : Inverted	0h	
	5	Fix	“0h” fixed	0h	
	6	WBSTON	Wide burst function ON 0h : OFF, 1h : ON	0h	
	7	Fix	“0h” fixed	0h	
3	0	SGPARA17	SGMODE control parameter	0h	1A2h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
4	0	SGPARA18	SGMODE control parameter	E0h	1A3h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	SGPARA19	SGMODE control parameter	0h	1A4h
	1				
	2	SGPARA20	SGMODE control parameter	1h	
	3				
	4	Fix	“0h” fixed	0h	
	5				
	6				
	7	Fix	“1h” fixed	1h	
6	0	Fix	“11h” fixed	11h	1A5h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
7	0	WBHSETL	Horizontal start position of wide burst WBHSET (LSB)	0h	1A6h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
8	0	WBHRSTL	Horizontal end position of wide burst WBHRST (LSB)	0h	1A7h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	WBHSETM	WBHSET (MSB)	0h	1A8h
	1				
	2	WBHRSTM	WBHRST (MSB)	0h	
	3				
	4	Fix	“7h” fixed	7h	
	5				
	6				
	7				
10	0	Fix	“37h” fixed	37h	1A9h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
11	0	SGPARA21	SGMODE control parameter	0h	1AAh
	1	SGPARA22	SGMODE control parameter	0h	
	2	Fix	“0h” fixed	0h	
	3				
	4				
	5				
	6				
	7				

Category 8 : FEADJ (EVRI)

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	ADDLY	Input data delay adjustment 0h : 0ns, 1h : 10ns delay	0h	1ABh
	1	AD1STINV	1stF/F clock select 0h : Normal, 1h : Inverted	0h	
	2	Fix	"0h" fixed	0h	
	3				
	4	DL1CK	AD data 1 delay and shifter function 0h : Normal, 1h : + 1delay, 2h : 1/2, 3h : 1/4	0h	
	5				
	6	Fix	"0h" fixed	0h	
	7	Fix	"0h" fixed	0h	
2	0	SYSDLY	Horizontal direction delay value adjustment	Fh	1ACh
	1				
	2				
	3				
	4	Fix	"0h" fixed	0h	
	5	EVR0STB	EVR0 standby control 0h : Normal, 1h : Standby	0h	
	6	EVR1STB	EVR1 standby control 0h : Normal, 1h : Standby	0h	
	7	EVR2STB	EVR2 standby control 0h : Normal, 1h : Standby	0h	
3	0	AGCCNT	AGC gain control (EVR0) (User release when AEHOLD = 1)	1Eh	1ADh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
4	0	EVR1CNT	MIRIS control (EVR1) (User release when MIRIS = 0 or AEHOLD = 1)	FFh	1AEh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	EVR2CNT	Output voltage setting in EVR2	FFh	1AFh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
6	0	Fix	“0h” fixed	0h	1B0h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Category 9 : MASKPG

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	MSK0HSET	Horizontal start position of MASK 0 (4-pixel units)	2h	1B1h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
2	0	MSK1HSET	Horizontal start position of MASK 1 (4-pixel units)	2h	1B2h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
3	0	MSK2HSET	Horizontal start position of MASK 2 (4-pixel units)	2h	1B3h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
4	0	MSK3HSET	Horizontal start position of MASK 3 (4-pixel units)	2h	1B4h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	MSK4HSET	Horizontal start position of MASK 4 (4-pixel units)	2h	1B5h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
6	0	MSK5HSET	Horizontal start position of MASK 5 (4-pixel units)	2h	1B6h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
7	0	MSK6HSET	Horizontal start position of MASK 6 (4-pixel units)	2h	1B7h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
8	0	MSK7HSET	Horizontal start position of MASK 7 (4-pixel units)	2h	1B8h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	MSK0HRST	Horizontal end position of MASK 0 (4-pixel units)	2h	1B9h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
10	0	MSK1HRST	Horizontal end position of MASK 1 (4-pixel units)	2h	1BAh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
11	0	MSK2HRST	Horizontal end position of MASK 2 (4-pixel units)	2h	1BBh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
12	0	MSK3HRST	Horizontal end position of MASK 3 (4-pixel units)	2h	1BCh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0	MSK4HRST	Horizontal end position of MASK 4 (4-pixel units)	2h	1BDh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
14	0	MSK5HRST	Horizontal end position of MASK 5 (4-pixel units)	2h	1BEh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
15	0	MSK6HRST	Horizontal end position of MASK 6 (4-pixel units)	2h	1BFh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
16	0	MSK7HRST	Horizontal end position of MASK 7 (4-pixel units)	2h	1C0h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
17	0	MSK0VSET	Vertical start position of MASK 0 (4-line units)	0h	1C1h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
18	0	MSK1VSET	Vertical start position of MASK 1 (4-line units)	0h	1C2h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
19	0	MSK2VSET	Vertical start position of MASK 2 (4-line units)	0h	1C3h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
20	0	MSK3VSET	Vertical start position of MASK 3 (4-line units)	0h	1C4h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
21	0	MSK4VSET	Vertical start position of MASK 4 (4-line units)	0h	1C5h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
22	0	MSK5VSET	Vertical start position of MASK 5 (4-line units)	0h	1C6h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
23	0	MSK6VSET	Vertical start position of MASK 6 (4-line units)	0h	1C7h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
24	0	MSK7VSET	Vertical start position of MASK 7 (4-line units)	0h	1C8h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
25	0	MSK0VRST	Vertical end position of MASK 0 (4-line units)	0h	1C9h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
26	0	MSK1VRST	Vertical end position of MASK 1 (4-line units)	0h	1CAh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
27	0	MSK2VRST	Vertical end position of MASK 2 (4-line units)	0h	1CBh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
28	0	MSK3VRST	Vertical end position of MASK 3 (4-line units)	0h	1CCh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
29	0 1 2 3 4 5 6 7	MSK4VRST	Vertical end position of MASK 4 (4-line units)	0h	1CDh
30	0 1 2 3 4 5 6 7	MSK5VRST	Vertical end position of MASK 5 (4-line units)	0h	1CEh
31	0 1 2 3 4 5 6 7	MSK6VRST	Vertical end position of MASK 6 (4-line units)	0h	1CFh
32	0 1 2 3 4 5 6 7	MSK7VRST	Vertical end position of MASK 7 (4-line units)	0h	1D0h

Byte	Bit	Parameter name	Description	Initial value	E2P address
33	0	MSKBYLV	B-Y setting value for MASK color – 128 to + 127	0h	1D1h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
34	0	MSKRYLV	R-Y setting value for MASK color – 128 to + 127	0h	1D2h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
35	0	MSKYLVL	Luminance level setting of MASK (LSB)	0h	1D3h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
36	0	MSKYLVM	Luminance level setting of MASK (MSB)	0h	1D4h
	1	MSKON	MASK function switching 0h : OFF, 1h : ON	0h	
	2	MSKHLD	Uses background color as MASK color 0h : OFF, 1h : ON	0h	
	3	PGON	Test pattern generator switching 0h : OFF, 1h : ON	0h	
	4	PGBIDINV	PG color identification signal inversion 0h : Normal, 1h : Inverted	0h	
	5	Fix	“1h” fixed	1h	
	6	PGGAIN	PG data gain adjustment 0h : × 0, 1h : × 1, 2h : × 2, 3h : × 4	2h	
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
37	0	PGPAT	PG pattern switching 0h : Color bar, 1h : Raster, 2h : Impulse, 3h : Serial setting	0h	1D5h
	1				
	2	PGHV	PG pattern direction setting 0h : Horizontal, 1h : Vertical	0h	
	3	PGRION	Ramp/inversion of impulse effect addition for PG pattern 0h : Normal, 1h : Addition	0h	
	4	PGRAWMIX	Output CCD signal except PG area 0h : Full-screen PG, 1h : CCD signal output	0h	
	5	PGCOLOR	Color specification of raster setting 0h : White, 1h : Yellow, 2h : Cyan, 3h : Green 4h : Magenta, 5h : Red, 6h : Blue, 7h : Simple horizontal ramp	0h	
	6				
	7				
38	0	MSKDLY	Delay adjustment of Y mask signal 0h to 7h : 0 to 7, 8h to Fh : – 8 to – 1	7h	1D6h
	1				
	2				
	3				
	4	MSKDLC	Delay adjustment of chroma mask signal 0h to 7h : 0 to 7, 8h to Fh : – 8 to – 1	8h	
	5				
	6				
	7				
39	0	PGSDCRS2	Mg + Ye data	0h	1D7h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
40	0	PGSDCRS1	G + Cy data	0h	1D8h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
41	0	PGSDCBS2	G + Ye data	0h	1D9h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
42	0	PGSDCBS1	Mg + Cy data	0h	1DAh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Category 10 : DIF

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	Fix	“1h” fixed	1h	1DBh
	1	MODEPARA8	MODESEL control parameter	0h	
	2	Fix	“1h” fixed	1h	
	3	Fix	“10h” fixed	10h	
	4				
	5				
	6				
	7				
2	0	EAVSTAL	EAV start position (LSB)	0h	1DCh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
3	0	EAVSTAM	EAV start position (MSB)	0h	1DDh
	1				
	2				
	3	Fix	“0h” fixed	0h	
	4				
	5				
	6				
	7				
4	0	SAVSTAL	SAV start position (LSB)	18h	1DEh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	SAVSTAM	SAV start position (MSB)	1h	1DFh
	1				
	2				
	3	Fix	"0h" fixed	0h	
	4				
	5				
	6				
	7				
6	0	FLD1FSTA	F bit start position of ODD (Field 1)	3h	1E0h
	1				
	2				
	3	FLD1VSTA	V bit start position of ODD (Field 1)	12h	
	4				
	5				
	6				
	7				
7	0	FLD2FSTA	F bit start position of EVEN (Field 2)	3h	1E1h
	1				
	2				
	3	FLD2VSTA	V bit start position of EVEN (Field 2)	13h	
	4				
	5				
	6				
	7				
8	0	RECYGAIN	Digital Y gain setting 0h to FFh : × 0 to × 1.99	80h	1E2h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0 1 2 3 4 5 6 7	RECRYGAIN	Digital R-Y gain setting 0h to FFh : × 0 to × 3.99	64h	1E3h
10	0 1 2 3 4 5 6 7	RECBYGAIN	Digital B-Y gain setting 0h to FFh : × 0 to × 3.99	88h	1E4h
11	0 1 2 3 4 5 6 7	Fix	“0h” fixed	0h	1E5h
12	0 1 2 3 4 5 6 7	Fix	“0h” fixed	0h	1E6h

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0	Fix	“0h” fixed	0h	1E7h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
14	0	Fix	“0h” fixed	0h	1E8h
	1				
	2	Fix	“0h” fixed	0h	
	3				
	4	DCKINV	DCK inversion control 0h : Normal, 1h : Inverted	0h	
	5	DCKDL	DCK delay adjustment 0h : 0ns, 1h : 5ns, 2h : 10ns, 3h : 15ns	0h	
	6				
	7	DIFON	DCK output ON/OFF control and digital signal processing operation 0h : OFF, 1h : Operation (output)	0h	

Category 11 : BLMDETS1

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	DEFPG	Quasi-blemish generation switching 0h : OFF, 1h : ON	0h	1ECh
	1	DEFMK	Display of blemish marker 0h : OFF, 1h : ON	0h	
	2	Fix	“0h” fixed	0h	
	3	Fix	“0h” fixed	0h	
	4	AREA	Display of blemish detection area 0h : OFF, 1h : ON	0h	
	5	Fix	“0h” fixed	0h	
	6				
	7				
2	0	DEFPGLVL	Quasi-blemish level setting (LSB)	0h	1EDh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
3	0	DEFPGLVM	Quasi-blemish level setting (MSB)	0h	1EEh
	1				
	2	Fix	“7h” fixed	7h	
	3				
	4				
	5				
	6				
	7	Fix	“0h” fixed	0h	
4	0	FLDWAIT	Number of waiting fields in Dynamic detection (even field only) 2h to FEh : 2FLD to 254FLD	0h	1EFh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	DETREFL	Threshold level of blemish detection (LSB) (Common use of Dynamic and Static)	0h	1F0h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
6	0	Fix	“0h” fixed	0h	1F1h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
7	0	Fix	“0h” fixed	0h	1F2h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
8	0	DARKREFL	Reference dark level of Dynamic detection (LSB)	0h	1F3h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	DETREFM	Threshold level of blemish detection (MSB) (Common use of Dynamic and Static)	0h	1F4h
	1				
	2	Fix	“0h” fixed	0h	
	3				
	4	Fix	“0h” fixed	0h	
	5				
	6	DARKREFM	Reference dark level of Dynamic detection (MSB)	0h	
	7				
10	0	IBLKS1L	S1 black level for Static detection (LSB)	0h	1F5h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
11	0	IBLKS2L	S2 black level for Static detection (LSB)	0h	1F6h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
12	0	IBLKS1M	S1 black level for Static detection (MSB)	0h	1F7h
	1	IBLKS2M	S2 black level for Static detection (MSB)	0h	
	2	Fix	“0h” fixed	0h	
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0	HSRTL	Blemish detection area, horizontal start position setting (LSB)	0h	1F8h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
14	0	VSRTL	Blemish detection area, vertical start position setting (LSB)	0h	1F9h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
15	0	HWIDTHL	Blemish detection area, horizontal width setting (LSB)	FFh	1FAh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
16	0	VWIDTHL	Blemish detection area, vertical width setting (LSB)	FFh	1FBh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
17	0	HSRTM	Blemish detection area, horizontal start position setting (MSB)	0h	1FCh
	1				
	2	VSRTM	Blemish detection area, vertical start position setting (MSB)	0h	
	3				
	4	HWIDTHM	Blemish detection area, horizontal width setting (MSB)	3h	
	5				
	6	VWIDTHM	Blemish detection area, vertical width setting (MSB)	3h	
	7				
18	0	ADDRRST	Blemish address reset 1h : Reset	0h	1FDh
	1	Fix	“0h” fixed	0h	
	2				
	3				
	4				
	5				
	6				
	7				
19	0	Fix	“0h” fixed	0h	1FEh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
20	0	DETLV00	Blemish level	0h	1FFh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
21	0				200h
	1				
	2	HCNT00	Horizontal address of blemish	0h	
	3				
	4				
	5				
	6				
	7				
22	0				201h
	1				
	2				
	3				
	4	VCNT00	Vertical address of blemish	0h	
	5				
	6				
	7				
23	0				202h
	1				
	2				
	3				
	4				
	5				
	6	Fix	“0h” fixed	0h	
	7	SD00	Type of blemish detection 0h : Static detection, 1h : Dynamic detection	0h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
24	0	DETLV01	Blemish level	0h	203h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
25	0				204h
	1				
	2	HCNT01	Horizontal address of blemish	0h	
	3				
	4				
	5				
	6				
	7				
26	0				205h
	1				
	2				
	3				
	4	VCNT01	Vertical address of blemish	0h	
	5				
	6				
	7				
27	0				206h
	1				
	2				
	3				
	4				
	5				
	6	Fix	“0h” fixed	0h	
	7	SD01	Type of blemish detection 0h : Static detection, 1h : Dynamic detection	0h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
28	0	DETLV02	Blemish level	0h	207h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
29	0				208h
	1				
	2	HCNT02	Horizontal address of blemish	0h	
	3				
	4				
	5				
	6				
	7				
30	0				209h
	1				
	2				
	3				
	4	VCNT02	Vertical address of blemish	0h	
	5				
	6				
	7				
31	0				20Ah
	1				
	2				
	3				
	4				
	5				
	6	Fix	“0h” fixed	0h	
	7	SD02	Type of blemish detection 0h : Static detection, 1h : Dynamic detection	0h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
32	0	DETLV03	Blemish level	0h	20Bh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
33	0				20Ch
	1				
	2	HCNT03	Horizontal address of blemish	0h	
	3				
	4				
	5				
	6				
	7				
34	0				20Dh
	1				
	2				
	3				
	4	VCNT03	Vertical address of blemish	0h	
	5				
	6				
	7				
35	0				20Eh
	1				
	2				
	3				
	4				
	5				
	6	Fix	“0h” fixed	0h	
	7	SD03	Type of blemish detection 0h : Static detection, 1h : Dynamic detection	0h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
36	0	DETLV04	Blemish level	0h	20Fh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
37	0				210h
	1				
	2	HCNT04	Horizontal address of blemish	0h	
	3				
	4				
	5				
	6				
	7				
38	0				211h
	1				
	2				
	3				
	4	VCNT04	Vertical address of blemish	0h	
	5				
	6				
	7				
39	0				212h
	1				
	2				
	3				
	4				
	5				
	6	Fix	“0h” fixed	0h	
	7	SD04	Type of blemish detection 0h : Static detection, 1h : Dynamic detection	0h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
40	0	DETLV05	Blemish level	0h	213h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
41	0				214h
	1				
	2	HCNT05	Horizontal address of blemish	0h	
	3				
	4				
	5				
	6				
	7				
42	0				215h
	1				
	2				
	3				
	4	VCNT05	Vertical address of blemish	0h	
	5				
	6				
	7				
43	0				216h
	1				
	2				
	3				
	4				
	5				
	6	Fix	“0h” fixed	0h	
	7	SD05	Type of blemish detection 0h : Static detection, 1h : Dynamic detection	0h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
44	0	DETLV06	Blemish level	0h	217h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
45	0				218h
	1				
	2	HCNT06	Horizontal address of blemish	0h	
	3				
	4				
	5				
	6				
	7				
46	0				219h
	1				
	2				
	3				
	4	VCNT06	Vertical address of blemish	0h	
	5				
	6				
	7				
47	0				21Ah
	1				
	2				
	3				
	4				
	5				
	6	Fix	“0h” fixed	0h	
	7	SD06	Type of blemish detection 0h : Static detection, 1h : Dynamic detection	0h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
48	0	DETLV07	Blemish level	0h	21Bh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
49	0				21Ch
	1				
	2	HCNT07	Horizontal address of blemish	0h	
	3				
	4				
	5				
	6				
	7				
50	0				21Dh
	1				
	2				
	3				
	4	VCNT07	Vertical address of blemish	0h	
	5				
	6				
	7				
51	0				21Eh
	1				
	2				
	3				
	4				
	5				
	6	Fix	“0h” fixed	0h	
	7	SD07	Type of blemish detection 0h : Static detection, 1h : Dynamic detection	0h	

Category 12 : CPU

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	MODESEL	DSP operation mode 0h, 3h, 6h and 9h : Analog/digital output 2h, 5h, 8h and Bh : 27M master MCK PLL	6h	2h
	1				
	2				
	3				
	4	Fix	"0h" fixed	0h	
	5				
	6				
	7				
2	0	ADJMODE	Adjustment mode 0h : Normal mode 20h : AGCMIN auto adjustment mode 21h : Pre-WB adjustment mode 22h : Blemish detection and compensation mode 31h : White balance gain output mode 32h : OPD evaluated value output mode	0h	3h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
3	0	PREWBMODE	Pre-WB adjustment mode (Effective when ADJMODE = 21h) 0h : No operation 1h : 3200K adjustment 2h : Low color temperature adjustment 3h : High color temperature adjustment	0h	4h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
4	0	CCDLEV	AGCMIN auto adjustment parameter	0h	5h
	1	Fix	"0h" fixed	0h	
	2				
	3				
	4				
	5	AGCMINFIN	End flag of AGCMIN auto adjustment 0h : Not end, 1h : End	0h	
	6	BLMDETFIN	End flag of Static detection 0h : Not end, 1h : End	0h	
	7	Fix	"0h" fixed	0h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	CPUHOLD	CPU hold 0h : Operation, 1h : Stop	0h	6h
	1	AWBHOLD	AWB hold 0h : Operation, 1h : Stop	0h	
	2	AEHOLD	AE hold 0h : Operation, 1h : Stop	0h	
	3	CLMPHOLD	Clamp hold 0h : Operation, 1h : Stop	0h	
	4	SGHOLD	SG hold 0h : Operation, 1h : Stop	0h	
	5	PDRHOLD	Port driver hold 0h : Operation, 1h : Stop	0h	
	6	Fix	"0h" fixed	0h	
	7				
6	0	Fix	"0h" fixed	0h	7h
	1	OUTGAIN	OUTGAIN 0h : OFF, 1h : ON	0h	
	2	Fix	"1h" fixed	1h	
	3	ASPR	Aperture compensation suppress 0h : OFF, 1h : ON	1h	
	4	CSPR	Chroma suppress 0h : OFF, 1h : ON	1h	
	5	Fix	"0h" fixed	0h	
	6				
	7				
7	0	GAMSEL	Gamma parameter select 0h : EEPROM value, 1h : User setting value (CAT13 setting value)	0h	8h
	1	Fix	"0h" fixed	0h	
	2	Fix	"0h" fixed	0h	
	3				
	4				
	5				
	6				
	7				
8	0	VHAPGCTL	External control of VH aperture compensation gain 0h : Disabled, 1h : Enabled	0h	9h
	1	Fix	"0h" fixed	0h	
	2	CRGAINCTL	External control of chroma gain 0h : Disabled 1h : Enabled	0h	
	3	Fix	"0h" fixed	0h	
	4	HUECTL	External control of HUE 0h : Disabled 1h : Enabled	0h	
	5	Fix	"0h" fixed	0h	
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	Fix	“0h” fixed	0h	Ah
	1				
	2				
	3				
	4				
	5				
	6				
	7				
10	0	BPSSEL	RS-232C bit rate selection 0h : 9600bps, 1h : 19200bps	1h	Bh
	1	Fix	“0h” fixed	0h	
	2				
	3				
	4				
	5				
	6				
	7				
11	0	CRLESSON	Anti color-rolling mode 0h : OFF, 1h : ON	0h	Ch
	1	CRLESSAWB	Anti color-rolling AWB 0h : OFF, 1h : ON	1h	
	2	U6DBDWN	6dB minus gain	1h	
	3	Fix	“0h” fixed	0h	
	4				
	5				
	6				
	7				
12	0	Fix	“1h” fixed	1h	Dh
	1	Fix	“0h” fixed	0h	
	2	Fix	“1h” fixed	1h	
	3	Fix	“0h” fixed	0h	
	4				
	5	SSELOFF	S pin control by SGMODE 0h : ON, 1h : OFF	0h	
	6	Fix	“0h” fixed	0h	
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0	YDLYOFF	YDLY control 0h : ON, 1h : OFF	1h	Eh
	1	SYSSELON	System configuration switching function 0h : OFF, 1h : ON	0h	
	2	SYSSELFLG	System selection flag	0h	
	3	CROFFCTLON	Low illuminance chroma OFF control 0h : Control OFF, 1h : Control ON	0h	
	4	CROFFJUDG	Low illuminance chroma OFF judgment result flag 0h : Chroma ON, 1h : Chroma OFF	0h	
	5	Fix	"0h" fixed	0h	
	6				
	7				
14	0	YDLY0	YDLY when YDACCKSEL = 0h (Effective when YDLYOFF = 0h)	0h	Fh
	1				
	2				
	3				
	4	Fix	"0h" fixed	0h	
	5				
	6				
	7				
15	0	YDLY1	YDLY when YDACCKSEL = 1h (Effective when YDLYOFF = 0h)	0h	10h
	1				
	2				
	3				
	4	Fix	"0h" fixed	0h	
	5				
	6				
	7				
16	0	MODESEL0	MODESEL when SYSSELFLG = 0h (Effective when SYSSELON = 1h)	0h	11h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
17	0	MODESEL1	MODESEL when SYSSELFLG = 1h (Effective when SYSSELON = 1h)	0h	12h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
18	0	SGMODE0	SGMODE when SYSSELFLG = 0h (Effective when SYSSELON = 1h)	0h	13h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
19	0	SGMODE1	SGMODE when SYSSELFLG = 1h (Effective when SYSSELON = 1h)	0h	14h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
20	0	EVR20	EVR2 output when SYSSELFLG = 0h (Effective when SYSSELON = 1h)	0h	15h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
21	0 1 2 3 4 5 6 7	EVR21	EVR2 output when SYSSELFLG = 1h (Effective when SYSSELON = 1h)	0h	16h
22	0 1 2 3 4 5 6 7	Fix	“1h” fixed	1h	17h
23	0 1 2 3 4 5 6 7	Fix	“Bh” fixed	Bh	18h
24	0 1 2 3 4 5 6 7	Fix	“Ah” fixed	Ah	19h

Byte	Bit	Parameter name	Description	Initial value	E2P address
25	0 1 2 3 4 5 6 7	Fix	“Ah” fixed	Ah	1Ah
26	0 1 2 3 4 5 6 7	Fix	“0h” fixed	0h	1Bh
27	0 1 2 3 4 5 6 7	Fix	“0h” fixed	0h	1Ch
28	0 1 2 3 4 5 6 7	Fix	“Ah” fixed	Ah	1Dh

Byte	Bit	Parameter name	Description	Initial value	E2P address
29	0 1 2 3 4 5 6 7	Fix	“Ah” fixed	Ah	1Eh
30	0 1 2 3 4 5 6 7	Fix	“Ah” fixed	Ah	1Fh
31	0 1 2 3 4 5 6 7	Fix	“Ah” fixed	Ah	20h
32	0 1 2 3 4 5 6 7	Fix	“Ah” fixed	Ah	21h

Byte	Bit	Parameter name	Description	Initial value	E2P address
33	0	Fix	“Ah” fixed	Ah	22h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
34	0	Fix	“0h” fixed	0h	23h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
35	0	Fix	“Ah” fixed	Ah	24h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
36	0	Fix	“Ah” fixed	Ah	25h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
37	0	Fix	“Ah” fixed	Ah	26h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
38	0	Fix	“Ah” fixed	Ah	27h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
39	0	Fix	“0h” fixed	0h	28h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Category 13 : PICT2

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	Fix	“2Dh” fixed	2Dh	29h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
2	0	Fix	“0h” fixed	0h	2Ah
	1				
	2				
	3				
	4				
	5				
	6				
	7				
3	0	Fix	“45h” fixed	45h	2Bh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
4	0	Fix	“BBh” fixed	BBh	2Ch
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	Fix	“FFh” fixed	FFh	2Dh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
6	0	Fix	“FFh” fixed	FFh	2Eh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
7	0	Fix	“80h” fixed	80h	2Fh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
8	0	Fix	“80h” fixed	80h	30h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	Fix	“2Fh” fixed	2Fh	31h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
10	0	Fix	“1Ch” fixed	1Ch	32h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
11	0	Fix	“6h” fixed	6h	33h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
12	0	OUTGAINMAX	OUTGAIN setting value (OUTGAIN = 1h)	2h	34h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0 1 2 3 4 5 6 7	RYGAINRATE	RYGAIN coefficient (OUTGAIN = 1h) RYGAIN ← RYGAIN × OUTGAINMAX × RYGAINRATE/FFh	C0h	35h
14	0 1 2 3 4 5 6 7	BYGAINRATE	BYGAIN coefficient (OUTGAIN = 1h) BYGAIN ← BYGAIN × OUTGAINMAX × BYGAINRATE/FFh	C0h	36h
15	0 1 2 3 4 5 6 7	YGAINRATE	YGAIN coefficient (OUTGAIN = 1h) YGAIN ← YGAIN × OUTGAINMAX × YGAINRATE/FFh	C0h	37h
16	0 1 2 3 4 5 6 7	ASPRSTA	Aperture compensation suppress start AGCCNT (Set value as ASPRSTA < ASPREND)	A0h	38h

Byte	Bit	Parameter name	Description	Initial value	E2P address
17	0	ASPREND	Aperture compensation suppress end AGCCNT (Set value as ASPRSTA < ASPREND)	D0h	39h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
18	0	ASPRMIN	Aperture compensation suppress, end suppress level	0h	3Ah
	1				
	2				
	3				
	4				
	5				
	6				
	7				
19	0	CSPRSTA	Chroma suppress start AGCCNT (Set value as CSPRSTA < CSPREND)	A0h	3Bh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
20	0	CSPREND	Chroma suppress end AGCCNT (Set value as CSPRSTA < CSPREND)	D0h	3Ch
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
21	0 1 2 3 4 5 6 7	CSPRMIN	Chroma suppress, end suppress level	8Ah	3Dh
22	0 1 2 3 4 5 6 7	Fix	“0h” fixed	0h	3Eh
23	0 1 2 3 4 5 6 7	Fix	“50h” fixed	50h	3Fh
24	0 1 2 3 4 5 6 7	Fix	“35h” fixed	35h	40h

Byte	Bit	Parameter name	Description	Initial value	E2P address
25	0 1 2 3 4 5 6 7	Fix	“45h” fixed	45h	41h
26	0 1 2 3 4 5 6 7	Fix	“3Bh” fixed	3Bh	42h
27	0 1 2 3 4 5 6 7	Fix	“48h” fixed	48h	43h
28	0 1 2 3 4 5 6 7	Fix	“39h” fixed	39h	44h

Byte	Bit	Parameter name	Description	Initial value	E2P address
29	0	Fix	“42h” fixed	42h	45h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
30	0	Fix	“3Dh” fixed	3Dh	46h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
31	0	Fix	“3Eh” fixed	3Eh	47h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
32	0	Fix	“41h” fixed	41h	48h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
33	0 1 2 3 4 5 6 7	Fix	“39h” fixed	39h	49h
34	0 1 2 3 4 5 6 7	Fix	“47h” fixed	47h	4Ah
35	0 1 2 3 4 5 6 7	Fix	“0h” fixed	0h	4Bh
36	0 1 2 3 4 5 6 7	Fix	“1h” fixed	1h	4Ch

Byte	Bit	Parameter name	Description	Initial value	E2P address
37	0 1 2 3 4 5 6 7	Fix	“FFh” fixed	FFh	4Dh
38	0 1 2 3 4 5 6 7	Fix	“EEh” fixed	EEh	4Eh
39	0 1 2 3 4 5 6 7	Fix	“11h” fixed	11h	4Fh
40	0 1 2 3 4 5 6 7	Fix	“1h” fixed	1h	50h

Byte	Bit	Parameter name	Description	Initial value	E2P address
41	0	Fix	“FFh” fixed	FFh	51h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
42	0	Fix	“EEh” fixed	EEh	52h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
43	0	Fix	“11h” fixed	11h	53h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
44	0	Fix	“F1h” fixed	F1h	54h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
45	0 1 2 3 4 5 6 7	Fix	“Eh” fixed	Eh	55h
46	0 1 2 3 4 5 6 7	Fix	“ECh” fixed	ECh	56h
47	0 1 2 3 4 5 6 7	Fix	“13h” fixed	13h	57h
48	0 1 2 3 4 5 6 7	Fix	“A0h” fixed	A0h	58h

Byte	Bit	Parameter name	Description	Initial value	E2P address
49	0 1 2 3 4 5 6 7	Fix	“D0h” fixed	D0h	59h
50	0 1 2 3 4 5 6 7	Fix	“Dh” fixed	Dh	5Ah
51	0 1 2 3 4 5 6 7	Fix	“1Ah” fixed	1Ah	5Bh
52	0	UYGAMSLV	Luminance signal gamma curve compression level switching for low luminance areas (Effective when GAMSEL = 1h) 0h : Strong, 1h : Weak	0h	5Ch
	1	Fix	“1h” fixed	1h	
	2 3 4	UYGAMSEL	Luminance signal variable gamma setting (Effective when GAMSEL = 1h)	0h	
	5 6 7	UYKNEESEL	Luminance signal variable knee setting (Effective when GAMSEL = 1h)	5h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
53	0	UCGAMMA	Chroma variable gamma parameter (Effective when GAMSEL = 1h) 0h to 7h : gamma small (line) to gamma large	0h	5Dh
	1				
	2				
	3	Fix	“0h” fixed	0h	
	4				
	5	UCKNEE	Chroma variable knee parameter (Effective when GAMSEL = 1h)	5h	
	6				
	7				
54	0	Fix	“0h” fixed	0h	5Eh
	1	UYGAMSON	Luminance signal gamma curve compression function for low luminance areas (Effective when GAMSEL = 1h) 0h : OFF, 1h : ON	0h	
	2	Fix	“0h” fixed	0h	
	3				
	4				
	5				
	6				
	7				
55	0	CRONPOINT	Low luminance chroma OFF function Chroma OFF → ON transition point setting (Set value as CRONPOINT < CROFFPOINT.)	C0h	5Fh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
56	0	CROFFPOINT	Low luminance chroma OFF function Chroma ON → OFF transition point setting (Set value as CRONPOINT < CROFFPOINT.)	D0h	60h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Category 14 : AE2

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	AEME	AE/ME 0h : Auto Exposure 1h : Manual Exposure	0h	61h
	1	MIRIS	Mechanical IRIS 0h : OFF 1h : ON	0h	
	2	BLCOFF	BackLight compensation OFF 0h : ON 1h : OFF	0h	
	3	AEREF	AE Refarence user mode 0h : OFF 1h : ON	0h	
	4	AGCMAX	AGC MAX gain select 0h : AGCMAXL 1h : AGCMAXH	0h	
	5	Fix	“0h” fixed	0h	
	6	AESHUT	AE SHUT mode ON 0h : OFF 1h : ON	0h	
	7	AGCOFF	AGC OFF mode 0h : AGCON 1h : AGCMIN Fix	0h	
2	0	NORMFLC	Flickerless by electronic shutter and AGC gain modulation 0h : OFF, 1h : ON	1h	62h
	1	LLFLC	Flickerless by low-speed side shutter limiter 0h : OFF, 1h : ON	0h	
	2	FIXSHTFLC	Flickerless by fixed electronic shutter 0h : OFF, 1h : ON	0h	
	3	Fix	“0h” fixed	0h	
	4				
	5				
	6				
	7				
3	0	VIDEOAE	VIDEO AE mode 0h : OFF, 1h : ON	0h	63h
	1	Fix	“0h” fixed	0h	
	2	SHTSEL	Electronic shutter speed selector 0h to 7h : Slow to fast	0h	
	3				
	4				
	5	Fix	“0h” fixed	0h	
	6				
	7				
4	0	BLCSEL	Backlight compensation mode selection 0h : Weighted average mode, 1h : Compensation gain fixed mode	0h	64h
	1	FBLCGAINSEL	Backlight compensation gain range selection 0h : × 0.0 to × 4.0, 1h : × 1.0 to × 1024.0	0h	
	2	Fix	“0h” fixed	0h	
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	FBLCGAIN	Backlight compensation gain fixed mode gain adjustment	C0h	65h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
6	0	AEW0	AE Window0 weight	1h	66h
	1				
	2				
	3				
	4	AEW1	AE Window1 weight	1h	
	5				
	6				
	7				
7	0	AEW2	AE Window2 weight	3h	67h
	1				
	2				
	3				
	4	AEW3	AE Window3 weight	3h	
	5				
	6				
	7				
8	0	AEW4	AE Window4 weight	Fh	68h
	1				
	2				
	3				
	4	Fix	“0h” fixed	0h	
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	AESTAB	Dead band width when tracing into hysteresis loop	0h	69h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
10	0	AEHYST	Dead band width when tracing out of hysteresis loop	0h	6Ah
	1				
	2				
	3				
	4				
	5				
	6				
	7				
11	0	AEWAIT	Counter value beyond AEHYST allowable range	0h	6Bh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
12	0	AESPEED	AE speed	6h	6Ch
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0	AEUSR	AE USR setting level (Effective when AEREF = 1h)	0h	6Dh
	1				
	2				
	3				
	4	Fix	“0h” fixed	0h	
	5				
	6				
	7				
14	0	Fix	“0h” fixed	0h	6Eh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
15	0	AGCMAXL	AE AGC MAX Low (Effective when AGCMAX = 0h)	C0h	6Fh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
16	0	AGCMAXH	AE AGC MAX High (Effective when AGCMAX = 1h)	FFh	70h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
17	0	SHUTMAX	Upper limit of shutter speed (Maximum shutter speed)	FFh	71h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
18	0	Fix	“0h” fixed	0h	72h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
19	0	IRISVMAX	Maximum value of EVR1CNT	FFh	73h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
20	0	IRISVMIN	Minimum value of EVR1CNT	0h	74h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
21	0	VCAM12	EVR1CNT setting value (– 12dB)	0h	75h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
22	0	VCAM6	EVR1CNT setting value (– 6dB)	13h	76h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
23	0	VCA0	EVR1CNT setting value (0dB)	4Dh	77h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
24	0	Fix	“87h” fixed	87h	78h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
25	0 1 2 3 4 5 6 7	Fix	“E8h” fixed	E8h	79h
26	0 1 2 3 4 5 6 7	Fix	“0h” fixed	0h	7Ah
27	0 1 2 3 4 5 6 7	AEDEADBAND	Dead band width adjustment	10h	7Bh
28	0 1 2 3 4 5 6 7	Fix	“20h” fixed	20h	7Ch

Byte	Bit	Parameter name	Description	Initial value	E2P address
29	0	Fix	“1h” fixed	1h	7Dh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Category 15 : AWB2

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	AWBMODE	AWB mode selection 0h : ATW, 1h : User fixed value 1, 2h : PUSH, 3h : User fixed value 3, 4h : MWB, 5h : User fixed value 2, 6h : HOLD, 7h : User fixed value 4	0h	7Eh
	1				
	2				
	3	Fix	“0h” fixed	0h	
	4				
	5				
	6				
	7				
2	0	AWBSEPOF	Luminance specific integration 0h : ON, 1h : OFF	0h	7Fh
	1	AWBTRG	Push lock system selection 0h : Conventional, 1h : Trigger	0h	
	2	Fix	“1h” fixed	1h	
	3	Fix	“0h” fixed	0h	
	4				
	5				
	6				
	7				
3	0	ATWFRAMOF	ATW operation frame 0h : ON, 1h : All canceled	0h	80h
	1	ATWFRM1OF	ATW operation frame 1 0h : ON, 1h : Canceled	0h	
	2	ATWFRM2OF	ATW operation frame 2 0h : ON, 1h : Canceled	0h	
	3	ATWFRM3OF	ATW operation frame 3 0h : ON, 1h : Canceled	0h	
	4	ATWLARGFRM	ATW operation frame expansion 0h : Normal, 1h : Enlarged	0h	
	5	Fix	“0h” fixed	0h	
	6				
	7				
4	0	GGAIN	G gain setting value (WBG initial value) “26h” is recommended.	26h	81h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0 1 2 3 4 5 6 7	AWBSPED	ATW speed adjustment 0h to FFh : Fast to slow	2h	82h
6	0 1 2 3 4 5 6 7	WBDLY	ATW response speed 0h to FFh : Fast to slow	10h	83h
7	0 1 2 3 4 5 6 7	ATWSTEP	Convergence step width adjustment for ATW 0h to FFh : Step width wide to step width narrow	8h	84h
8	0 1 2 3 4 5 6 7	Fix	“2h” fixed	2h	85h

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	Fix	“2h” fixed	2h	86h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
10	0	Fix	“2h” fixed	2h	87h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
11	0	Fix	“2h” fixed	2h	88h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
12	0	ATWRSFT	ATW convergence point, shift amount of R direction	0h	89h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0	ATWBSFT	ATW convergence point, shift amount of B direction	0h	8Ah
	1				
	2				
	3				
	4				
	5				
	6				
	7				
14	0	WBDBAND	Judgment frame for completion of convergence operation	10h	8Bh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
15	0	DBANDR	Judgment frame for start of re-convergence, R direction	12h	8Ch
	1				
	2				
	3				
	4				
	5				
	6				
	7				
16	0	DBANDB	Judgment frame for start of re-convergence, B direction	12h	8Dh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
17	0	DBANDM	Judgment frame for start of re-convergence, Mg direction	12h	8Eh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
18	0	DBANDG	Judgment frame for start of re-convergence, G direction	12h	8Fh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
19	0	FRAMRMIN	ATW operation frame 2, R/G	2Bh	90h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
20	0	FRAMBMIN	ATW operation frame 2, B/G	2Bh	91h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
21	0	FRAMRMAX	ATW operation frame 3, R/G	10h	92h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
22	0	FRAMMG	ATW operation frame 3, Mg direction	2Bh	93h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
23	0	LARGFRMR0	For large frame, R direction expansion of low color temperature side	10h	94h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
24	0	LARGFRMB1	For large frame, B direction expansion of high color temperature side	10h	95h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
25	0	FRAMFL	ATW operation frame 1, fluorescent light frame	20h	96h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
26	0	AWBRBWE	ATW operation frame 1, R and B directions frame expansion (Effective when ATWFRM3OF = 1h)	0h	97h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
27	0	AWBMGWE	ATW operation frame 1, Mg and G directions frame expansion (Effective when ATWFRM3OF = 1h)	0h	98h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
28	0	UWBYREFL	Integration range (lower luminance limit)	4h	99h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
29	0	INTSLICE	Luminance specific integration, integration range slice level	80h	9Ah
	1				
	2				
	3				
	4				
	5				
	6				
	7				
30	0	UWBYREFH	Integration range (upper luminance limit)	D0h	9Bh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
31	0	HLCUT	Luminance specific integration, high luminance block area setting	80h	9Ch
	1				
	2				
	3				
	4				
	5				
	6				
	7				
32	0	ALLSTEP	Adjusts the push convergence speed 0h to FFh : Fast to slow	2h	9Dh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
33	0 1 2 3 4 5 6 7	PLRGAIN	Push lock/MWB R gain	3Eh	9Eh
34	0 1 2 3 4 5 6 7	PLBGAIN	Push lock/MWB B gain	38h	9Fh
35	0 1 2 3 4 5 6 7	WBUSRR1	User R gain 1 (WBR ← WBUSRR1 when AWBMODE = 1h)	76h	A0h
36	0 1 2 3 4 5 6 7	WBUSRB1	User B gain 1 (WBB ← WBUSRB1 when AWBMODE = 1h)	34h	A1h

Byte	Bit	Parameter name	Description	Initial value	E2P address
37	0 1 2 3 4 5 6 7	WBUSRR2	User R gain 2 (WBR ← WBUSRR2 when AWBMODE = 5h)	53h	A2h
38	0 1 2 3 4 5 6 7	WBUSRB2	User B gain 2 (WBB ← WBUSRB2 when AWBMODE = 5h)	44h	A3h
39	0 1 2 3 4 5 6 7	WBUSRR3	User R gain 3 (WBR ← WBUSRR3 when AWBMODE = 3h)	65h	A4h
40	0 1 2 3 4 5 6 7	WBUSRB3	User B gain 3 (WBB ← WBUSRB3 when AWBMODE = 3h)	39h	A5h

Byte	Bit	Parameter name	Description	Initial value	E2P address
41	0	WBUSRR4	User R gain 4 (WBR ← WBUSRR4 when AWBMODE = 7h)	8Fh	A6h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
42	0	WBUSRB4	User B gain 4 (WBB ← WBUSRB4 when AWBMODE = 7h)	2Ah	A7h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
43	0	ADJWBGAIN	WB gain fine tuning 0h : OFF, 1h : ON (Available during HOLD Mode)	0h	A8h
	1	ADJRBSEL	WB gain incremental adjustment 0h : R gain adjustment, 1h : B gain adjustment	0h	
	2	Fix	“0h” fixed	0h	
	3				
	4				
	5				
	6				
	7				
44	0	CRFRAMOFF	AWB operation frame for anti-color rolling 0h : ON, 1h : All canceled	0h	A9h
	1	CRFRM1OFF	AWB operation frame for anti-color rolling 1 0h : ON, 1h : Canceled	0h	
	2	CRFRM2OFF	AWB operation frame for anti-color rolling 2 0h : ON, 1h : Canceled	0h	
	3	CRFRM3OFF	AWB operation frame for anti-color rolling 3 0h : ON, 1h : Canceled	1h	
	4	Fix	“0h” fixed	0h	
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
45	0 1 2 3 4 5 6 7	CRRGMAXL	Anti-color rolling AWB operation frame, R/G maximum value (LSB)	0h	AAh
46	0 1 2 3 4 5 6 7	CRRGMAXM	Anti-color rolling AWB operation frame, R/G maximum value (MSB)	15h	ABh
47	0 1 2 3 4 5 6 7	CRRGMINL	Anti-color rolling AWB operation frame, R/G minimum value (LSB)	0h	ACh
48	0 1 2 3 4 5 6 7	CRRGMINM	Anti-color rolling AWB operation frame, R/G minimum value (MSB)	7h	ADh

Byte	Bit	Parameter name	Description	Initial value	E2P address
49	0 1 2 3 4 5 6 7	CRBGMAXL	Anti-color rolling AWB operation frame, B/G maximum value (LSB)	0h	AEh
50	0 1 2 3 4 5 6 7	CRBGMAXM	Anti-color rolling AWB operation frame, B/G maximum value (MSB)	1Eh	AFh
51	0 1 2 3 4 5 6 7	CRBGMINL	Anti-color rolling AWB operation frame, B/G minimum value (LSB)	0h	B0h
52	0 1 2 3 4 5 6 7	CRBGMINM	Anti-color rolling AWB operation frame, B/G minimum value (MSB)	3h	B1h

Byte	Bit	Parameter name	Description	Initial value	E2P address
53	0 1 2 3 4 5 6 7	CRRSFT	Anti-color rolling AWB Convergence point, shift amount of R direction	0h	B2h
54	0 1 2 3 4 5 6 7	CRBSFT	Anti-color rolling AWB Convergence point, shift amount of B direction	0h	B3h
55	0 1 2 3 4 5 6 7	CRDBANDR	Anti-color rolling AWB Dead band width of R direction for determination of convergence start	10h	B4h
56	0 1 2 3 4 5 6 7	CRDBANDB	Anti-color rolling AWB Dead band width of B direction for determination of convergence start	10h	B5h

Byte	Bit	Parameter name	Description	Initial value	E2P address
57	0 1 2 3 4 5 6 7	CRDBANDM	Anti-color rolling AWB Dead band width of Mg direction for determination of convergence start	10h	B6h
58	0 1 2 3 4 5 6 7	CRDBANDG	Anti-color rolling AWB Dead band width of G direction for determination of convergence start	10h	B7h
59	0 1 2 3 4 5 6 7	CRLESSSTEP	Anti-color rolling AWB Convergence speed adjustment parameter 0h to FFh : Fast to slow	1h	B8h
60	0 1 2 3 4 5 6 7	CRLESSDLY	Anti-color rolling AWB Response speed adjustment parameter 0h to FFh : Fast to slow	0h	B9h

Byte	Bit	Parameter name	Description	Initial value	E2P address
61	0	Fix	“8h” fixed	8h	BAh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
62	0	MASKCNT	Timing setting when ATW starts up	7h	BBh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Category 16 : OPDWND2

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	Fix	“0h” fixed	0h	BCh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
2	0	Fix	“8h” fixed	8h	BDh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
3	0	Fix	“0h” fixed	0h	BEh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
4	0	Fix	“8Ch” fixed	8Ch	BFh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	OPDW4HST	Window4 horizontal start position (Grid step) (Normal)	5h	C0h
	1				
	2				
	3				
	4	OPDW4VST	Window4 vertical start position (Grid step) (Normal)	5h	
	5				
	6				
	7				
6	0	OPDW4HSTM	Window4 horizontal start position (Grid step) (Mirror)	5h	C1h
	1				
	2				
	3				
	4	OPDW4VSTM	Window4 vertical start position (Grid step) (Mirror)	5h	
	5				
	6				
	7				
7	0	OPDW4HW	Window4 horizontal width setting (Grid step) (Normal/Mirror)	5h	C2h
	1				
	2				
	3				
	4	OPDW4VW	Window4 vertical width setting (Grid step) (Normal/Mirror)	5h	
	5				
	6				
	7				
8	0	OPDWMK	Window display 0h : OFF, 1h : ON	0h	C3h
	1	OPDDISP	Window selection 0h : NONE, 1h : Window0, 2h : Window1, 3h : Window2, 4h : Window3, 5h : Window4, 6h : None, 7h : All windows	5h	
	2				
	3				
	4	Fix	“0h” fixed	0h	
	5	Fix	“0h” fixed	0h	
	6				
	7	WINDOUT	Window pulse (Port 4 output) 0h : OFF, 1h : ON	0h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	Fix	“FFh” fixed	FFh	C4h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
10	0	Fix	“3h” fixed	3h	C5h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Category 17 : EXTSYNC2

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	Fix	“0h” fixed	0h	C6h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
2	0	Fix	“0h” fixed	0h	C7h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
3	0	CTRLSFTVL	Shifter-related parameters (LSB)	0h	C8h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
4	0	CTRLSFTVM	Shifter-related parameters (MSB)	0h	C9h
	1				
	2	Fix	“0h” fixed	0h	
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	Fix	“0h” fixed	0h	CAh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
6	0	Fix	“0h” fixed	0h	CBh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
7	0	Fix	“0h” fixed	0h	CCh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
8	0	Fix	“0h” fixed	0h	CDh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	Fix	“0h” fixed	0h	CEh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
10	0	Fix	“0h” fixed	0h	CFh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
11	0	Fix	“0h” fixed	0h	D0h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
12	0	Fix	“0h” fixed	0h	D1h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0	Fix	“0h” fixed	0h	D2h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
14	0	Fix	“0h” fixed	0h	D3h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
15	0	PRSTSFTVL	Pre-set value for shifter operation (LSB)	0h	D4h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
16	0	PRSTSFTVM	Pre-set value for shifter operation (MSB)	0h	D5h
	1				
	2	Fix	“0h” fixed	0h	
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
17	0	SGMODE	External sync mode setting 0h : INT, 1h : LL	0h	D6h
	1	Fix	“0h” fixed	0h	
	2				
	3				
	4				
	5	ATMODEON	External sync auto mode 0h : OFF, 1h : ON	0h	
	6	Fix	“0h” fixed	0h	
	7				
18	0	SFTUP	Key operation, increment	0h	D7h
	1	SFTDWN	Key operation, decrement	0h	
	2	Fix	“0h” fixed	0h	
	3				
	4				
	5				
	6				
	7				
19	0	Fix	“1Eh” fixed	1Eh	D8h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
20	0	Fix	“2h” fixed	2h	D9h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
21	0	Fix	“Ah” fixed	Ah	DAh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
22	0	SFTSTEP	Variation width setting for shift value 1h to 1Bh (1Ch to 1Fh are setting prohibited.)	1h	DBh
	1				
	2				
	3				
	4				
	5	Fix	“0h” fixed	0h	
	6				
	7				
23	0	Fix	“3h” fixed	3h	DCh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Category 18 : FIX

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	Fix	“0h” fixed	0h	DDh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
2	0	Fix	“0h” fixed	0h	DEh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
3	0	Fix	“0h” fixed	0h	DFh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
4	0	Fix	“0h” fixed	0h	E0h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	Fix	“0h” fixed	0h	E1h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
6	0	Fix	“50h” fixed	50h	E2h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
7	0	Fix	“50h” fixed	50h	E3h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
8	0	Fix	“FFh” fixed	FFh	E4h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	Fix	“E0h” fixed	E0h	E5h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
10	0	Fix	“C0h” fixed	C0h	E6h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
11	0	Fix	“A0h” fixed	A0h	E7h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
12	0	Fix	“80h” fixed	80h	E8h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0	Fix	“60h” fixed	60h	E9h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
14	0	Fix	“38h” fixed	38h	EAh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
15	0	Fix	“4Bh” fixed	4Bh	EBh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
16	0	Fix	“80h” fixed	80h	ECh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Category 19 : PREADJ

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	AGCMIN	AGC minimum value	28h	EDh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
2	0	PRER0	R gain in low color temperature	39h	EEh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
3	0	AWBPRER	R gain in 3200K	63h	EFh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
4	0	PRER1	R gain in high color temperature	8Ch	F0h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	PREB0	B gain in low color temperature	A7h	F1h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
6	0	AWBPREB	B gain in 3200K	48h	F2h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
7	0	PREB1	B gain in high color temperature	2Bh	F3h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
8	0	ATWSTARTR	R gain of ATW starting	63h	F4h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	ATWSTARTB	B gain of ATW starting	48h	F5h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
10	0	MWBPRESETR	Preset R gain for MWB	63h	F6h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
11	0	MWBPRESETB	Preset B gain for MWB	48h	F7h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
12	0	PRERDIVG1L	R and G Low in high color temperature	17h	F8h
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0 1 2 3 4 5 6 7	PRERDIVG1H	R and G High in high color temperature	Bh	F9h
14	0 1 2 3 4 5 6 7	PREBDIVG1L	B and G Low in high color temperature	48	FAh
15	0 1 2 3 4 5 6 7	PREBDIVG1H	B and G High in high color temperature	1B	FBh
16	0 1 2 3 4 5 6 7	PRERDIVG0L	R and G Low in low color temperature	EA	FCh

Byte	Bit	Parameter name	Description	Initial value	E2P address
17	0	PRERDIVG0H	R and G High in low color temperature	1B	FDh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
18	0	PREBDIVG0L	B and G Low in low color temperature	F	FEh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
19	0	PREBDIVG0H	B and G High in low color temperature	7	FFh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Category 20 : PORT

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	P0ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	100h
	1				
	2				
	3				
	4	P0WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				
2	0	P0BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	1h	101h
	1				
	2				
	3				
	4				
	5				
	6				
	7	P0IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	
3	0	P0CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Fh	102h
	1				
	2				
	3				
	4				
	5	P0LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	0h	
	6				
	7				
4	0	P1ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	103h
	1				
	2				
	3				
	4	P1WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	P1BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	1h	104h
	1				
	2				
	3				
	4				
	5				
	6				
	7	P1IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	
6	0	P1CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Fh	105h
	1				
	2				
	3				
	4				
	5	P1LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	1h	
	6				
	7				
7	0	P2ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	106h
	1				
	2				
	3				
	4	P2WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				
8	0	P2BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	1h	107h
	1				
	2				
	3				
	4				
	5				
	6				
	7	P2IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0	P2CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Fh	108h
	1				
	2				
	3				
	4				
	5	P2LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	2h	
	6				
	7				
10	0	P3ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	109h
	1				
	2				
	3				
	4	P3WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				
11	0	P3BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	Bh	10Ah
	1				
	2				
	3				
	4				
	5				
	6				
	7	P3IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	
12	0	P3CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Ch	10Bh
	1				
	2				
	3				
	4				
	5	P3LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	0h	
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0	P4ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	10Ch
	1				
	2				
	3				
	4	P4WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				
14	0	P4BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	1h	10Dh
	1				
	2				
	3				
	4				
	5				
	6				
	7	P4IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	
15	0	P4CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Eh	10Eh
	1				
	2				
	3				
	4				
	5	P4LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	2h	
	6				
	7				
16	0	P5ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	10Fh
	1				
	2				
	3				
	4	P5WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
17	0	P5BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	1h	110h
	1				
	2				
	3				
	4				
	5				
	6				
	7	P5IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	
18	0	P5CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Eh	111h
	1				
	2				
	3				
	4				
	5	P5LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	3h	
	6				
	7				
19	0	P6ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	112h
	1				
	2				
	3				
	4	P6WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				
20	0	P6BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	2h	113h
	1				
	2				
	3				
	4				
	5				
	6				
	7	P6IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
21	0	P6CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Eh	114h
	1				
	2				
	3				
	4				
	5	P6LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	0h	
	6				
	7				
22	0	P7ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	115h
	1				
	2				
	3				
	4	P7WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				
23	0	P7BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	1h	116h
	1				
	2				
	3				
	4				
	5				
	6				
	7	P7IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	
24	0	P7CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Eh	117h
	1				
	2				
	3				
	4				
	5	P7LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	4h	
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
25	0	P8ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	118h
	1				
	2				
	3				
	4	P8WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				
26	0	P8BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	1h	119h
	1				
	2				
	3				
	4				
	5				
	6				
	7	P8IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	
27	0	P8CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Eh	11Ah
	1				
	2				
	3				
	4				
	5	P8LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	0h	
	6				
	7				
28	0	P9ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	11Bh
	1				
	2				
	3				
	4	P9WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
29	0	P9BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	1h	11Ch
	1				
	2				
	3				
	4				
	5				
	6				
	7	P9IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	
30	0	P9CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Eh	11Dh
	1				
	2				
	3				
	4				
	5	P9LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	6h	
	6				
	7				
31	0	P10ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	11Eh
	1				
	2				
	3				
	4	P10WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				
32	0	P10BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	1h	11Fh
	1				
	2				
	3				
	4				
	5				
	6				
	7	P10IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
33	0	P10CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	1h	120h
	1				
	2				
	3				
	4				
	5	P10LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	4h	
	6				
	7				
34	0	P11ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	121h
	1				
	2				
	3				
	4	P11WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				
35	0	P11BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	7h	122h
	1				
	2				
	3				
	4				
	5				
	6				
	7	P11IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	
36	0	P11CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Ch	123h
	1				
	2				
	3				
	4				
	5	P11LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	0h	
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
37	0	P12ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	124h
	1				
	2				
	3				
	4	P12WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				
38	0	P12BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	1h	125h
	1				
	2				
	3				
	4				
	5				
	6				
	7	P12IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	
39	0	P12CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Ch	126h
	1				
	2				
	3				
	4				
	5	P12LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	0h	
	6				
	7				
40	0	P13ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	127h
	1				
	2				
	3				
	4	P13WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
41	0	P13BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	1h	128h
	1				
	2				
	3				
	4				
	5				
	6				
	7	P13IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	
42	0	P13CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Ch	129h
	1				
	2				
	3				
	4				
	5	P13LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	1h	
	6				
	7				
43	0	P14ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	12Ah
	1				
	2				
	3				
	4	P14WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				
44	0	P14BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	1h	12Bh
	1				
	2				
	3				
	4				
	5				
	6				
	7	P14IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	

Byte	Bit	Parameter name	Description	Initial value	E2P address
45	0	P14CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Ch	12Ch
	1				
	2				
	3				
	4				
	5	P14LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	2h	
	6				
	7				
46	0	P15ADJ	Input port setting : Coefficient setting, Output port setting : Not used	0h	12Dh
	1				
	2				
	3				
	4	P15WID	Bit width setting 0h to Fh : Bit width (1-bit width to 16-bit width)	0h	
	5				
	6				
	7				
47	0	P15BYTE	Byte number setting 0h : Not used, 1h to 40h : Byte number	1h	12Eh
	1				
	2				
	3				
	4				
	5				
	6				
	7	P15IOSEL	Port I/O selection 0h : Input port setting, 1h : Output port setting	0h	
48	0	P15CAT	Category number setting 0h : Port not used, 1h to 18h : Category number	Ch	12Fh
	1				
	2				
	3				
	4				
	5	P15LSB	Input port setting 0h to 7h : LSB setting of the data (Max. 16 bits) Output port setting 0h to 7h : Output bit setting	3h	
	6				
	7				

Category 21 : BLMDET2

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	Fix	“0h” fixed	0h	130h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
2	0	Fix	“1h” fixed	1h	131h
	1	Fix	“0h” fixed	0h	
	2	UDYNDETON	Dynamic blemish detection mode switching 0h : OFF, 1h : ON	1h	
	3	Fix	“0h” fixed	0h	
	4				
	5				
	6				
	7				

Category 22 : SOUT1

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	Fix	“0h” fixed	0h	—
	1	EXVDET	Ext-VD input detection flag 1h : Input detected	0h	
	2	Fix	“0h” fixed	0h	
	3				
	4				
	5				
	6				
	7				
2	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
3	0	Fix	“4h” fixed	4h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
4	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0 1 2 3 4 5 6 7	Fix	“0h” fixed	0h	—
6	0 1 2 3 4 5 6 7	Fix	“0h” fixed	0h	—
7	0 1 2 3 4 5 6 7	INTY0L	Luminance integration value of the window 0 (LSB)	0h	—
8	0 1 2 3 4 5 6 7	INTY0M	Luminance integration value of the window 0 (MSB)	0h	—

Byte	Bit	Parameter name	Description	Initial value	E2P address
9	0 1 2 3 4 5 6 7	INTY1L	Luminance integration value of the window 1 (LSB)	0h	—
10	0 1 2 3 4 5 6 7	INTY1M	Luminance integration value of the window 1 (MSB)	0h	—
11	0 1 2 3 4 5 6 7	INTY2L	Luminance integration value of the window 2 (LSB)	0h	—
12	0 1 2 3 4 5 6 7	INTY2M	Luminance integration value of the window 2 (MSB)	0h	—

Byte	Bit	Parameter name	Description	Initial value	E2P address
13	0 1 2 3 4 5 6 7	INTY3L	Luminance integration value of the window 3 (LSB)	0h	—
14	0 1 2 3 4 5 6 7	INTY3M	Luminance integration value of the window 3 (MSB)	0h	—
15	0 1 2 3 4 5 6 7	INTY4L	Luminance integration value of the window 4 (LSB)	0h	—
16	0 1 2 3 4 5 6 7	INTY4M	Luminance integration value of the window 4 (MSB)	0h	—

Byte	Bit	Parameter name	Description	Initial value	E2P address
17	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
18	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
19	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
20	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
21	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
22	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
23	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
24	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
25	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
26	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
27	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
28	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
29	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
30	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
31	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
32	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
33	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
34	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
35	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
36	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
37	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
38	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
39	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
40	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
41	0 1 2 3 4 5 6 7	Fix	“0h” fixed	0h	—
42	0 1 2 3 4 5 6 7	Fix	“0h” fixed	0h	—
43	0 1 2 3 4 5 6 7	INTRL	Red integration value (LSB)	0h	—
44	0 1 2 3 4 5 6 7	INTR	Red integration value (MID)	0h	—

Byte	Bit	Parameter name	Description	Initial value	E2P address
45	0 1 2 3 4 5 6 7	INTRM	Red integration value (MSB)	0h	—
46	0 1 2 3 4 5 6 7	INTGL	Green integration value (LSB)	0h	—
47	0 1 2 3 4 5 6 7	INTG	Green integration value (MID)	0h	—
48	0 1 2 3 4 5 6 7	INTGM	Green integration value (MSB)	0h	—

Byte	Bit	Parameter name	Description	Initial value	E2P address
49	0	INTBL	Blue integration value (LSB)	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
50	0	INTB	Blue integration value (MID)	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
51	0	INTBM	Blue integration value (MSB)	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
52	0	AWBCNTL	Integration value of pixels (LSB)	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Byte	Bit	Parameter name	Description	Initial value	E2P address
53	0 1 2 3 4 5 6 7	AWBCNTM	Integration value of pixels (MSB)	0h	—
54	0 1 2 3 4 5 6 7	Fix	“0h” fixed	0h	—
55	0 1 2 3 4 5 6 7	Fix	“0h” fixed	0h	—
56	0 1 2 3 4 5 6 7	Fix	“0h” fixed	0h	—

Byte	Bit	Parameter name	Description	Initial value	E2P address
57	0	Fix	“0h” fixed	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Category 23 : SOUT2

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0 1 2 3 4 5 6 7	AWBOUT1	AWB adjustment data White Balance gain output mode : WBR OPD evaluated value output mode : R and G (LSB)	0h	—
2	0 1 2 3 4 5 6 7	AWBOUT2	AWB adjustment data White Balance gain output mode : WBG OPD evaluated value output mode : R and G (MSB)	0h	—
3	0 1 2 3 4 5 6 7	AWBOUT3	AWB adjustment data White Balance gain output mode : WBB OPD evaluated value output mode : B and G (LSB)	0h	—
4	0 1 2 3 4 5 6 7	AWBOUT4	AWB adjustment data White Balance gain output mode : — OPD evaluated value output mode : B and G (MSB)	0h	—

Byte	Bit	Parameter name	Description	Initial value	E2P address
5	0	AESCLL	AE SCALE (LSB)	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				
6	0	AESCLM	AE SCALE (MSB)	0h	—
	1				
	2				
	3				
	4				
	5				
	6				
	7				

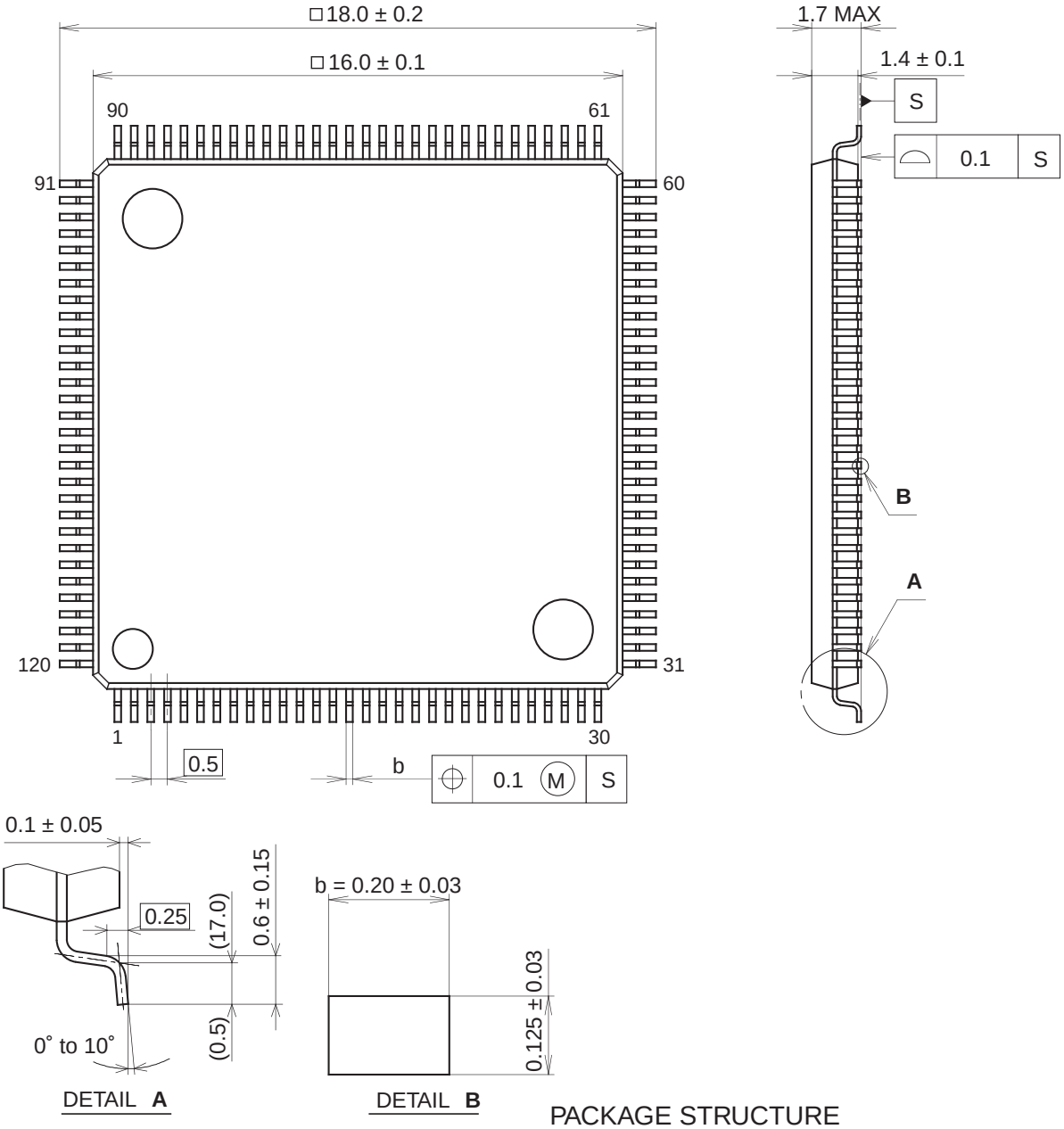
Category 24 : TEST

Byte	Bit	Parameter name	Description	Initial value	E2P address
1	0	Fix	“0h” fixed	0h	1E9h
	1				
	2				
	3				
	4				
	5				
	6				
	7				
2	0	Fix	“0h” fixed	0h	1EAh
	1				
	2				
	3				
	4				
	5				
	6				
	7				
3	0	Fix	“0h” fixed	0h	1EBh
	1				
	2				
	3				
	4				
	5				
	6				
	7				

Package Outline

(Unit : mm)

120PIN LQFP (PLASTIC)



SONY CODE	LQFP-120P-L01
EIAJ CODE	LQFP120-P-1616
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.8g