SONY

Distribution Restraint	Internal	Outside
	Limited	Limited

Signal Processing LSI for Single CCD Color Camera

CXD4150AR

Description

The CXD4150AR is a signal processing LSI for Ye, Cy, Mg and G single CCD color cameras.
In addition to basic camera signal processing functions, it includes an AE/AWB detection circuit, a sync signal generation circuit and an external sync circuit, etc.
This chip realizes basic camera control functions such as AE/AWB with an internal RISK-CPU and an external microcomputer.

Applications: Industrial CCD cameras (Surveillance/FA/image input cameras)
Multimedia CCD cameras (Teleconferencing/personal computer cameras)

Features

- ◆ Generates sync signals for the single CCD camera
  Luminance signal processing
  Chroma signal processing
- ◆ Supports NTSC/PAL systems
- ◆ Supports 760H system CCD image sensor
- ◆ Analog output pin
  - 10-bit D/A converter output
- ◆ YCrCb digital output pin
  - Conforms to ITU-R BT.656 data format
- ◆ Supports external sync functions
  - Built-in phase comparator
- ◆ Built-in AE/AWB/AF detector
- ◆ Block control functions with an internal RISK-CPU
  - AE/AWB/YC/CLAMP/SG/defect detection and compensation/EZOOM/ITU-R BT.656 interface control function
- ◆ Peripheral IC control function
  - TG/EVR/AFE/EEPROM communication control/CXD3151R/CXD3160R
- ◆ Serial communication function (2-mode selection)
  - Microcomputer communication/start-stop synchronous system communication (RS-232C)
- ◆ Electronic zoom function (Mirror inversion)
- ◆ Motion detection function
- ◆ Supports CXD4111

E07302A74

Absolute Maximum Ratings

◆ Supply voltage	V_{DD}	V_{SS} – 0.5 to +2.5	V
	V_{DE}	V_{SS} – 0.5 to +4.5	V
	AVD	AVS – 0.5 to +4.5	V
◆ Input voltage	V_I	V_{SS} – 0.3 to V_{DE} + 0.3	V
◆ Output voltage	V_O	V_{SS} – 0.3 to V_{DE} + 0.3	V
◆ Operating temperature	Topr	–20 to +75	℃
◆ Storage temperature	Tstg	–55 to +150	℃

Recommended Operating Conditions

◆ Supply voltage	V_{DD}	1.35 to 1.65	V
	V_{DE}	3.0 to 3.6	V
	AVD	3.0 to 3.6	V
◆ Operating temperature	Topr	–20 to +75	℃

Applicable CCD Image Sensors*1

◆ 760H color CCDs (Type 1/3, 1/4, NTSC/PAL)

*1 When using 1/3 types, an external buffer circuit (3.3V → 5.0V voltage step-up) is required.

Supported Related LSI

TG : CXD2493R/CXD2494R
AFE : CXD3301R
EEPROM : BR25L160-W (ROHM Co., Ltd.)
HN58X2516I (Renesas Technology Corp.)
AT25160A (Atmel Corporation)
WDR-DSP : CXD3151R
Memory : CXD3160R/CXD4111GG

Notes on Handling

Use Restrictions

- The Products are intended for incorporation into such general electronic equipment as general CCTV surveillance, image input cameras, FA cameras, teleconferencing cameras and personal computer cameras in accordance with the terms and conditions set forth in this specifications book and otherwise notified by Sony from time to time.
- You should not use the Products for critical applications, as car use products, which may pose a life- or injury-threatening risk or are highly likely to cause significant property damage in the event of failure of the Products. In addition, you should not use the Products in weapon or military equipment.
- Sony disclaims and does not assume any liability and damages arising out of misuse, improper use, modification, use of the Products for the above-mentioned critical applications, weapon and military equipment, or any deviation from the requirements set forth in this specifications book.

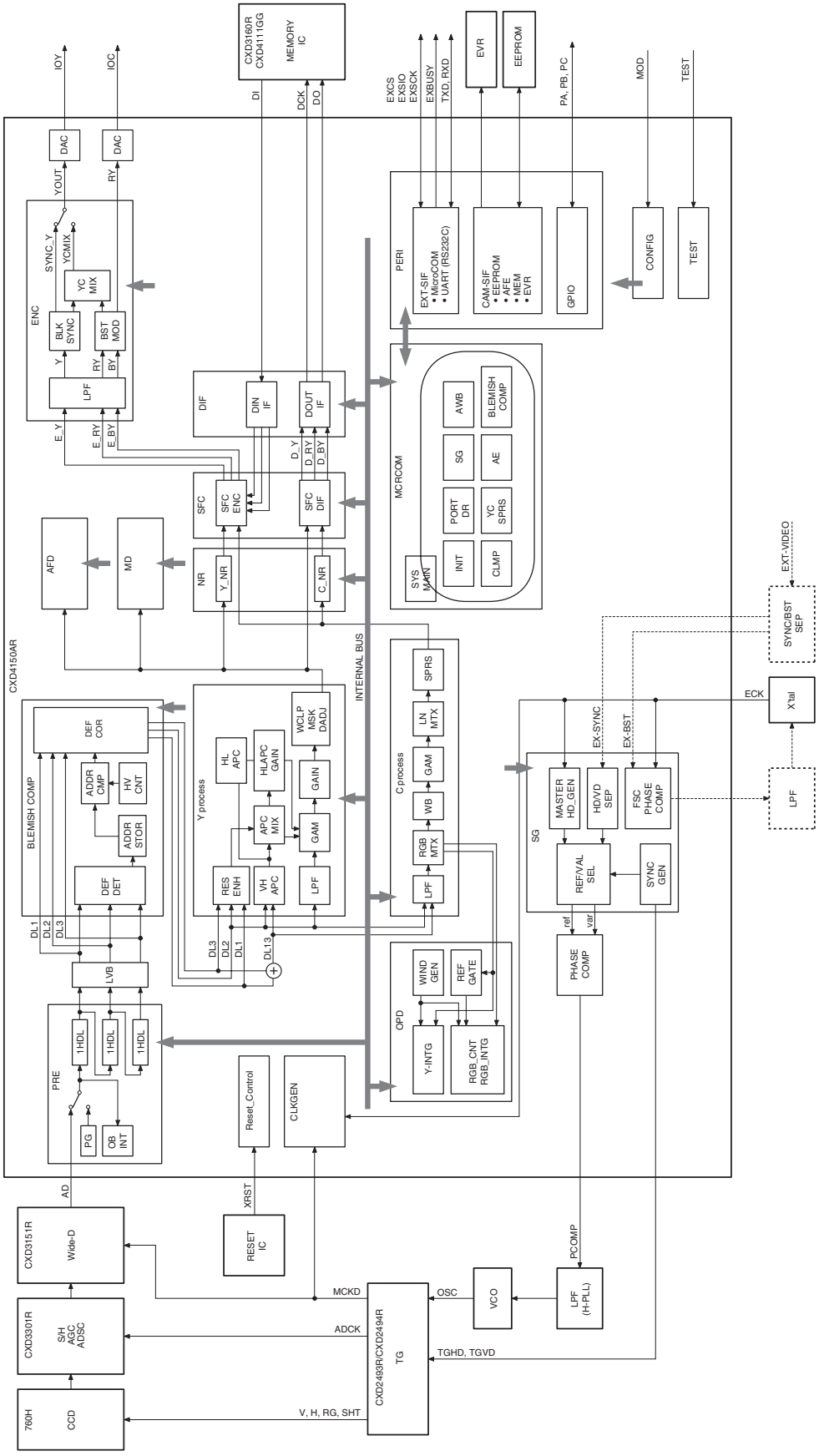
Design for Safety

- Sony is making continuous efforts to further improve the quality and reliability of the Products; however, failure of a certain percentage of the Products is inevitable. Therefore, you should take sufficient care to ensure the safe design of your products such as component redundancy, anti-conflagration features, and features to prevent misoperation in order to avoid accidents resulting in injury or death, fire or other social damage as a result of such failure.

Other Applicable Terms and Conditions

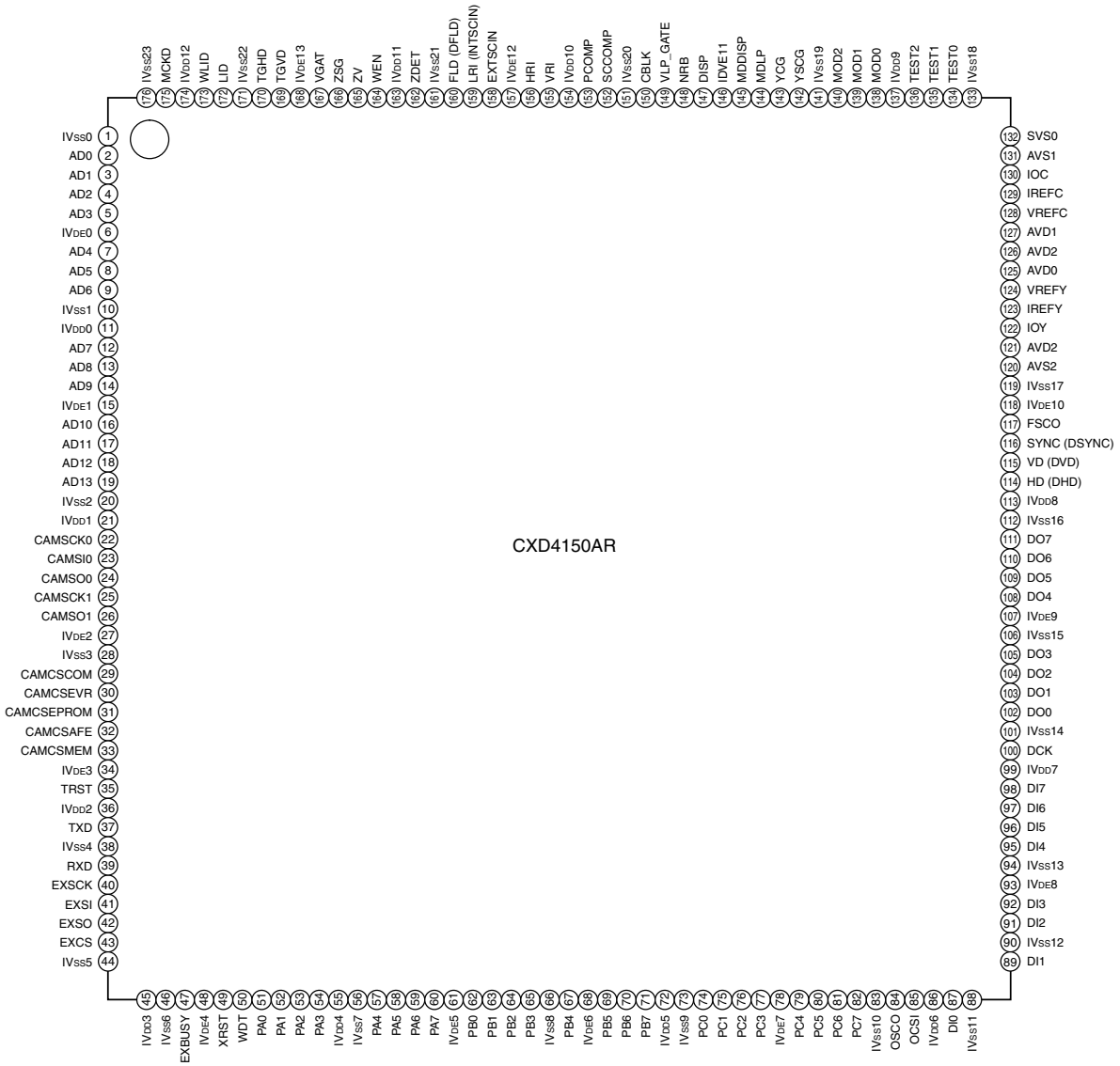
- The terms and conditions in the Sony additional specifications, which will be made available to you when you order the Products, shall also be applicable to your use of the Products as well as to this specifications book. You should review those terms and conditions when you consider purchasing and/or using the Products.

Block Diagram



Pin Configuration

(Top View)



Note) Symbols in parentheses are the signal names when the function is switched by the communication parameter settings.

Pin Description

Pin No.	Symbol	I/O	Description
1	$IV_{SS}0$ (DGND)	—	GND
2	AD0	I	External A/D signal input (LSB)
3	AD1	I	External A/D signal input
4	AD2	I	External A/D signal input
5	AD3	I	External A/D signal input
6	$IV_{DE}0$ (D3.3V)	—	I/O power supply
7	AD4	I	External A/D signal input
8	AD5	I	External A/D signal input
9	AD6	I	External A/D signal input
10	$IV_{SS}1$ (DGND)	—	GND
11	$IV_{DD}0$ (D1.5V)	—	Logic power supply
12	AD7	I	External A/D signal input
13	AD8	I	External A/D signal input
14	AD9	I	External A/D signal input
15	$IV_{DE}1$ (D3.3V)	—	I/O power supply
16	AD10	I	External A/D signal input
17	AD11	I	External A/D signal input
18	AD12	I	External A/D signal input
19	AD13	I	External A/D signal input (MSB)
20	$IV_{SS}2$ (DGND)	—	GND
21	$IV_{DD}1$ (D1.5V)	—	Logic power supply
22	CAMSCK0	O	Serial clock for peripheral ICs
23	CAMSI0	I	Serial data IN for peripheral ICs
24	CAMSO0	O	Serial data OUT for peripheral ICs
25	CAMSCK1	O	Serial clock for peripheral ICs
26	CAMSO1	O	Serial data OUT for peripheral ICs
27	$IV_{DE}2$ (D3.3V)	—	I/O power supply
28	$IV_{SS}3$ (DGND)	O	GND
29	CAMCSCOM	O	Chip select for peripheral ICs
30	CAMCSEVR	O	Chip select for peripheral ICs
31	CAMCSEPROM	O	Chip select for peripheral ICs
32	CAMCSAFE	O	Chip select for peripheral ICs
33	CAMCSMEM	O	Chip select for peripheral ICs
34	$IV_{DE}3$ (D3.3V)	—	I/O power supply
35	TRST	I	Test pin
36	$IV_{DD}2$ (D1.5V)	—	Logic power supply
37	TXD	I	UART receive data input
38	$IV_{SS}4$ (DGND)	—	GND

Pin No.	Symbol	I/O	Description
39	RXD	O	UART transmit data output
40	EXSCK	I	Serial clock for microcomputer communication
41	EXSI	I	Serial data input for microcomputer communication
42	EXSO	O	Serial data output for microcomputer communication
43	EXCS	I	Chip select for microcomputer communication
44	IVSS5 (DGND)	—	GND
45	IVDD3 (D1.5V)	—	Logic power supply
46	IVSS6 (DGND)	—	GND
47	EXBUSY	O	Busy signal for microcomputer communication
48	IVDE4 (D3.3V)	—	I/O power supply
49	XRST	I	Reset input
50	WDT	O	Watchdog timer output
51	PA0	I/O	Port A
52	PA1	I/O	Port A
53	PA2	I/O	Port A
54	PA3	I/O	Port A
55	IVDD4 (D1.5V)	—	Logic power supply
56	IVSS7 (DGND)	—	GND
57	PA4	I/O	Port A
58	PA5	I/O	Port A
59	PA6	I/O	Port A
60	PA7	I/O	Port A
61	IVDE5 (D3.3V)	—	I/O power supply
62	PB0	I/O	Port B
63	PB1	I/O	Port B
64	PB2	I/O	Port B
65	PB3	I/O	Port B
66	IVSS8 (DGND)	—	GND
67	PB4	I/O	Port B
68	IVDE6 (D3.3V)	—	I/O power supply
69	PB5	I/O	Port B
70	PB6	I/O	Port B
71	PB7	I/O	Port B
72	IVDD5 (D1.5V)	—	Logic power supply
73	IVSS9 (DGND)	—	GND
74	PC0	I/O	Port C/AFD output
75	PC1	I/O	Port C/AFD output
76	PC2	I/O	Port C/AFD output
77	PC3	I/O	Port C/AFD output
78	IVDE7 (D3.3V)	—	I/O power supply

Pin No.	Symbol	I/O	Description
79	PC4	I/O	Port C/AFD output
80	PC5	I/O	Port C/AFD output
81	PC6	I/O	Port C/AFD output
82	PC7	I/O	Port C/AFD output
83	IVSS10 (DGND)	—	GND
84	OSCO	O	SC oscillator output
85	OSCI	I	SC oscillator input
86	IVDD6 (D1.5V)	—	Logic power supply
87	DI0	I	Digital input
88	IVSS11 (DGND)	—	GND
89	DI1	I	Digital input
90	IVSS12 (DGND)	—	GND
91	DI2	I	Digital input
92	DI3	I	Digital input
93	IVDE8 (D3.3V)	—	I/O power supply
94	IVSS13 (DGND)	—	GND
95	DI4	I	Digital input
96	DI5	I	Digital input
97	DI6	I	Digital input
98	DI7	I	Digital input
99	IVDD7 (D1.5V)	—	Logic power supply
100	DCK	I/O	Digital interface clock
101	IVSS14 (DGND)	—	GND
102	DO0	O	Digital output
103	DO1	O	Digital output
104	DO2	O	Digital output
105	DO3	O	Digital output
106	IVSS15 (DGND)	—	GND
107	IVDE9 (D3.3V)	—	I/O power supply
108	DO4	O	Digital output
109	DO5	O	Digital output
110	DO6	O	Digital output
111	DO7	O	Digital output
112	IVSS16 (DGND)	—	GND
113	IVDD8 (D1.5V)	—	Logic power supply
114	HD (DHD)	O	Horizontal sync signal output
115	VD (DVD)	O	Vertical sync signal output
116	SYNC (DSYNC)	O	Composite sync signal output
117	FSCO	O	Subcarrier output
118	IVDE10 (D3.3V)	—	I/O power supply

Pin No.	Symbol	I/O	Description
119	IVSS17 (DGND)	—	GND
120	AVS2 (AGND)	—	Analog GND
121	AVS0 (AGND)	—	Analog GND
122	IOY	O	Luminance signal (current) output
123	IREFY	O	Reference current setting
124	VREFY	I	Reference voltage setting
125	AVD0 (A3.3V)	—	Analog power supply
126	AVD2 (A3.3V)	—	Analog power supply
127	AVD1 (A3.3V)	—	Analog power supply
128	VREFC	I	Reference voltage setting
129	IREFC	O	Reference current setting
130	IOC	O	Chroma signal (current) output
131	AVS1 (AGND)	—	Analog GND
132	SVS0	—	GND for guard band connection
133	IVSS18 (DGND)	—	GND
134	TEST0	I	Test mode selection
135	TEST1	I	Test mode selection
136	TEST2	I	Test mode selection
137	IVDD9 (D1.5V)	—	Logic power supply
138	MOD0	I	Operating mode selection
139	MOD1	I	Operating mode selection
140	MOD2	I	Operating mode selection
141	IVSS19 (DGND)	—	GND
142	YSCG	I	OSD display period signal input
143	YCG	I	OSD signal input (R/G/B signal)
144	MDLP	O	MDVLP output
145	MDDISP	O	MD alarm output
146	IVDE11 (D3.3V)	—	I/O power supply
147	DISP	O	OPD detection frame output
148	NRB	O	Color identification signal output
149	VLP_GATE	O	Internal signal output
150	CBLK	O	Internal signal output
151	IVSS20 (DGND)	—	GND
152	SCCOMP	O	Subcarrier phase comparison output
153	PCOMP	O	HPLL/VPLL phase comparison output
154	IVDD10 (D1.5V)	—	Logic power supply
155	VRI	I	External sync signal input (V reset signal input)
156	HRI	I	External sync signal input (H reset signal input)
157	IVDE12 (D3.3V)	—	I/O power supply
158	EXTSCIN	I	External sync signal input (External burst signal input)

Pin No.	Symbol	I/O	Description
159	LRI (INTSCIN)	I/O	External sync signal I/O (LALT output/LALT reset input/internal subcarrier input)
160	FLD (DFLD)	O	Field identification signal output
161	IVSS21 (DGND)	—	GND
162	ZDET	O	Blemish compensation pulse (for CXD3151R)
163	IVDD11 (D1.5V)	—	Logic power supply
164	WEN	I	Memory IC write enable
165	ZV	I	Line reference signal for blemish compensation
166	ZSG	I	Field reference signal for blemish compensation
167	VGAT	O	Vertical clock pulse elimination control signal for EZOOM
168	IVDE13 (D3.3V)	—	I/O power supply
169	TGVD	O	Vertical sync signal for timing generator
170	TGHD	O	Horizontal sync signal for timing generator
171	IVSS22 (DGND)	—	GND
172	LID	I	Line identification signal
173	WLID	I/O	Connect to GND (SS-3)/ Line identification signal for WD (SS-3WD)
174	IVDD12 (D1.5V)	—	Logic power supply
175	MCKD	I	Master clock input (base oscillation frequency)
176	IVSS23 (DGND)	—	GND

Electrical Characteristics

DC Characteristics

(within the recommended operating range)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DE}		3.0	3.3	3.6	V
	V_{DD}		1.35	1.5	1.65	V
	AVD		3.0	3.3	3.6	V
Input voltage 1	V_{IH}*1		2.0			V
	V_{IL}*1				0.8	V
Input rise/fall time	tr, tf		0		10	ns
Input voltage 2	V_{T+}*1		2.3			V
	V_{T-}*1				0.7	V
Hysteresis	$V_{T+} - V_{T-}$*1			0.5		V
Output voltage 1	V_{OH}	I_{OH} = 2.0mA	V_{DE} – 0.4			V
	V_{OL}	I_{OL} = 2.0mA			0.4	V
Output voltage 2	V_{OH}*2	I_{OH} = 4.0mA	V_{DE} – 0.4			V
	V_{OL}*2	I_{OL} = 4.0mA			0.4	V
Output voltage 3	V_{OH}*3	I_{OH} = 8.0mA	V_{DE} – 0.4			V
	V_{OL}*3	I_{OL} = 8.0mA			0.4	V
Input leakage current 1	I_I	V_{IN} = V_{SS} or V_{DE}	–10		10	μA
Input leakage current 2	I_{IH}*4	V_{IN} = V_{DE}	40	100	240	μA
Output leakage current	I_{OZ} (in Hi-Z)*5	V_{IN} = V_{SS} or V_{DE}	–10		10	μA
Logic threshold	LV_{TH}*6			0.5V_{DE}		V
Input voltage 3	V_{IH}*6		1.7			V
	V_{IL}*6				0.7	V
Feedback resistance	RFB*6	V_{IN} = V_{SS} or V_{DE}		1M		Ω
Output voltage	V_{OH}*6	V_{IN} = V_{SS} or V_{DE}	0.5V_{DE}			V
	V_{OL}*6	V_{IN} = V_{SS} or V_{DE}			0.5V_{DE}	V

*1 TXD, XRST, PA[0:7], PB[0:7], PC[0:7], LRI (INTSCIN)
*2 CAMCSCOM, RXD, EXSO, EXBUSY, WDT, PA[0:7], PB[0:7], PC[0:7], DO[0:7], HD (DHD), VD (DVD), SYNC (DSYNC), FSCO, FLD (DFLD), LRI (INTSCIN), SCCOMP, ZDET, VGAT, TGVD, TDHD, WLID, YSCG, YCG, MDLP, MDDISP, DISP, NRB, VLP_GATE, CBLK
*3 DCK
*4 AD[0:3], TRST
*5 EXSO, HD (DHD), VD (DVD), SYNC (DSYNC), FSCO, FLD (DFLD), SCCOMP
*6 OSCO, OSCI

Input/Output Capacitance

(V_{DE} = V_I = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}			7	pF
Output pin capacitance	C_{OUT}			7	pF
I/O pin capacitance	$C_{I/O}$			7	pF

AC Characteristics

(Load capacitance: 15pF to 25pF)

Correlation diagram of basic specifications

Input

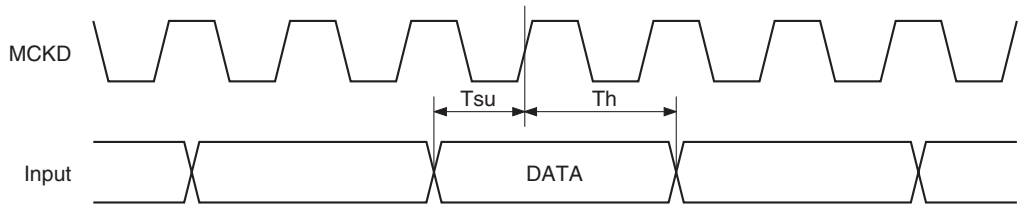


Fig. 1. Input AC Specifications

Output

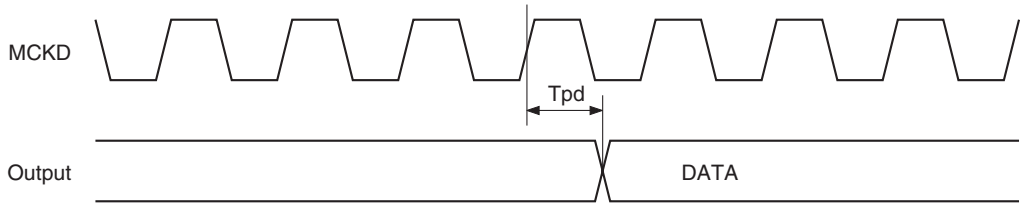


Fig. 2. Output AC Specifications

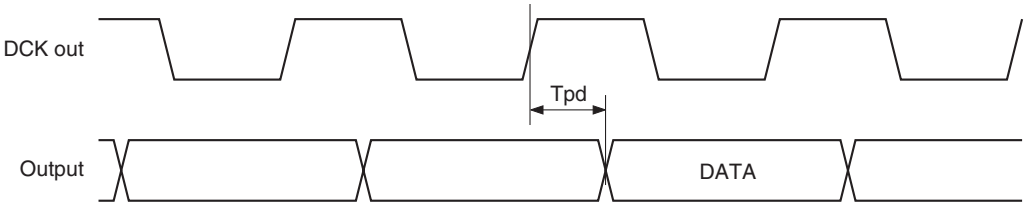


Fig. 3. Output AC Specifications

◆ **AD pin**

See Fig. 1 for the specifications correlation diagram.

(within the recommended operating range)

Pin name	Symbol	Item	Min.	Typ.	Max.	Unit
AD[13:0]	Tsu	Input setup time	9	—	—	ns
	Th	Input hold time	3	—	—	ns

◆ **TG pin**

See Fig. 1 for the specifications correlation diagram.

(within the recommended operating range)

Pin name	Symbol	Item	Min.	Typ.	Max.	Unit
LID, ZSG, ZV	Tsu	Input setup time	17	—	—	ns
	Th	Input hold time	0	—	—	ns

◆ **WLID**

Input when Wide-D (CXD3151) is not used, Output when Wide-D is used.
It is grounded at input, and it is connected to LID of the CXD3151 at output.

See Fig. 2 for the specifications correlation diagram.

(within the recommended operating range)

Pin name	Symbol	Item	Min.	Typ.	Max.	Unit
WLID	Tpd	Output delay time	9	—	28	ns

◆ **TGHD, TGVD**

See Fig. 2 for the specifications correlation diagram.

(within the recommended operating range)

Pin name	Symbol	Item	Min.	Typ.	Max.	Unit
TGHD	Tpd	Output delay time	4.5	—	18.5	ns
TGVD	Tpd	Output delay time	1	—	18	ns

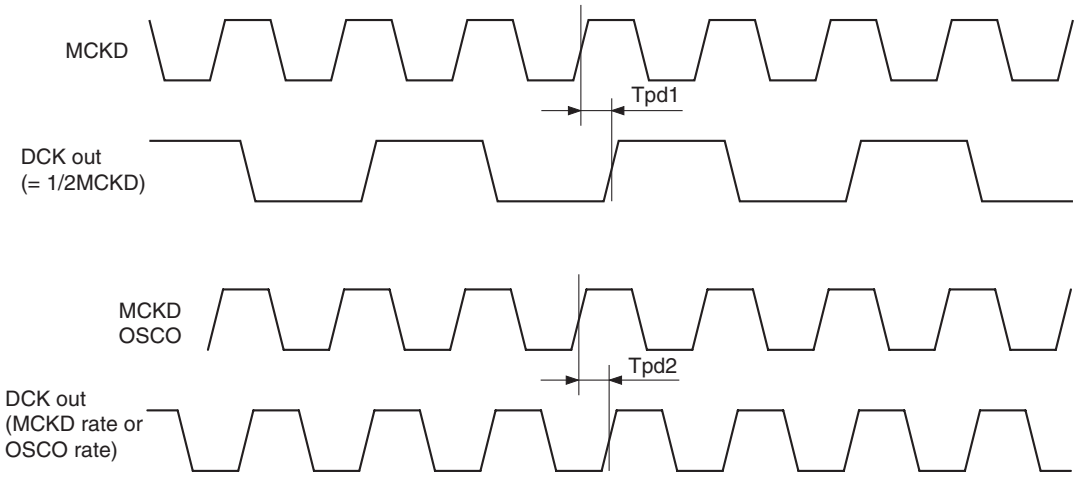
◆ **Defect detection**

See Fig. 2 for the specifications correlation diagram.

(within the recommended operating range)

Pin name	Symbol	Item	Min.	Typ.	Max.	Unit
ZDET	Tpd	Output delay time	8	—	31	ns

◆ **DCK**



(within the recommended operating range)

Pin name	Symbol	Item	Min.	Typ.	Max.	Unit
DCK	Tpd1	DCK output delay time at 1/2MCKD	3.78	—	12.23	ns
DCK	Tpd2	DCK output delay time at MCKD or OSCO rate	4.38	—	14.59	ns

◆ **AFD pin**

PC pin specifications

See Fig. 3 for the specifications correlation diagram.

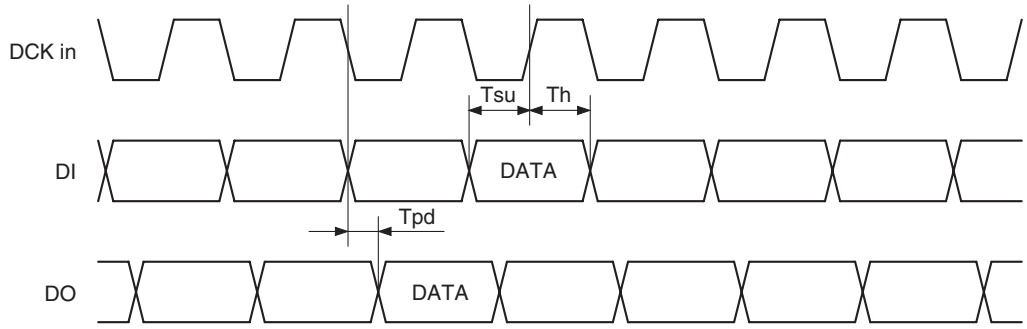
(within the recommended operating range)

Pin name	Symbol	Item	Min.	Typ.	Max.	Unit
PC[7:0]	Tpd	Output delay time	16	—	37	ns

◆ **DI, DO, FLD pins**

DI, DO, FLD pin specifications

The polarity of DI data receive and DO data output can be set to non-inverse or inverse using the parameter settings.

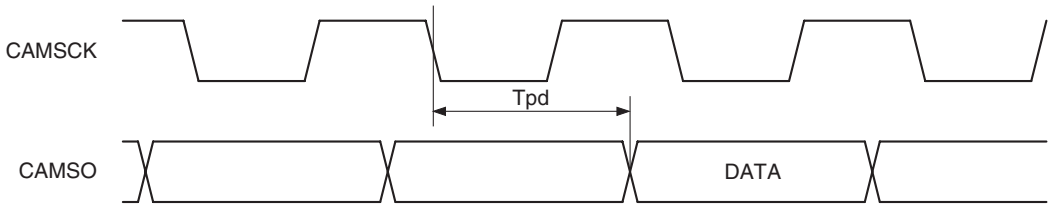


(within the recommended operating range)

Pin name	Symbol	Item	Min.	Typ.	Max.	Unit
DI[7:0]	Tsu	DI input setup time	22.4	—	—	ns
	Th	DI input hold time	2.2	—	—	ns
DO[7:0]	Tpd	DO output delay time	16.25	—	27.85	ns
FLD	Tpd	FLD output delay time	14.25	—	25.85	ns

◆ **Serial communication**

SC, SCK, SO and SI are signals for performing serial communication with the peripheral ICs.



(within the recommended operating range)

Pin name	Symbol	Item	Min.	Typ.	Max.	Unit
CAMSO0	Tpd	CAMSO0 output delay time	—	—	MCK cycle × 0.9	ns
CAMSO1	Tpd	CAMSO1 output delay time	—	—	MCK cycle × 0.9	ns
EXSO	Tpd	EXSO output delay time	—	—	Cycle × 0.9	ns

◆ **Sync signal output for memory interface**

If a sync signal for the memory interface is output when using a digital out system, it is output from the HD (DHD) and VD (DVD) pins. The AC specifications are shown below.

See Fig. 2 for the specifications correlation diagram.

(DCK cycle = 33ns, within the recommended operating range)

Pin name	Symbol	Item	Min.	Typ.	Max.	Unit
HD (DHD)	Tpd	DHD output delay time	3.3	—	29.5	ns
VD (DVD)	Tpd	DVD output delay time	3.3	—	29.5	ns

◆ **Sync signal output at DCK = 1/2MCKD**

The AC specifications during output of the sync signal at DCK = 1/2MCKD are shown below.

See Fig. 2 for the specifications correlation diagram.

(DCK cycle = 66ns, within the recommended operating range)

Pin name	Symbol	Item	Min.	Typ.	Max.	Unit
HD (DHD)	Tpd	DHD output delay time	21	—	47	ns
VD (DVD)	Tpd	DVD output delay time	21	—	47	ns

Startup Procedure

The CXD4150AR uses EEPROM communication to perform initialization at power-on startup.
Even when starting the CXD4150AR without connecting EEPROM, set port A (PA1, PA0) as shown below.
The port A value is read using the internal program initialization process, and it is identified as CCD type, TV system or TG type. If the CCD type, TV system or TG type is not set correctly, communication to the peripheral LSIs will not operate properly.

System	PA1 (WDCCD)		PA0 (NT/PAL)	
	External pin	Internal parameter	External pin	Internal parameter
SS-3 760H NTSC	High	0	High	0
SS-3 760H PAL	High	0	Low	1
SS-3WD 760H NTSC	Low	1	High	0
SS-3WD 760H PAL	Low	1	Low	1

Operation Mode Pin Setting Procedure

The operation mode is selected by the MOD0, MOD1 and MOD2 pins. These pins are used internally for selecting the clock. The MOD pin setting procedure varies depending on the conditions of the respective system. The clock system will not operate correctly if the proper settings are not made. Make the correct setting using the setting procedure described below.

MOD pin			param	Output mode	System conditions	Clock pins		
2	1	0	DCKAFD			MCKD	DCK	OSCI
Low	Low	Low	1	Analog output mode	The DO pin is not used. CXD3160 and CXD4111 are not connected.	Slave	MCKD output	SC input
			0				Hi-Z	
	High	Low	0	Analog & digital output mode	The DO pin is used. CXD3160 and CXD4111 are connected.	Slave	MCKD output	SC input
		High	0		FW limited mode			
High	Low	Low	0	Digital output mode	The DAC output signal is not used. The subcarrier lock is not used. No external sync.	Independent	MCKD output	No oscillator

Note) Mode settings not described here are outside the scope of the operation.

Serial Communication Bus Connection Procedure for Peripheral ICs

The peripheral IC serial bus has two channels. Connect the ICs as shown below.

Peripheral IC	CS pin	CH	Clock pin and data bus
CXD2493R CXD2494R	CAMCSCOM	Ch1	CAMSCK1/CAMSO1
CXD3301R	CAMCSAFE		
CXD3160R CXD4111GG	CAMCSMEM	Ch0	CAMSCK0/CAMSI0,CAMSO0
EEPROM	CAMCSEPROM		
EVR	CAMCSEVR		

Microcomputer Communication

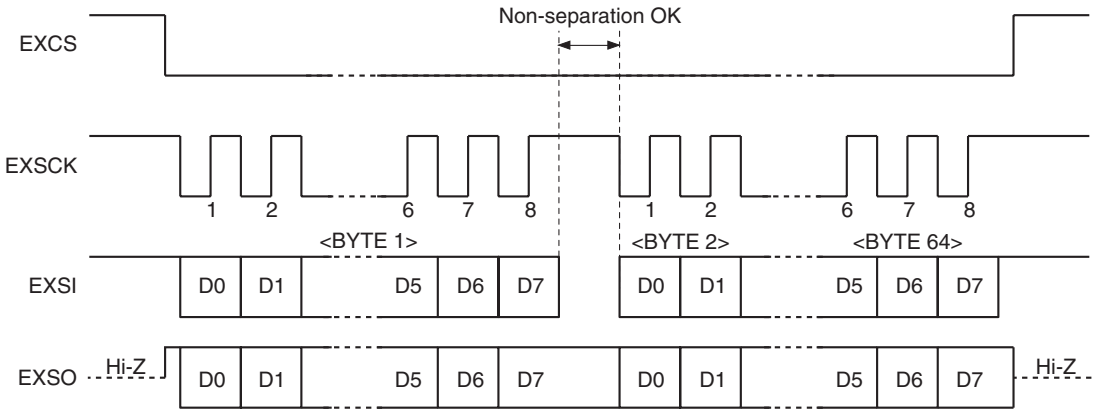
1. The serial data interface circuit of the CXD4150AR is intended for connection with a general-purpose, single-chip microcomputer.A

2. Bidirectional serial clock synchronous communication is performed between the CXD4150AR and microcomputer using full duplex synchronous communication.

3. The following five connections are made between the CXD4150AR and microcomputer.
   When viewed from the CXD4150AR:
   - EXSCK = Serial transmission clock
   - EXSI = CXD4150AR serial data input
   - EXSO = CXD4150AR serial data output
   - EXCS = CXD4150AR chip select
   - EXBUSY = Busy signal output during CXD4150AR communication prohibit period

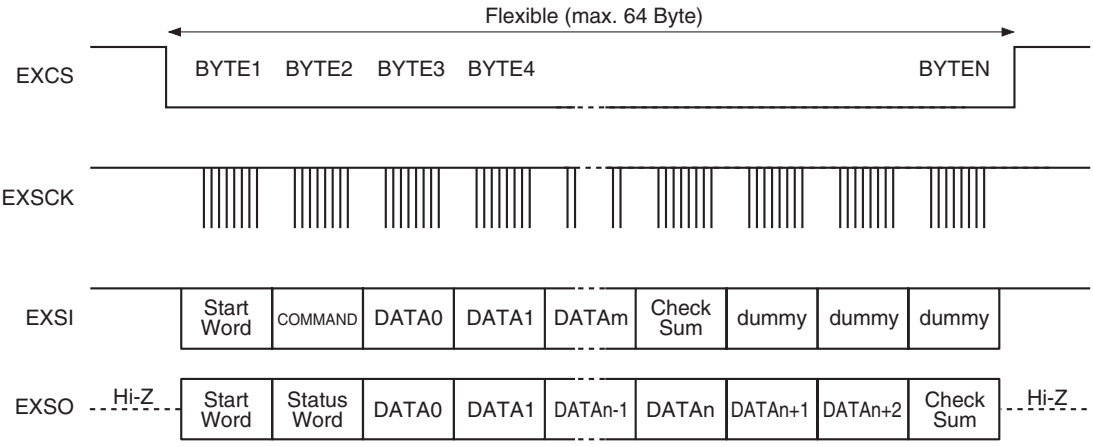
4. Communication timing
   (1) EXCS is set to Low to activate the CXD4150AR communication circuit.
   (2) The EXSI data is read at the EXSCK rising cycle.
   (3) EXSO is output at the EXSCK falling cycle.
   (4) The serial data is in 8-bit units, and the data size is 1 packet = variable length of 3 to 64 bytes. The serial output is output in synchronization with the serial input.
   (5) EXCS is set to High to end communication.

   Note) ◆ The communication data is LSB first.
   ◆ Set EXSCK to High before setting EXCS to Low (pull-up is also possible).



Communication Timing

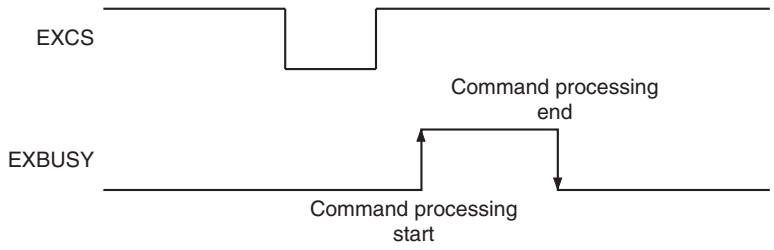
5. Communication format
One packet is a variable length of 3 to 64 bytes. It is assembled in accordance with the command specifications. As shown in the communication format example below, the result for the transmit command is received by the next packet. As a result, be sure to supply the necessary number of clock bytes for data reception. If the number of sending bytes is short, dummy data is added. When the communication for one packet is completed, raise EXCS to High.



Communication Format Example

6. Communication prohibit periods
The CXD4150AR has the serial communication prohibit periods below. During these periods, external microcomputer communication cannot be accepted.
   (1) DSP initialization period (35 fields after reset cancel) such as when the power is turned on
   (2) Period from TGVD falling to completion of communication with peripheral ICs
   (3) CPU memory read/write period (EXBUSY = High)
   (4) EEPROM READ/WRITE/CLEAR period (EXBUSY = High)

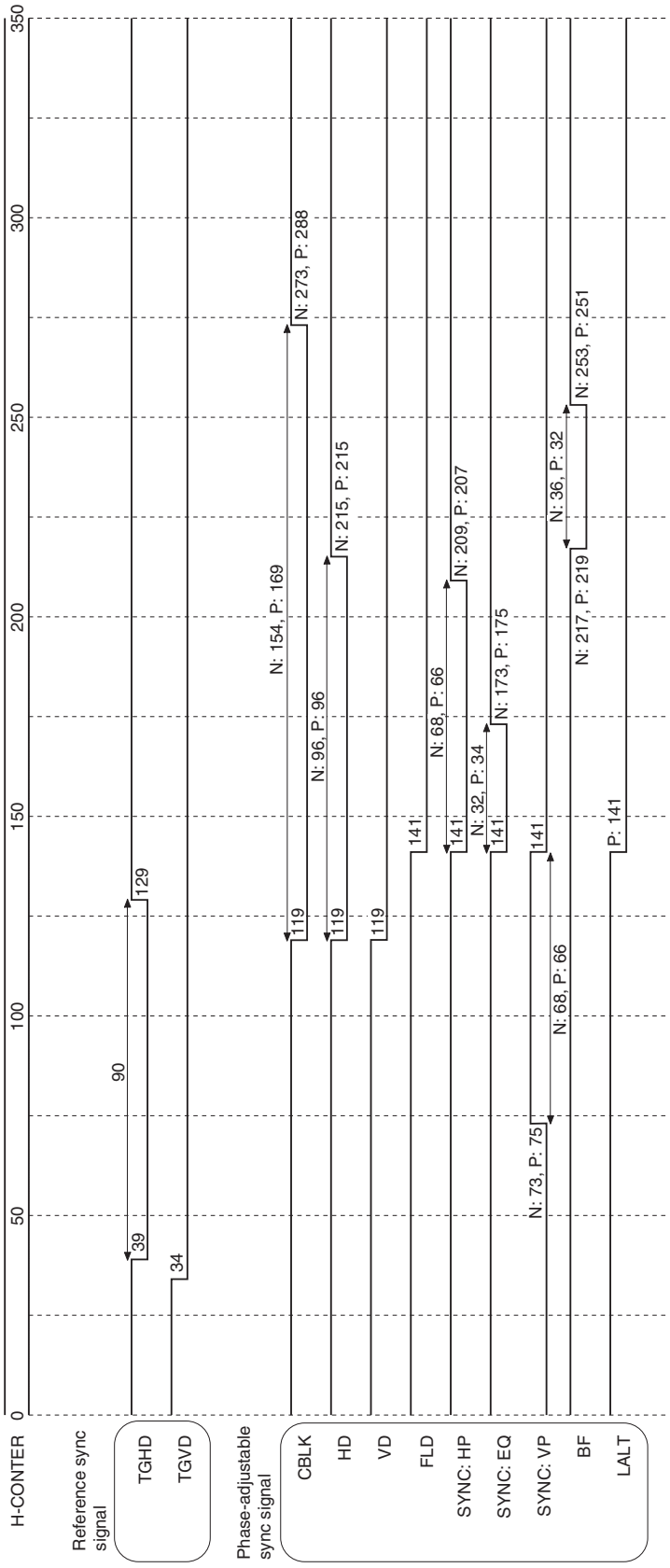
7. Serial data latch timing
Command processing (including the sending data setting) starts at EXBUSY rising after one packet is completed. The processing ends at EXBUSY falling. The processing time depends on the command content.



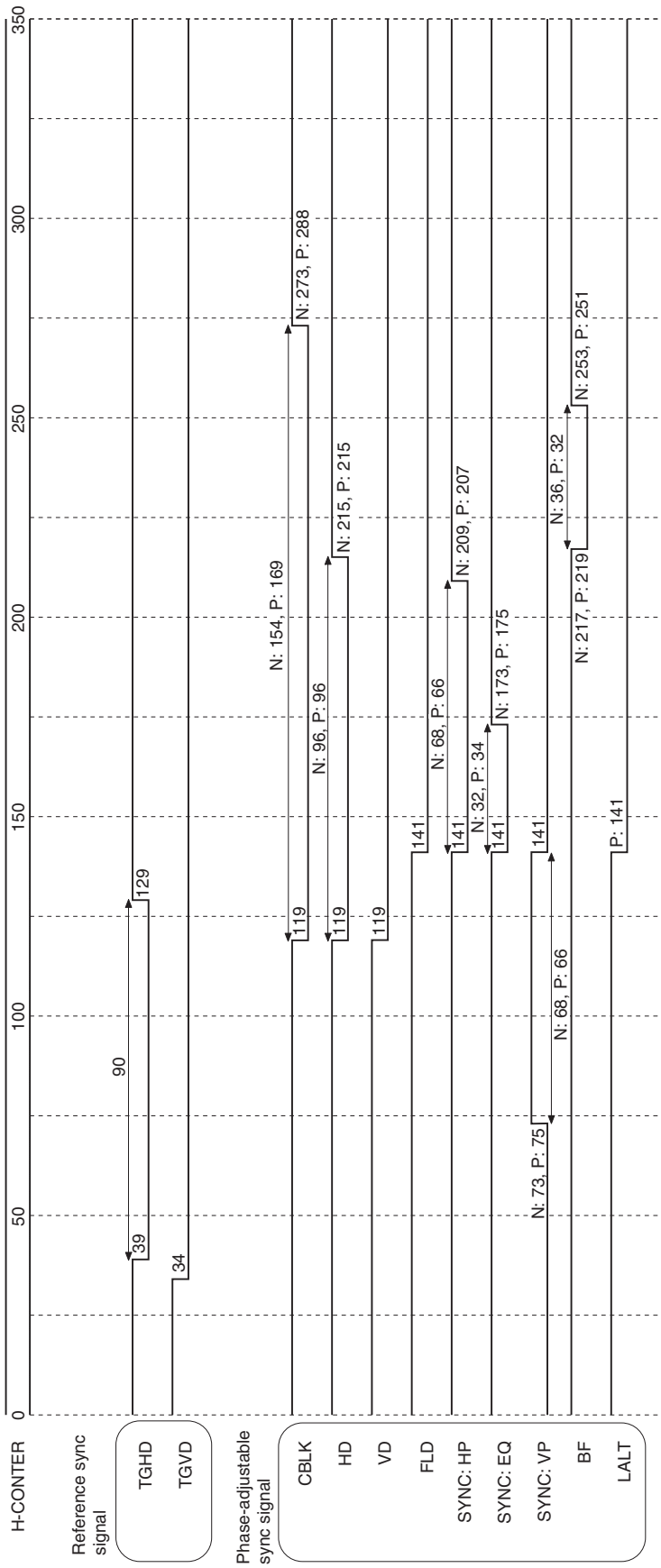
Latch Timing of External Microcomputer Communication Data

Timing Chart

1. 760H Horizontal Timing Chart MCK: NTSC 910fH (14.31818MHz/69.84ns)

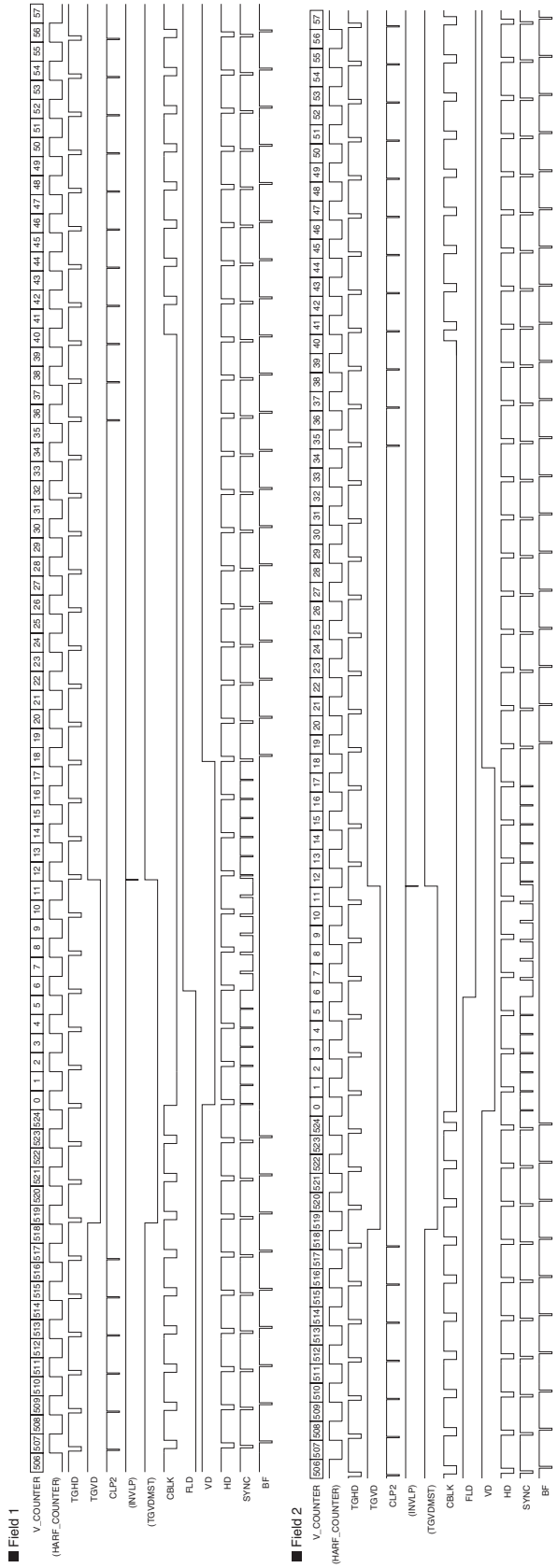


2. 760H Horizontal Timing Chart **MCK: PAL 908fH (14.1875MHz/70.48ns)**



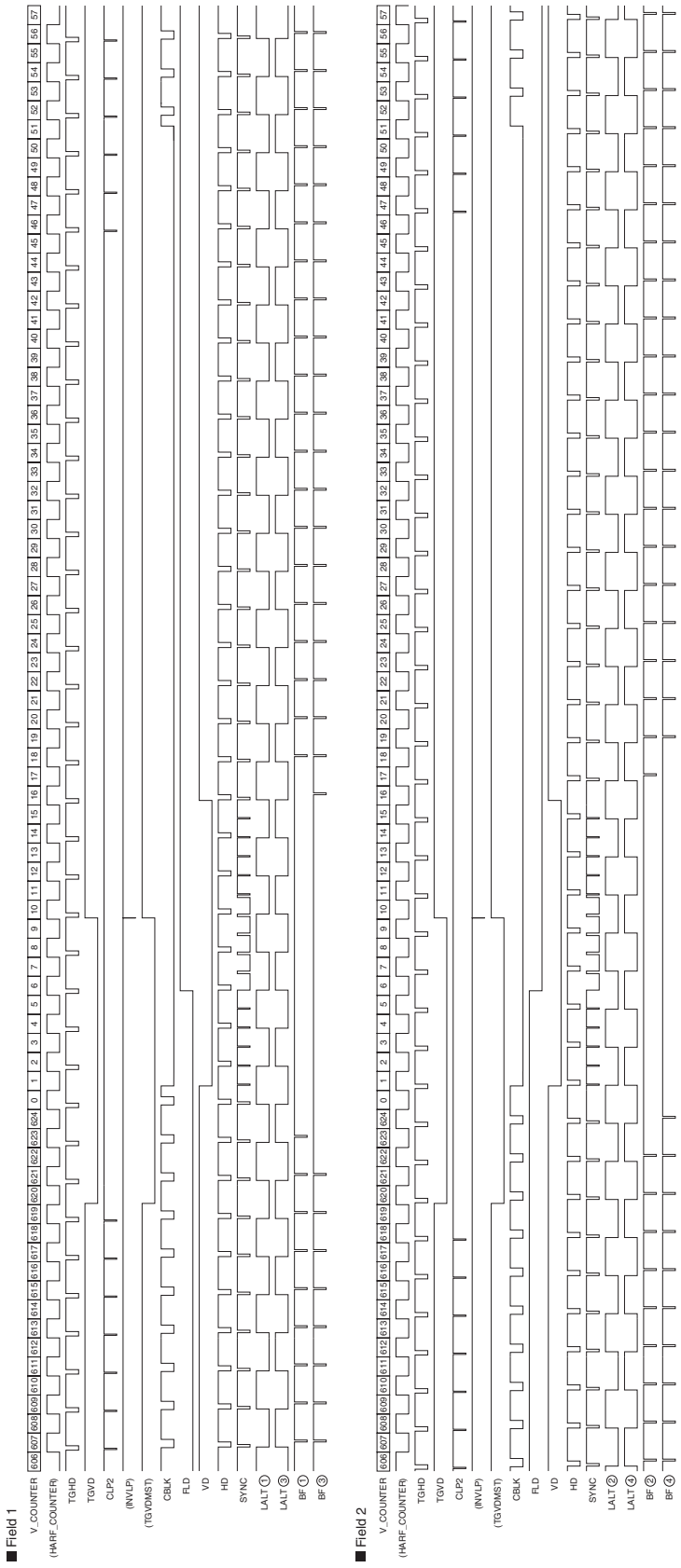
3. 760H NTSC Vertical Timing Chart

Note) This timing chart is for the default setting. The system delay when the timing chart CXD3160R is connected is not taken into account.



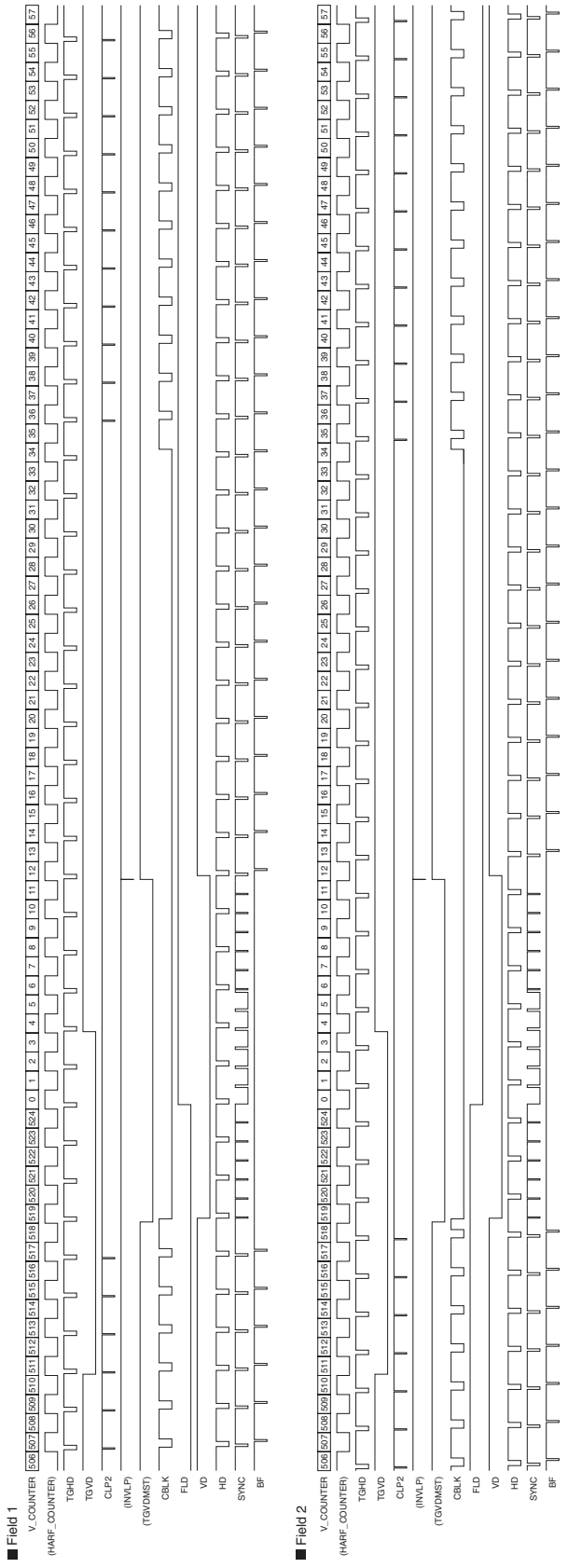
4. 760H PAL Vertical Timing Chart

Note) This timing chart is for the default setting. The system delay when the timing chart CXD3160R is connected is not taken into account.



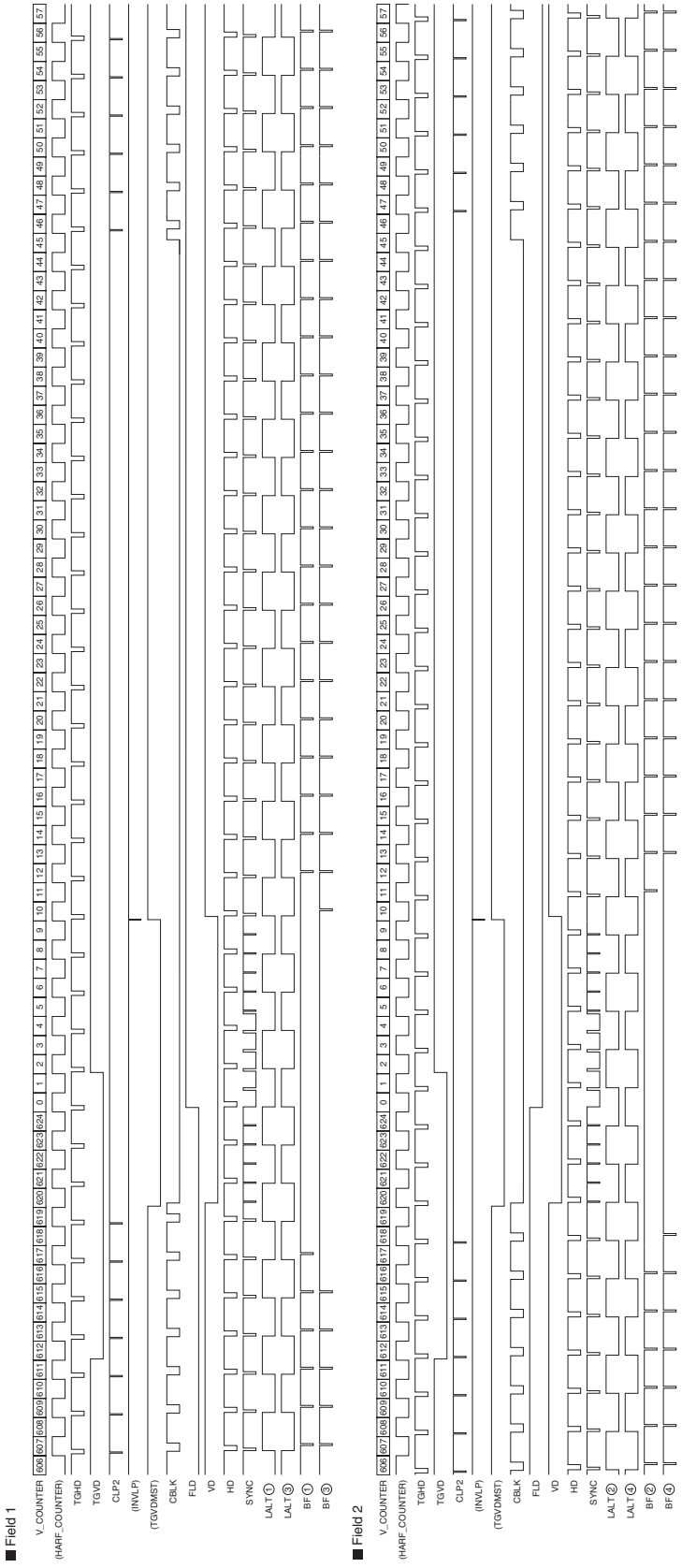
5. 760H NTSC Vertical Timing Chart (SS-3 WD System)

Note) This timing chart is for the default setting. The system delay when the timing chart CXD3160R is connected is not taken into account.



6. 760H PAL Vertical Timing Chart (SS-3 WD System)

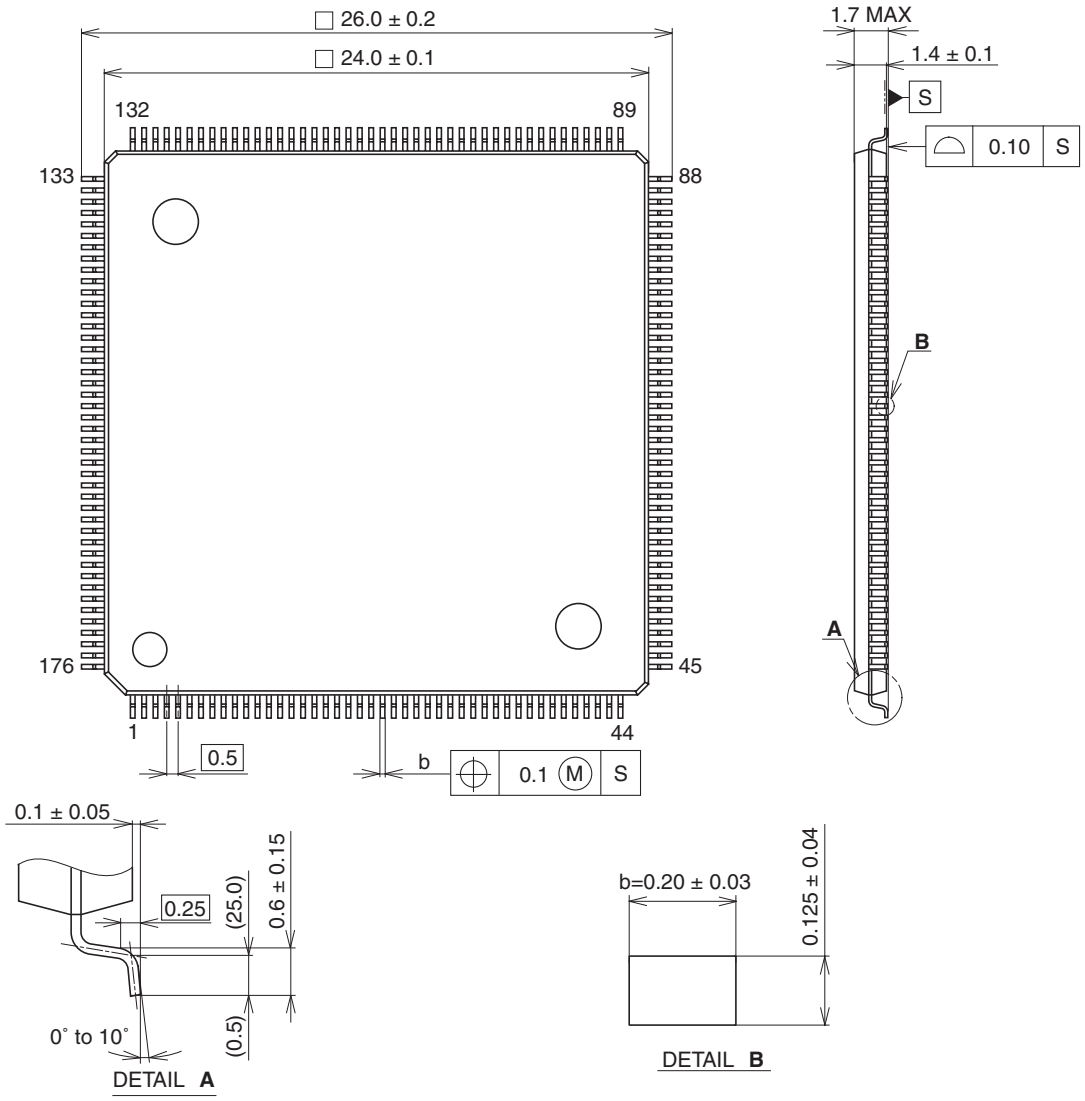
Note) This timing chart is for the default setting. The system delay when the timing chart CXD3160R is connected is not taken into account.



Package Outline

(Unit: mm)

176PIN LQFP (PLASTIC)



SONY CODE	LQFP-176P-L01
EIAJ CODE	P-LQFP176-24x24-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.8g